

Dual P-Channel 20 V (D-S) MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	-20					
$R_{DS(on)}$ max. (Ω) at V_{GS} = -10 V	0.0192					
$R_{DS(on)}$ max. (Ω) at $V_{GS} = -4.5 \text{ V}$	0.0330					
Q _g typ. (nC)	20					
I _D (A) ^{a, e}	-8					
Configuration	Dual					

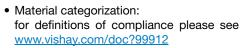
ORDERING INFORMATION

Lead (Pb)-free and halogen-free

Package

FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested

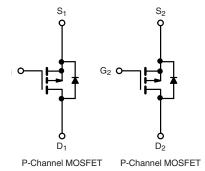




RoHS COMPLIANT HALOGEN **FREE**

APPLICATIONS

- · Load switching
 - Computer
 - Game systems
- · Battery switching - 2-cell Li-ion



PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	-20	V	
Gate-source voltage	V_{GS}	± 20	V	
	T _C = 25 °C		-8 e	
Continuous drain current (T _J = 150 °C)	T _C = 70 °C		-8 e	
	T _A = 25 °C	I _D	-8 b, c, e	
	T _A = 70 °C		-6.7 b, c	
Pulsed drain current (10 µs pulse width)	I _{DM}	-30	А	
	T _C = 25 °C		-2.5	
Source-drain current diode current	T _A = 25 °C	I _S	-1.7 ^{b, c}	
Pulsed source-drain current	I _{SM}	-30		
Single pulse avalanche current	. 0.4	I _{AS}	-11	
Single-pulse avalanche energy	L = 0.1 mH	E _{AS}	6	mJ
Maximum power dissipation	T _C = 25 °C		3.1	
	T _C = 70 °C		2	10/
	T _A = 25 °C	P _D	2 b, c	W
	T _A = 70 °C		1.28 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stq}	-50 to +150	°C	

SO-8

Si4943CDY-T1-GE3

THERMAL RESISTANCE RATINGS					
		LIN			
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient b, d	t ≤ 10 s	R _{thJA}	50	62.5	°C/W
Maximum junction-to-foot (drain)	Steady state	R_{thJF}	30	40	0/ **

Notes

- a. Based on T_C = 25 °C b. Surface mounted on 1" x 1" FR4 board
- t = 10 s
- d. Maximum under steady state conditions is 110 °C/W
- e. Package limited

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.A	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V, I}_{D} = -250 \mu\text{A}$	-20	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	L 050 A	-	-21	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = -250 μA	-	5.4	-	mV/°C	
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1	-	-3	V	
Gate-body leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	-100	nA	
Zava gata valtaga duain avuvant	_	V _{DS} = -20 V, V _{GS} = 0 V	-	-	-1	μА	
Zero gate voltage drain current	I _{DSS}	V _{DS} = -20 V, V _{GS} = 0 V, T _J = 55 °C	-	-	-10		
On-state drain current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = -10 V	-30	-	-	Α	
D	<u> </u>	$V_{GS} = -10 \text{ V}, I_D = -8.3 \text{ A}$	-	0.0160	0.0192	Ω	
Drain-source on-state resistance b	R _{DS(on)}	$V_{GS} = -4.5 \text{ V}, I_D = -6.4 \text{ A}$	-	0.0275	0.0330		
Forward transconductance b	9 _{fs}	$V_{DS} = -10 \text{ V}, I_D = -8.3 \text{ A}$	-	19	-	S	
Dynamic ^a							
Input capacitance	C _{iss}		-	1945	-	pF	
Output capacitance	C _{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	460	-		
Reverse transfer capacitance	C _{rss}		-	385	-		
Telel celes de con	0	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -8.3 \text{ A}$	-	41	62	62 30 - -	
Total gate charge	Q_g		-	20	30		
Gate-source charge	Q _{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V}, I_D = -8.3 \text{ A}$	-	7	-		
Gate-drain charge	Q _{qd}		-	9	-		
Gate resistance	R_{g}	f = 1 MHz	0.5	2.5	5	Ω	
Turn-on delay time	t _{d(on)}		-	13	20		
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_1 = 1.5 \Omega$	-	11	17		
Turn-off delay time	t _{d(off)}	$I_D \cong -6.7 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	35	53		
Fall time	t _f		-	10	15		
Turn-on delay time	t _{d(on)}		-	50	75	ns	
Rise time	t _r	$V_{DD} = -10 \text{ V}, R_1 = 1.5 \Omega$	-	71	107		
Turn-off delay time	t _{d(off)}	$I_D \cong -6.7 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	29	44		
Fall time	t _f		-	15	23		
Drain-Source Body Diode Characteris	tics						
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	-2.5	^	
Pulse diode forward current ^a	I _{SM}		-	-	-30	Α	
Body diode voltage	V _{SD}	I _S = -6.7 A	-	-0.77	-1.2	V	
Body diode reverse recovery time	t _{rr}		-	30	45	ns	
Body diode reverse recovery charge	Q _{rr}	1 07 A 4:/-H 400 A / - T 05 00	-	17	26	nC	
Reverse recovery fall time	ta	$I_F = -6.7 \text{ A, di/dt} = 100 \text{ A/}\mu\text{s, T}_J = 25 ^{\circ}\text{C}$		13	-		
Reverse recovery rise time	t _b		_	17	_	ns	

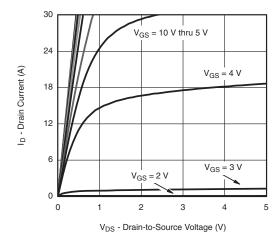
Notes

- a. Guaranteed by design, not subject to production testing
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %

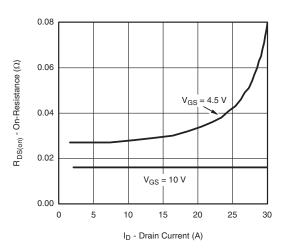
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



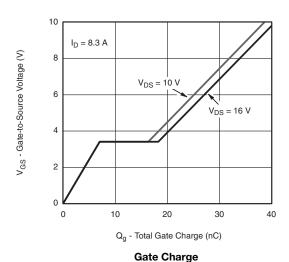
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

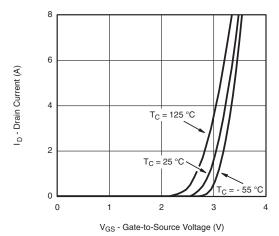


Output Characteristics

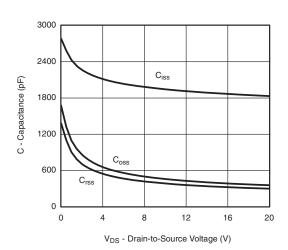


On-Resistance vs. Drain Current and Gate Voltage

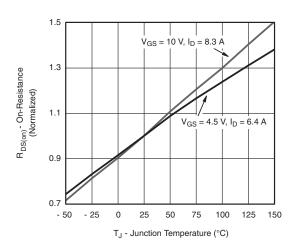




Transfer Characteristics



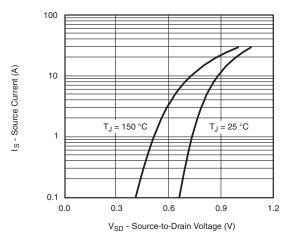
Capacitance



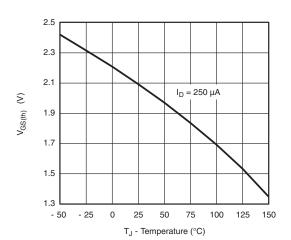
On-Resistance vs. Junction Temperature



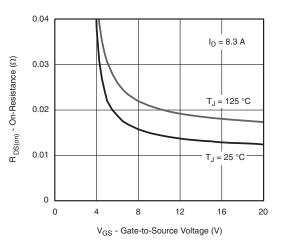
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



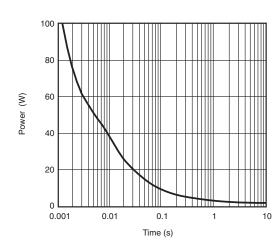
Source-Drain Diode Forward Voltage



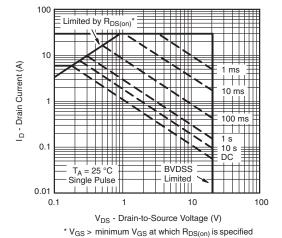
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

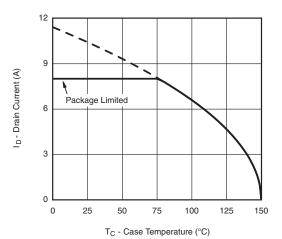


Single Pulse Power, Junction-to-Ambient

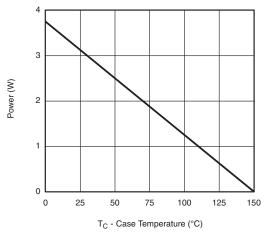


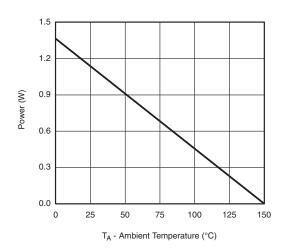
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating a





Power Derating, Junction-to-Foot

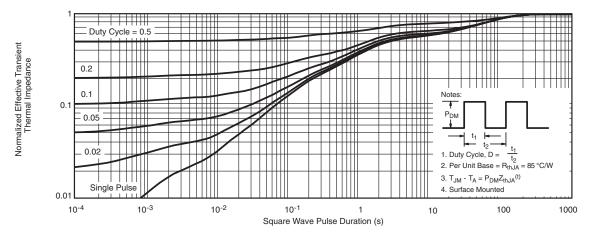
Power Derating, Junction-to-Ambient

Note

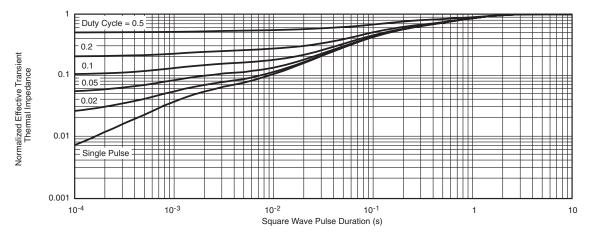
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



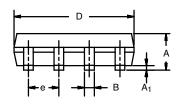
Normalized Thermal Transient Impedance, Junction-to-Foot

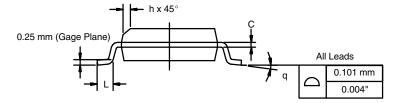
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SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







	MILLIM	IETERS	INCHES			
DIM	Min	Max	Min	Max		
Α	1.35	1.75	0.053	0.069		
A ₁	0.10	0.20	0.004	0.008		
В	0.35	0.51	0.014	0.020		
С	0.19	0.25	0.0075	0.010		
D	4.80	5.00	0.189	0.196		
Е	3.80	4.00	0.150	0.157		
е	1.27 BSC		0.050 BSC			
Н	5.80	6.20	0.228	0.244		
h	0.25	0.50	0.010	0.020		
L	0.50	0.93	0.020	0.037		
q	0°	8°	0°	8°		
S	0.44	0.64	0.018	0.026		
ECN: C-06527-Rev. I. 11-Sep-06						

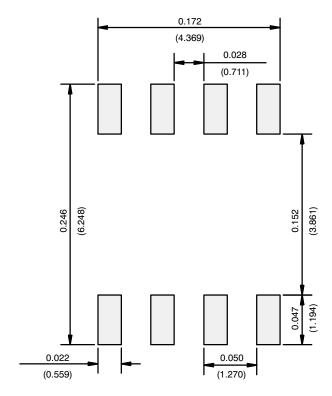
DWG: 5498

Document Number: 71192 www.vishay.com 11-Sep-06

LON NOTE



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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