

MOSFET – Dual N-Channel, POWER TRENCH®

60 V, 8.2 A, 17 mΩ

FDMC89521L

General Description

This device includes two 60 V N-Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Features

- Max $r_{DS(on)}$ = 17 mΩ at V_{GS} = 10 V, I_D = 8.2 A
- Max $r_{DS(on)}$ = 27 mΩ at V_{GS} = 4.5 V, I_D = 6.7 A
- Termination is Lead-free
- These Devices are RoHS Compliant

Applications

- Battery Protection
- Load Switching
- Bridge Topologies

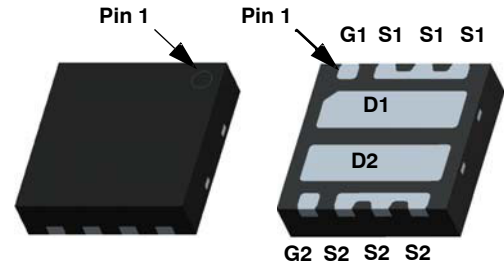
MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	60	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous T_A = 25°C (Note 1a) – Pulsed	8.2 40	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	32	mJ
P_D	Power Dissipation T_C = 25°C	16	W
	Power Dissipation T_A = 25°C (Note 1a)	1.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

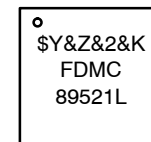
Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	65	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	155	°C/W



Power 33

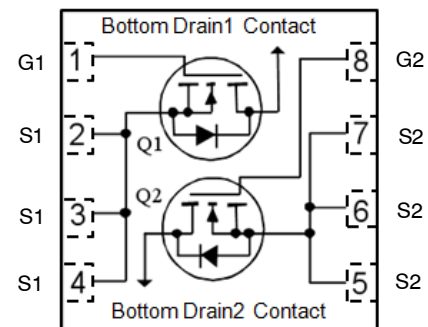
WDFN8 3x3, 0.65P
CASE 511DG

MARKING DIAGRAM



\$Y = onsemi Logo
 &Z = Assembly Plant Code
 &2 = Numeric Date Code
 &K = Lot Code
 FDMC89521L = Specific Device Code

PIN ASSIGNMENT



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC89521L

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		30		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 48 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = 250 μA	1	1.9	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 250 μA, referenced to 25°C		–6		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 8.2 A		13	17	mΩ
		V _{GS} = 4.5 V, I _D = 6.7 A		21	27	
		V _{GS} = 10 V, I _D = 8.2 A, T _J = 125°C		20	26	
g _{FS}	Forward Transconductance	V _{DD} = 10 V, I _D = 8.2 A		28		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 30 V, V _{GS} = 0 V f = 1 MHz		1228	1635	pF
C _{oss}	Output Capacitance			243	325	pF
C _{rss}	Reverse Transfer Capacitance			10	15	pF
R _g	Gate Resistance			0.7		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 30 V, I _D = 8.2 A, V _{GS} = 10 V, R _{GEN} = 6 Ω		7.9	16	ns
t _r	Rise Time			2.1	10	ns
t _{d(off)}	Turn-Off Delay Time			18	33	ns
t _f	Fall Time			1.7	10	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to 10 V, V _{DD} = 30 V, I _D = 8.2 A		17	24	nC
		V _{GS} = 0 V to 4.5 V, V _{DD} = 30 V, I _D = 8.2 A		7.9	12	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 30 V, I _D = 8.2 A		3.8		nC
Q _{gd}	Gate to Drain “Miller” Charge			1.9		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

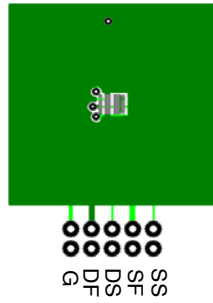
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 8.2 A (Note 2)		0.85	1.3	V
		V _{GS} = 0 V, I _S = 1.6 A (Note 2)		0.75	1.2	
t _{rr}	Reverse Recovery Time	I _F = 8.2 A, di/dt = 100 A/μs		25	40	ns
Q _{rr}	Reverse Recovery Charge			11	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

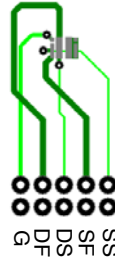
FDMC89521L

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 65°C/W when mounted on a 1 in² pad of 2 oz copper



b. 155°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
3. E_{AS} of 32 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 1$ mH, $I_{AS} = 8$ A, $V_{DD} = 54$ V, $V_{GS} = 10$ V. 100% tested at $L = 3$ mH, $I_{AS} = 5.4$ A.

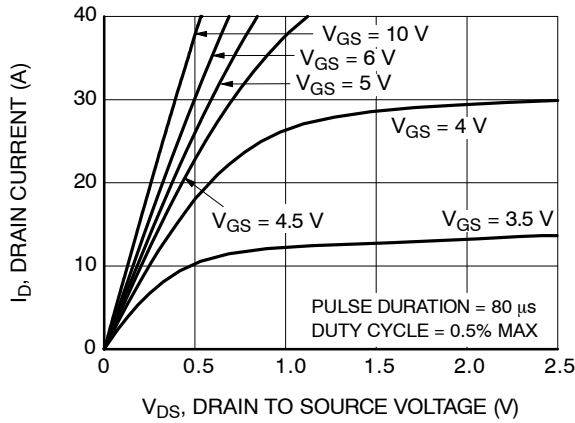
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Figure 1. On-Region Characteristics

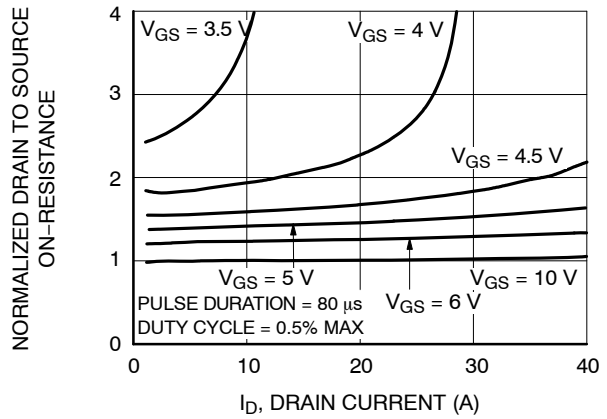


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

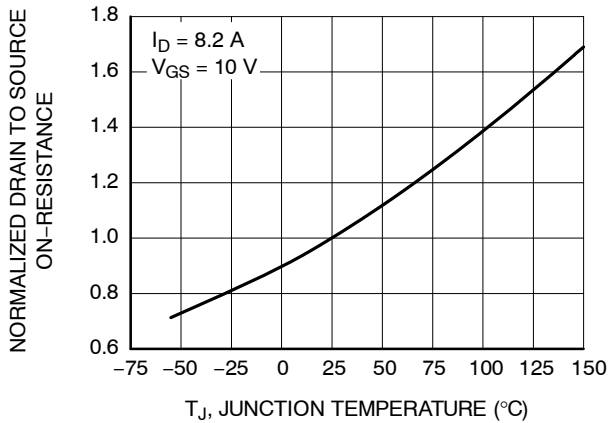


Figure 3. Normalized On-Resistance vs. Junction Temperature

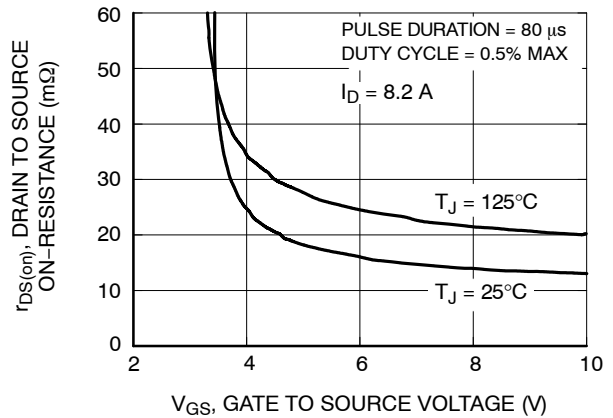


Figure 4. On-Resistance vs. Gate to Source Voltage

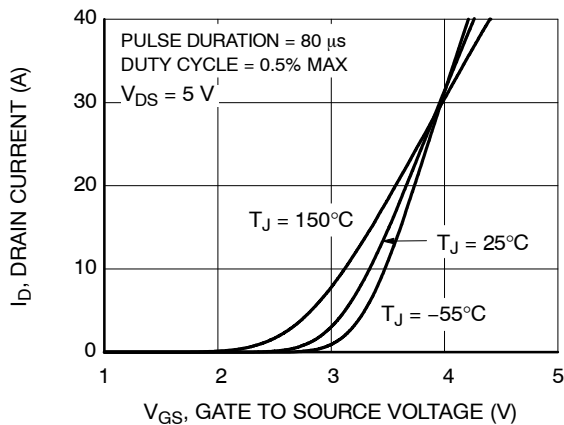


Figure 5. Transfer Characteristics

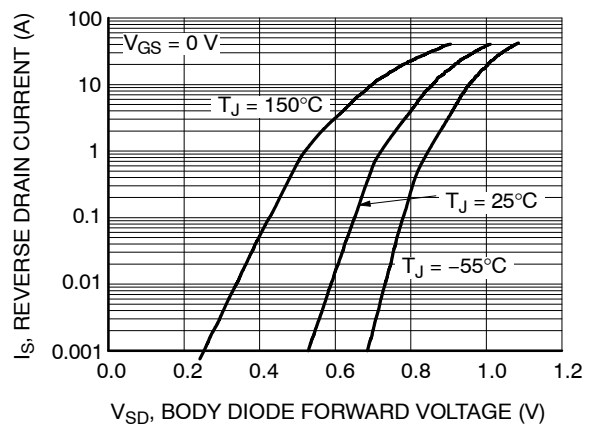


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

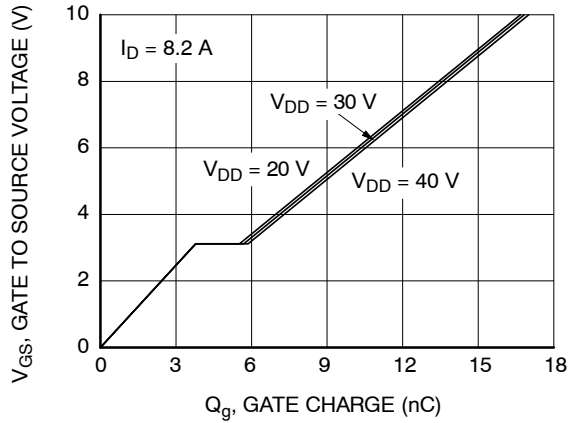


Figure 7. Gate Charge Characteristics

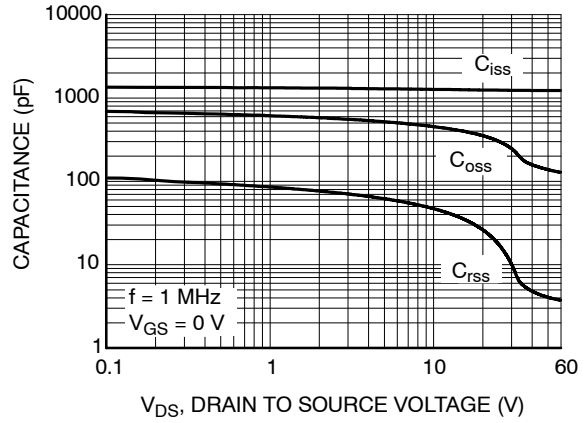


Figure 8. Capacitance vs. Drain to Source Voltage

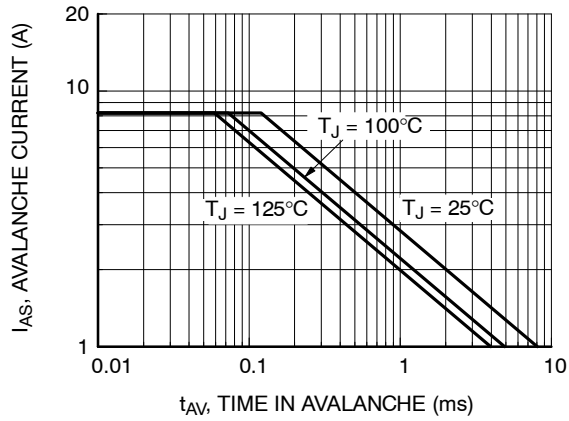


Figure 9. Unclamped Inductive Switching Capability

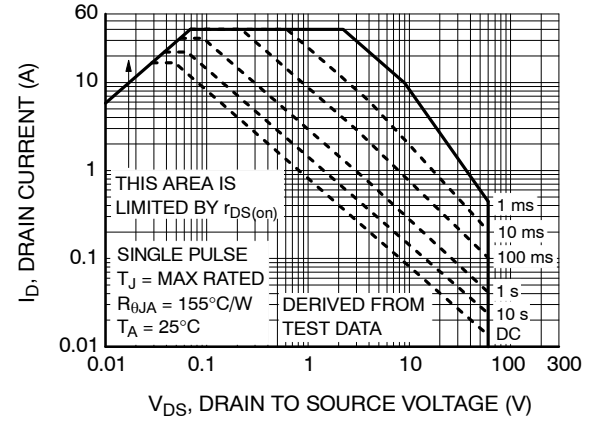


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

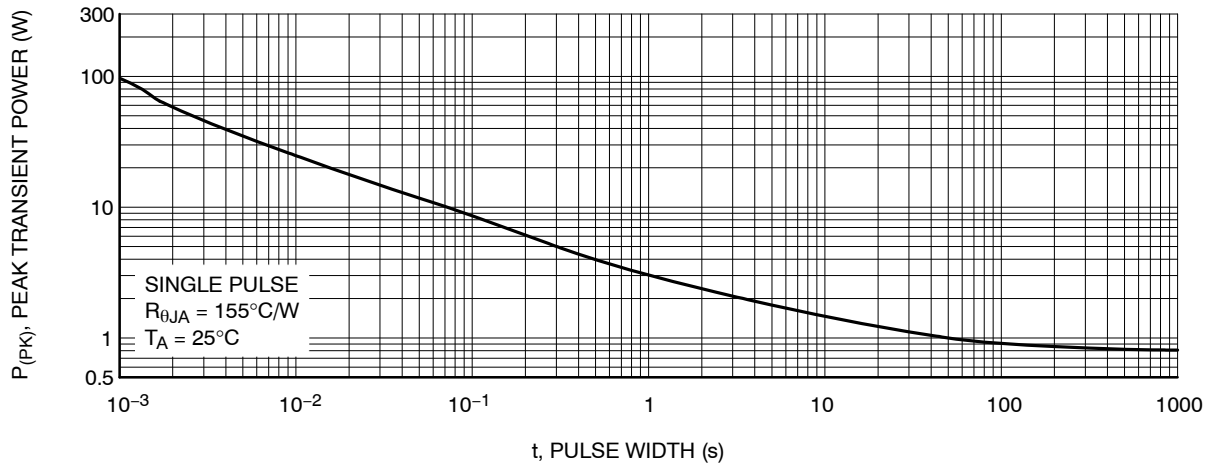


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

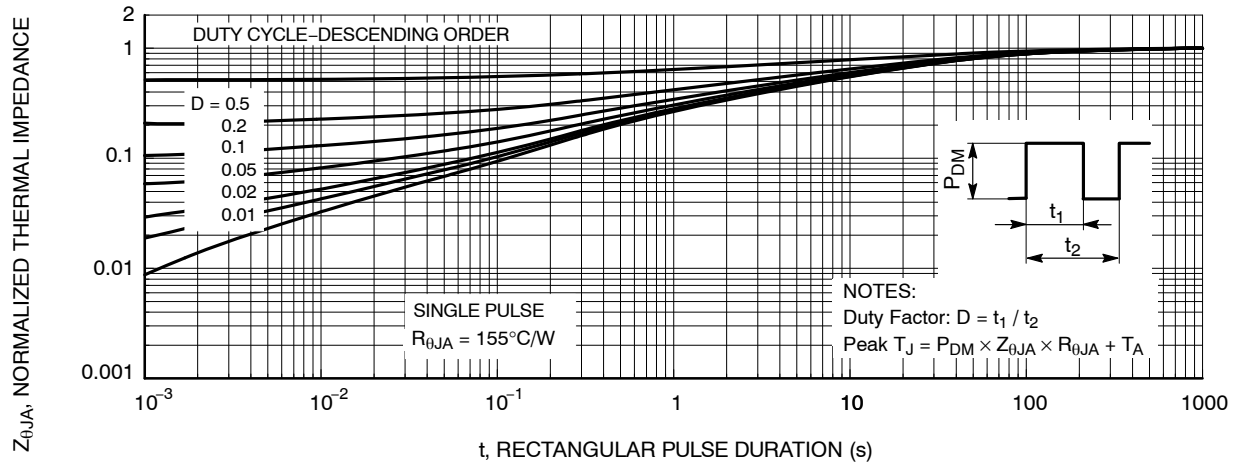


Figure 12. Junction-to-Case Transient Thermal Response Curve

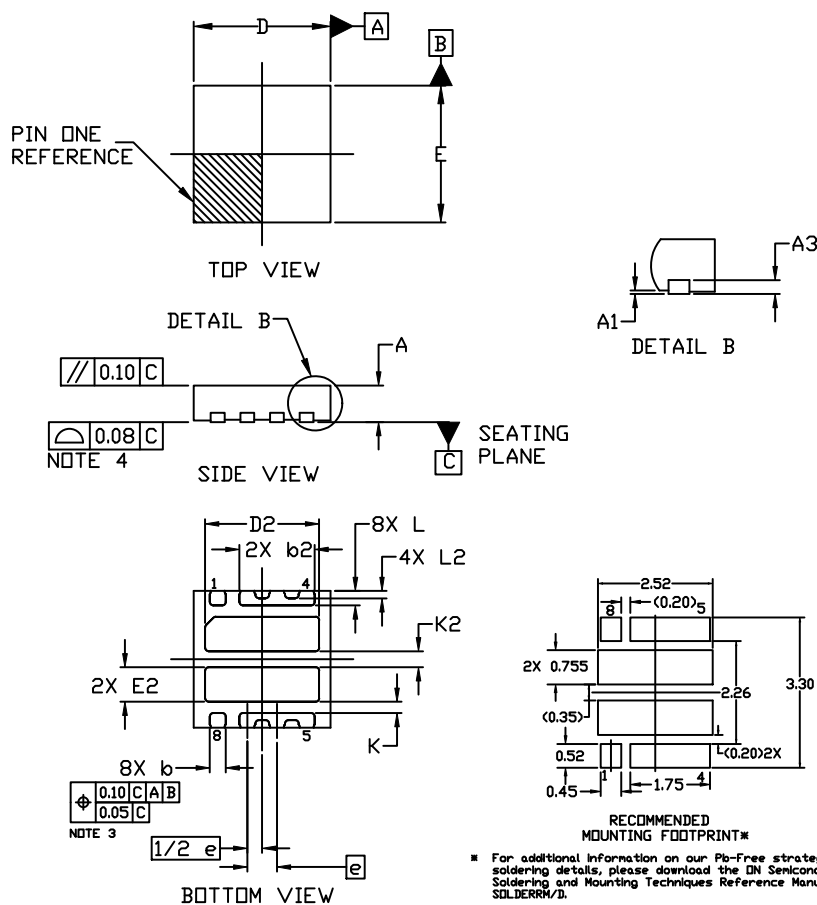
ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDMC89521L	FDMC89521L	WDFN8 3x3, 0.65P (Pb-Free)	3000 / Tape & Reel

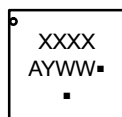
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3x3, 0.65P
CASE 511DG
ISSUE A

DATE 12 FEB 2019



GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "u", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION **b** APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.30	0.35	0.40
b2	1.65 REF		
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e	0.65 BSC		
K	0.25	---	---
K2	0.35 REF		
L	0.27	0.32	0.37
L2	0.163 REF		

■ For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, [SOLDERING/D](http://www.onsemi.com/SOLDERING).

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DESCRIPTION:	WDFN8 3x3, 0.65P	PAGE 1 OF 1

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