

MOSFET – N & P-Channel, POWERTRENCH® 30 V

FDC6333C

General Description

These N & P-Channel MOSFETs are produced using onsemi's advanced POWERTRENCH process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

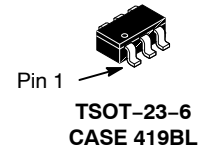
Features

- *Q1* 2.5 A, 30 V
 - ♦ $R_{DS(on)} = 95 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 - ♦ $R_{DS(on)} = 150 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- *Q2* -2.0 A, -30 V
 - ♦ $R_{DS(on)} = 130 \text{ m}\Omega @ V_{GS} = -10 \text{ V}$
 - ♦ $R_{DS(on)} = 220 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
- Low Gate Charge
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- SUPERSOT™-6 Package: Small Footprint (72% Smaller than SO-8); Low Profile (1 mm Thick)
- This is a Pb-Free Device

Applications

- DC-DC Converter
- Load Switch
- LCD Display Inverter

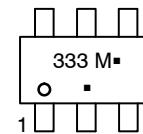
	V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
Q1	30 V	95 m Ω @ 10 V	2.5 A
		150 m Ω @ 4.5 V	
Q2	-30 V	130 m Ω @ -10 V	-2.0 A
		220 m Ω @ -4.5 V	



Pin 1

TSOT-23-6
CASE 419BL

MARKING DIAGRAM



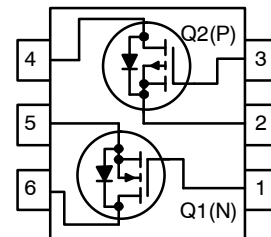
333 = Specific Device Code

M = Assembly Operation Month

▪ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

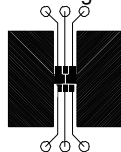
Symbol	Parameter	Ratings		Unit
		Q1	Q2	
V_{DSS}	Drain–Source Voltage	30	–30	V
V_{GSS}	Gate–Source Voltage	± 16	± 25	V
I_D	Drain Current – Continuous (Note 1a)	2.5	–2.0	A
	Drain Current – Pulsed	8	–8	
P_D	Power Dissipation for Single Operation	(Note 1a)	0.96	W
		(Note 1b)	0.9	
		(Note 1c)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

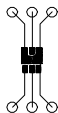
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 1a)	130	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case (Note 1)	60	$^\circ\text{C}/\text{W}$

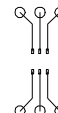
1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $130^\circ\text{C}/\text{W}$ when mounted on a 0.125 in^2 pad of 2 oz. copper.



b. $140^\circ\text{C}/\text{W}$ when mounted on a 0.004 in^2 pad of 2 oz. copper.



c. $180^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain–Source Breakdown Voltage	Q1	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	–	–	V
		Q2	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	–30	–	–	
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	Q1	$I_D = 250\text{ }\mu\text{A}$, Ref. to 25°C	–	27	–	$\text{mV}/^\circ\text{C}$
		Q2	$I_D = -250\text{ }\mu\text{A}$, Ref. to 25°C	–	–22	–	
I_{DSS}	Zero Gate Voltage Drain Current	Q1	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	–	–	1	μA
		Q2	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	–	–	–1	
I_{GSSF}	Gate–Body Leakage, Forward	Q1	$V_{GS} = 16\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	nA
		Q2	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	–	–	100	
I_{GSSR}	Gate–Body Leakage, Reverse	Q1	$V_{GS} = -16\text{ V}, V_{DS} = 0\text{ V}$	–	–	–100	nA
		Q2	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	–	–	–100	

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	Q1	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	1.8	3	V
		Q2	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	–1	–1.8	–3	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	Q1	$I_D = 250\text{ }\mu\text{A}$, Ref. to 25°C	–	4	–	$\text{mV}/^\circ\text{C}$
		Q2	$I_D = -250\text{ }\mu\text{A}$, Ref. to 25°C	–	–4	–	

FDC6333C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.) (continued)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 2)							
R _{DS(on)}	Static Drain–Source On–Resistance	Q1	V _{GS} = 10 V, I _D = 2.5 A	–	73	95	mΩ
			V _{GS} = 4.5 V, I _D = 2.0 A	–	90	150	
			V _{GS} = 10 V, I _D = 2.5 A, T _J = 125°C	–	106	148	
		Q2	V _{GS} = –10 V, I _D = –2.0 A	–	95	130	
			V _{GS} = –4.5 V, I _D = –1.7 A	–	142	220	
			V _{GS} = 10 V, I _D = –2.0 A, T _J = 125°C	–	149	216	
I _{D(on)}	On–State Drain Current	Q1	V _{GS} = 10 V, V _{DS} = 5 V	8	–	–	A
		Q2	V _{GS} = –10 V, V _{DS} = –5 V	–8	–	–	
g _{FS}	Forward Transconductance	Q1	V _{DS} = 5 V, I _D = 2.5 A	–	7	–	S
		Q2	V _{DS} = –5 V, I _D = –2.0 A	–	3	–	

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	Q1	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	282	–	pF
		Q2	V _{DS} = –15 V, V _{GS} = 0 V, f = 1.0 MHz	–	185	–	
C _{oss}	Output Capacitance	Q1	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	49	–	
		Q2	V _{DS} = –15 V, V _{GS} = 0 V, f = 1.0 MHz	–	56	–	
C _{rss}	Reverse Transfer Capacitance	Q1	V _{DS} = 15 V, V _{GS} = 0 V, f = 1.0 MHz	–	20	–	
		Q2	V _{DS} = –15 V, V _{GS} = 0 V, f = 1.0 MHz	–	26	–	

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	Q1	For Q1: V _{DS} = 15 V, I _{DS} = 1 A, V _{GS} = 10 V, R _{GEN} = 6 Ω For Q2: V _{DS} = –15 V, I _{DS} = –1 A, V _{GS} = –10 V, R _{GEN} = 6 Ω	–	4.5	9	ns
		Q2		–	4.5	9	
t _r	Turn–On Rise Time	Q1		–	6	12	
		Q2		–	13	23	
t _{d(off)}	Turn–Off Delay Time	Q1		–	19	34	
		Q2		–	11	20	
t _f	Turn–Off Fall Time	Q1		–	1.5	3	
		Q2		–	2	4	
Q _g	Total Gate Charge	Q1		–	4.7	6.6	nC
		Q2		–	4.1	5.7	
Q _{gs}	Gate–Source Charge	Q1		–	0.9	–	
		Q2		–	0.8	–	
Q _{gd}	Gate–Drain Charge	Q1		–	0.6	–	
		Q2		–	0.4	–	

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current	Q1		–	–	0.8	A
		Q2		–	–	–0.8	
V _{SD}	Drain–Source Diode Forward Voltage	Q1	V _{GS} = 0 V, I _S = 0.8 A (Note 2)	–	0.8	1.2	V
		Q2	V _{GS} = 0 V, I _S = 0.8 A (Note 2)	–	0.8	–1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

TYPICAL CHARACTERISTICS: N-CANNEL

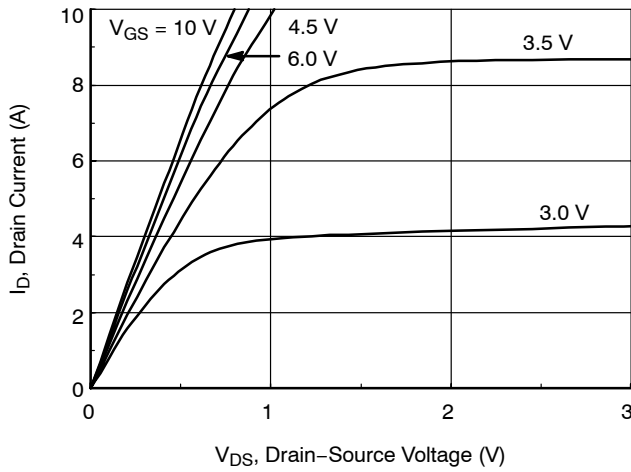


Figure 1. On-Region Characteristics

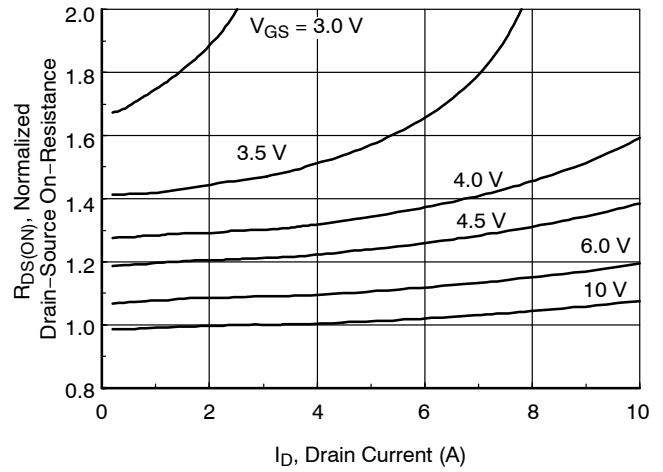


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

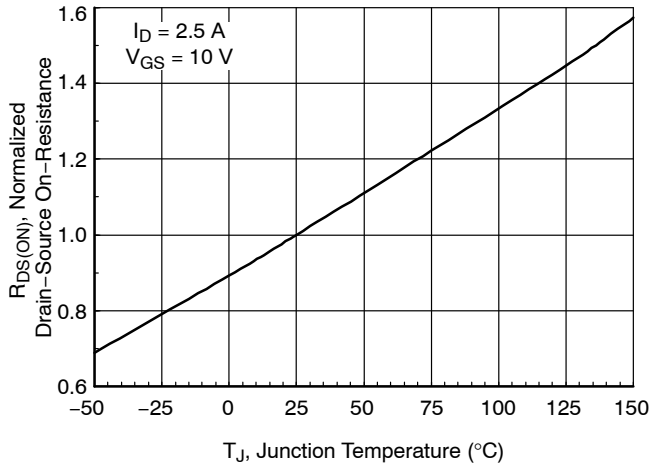


Figure 3. On-Resistance Variation with Temperature

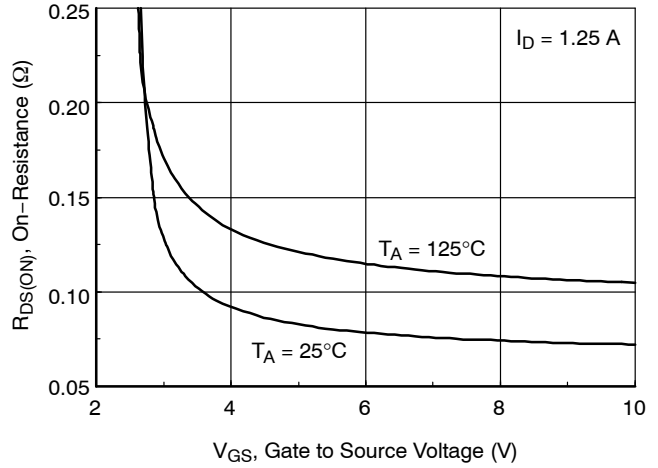


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

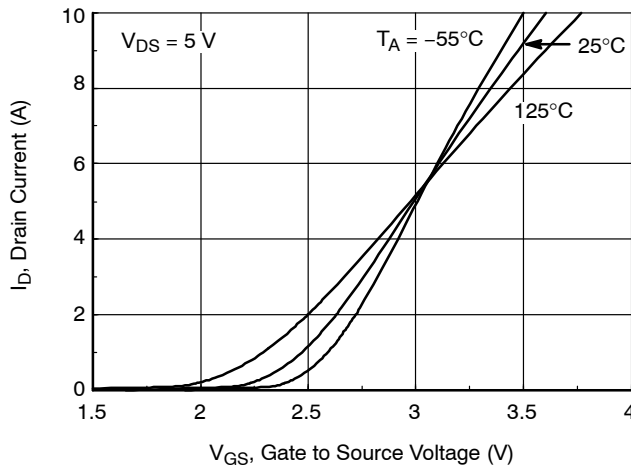


Figure 5. Transfer Characteristics

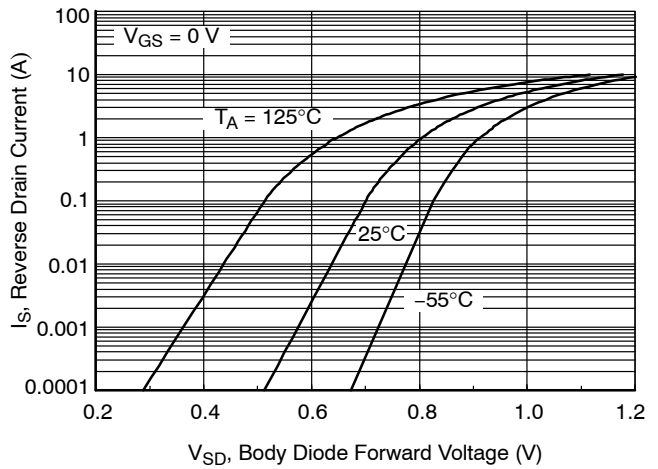


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: N-CHANNEL (continued)

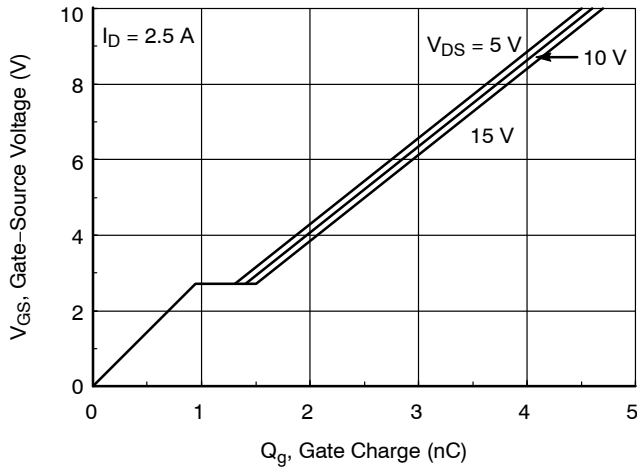


Figure 7. Gate Charge Characteristics

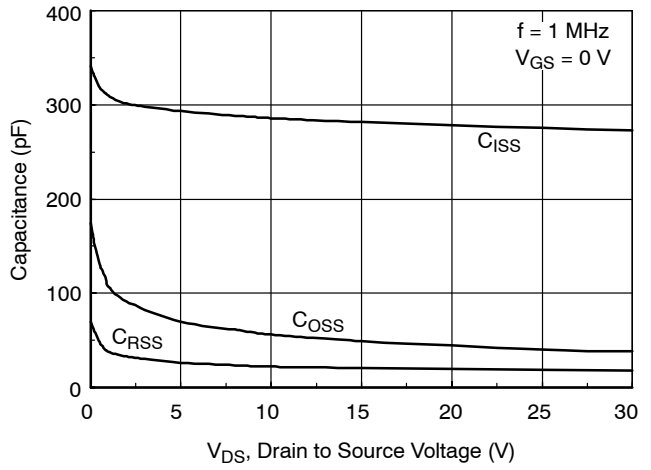


Figure 8. Capacitance Characteristics

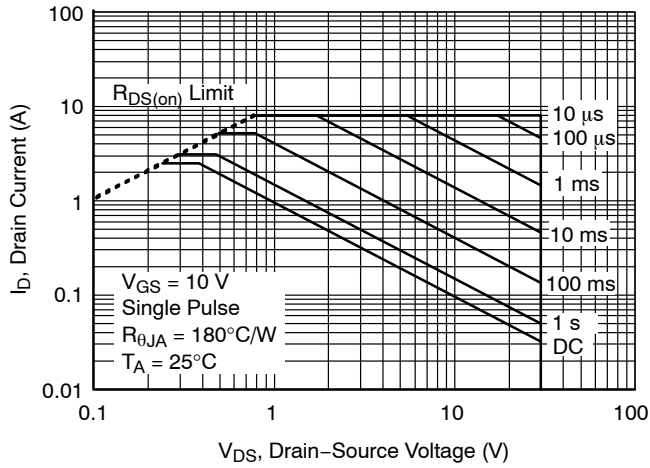


Figure 9. Maximum Safe Operating Area

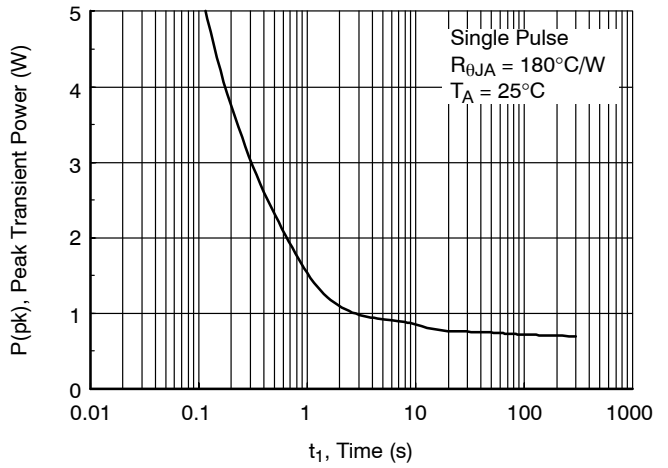


Figure 10. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS: P-CHANNEL

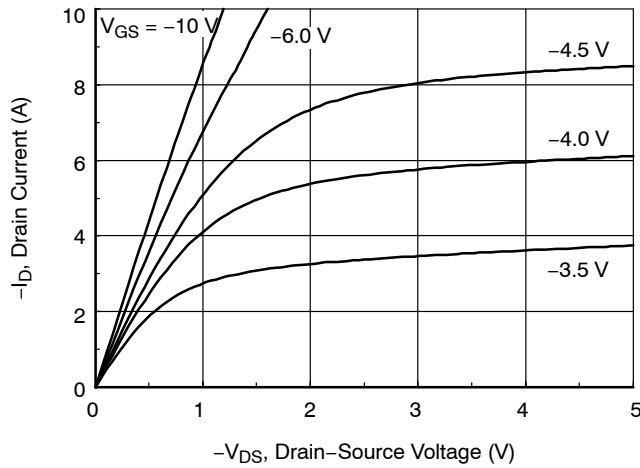


Figure 11. On-Region Characteristics

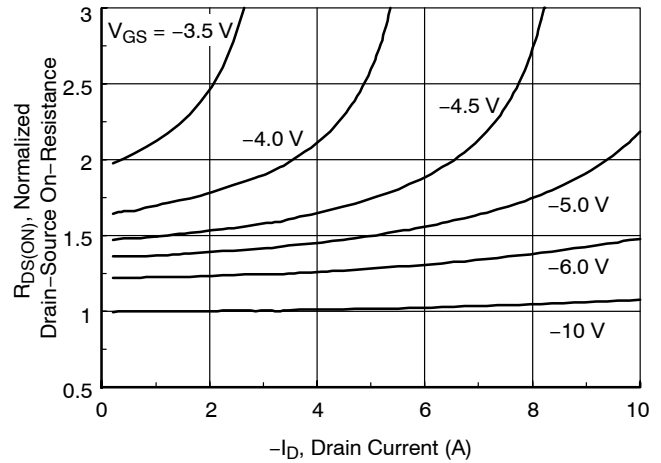


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage

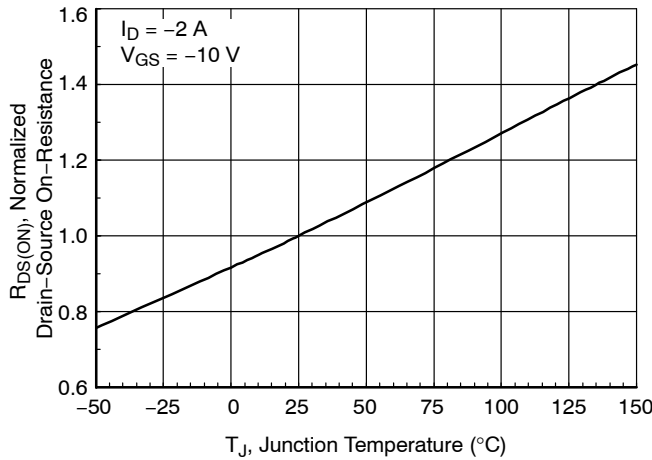


Figure 13. On-Resistance Variation with Temperature

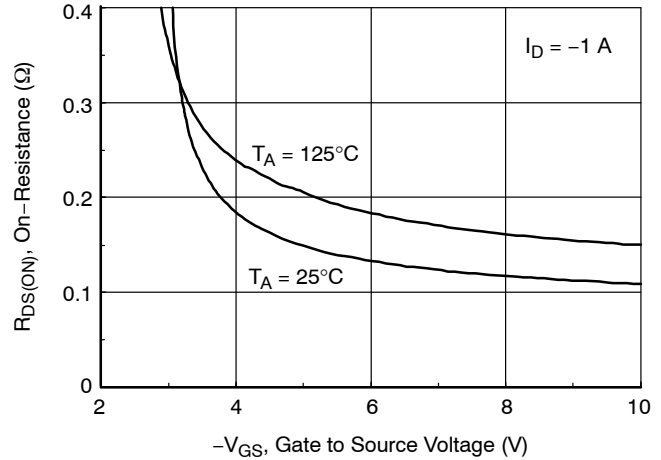


Figure 14. On-Resistance Variation with Gate-to-Source Voltage

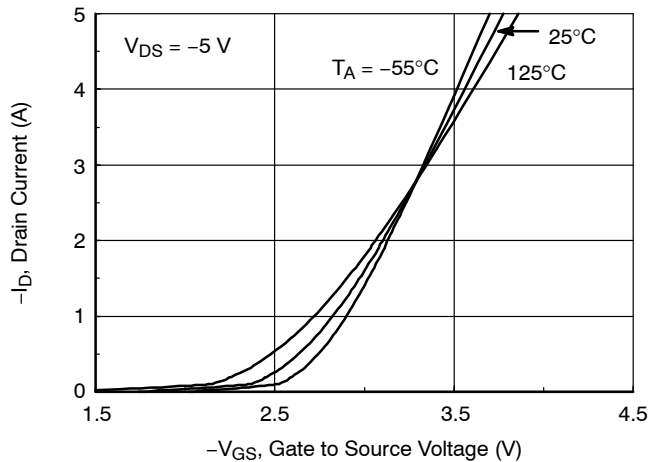


Figure 15. Transfer Characteristics

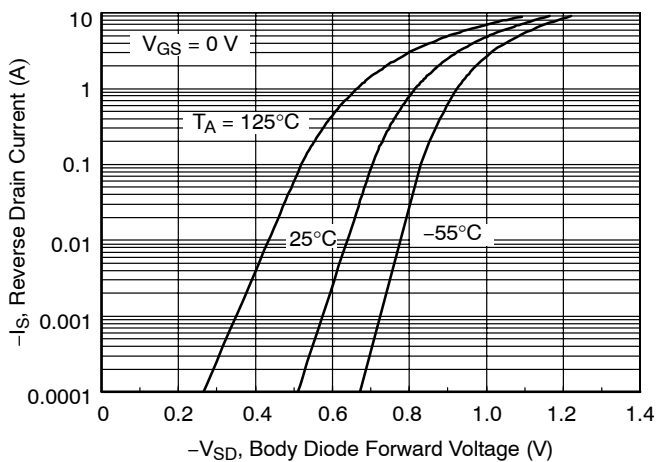


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS: P-CHANNEL (continued)

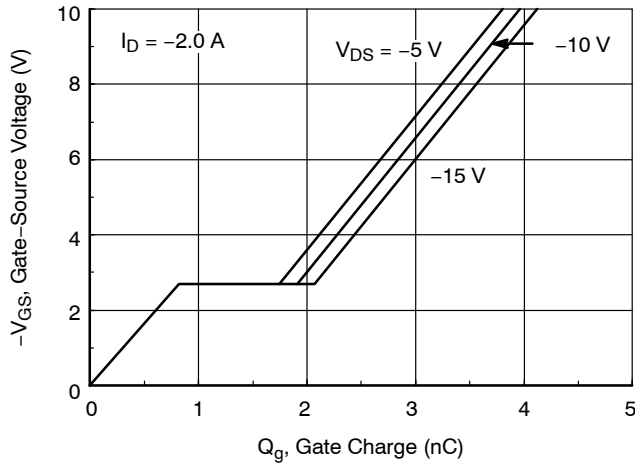


Figure 17. Gate Charge Characteristics

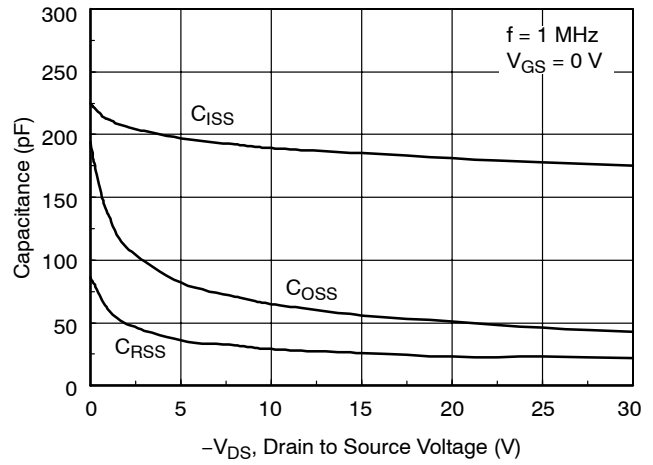


Figure 18. Capacitance Characteristics

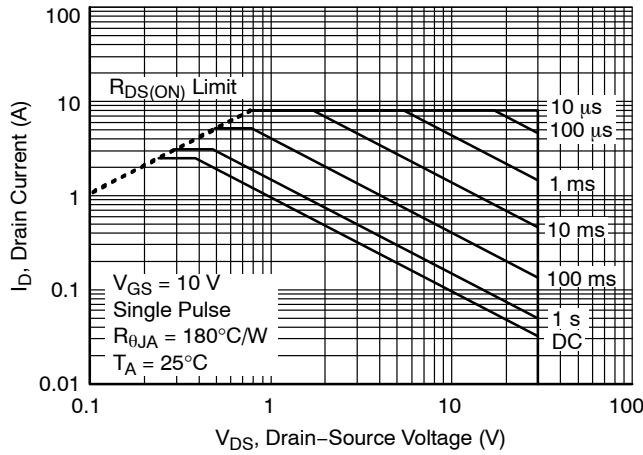


Figure 19. Maximum Safe Operating Area

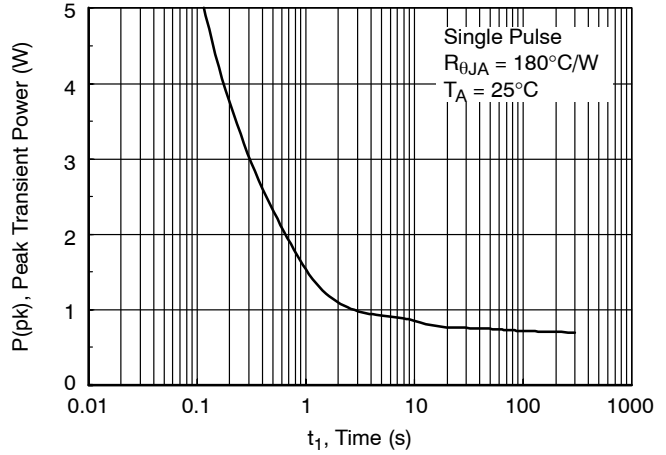


Figure 20. Single Pulse Maximum Power Dissipation

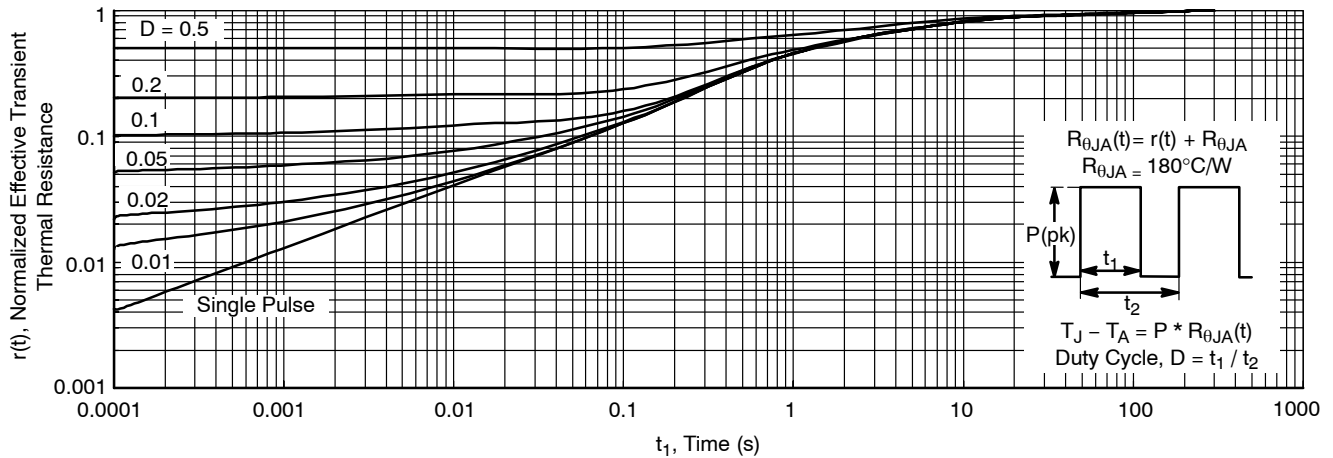


Figure 21. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

FDC6333C

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDC6333C	333	TSOT-23-6 (Pb-Free)	7"	8 mm	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

ON



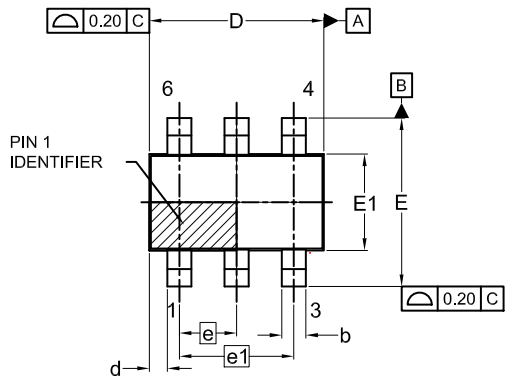
SCALE 2:1

TSOT23 6-Lead

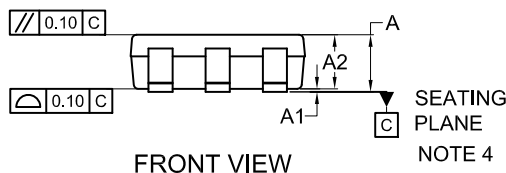
CASE 419BL

ISSUE A

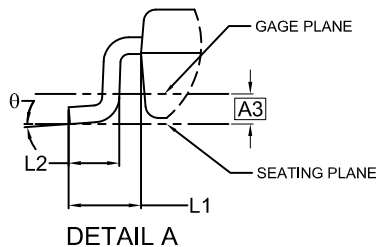
DATE 31 AUG 2020



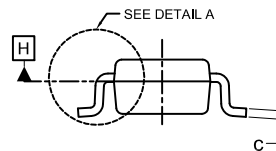
TOP VIEW



FRONT VIEW

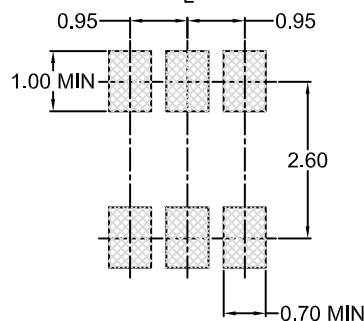


DETAIL A



SIDE VIEW

SYMM



LAND PATTERN
RECOMMENDATION

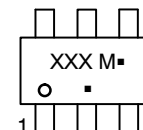
*FOR ADDITIONAL INFORMATION ON OUR
Pb-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	—	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	TSOT23 6-Lead	PAGE 1 OF 1

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