N and P Channel Enhancement Mode Power MOSFET

Description

The 6706A uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

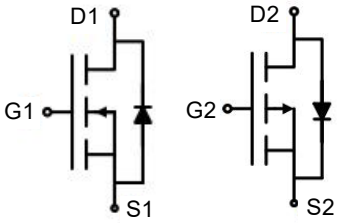
General Features

- NMOS
- V_{DS} 30V
- I_D (at V_{GS} = 10V) 6.5A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 20mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 30mΩ
- 100% Avalanche Tested
- RoHS Compliant

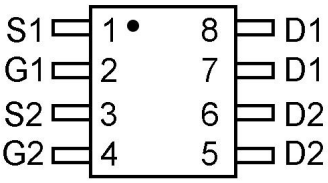
- PMOS
- V_{DS} -30V
- I_D (at V_{GS} = -10V) -5A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 45mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 70mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



pin assignment

SOP-8 Dual

Ordering Information

Device	Package	Marking	Packaging
6706A	SOP-8 Dual	6706	4000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Continuous Drain Current	I_D	6.5	-5	A
Pulsed Drain Current (note1)	I_{DM}	26	-20	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	2	2	W
Single pulse avalanche energy （note2）	E_{AS}	9	14	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

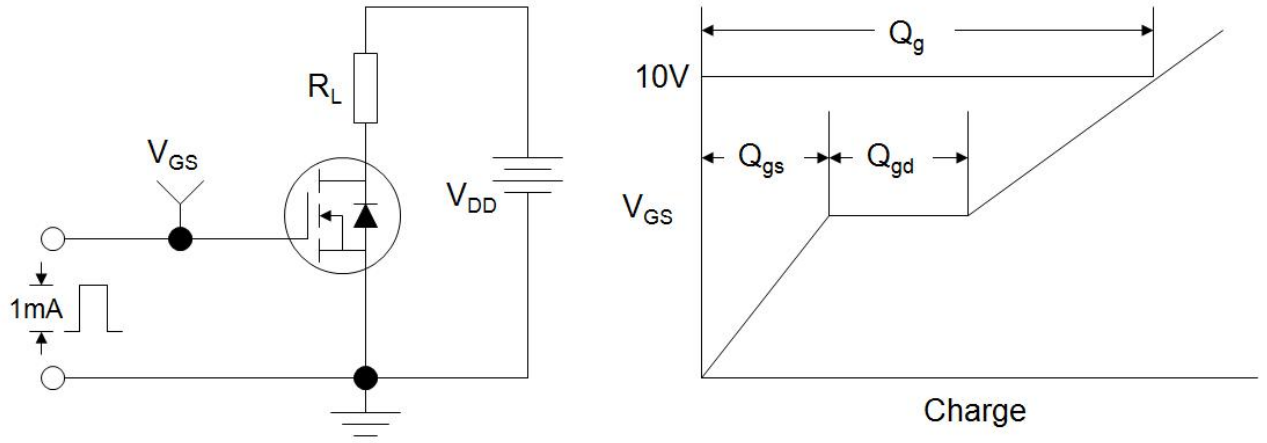
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62.5	62.5	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.5	2.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 5A	--	16	20	mΩ
		V_{GS} = 4.5V, I_D = 5A	--	24	30	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 5A	--	15	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz	--	479	--	pF
Output Capacitance	C_{oss}		--	68	--	
Reverse Transfer Capacitance	C_{rss}		--	59	--	
Total Gate Charge	Q_g	V_{DD} = 15V, I_D = 5A, V_{GS} = 10V	--	14.8	--	nC
Gate-Source Charge	Q_{gs}		--	2.6	--	
Gate-Drain Charge	Q_{gd}		--	2.9	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15V, I_D = 5A, R_G = 3Ω	--	4.5	--	ns
Turn-on Rise Time	t_r		--	2.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	14.5	--	
Turn-off Fall Time	t_f		--	3.5	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	6.5	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} =5A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 5A, V_{GS} = 0V di/dt=100A/us	--	56	--	nC
Reverse Recovery Time	Trr		--	47	--	ns

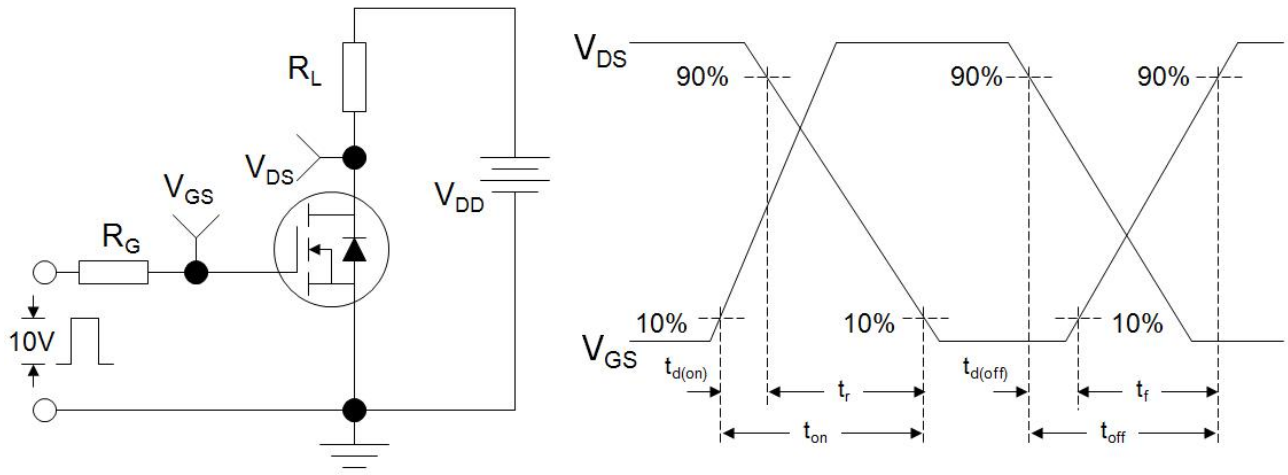
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=30V,VGS=10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 25mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

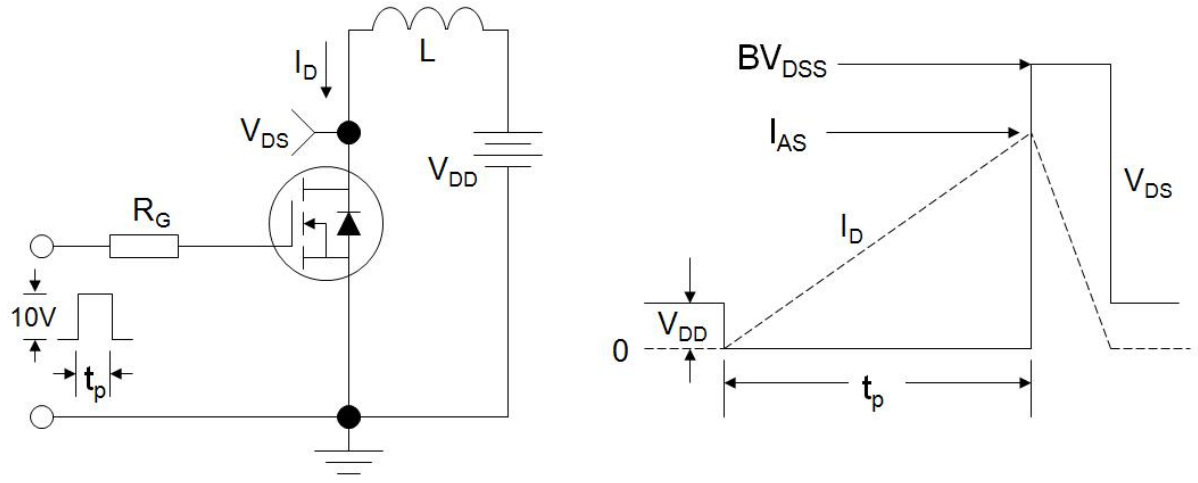
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

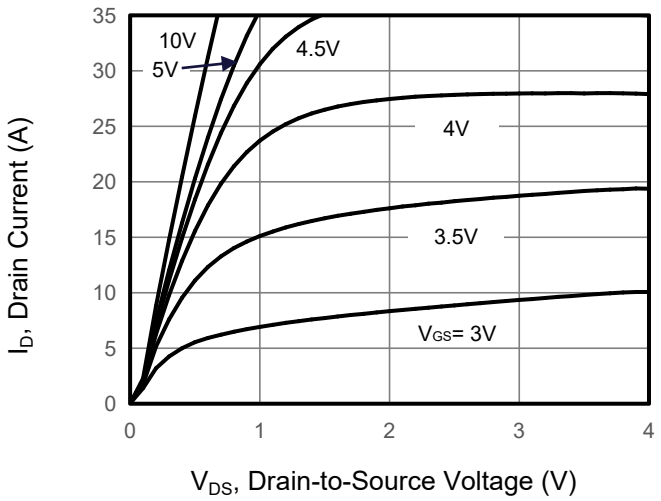


Figure 2. Transfer Characteristics

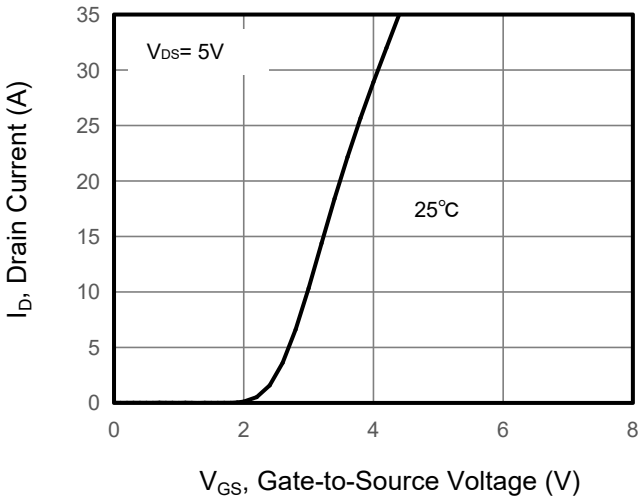


Figure 3. Drain Source On Resistance

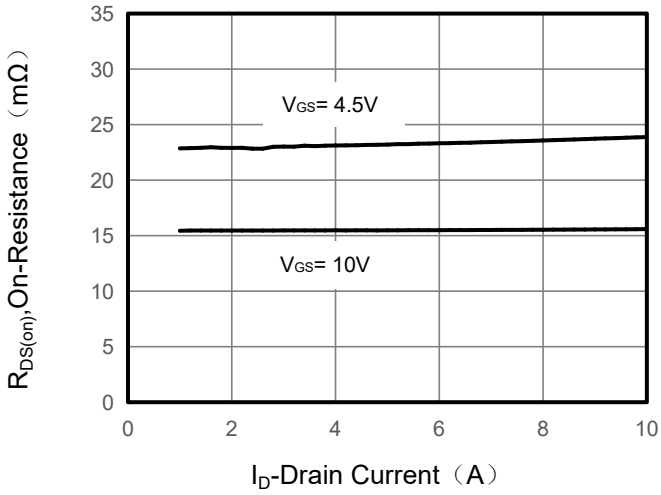


Figure 4. Gate Charge

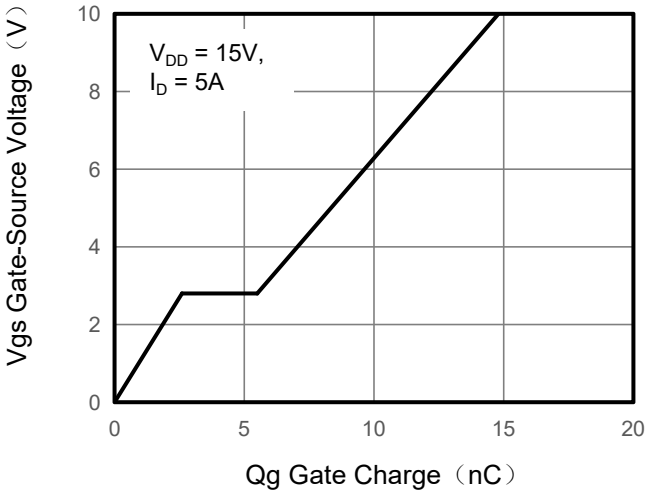


Figure 5. Capacitance

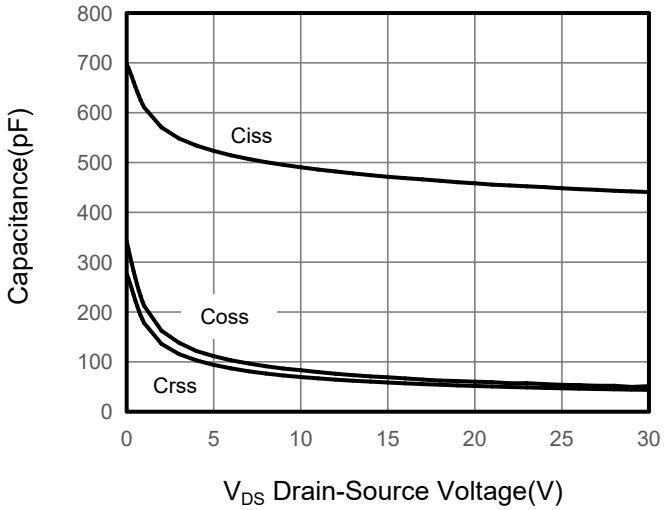
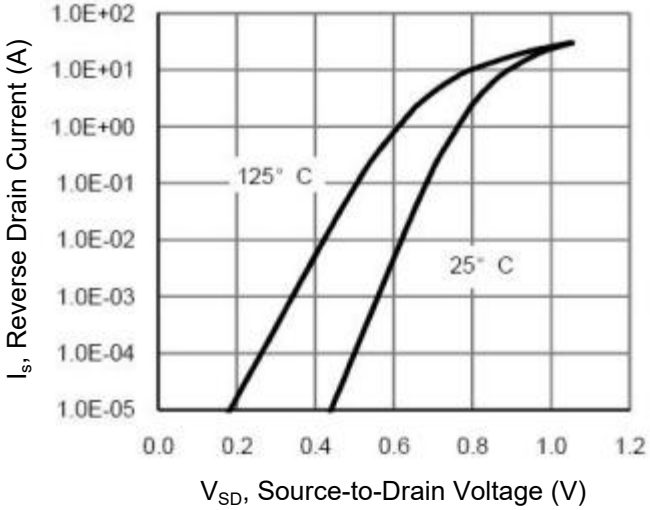


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

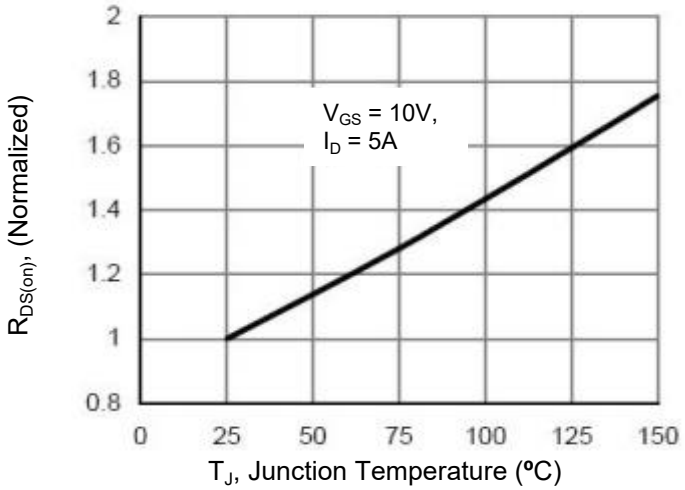


Figure 8. Safe Operation Area

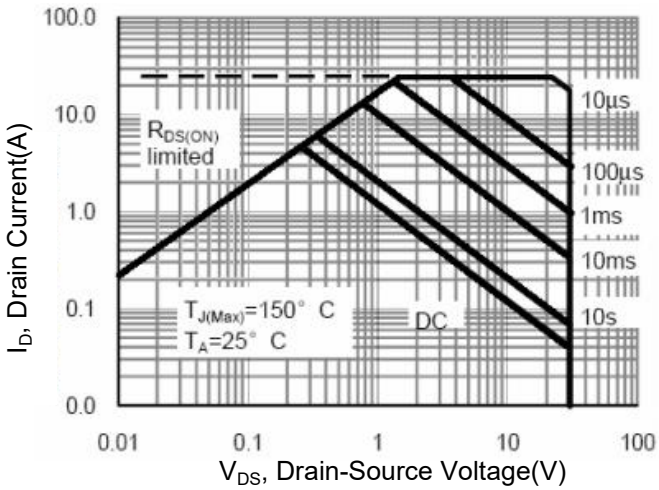
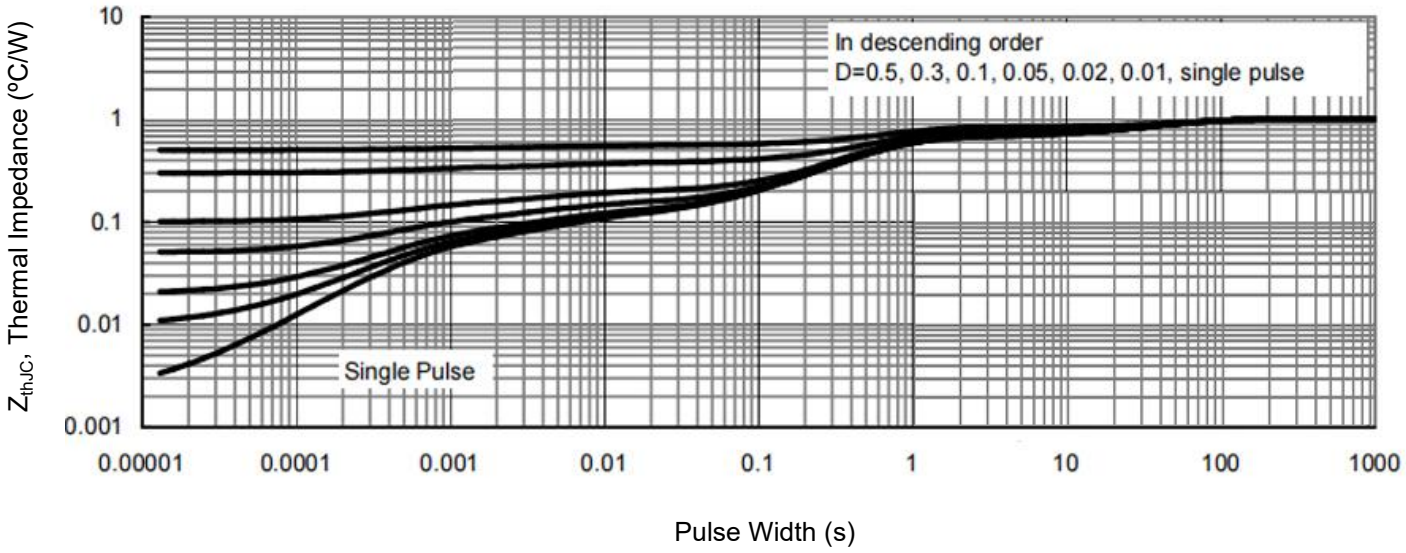


Figure 9. Normalized Maximum Transient Thermal Impedance

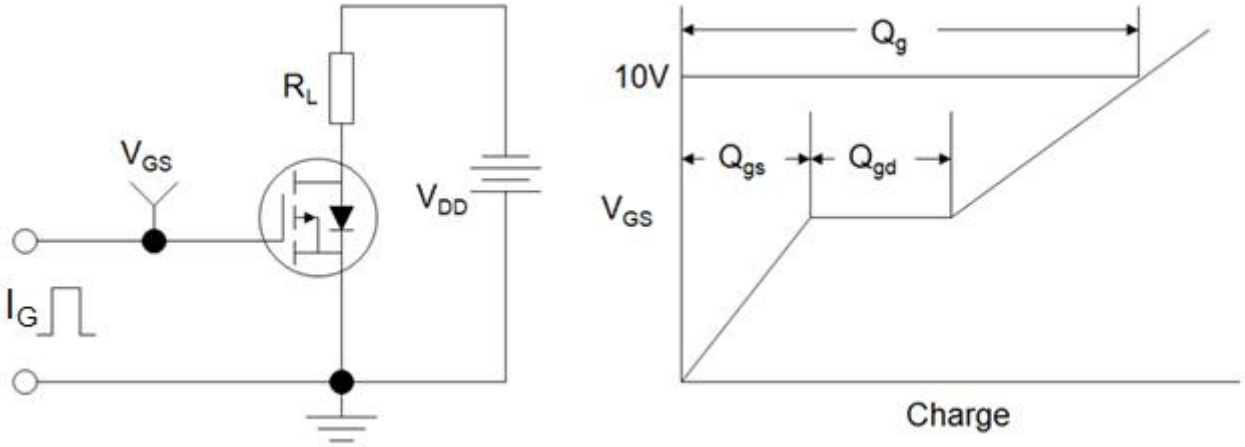


PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.5	-2.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -4A	--	37	45	mΩ
		V_{GS} = -4.5V, I_D = -4A	--	57	70	
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -4A	--	8	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	--	608	--	pF
Output Capacitance	C_{oss}		--	75	--	
Reverse Transfer Capacitance	C_{rss}		--	68	--	
Total Gate Charge	Q_g	V_{DD} = -15V, I_D = -4A, V_{GS} = -10V	--	11	--	nC
Gate-Source Charge	Q_{gs}		--	2	--	
Gate-Drain Charge	Q_{gd}		--	2.6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -4A, R_G = 3Ω	--	7.5	--	ns
Turn-on Rise Time	t_r		--	5.5	--	
Turn-off Delay Time	$t_{d(off)}$		--	19	--	
Turn-off Fall Time	t_f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-5	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -4A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -4A, V_{GS} = 0V di/dt=-100A/us	--	66	--	nC
Reverse Recovery Time	T_{rr}		--	53	--	ns

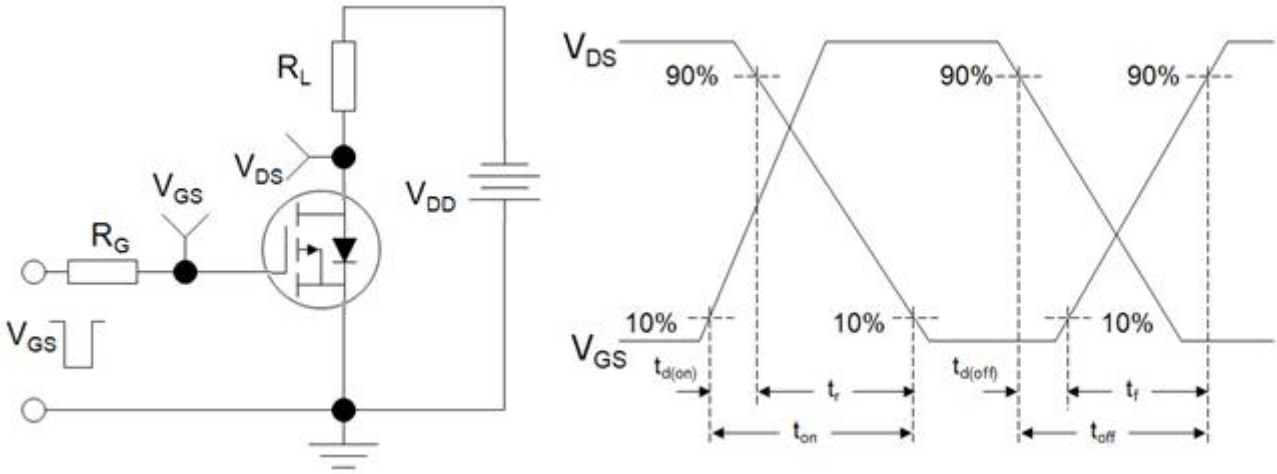
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=-30V,VGS=-10V,L=0.5mH,Rg=25Ω
   The table shows the minimum avalanche energy, which is 36mJ when the device is tested until failure
3. Identical low side and high side switch with identical R_G

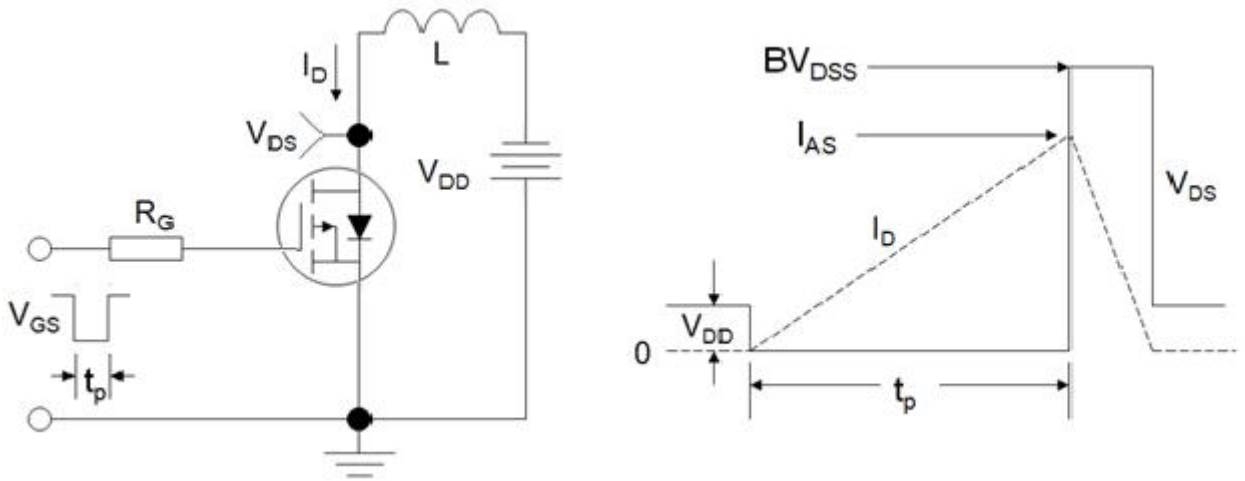
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

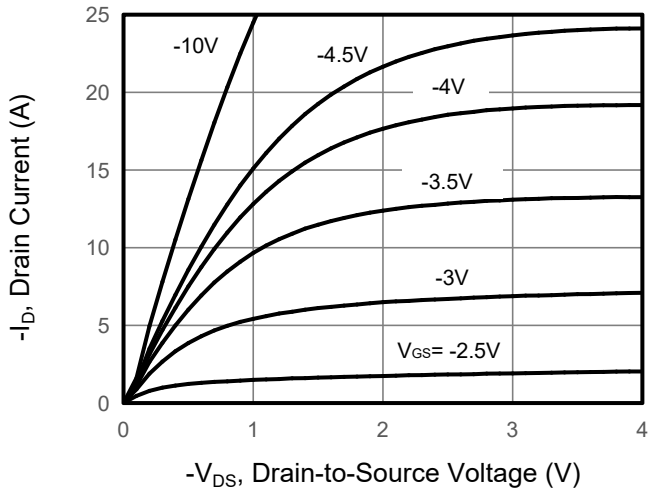


Figure 2. Transfer Characteristics

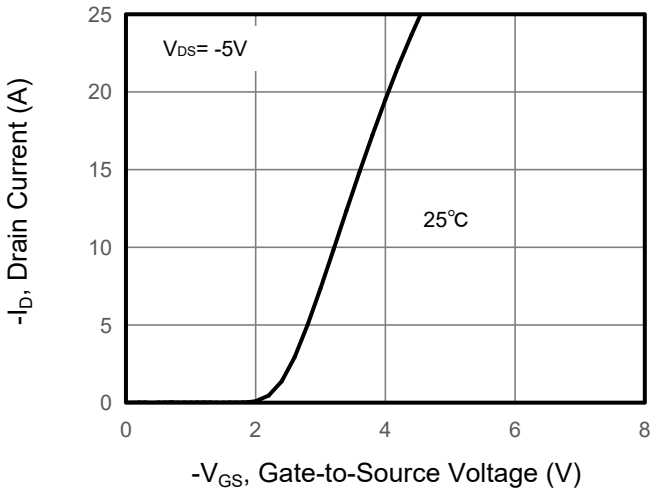


Figure 3.Drain Source On Resistance

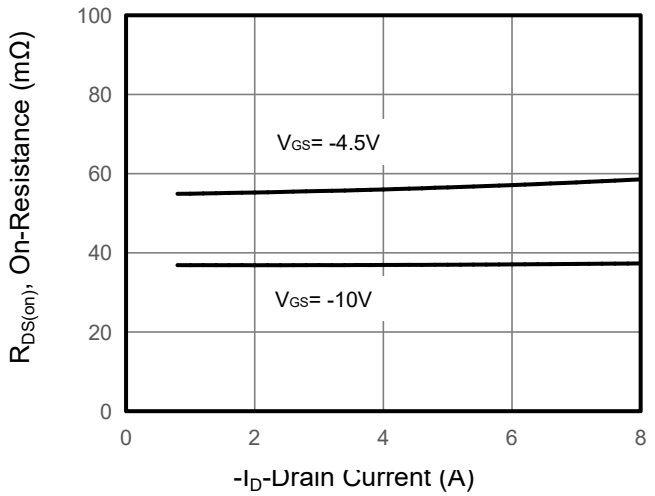


Figure 4. Gate Charge

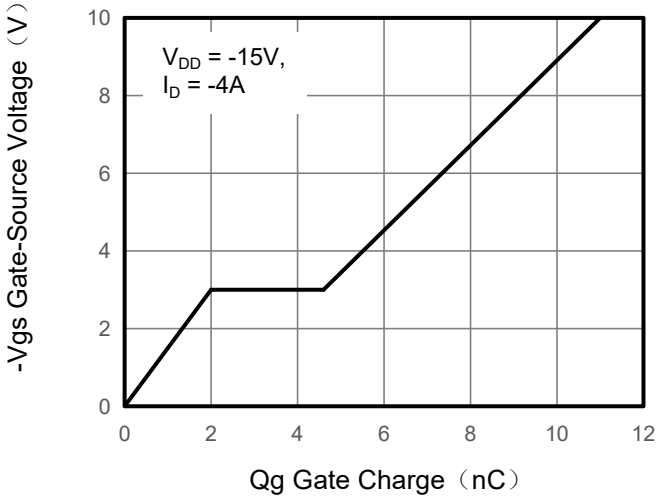


Figure 5. Capacitance

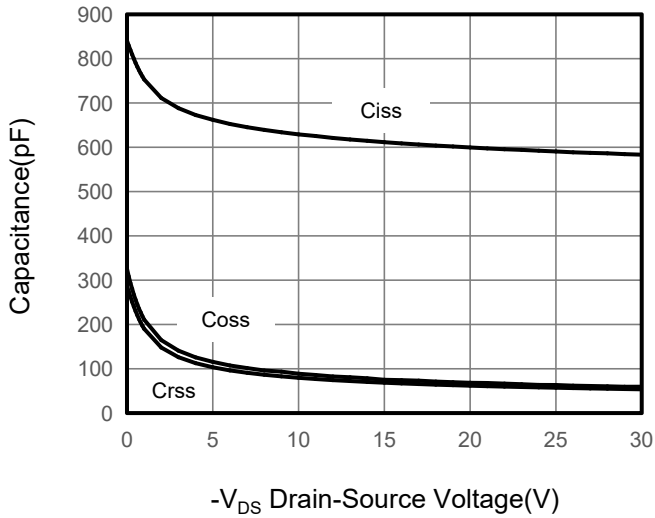


Figure 6. Source-Drain Diode Forward

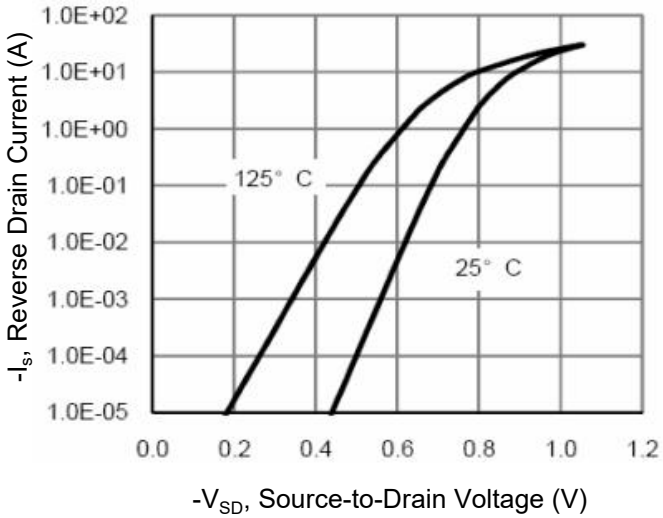


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Figure 7. Drain-Source On-Resistance

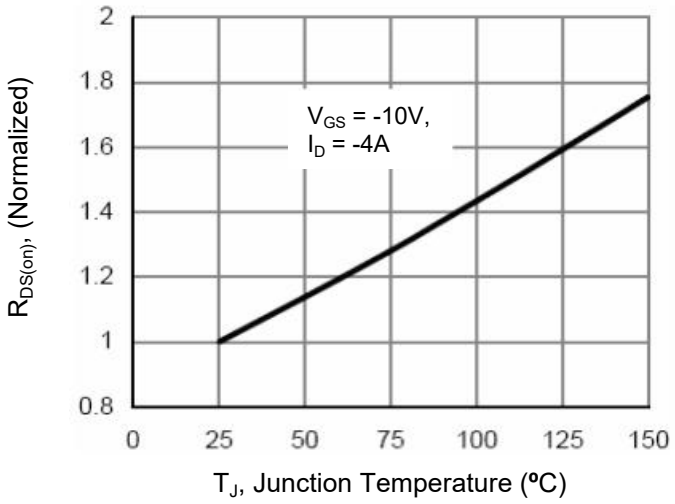


Figure 10. Safe Operation Area

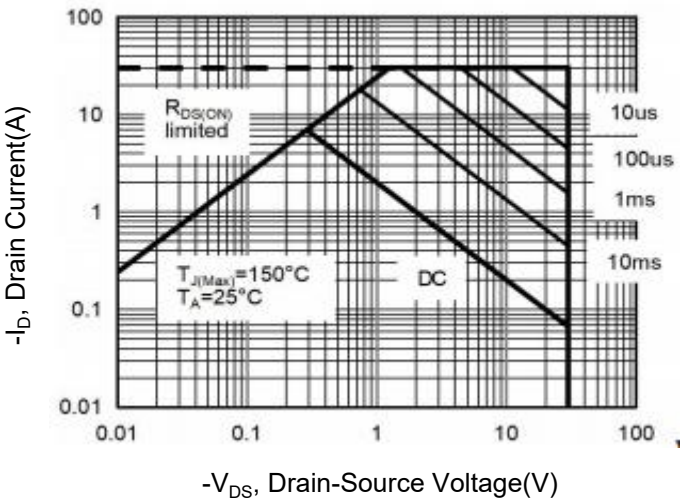
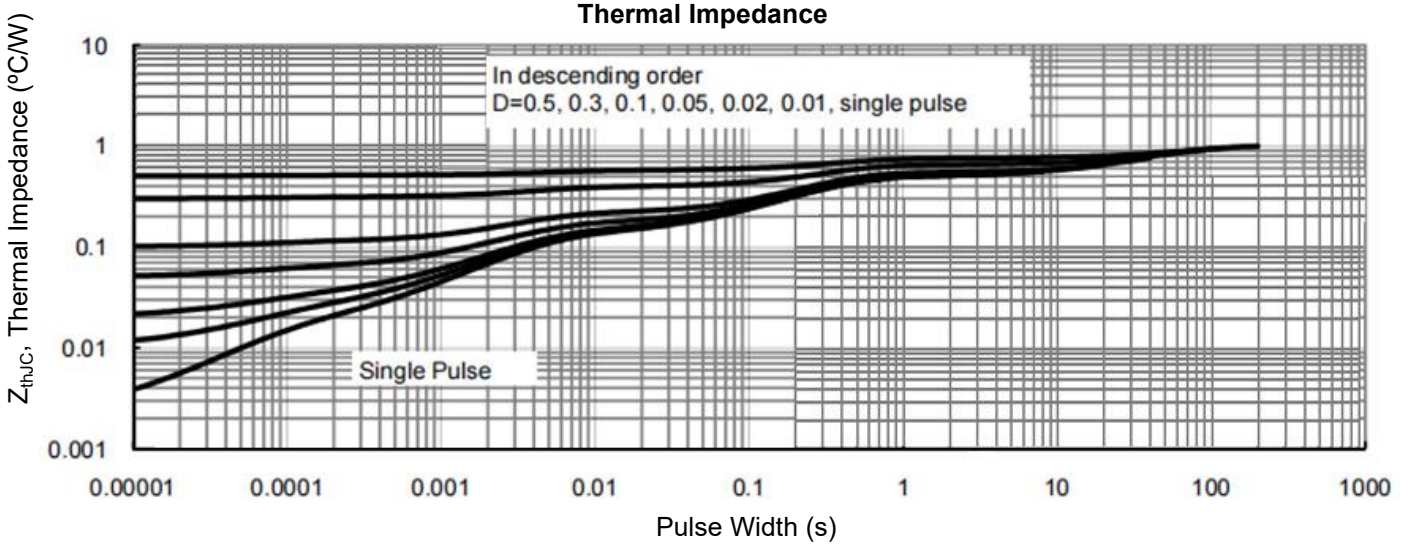
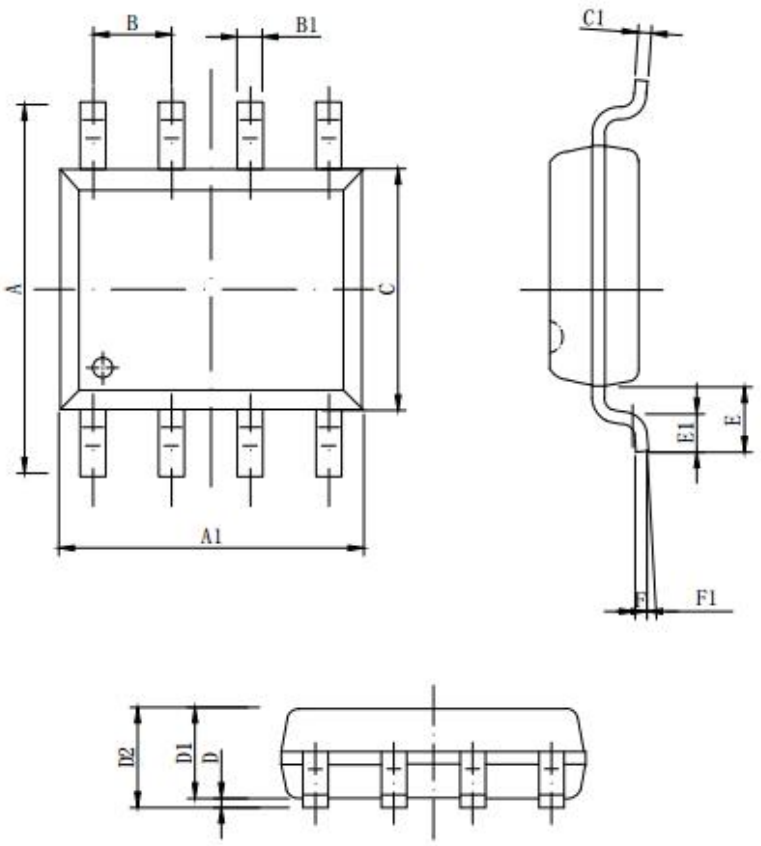


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Dual Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B		1.270BSC	
B1	0.35^8x	0.40^8x	0.45^8x
C	3.780	3.880	3.980
C1	--	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
D2	1.500	1.600	1.700
E		1.060REF	
E1	0.400	0.700	0.100
F		0.250BSC	
F1	2°	4°	6°