Evaluating the LTC9101-2A/LTC9101-2 and LTC9102 48-Channel IEEE 802.3at/bt PSE

GENERAL DESCRIPTION

The EVAL-LTC9101-2 is a 48-channel IEEE 802.3at/bt compliant power sourcing equipment (PSE). The EVAL-LTC9101-2 KIT includes the DC3159A-D or DC3159A-C daughter card, the DC3017A-B motherboard, and features the LTC9101-2A/LTC9101-2 and LTC9102 chipset.

In the EVAL-LTC9101-2 KIT, the daughter card has a single LTC9101-2A or LTC9101-2 digital controller. The DC3159A-D daughter card has the LTC9101-2A and the DC3159A-C has the LTC9101-2. The digital controller interfaces with four LTC9102 (12-channel) analog controllers for a total of 48 PSE channels.

The LTC9101-2A/LTC9101-2 use a proprietary isolated data interface allowing the LTC9101-2 to directly connect to the host controller I^2C interface and eliminating the need for costly optocouplers and an additional 3.3 V supply.

The EVAL-LTC9101-2A Kit connects to up to forty-eight, 802.3af/at PDs with an Ethernet splitter for each two ports for 2-pair power evaluation. This kit version requires host control over I^2C.

The EVAL-LTC9101-2 Kit connects to up to twenty-four, 802.3af/at/bt PDs directly at each port for 4-pair power evaluation. This kit version can operate autonomously or with host control over I^2C.

Indicator LEDs quickly show channel status for the 48 power channels. An optional on-board buck regulator provides 3.3 V from the V_{EE} supply for the digital circuity. This demonstration manual provides an EVAL-LTC9101-2 KIT overview and quick start procedure.

Design files for this circuit board are available at

https://www.analog.com/EVAL-LTC9101-2-KIT

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REVISION HISTORY

8/2023—Revision 0: Initial Version

EVAL-LTC9101-2 EVALUATION BOARD PHOTO

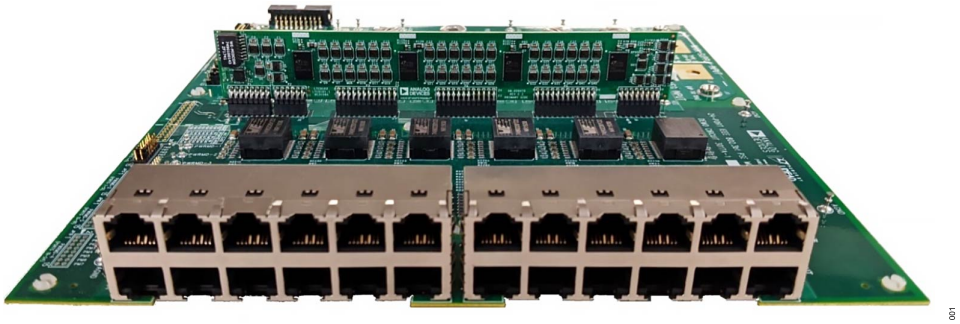

Figure 1. EVAL-LTC9101-2 Evaluation Board Photo

Table 1. EVAL-LTC9101-2-KIT Options

Demo Kit	IEEE Standard	Daughter Card	Mother Board	LTC9101 Version	2-Pair Ports	4-Pair Ports
EVAL-LTC9101-2A	802.3at	DC3159A-D	DC3017A-B	-2A	48	0
EVAL-LTC9101-2	802.3bt	DC3159A-C	DC3017A-B	-2	0	24

QUICK START PROCEDURE

Follow the procedure below and see Figure 2 through Figure 4, and Table 2 through Table 4 for proper equipment setup and default configuration.

NOTE: Step 1 only applies to the EVAL-LTC9101-2.

1. For autonomous operation with the EVAL-LTC9101-2, set the jumper PWRMD-1 (JP1) on the DC3017A-B motherboard to PM3 through PM7. See Table 2 for all PWRMD-1 options and the PWRMD Settings section for more information.
2. On the DC3017A-B motherboard, set the address switches AD2 and AD3 (SW5) to LO and JP22 (AD1) to LO for the default 0x20 base I^2C address.
3. On the DC3017A-B motherboard, set the CFG1 (JP20) and CFG1 (JP21) jumpers to HI to set CFG[1:0] logically to 11b to enable all ports. See Table 3 for more configuration options.
4. Align pin 1 of the 16-pin male connector P1 on the DC3159A daughter card with pin 1 of the 16-pin female connector J11 on the DC3017A-B motherboard as shown in Figure 3. The six male connectors and six female sockets should match. Keyed pins in J16 and J12 assist with the alignment shown in Figure 4. Carefully push the daughter card straight down until the male and female connectors are flush with each other.
5. Connect a supply to the DC3017A-B motherboard with the positive rail to POS INPUT (+) and negative rail to NEG INPUT (-) as shown in Figure 4. Use a power supply capable of sourcing the maximum power for all ports to be tested. Ramp the supply up to within the recommended voltage range specified in Table 4.

   NOTE: Banana jacks J8 and J10 should only be used for up to 15 A of supply current. Use the lug nut terminals J7 and J9 for supply currents of up to 50 A; enough for 24 ports at maximum IEEE 802.3bt power.
6. Connect the DC590B or other I^2C host controller at 14-pin connector (J1) as shown in Figure 4. Host control is required for EVAL-LTC9101-2A.
7. Connect IEEE 802.3af, 802.3at, or 802.3bt PDs to the motherboard's RJ45 connectors J3 and J4, as shown in Figure 4.

Table 2. EVAL-LTC9101-2 PWRMD-1 (JP1) Jumper Settings

PWRMD-1 Jumper Setting	R_{PWRMD} Resistor	Mode
PM0	OPEN	DISABLED
PM1	24.3k	RESERVED
PM2	18.7k	RESERVED
PM3	14.3k	Class 4: 25.5W
PM4	11.0k	Class 5: 40W
PM5	8.45k	Class 6: 51W
PM6	6.49k	Class 7: 62W
PM7	1.00k	Class 8: 71.3W

Table 3. EVAL-LTC9101-2-KIT CFG1 and CFG0 Jumper Settings

Jumper		# of Analog	
CFG1 (JP21)	CFG0 (JP20)	Controllers	Number of Channels
LO	LO	1	12
LO	HI	2	24
HI	LO	3	36
HI	HI	4	48

Table 4. EVAL-LTC9101-2-KIT Power Supply Voltage per PSE Type

IEEE 802.3 Type, Max Class	Supply Voltage Range
Type 2, up to Class 4 Type 3, up to Class 6	51 V to 57 V
Type 4, up to Class 8	53 V to 57 V

QUICK START PROCEDURE

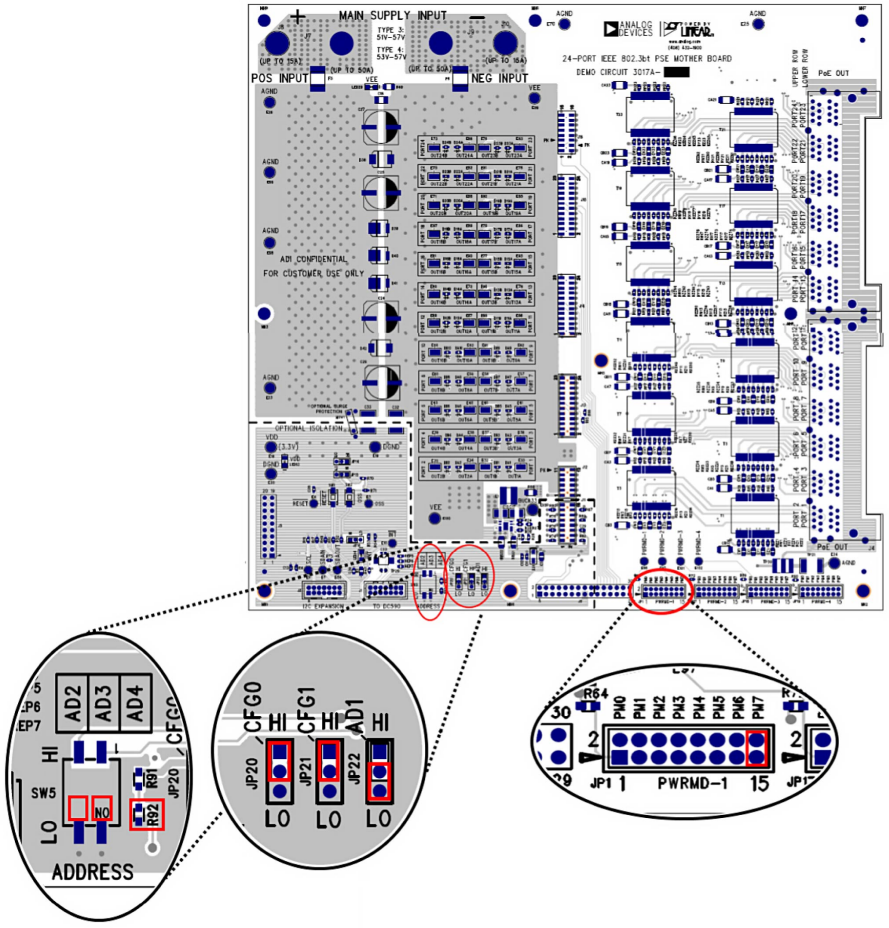

Figure 2. Default Settings for DC3017A-B Motherboard, Jumpers PWRMD0, AD1, CFG0, and CFG1; Switches: AD2 and AD3; Resistor options for AD4

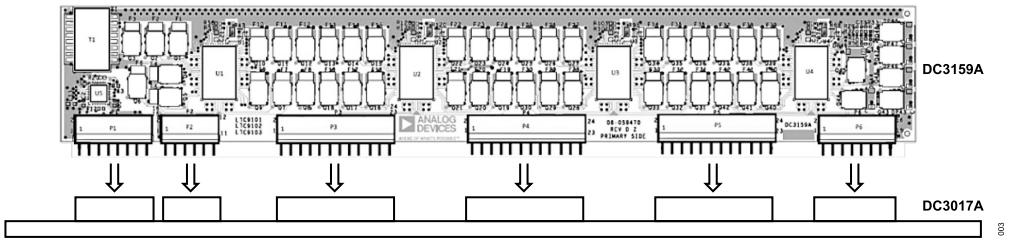

Figure 3. Inserting the DC3159A Daughter Card into J1 through J6 of the DC3017A-B Motherboard

QUICK START PROCEDURE

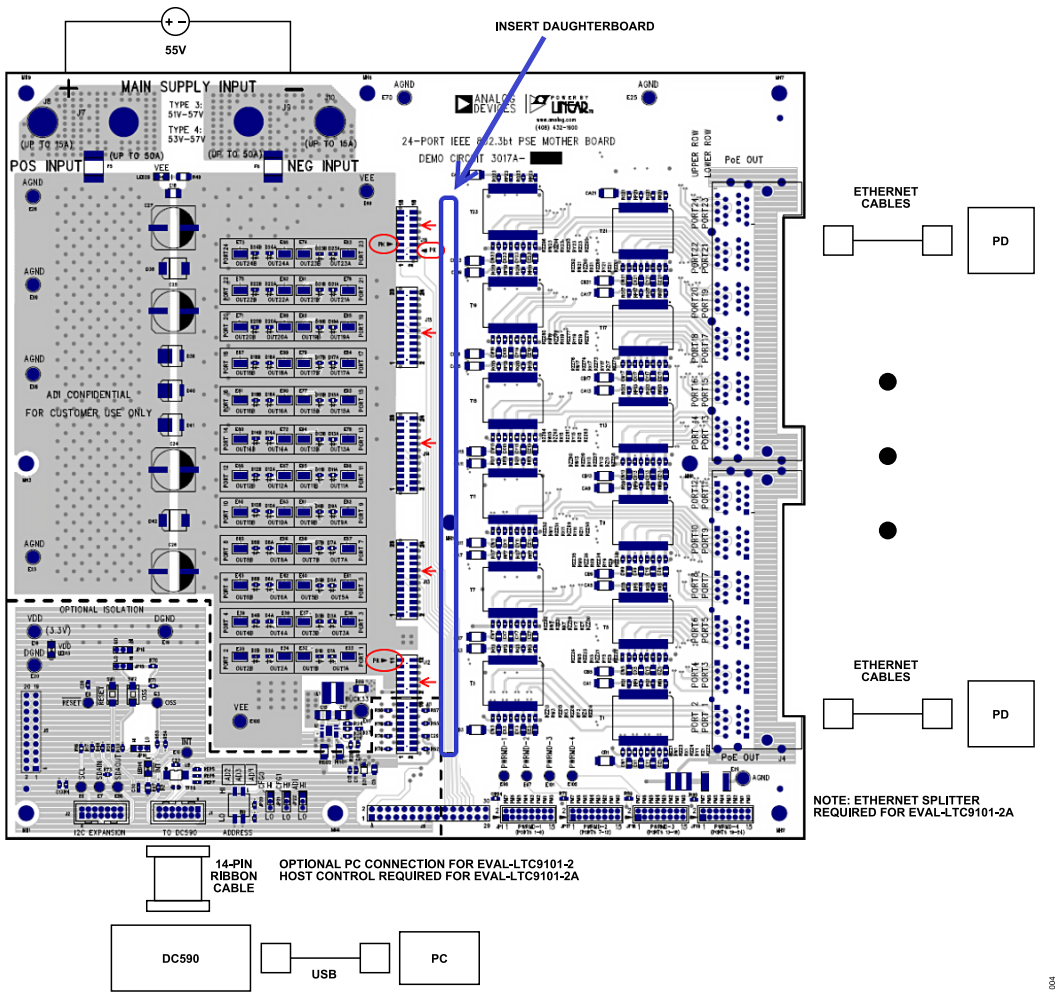

Figure 4. EVAL-LTC9101-2-KIT Connections

EVAL-LTC9101-2-KIT OVERVIEW

The EVAL-LTC9101-2-KIT includes the DC3017A-B, a 24-Port, 4-pair IEEE 802.3at/bt PoE PSE motherboard for a PSE endpoint. This motherboard accepts either the DC3159A-C or DC3159A-D daughter card with up to forty-eight power channels. It contains two, 2x6, RJ45 connectors and twenty-four 1000BASE-T Ethernet transformers rated for IEEE 802.3bt Type 4, Class 8 power levels. The DC3017A-B motherboard also has switches, jumpers, and push buttons for configuring the PSE, with status LEDs and test points.

PORT OUTPUT

The PDs are connected using an Ethernet cable (Cat5, Cat5e or better cabling as specified by IEEE 802.3) to any of the ports at the two, 2×6, RJ45 connectors J3 and J4 on the DC3017A-B motherboard. The LTC9101-2A delivers power over one power channel as a 2-pair PSE. The LTC9101-2 delivers power over two power channels as a 4-pair PSE. The term “channel” refers to the PSE circuitry assigned to a corresponding pairset. Each port on the DC3017A-B is connected as a 4-pair port driven by two power channels; OUTnA and OUTnB connect to port n (n = port #). OUTnA pairset connects to Alternative A (pairs 1, 2 and 3, 6) and OUTnB pairset connects to Alternative B (pairs 4, 5 and 7, 8). Test points for each channel output, OUT1A through OUT24B are provided.

A 2-pair PSE uses a single power channel per port, connected to either Alternative A or Alternative B. EVAL-LTC9101-2A requires an Ethernet splitter to separate each 4-pair port into two 2-pair ports. See Evaluating the EVAL-LTC9101-2A for more information. See Figure 5 for the port output map of the EVAL-LTC9101-2A.

The EVAL-LTC9101-2 supports 24, 4-pair ports. See Figure 6 for the port output map of the EVAL-LTC9101-2.

DAUGHTER CARD INSERTION PRECAUTIONS

When inserting or removing the daughter card into the DC3017A-B motherboard, verify all supplies and LEDs are off. Push the card straight down for insertion or pull straight up for removal to avoid bending the connector pins. Follow the instructions in the Quick Start Procedure for alignment and see Figure 3.

LED INDICATORS

The V_{EE} LED (D29) and V_{DD} LED (LED13) indicate if a voltage is present at the respective supplies. Verify these LEDs are off before inserting or removing the daughter card.

Each port pairset power channel has a respective OUTnM (n = port #, M = port powered pairset; with A = Alternative A and B = Alternative B) LED to indicate if the channel is detecting, classifying, or powered. A blue LED is connected to each OUTnA, while a green LED is connected to each OUTnB. The red $\overline{INT}$ LED (LED14) indicates if the interrupt line is pulled low by the daughter card.

I²C ADDRESS

LTC9101-2A or LTC9101-2’s primary 7-bit serial bus address is $01A_4A_3A_2A_10b$, with bits A[4:1] set by the pins AD[4:1] respectively. AD1 is set by the AD1 jumper (JP22), AD2 and AD3 are set by the Address switch (SW5), and AD4 is set by resistor stuff options, R91 (HI) and R92 (LO).

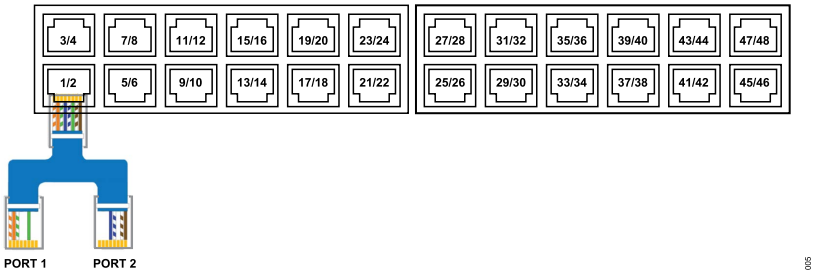

Figure 5. EVAL-LTC9101-2A Port Output Map

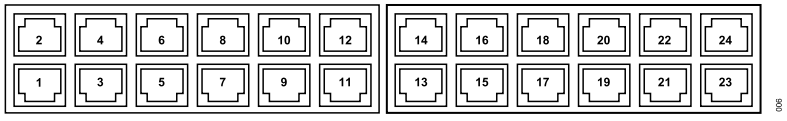

Figure 6. EVAL-LTC9101-2 Port Output Map

EVAL-LTC9101-2-KIT OVERVIEW

MAIN V_{EE} POE SUPPLY

The V_{EE} supply is the main PoE supply connected to the DC3017A motherboard. See the Quick Start Procedure for proper connection and Table 4 for appropriate supply voltage ranges.

Choose a power supply with a current limit set higher than the maximum allowed output power at each port. Use the appropriate input supply connections per the maximum current expected during testing; banana jacks for up to 15 A or Panduit S4-14R lug nuts for up to 50 A, as seen in Figure 7. The lugs are designed for crimping to 4 AWG welding cable. Use a Thomas & Betts WT115 crimping tool to crimp the S4-14R lugs to 4 AWG welding cable; do not mash or solder the lugs. To avoid damage to the motherboard, do not over tighten the lugs. A torque sufficient to fully compress the split washer (roughly equivalent to 400 in-oz applied to the ¼-28 hex nut) is sufficient to produce good electrical contact.

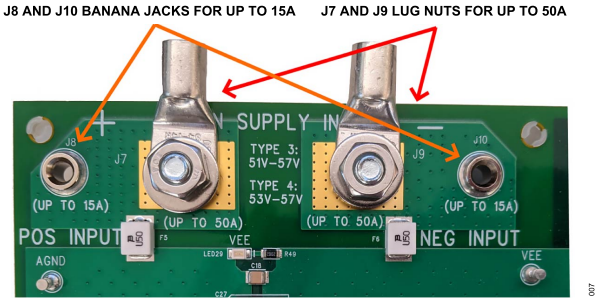

Figure 7. Motherboard Power Supply Connections

ISOLATION

The IEEE 802.3 Ethernet specifications require network segments (including the analog PoE circuitry) to be electrically isolated from the chassis ground. The DC3017A motherboard and DC3159A daughter card layouts and high voltage capacitors provide an isolation barrier between Analog and Digital domains. Transformers provide a galvanic barrier between DGND and AGND on the DC3159A daughter card. By default, this isolation barrier is bridged by resistors on the motherboard to allow for evaluation using a single power supply. Remove RISO1 and RISO2, then provide an external 3.3 V supply between V_{DD} and DGND to evaluate this board as an isolated system.

All RJ45 shields and terminations are connected to chassis ground. AGND and V_{EE} each connect to chassis ground with two pairs of 1 nF, 2 kV capacitors (C6-C9). AGND and V_{EE} also connect to DGND each with 10 nF, 2 kV capacitors (C32-C33). An optional 0 Ω resistor can be installed at RISO3 to tie the chassis ground to DGND. Two series 1206, 5.1 MΩ resistors connect between AGND and DGND for high voltage capacitance discharge. See Figure 8 for connections between Analog and Digital domains, as well as chassis ground on the DC3017A motherboard.

The DC3159A daughter card is laid out with isolation.

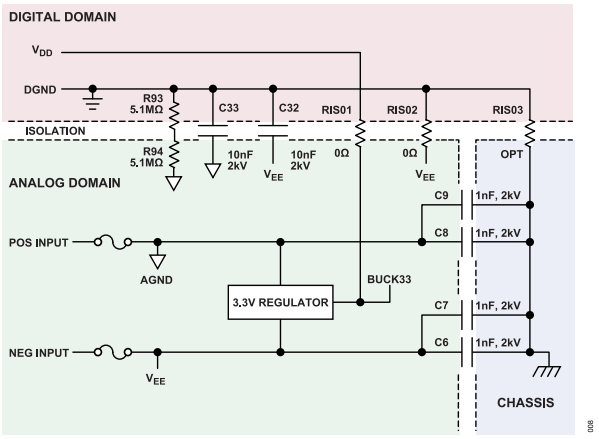

Figure 8. Motherboard Power Supply Connections and Isolation Barriers

PWRMD SETTINGS

The LTC9101-2/LTC9102 operating mode and maximum class while in auto mode depends on the PWRMD0 pin state of the LTC9102 at bus address ID:00b during reset. Reset occurs on a V_{DD} or V_{EE} power cycle, $\overline{RESET}$ pin is pulled low and released high, or when the global Reset All bit is set. Changing the state of this pin will not change the PSE configuration until a reset occurs. The PWRMD0 pin connects to the R_{PWRMD} resistor using the PWRMD-1 jumper. R_{PWRMD} is used to automatically determine the power allocation per port. See Table 2 for the PWRMD0 and R_{PWRMD} settings. The LTC9101-2A does not check the PWRMD0 pin state.

DEVICE CONFIGURATION

The CFG0 and CFG1 pins configure the number of analog controllers in the system. Each pin connects to a jumper that pulls either HI for a logical 1, or LO for logical 0. CFG1 and CFG0 set the number of analog controllers in the system. See Table 3 for the CFG[1:0] settings.

DIGITAL CONNECTIONS

The DC590 USB to I^2C controller board is connected to the DC3017A-B motherboard at J1 through a 14-pin ribbon cable. The LTC9101-2A or LTC9101-2 I^2C address is set by the pins AD4, AD3, AD2, and AD1. See I2C Address section for more information. SDAOUT and SDAIN can be tied together through a shunt resistor, R73. Turrets on the DC3017A-B motherboard provide test points for SCL, SDAIN, SDAOUT, V_{DD}, DGND, $\overline{INT}$, OSS, and $\overline{RESET}$.

OSS AND $\overline{RESET}$ PUSH BUTTONS

Push button switch SW1, when pressed, pulls the $\overline{RESET}$ pin of the daughter card logic low. The PSE controller is then held inactive with all ports off. When SW1 is released, $\overline{RESET}$ is pulled high, and the PSE returns to the reset state.

Push button switch SW2, when pressed pulls the overload supply shutdown input, OSS pin of the daughter card logic low. When

EVAL-LTC9101-2-KIT OVERVIEW

pressed, all ports that have their corresponding mask bit set in the mconfig register of the PSE controller will be shutdown. These ports must then be manually re-enabled via I^2C or by resetting the PSE.

ON BOARD 3.3 V SUPPLY

The DC3017A-B motherboard has an on board (non-isolated) 3.3 V/100 mA buck regulator that provides a local 3.3 V, with the net named BUCK33. This on board logic supply is for demonstration purposes only and allows for use of a single supply while evaluating the EVAL-LTC9101-2-KIT.

SURGE TESTING

The EVAL-LTC9101-2-KIT can be configured with either the Digital domain connected to reference ground plane, or with the Digital domain floating with the Analog domain for different surge test setups. The default EVAL-LTC9101-2-KIT configuration has DGND connected to V_{EE} and floating from chassis ground.

EVALUATING THE EVAL-LTC9101-2A

The LTC9101-2A/LTC9102 PSE chipset supports only 2-pair operation, but the DC3017A-B motherboard layout is specifically for 4-pair ports. Each 4-pair port must be physically split into two separate 2-pair ports using an Ethernet splitter such as Tripp Lite's N035-001 or a custom "Y-Cable". One N035-001 is included with the EVAL-LTC9101-2A for evaluation purposes.

An Ethernet splitter splits the pairsets from one RJ45 port at the PSE to two separate RJ45 ports that connect to two separate PDs. An Ethernet splitter is required for each RJ45 port on the EVAL-LTC9101-2A. Figure 9 shows a "Y-Cable" that connects Alternative A from the EVAL-LTC9101-2A (pairs 1, 2 and 3, 6) to the Alternative A of one PD, and connects Alternative B from the EVAL-LTC9101-2A (pairs 4, 5 and 7, 8) to Alternative B for the second PD. The odd port is Alternative A, while the even port is Alternative B.

The LTC9101-2A/LTC9102 PSE chipset requires host control over I^2C. A DC590 connected to J1 on the motherboard allows for I^2C configuration via the users PC. For more information contact Analog Devices Applications.

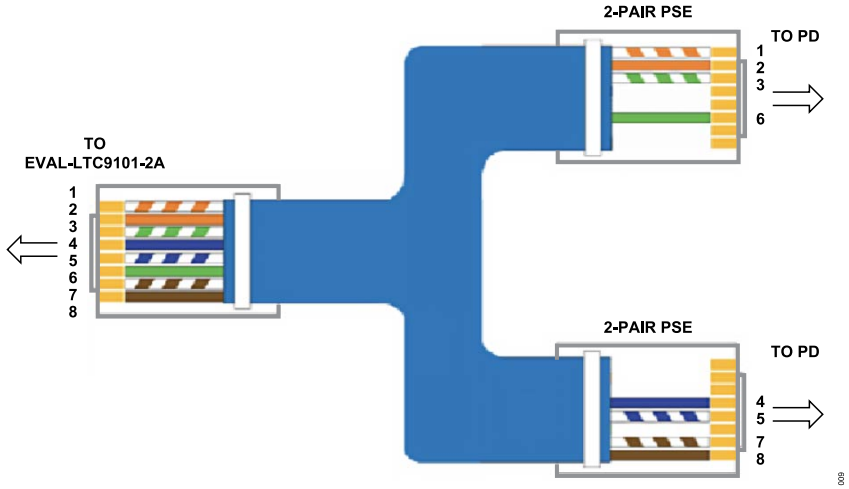

Figure 9. Example Connections and Pin-Out for Ethernet Splitter or "Y-Cable"

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.