TI Designs

IEC 61000 ESD, EFT, and Surge Bus Protection for CAN Reference Design



TI Designs

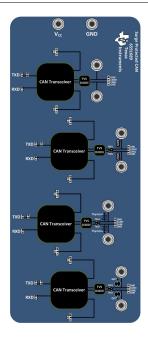
TI Designs provide the foundation that you need including methodology, testing and design files to quickly evaluate and customize the system. TI Designs help *you* accelerate your time to market.

Design Resources

TIDA-00629 Design Folder
TCAN1042 Product Folder
TCAN1051 Product Folder
SN65HVD267 Product Folder
SN65HVD257 Product Folder
SLOA101 Application Report



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Design Features

- Board Level IEC 61000-4-2 ESD Evaluation
- Board Level IEC 61000-4-4 EFT Evaluation
- Board Level IEC 61000-4-5 Surge Evaluation
- Easy Control of Transceivers Logic I/O Pins
- Pad Site Evaluation of Multiple TVS Diode Structures
- Bourns Transient Blocking Unit (TBU) High Speed Protection
- Bourns Radial Leaded Metal Oxide Varistor (MOV)
 Overvoltage Protection
- Bourns Thyristor Overvoltage Protection
- Bourns Gas Discharge Tube (GDT) Overvoltage Protection
- General Purpose Evaluation Module For Half-Duplex TI CAN Transceivers

Featured Applications

- Classical CAN and CAN FD Operation in Highly Loaded CAN Networks Down to 10- kbps Networks Using TXD DTO
- Industrial Automation, Control, Sensors, and Drive Systems
- Building, Security, and Climate Control Automation
- CAN Bus Standards Such as CANopen, DeviceNet, NMEA2000, ARNIC825, ISO11783, and CANaerospace





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Design Overview www.ti.com

1 Design Overview

Industrial networks such as CAN, RS-485, RS-422, RS-232, and Profibus are expected to withstand harsh system-level transients in their end applications without being damaged. These events can be caused by electrostatic discharge during handling, interruption of inductive loads, relay contact bounce, or lightning strikes. Designing to meet these requirements can be challenging without the proper tools and knowledge about the standards that the design requires.

The IEC 61000 ESD, EFT, and Surge Bus Protection for CAN Reference Design (TIDUB36) shows a practical example of how to protect the most sensitive components against these lethal transients. This documentation walks through the ISO 11898 standard, the IEC 61000-4-x transient test standards, and the implementation of system level protection against these transients with overall schematic design and layout.

2 Standards

There are many standards that may be referenced by engineers looking to ensure ESD robustness in their end design. Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM) are the most common ESD standards in industry, as most vendors provide data on these parameters in the supporting documentation for a given device. These traditional ESD models do not take into account system-level ESD events and are solely meant as device level specs. These specifications ensure that the device makes it through the handling and assembly process without being damaged by ESD.

HBM, MM, and CDM are sufficient models for many applications, but some industrial applications are subjected too much greater stresses than the energy levels that these standards deliver. The next three sections discuss the IEC 61000-4-2 Electrostatic Discharge Immunity Test, IEC 61000-4-4 Electrical Fast Transient/Burst Immunity Test, the IEC 61000-4-5 Surge Immunity Test standards and the expected levels of energy the industrial system may see.



www.ti.com Standards

2.1 IEC 61000-4-2 Electrostatic Discharge Immunity Test

The IEC 61000-4-2 ESD immunity test is a system-level ESD test that imitates a charged operator discharging onto an end system. The characteristics of the IEC ESD test differ from that of other ESD standards in rise times, the amount of energy delivered during the strike, and the number of strikes administered during the testing. There are two types of testing methods involved with the IEC ESD: contact discharge and air discharge. The contact ESD test discharges an ESD pulse from an IEC ESD gun directly onto the device under test (DUT). The air ESD discharge test involves moving the charged ESD gun towards the DUT until the air breaks down enough to allow conduction of the ESD strike between the ESD gun and the DUT. The IEC ESD testing is performed with both positive and negative polarities, and a passing score is not achieved unless both polarities at a single level are survived. Table 1 lists the IEC 61000-4-2 ESD test voltage levels and the peak current levels.

			_		
CONTACT DISCHARGE			AIR DISCHARGE		
Level	Level Test Voltage (kV) Peak Cu		Level	Test Voltage (kV)	
1	2	7.5	1	2	
2	4	15	2	4	
3	6	22.5	3	8	
4	8	30	4	15	
*	Special	Special	*	Special	

Table 1. IEC 61000-4-2 ESD Test Voltage Levels

NOTF:

* is an open level. The level must be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be required.

Figure 1 shows the basic shape of the IEC ESD pulse and shows the timing sequence of the test pulses.

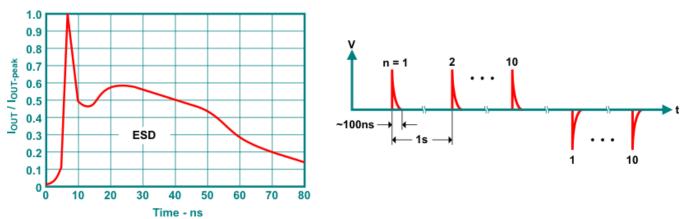


Figure 1. Current Waveform of the IEC ESD Pulse and Timing Sequence of the Test



Standards www.ti.com

2.2 IEC 61000-4-4 Electrical Fast Transient and Burst Immunity Test

The IEC 61000-4-4 electrical fast transient (EFT) or burst immunity test is meant to simulate the switching transients caused by the interruption of inductive loads, and relay contact bounce. The EFT test is performed on power lines, I/O data lines, I/O control lines and earth wires. The EFT test is a burst of pulses that have predetermined amplitude and limited duration. The typical duration of a burst is 15 ms at a repetition rate of 5 kHz, although 100 kHz repetition is a more realistic test. The burst period, which is the time from the start of one burst to the start of the next burst, is 300 ms. The test requires the application of six burst frames of ten seconds duration with ten second pauses between frames. In a typical EFT test sequence 3 million pulses are delivered to the DUT through a capacitive clamp which couples the energy into the system. Table 2 lists the IEC 61000-4-4 EFT test voltage levels and repetition rates:

ON POWER PORT, PE ON I/O SIGNAL, DATA AND CONTROL PORTS Repetition Level Test Voltage (kV) Test Voltage (kV) Repetition Rate (kHz) Rate (kHz) 0.5 5 or 100 0.25 5 or 100 5 or 100 2 1 0.5 5 or 100 3 2 5 or 100 1 5 or 100 4 4 5 or 100 2 5 or 100 Special Special Special

Table 2. IEC 16000-4-2 ESD Test Voltage Levels

NOTE: * is an open level. The level must be specified in the dedicated equipment specification.



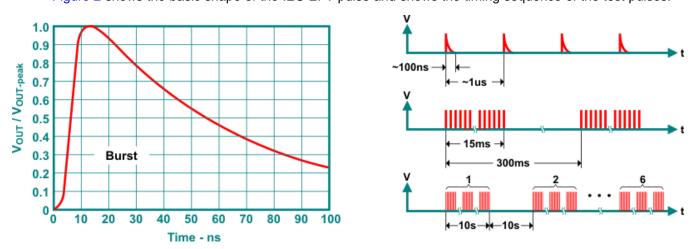


Figure 2. Voltage Waveform of an EFT (Burst) Pulse and Timing Sequence of an Entire Test Cycle



www.ti.com Standards

2.3 IEC 61000-4-5 Surge Immunity Test

The IEC 61000-4-5 surge immunity test is the most severe transient immunity test in terms of current and duration. This test is meant to simulate transients caused by direct or indirect lightning strikes as well as the switching of power systems including load changes and short circuits.

The surge generator's output waveforms are specified for open and short circuit conditions. Characteristics for this test are high current (due to low generator impedance) and long pulse duration. Pulse duration for the surge immunity test is approximately 1000 times longer than that of IEC ESD and IEC EFT, resulting in high-energy pulses.

This test requires five positive surge pulses and five negative surge pulses with a time interval between pulses of one minute. Typically though, this time interval is reduced to something shorter than one minute to help reduce overall test time. Table 3 lists the IEC surge open circuit voltage test levels.

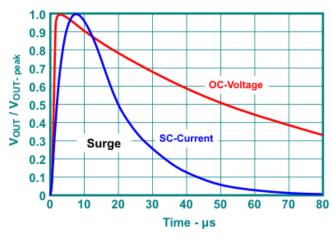
LEVEL	OPEN-CIRCUIT VOTLAGE ±10% (kV)
1	0.5
2	1
3	2
4	4
*	Special

Table 3. IEC Surge Open Circuit Voltage Test Levels

NOTE: *

* May be any level above, below, or in between the other levels. This level may be specified in the product standard.

Figure 3 shows the basic shape of the IEC surge pulse and shows the timing sequence of the test pulses.



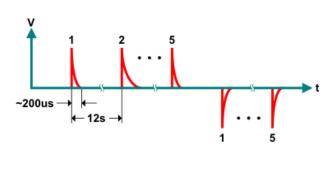


Figure 3. Voltage and Current Waveform of a Surge Pulse and Timing Sequence of a Test Cycle



System Description www.ti.com

3 System Description

In this TI Design, there are four different protection circuit architectures using devices from Bourns Inc[™]. Circuit one encompasses a TVS diode on the bus pins, circuit two implements the same TVS diode on the bus pins along with metal oxide varistors (MOVs) and a transient blocking unit (TBU). Circuit three again uses the TVS diode and TBU, but the MOV is replaced by a thyristor, and in circuit four the thyristor is swapped for a gas discharge tube (GDT). All of these circuits provide protection for the CAN transceiver from lethal ESD, EFT (burst), and surge transients.

The TVS diode acts as a clamping circuit redirecting the transient energy to ground, protecting the transceiver from dangerous over voltage conditions. The MOV, thyristor, and GDT protect the Bourns TBU from exposure to excessive transient voltage, clamping the transient to a level less than the impulse. When the transient current exceeds the TBU trigger current limit, the sub-microsecond response of the TBU limits the current flow to the transceiver. The MOV, thyristor, and GDT reduce the transients to a few hundred volts of clamping voltage while the TBUs limit transient current to less than 1 mA. Figure 4 shows the TI Design with all components.

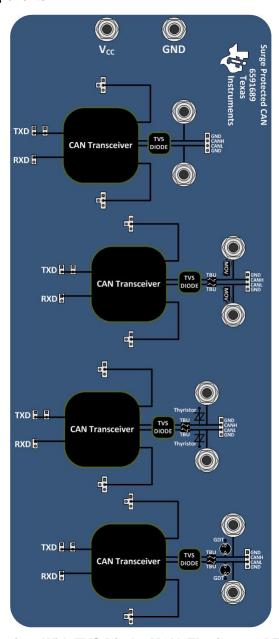


Figure 4. CAN Transceiver With TVS Diode, MOV, Thyristor, GDT, and TBU MOSFETs



4 ISO11898-4 2 Standard and Transceivers

4.1 ISO11898-2 Standard

Controller area network or CAN is an International Standardization Organization (ISO) defined serial communication bus originally developed for the automotive industry to replace the complex wiring harness with a two-wire bus. The specification calls for high immunity to electrical interference and the ability to self-diagnose and repair data errors. These features have led to expanded popularity for CAN in industrial applications such as building automation, process control automation, elevators, construction equipment, and robotics, amongst many others.

The CAN communications standard, ISO-11898, follows the open systems interconnection (OSI) model and defines functions in terms of layers. The specification of the physical layer, which is where the TI transceiver resides, is summarized in section two of the ISO11898 standard (ISO11898-2). ISO11898-2 describes the physical layer for classical CAN as a differential bus technology that supports a maximum signaling rate of 1Mbps over a bus length of 40 meters with a maximum of 30 nodes. The ISO 11898-2 document also describes the DC and AC requirements that a CAN transceiver must meet in order to be considered complaint. The document states that a transceiver must support a minimum output differential voltage of 1.5 V across a 54Ω load and a nominal differential input capacitance of 10-pF.

TI CAN transceivers meet or exceed the requirements set by the ISO 11898 standard and support other features such as V_{IO} voltage support, shutdown mode, slope control, and integrated IEC ESD protection. While all of these features are nice to have, this TI Design only focuses on the SN65HVD267 (a standard 5-V CAN transceiver with integrated IEC ESD protection designed for 2-Mbps operation), and the SN65HVD257 (a standard 5-V CAN transceiver with integrated IEC ESD protection designed for 1-Mbps operation).

4.1.1 TCAN1042

The TCAN1042 transceiver supports half-duplex operation and is designed for CAN FD data bus networks in demanding industrial applications. The TCAN1042 is powered by a 5-V supply, supports CAN FD data rates up to 5 Mbps, and is fully compliant to the ISO11898-2 standard. The TCAN1042 is feature-rich with under voltage protection (UVLO) on the supply pins and VIO pin, \pm 70-bus fault protection, receiver dominant state timeout (RXD DTO), driver dominant state timeout (RXD DTO), and thermal shutdown protection. The bus pins, CANH and CANL, have integrated ESD protection making them robust to ESD events with high levels of protection against HBM, CDM, IEC 61000-4-2, and ISO7637. The TCAN1042 exceeds \pm 8-kV contact and \pm 15-kV air discharge of IEC61000-4-2 ESD protection, and \pm 10 kV HBM protection on die.

4.1.2 TCAN1051

The TCAN1051 transceiver compliments the TCAN1042 described in Section 4.1.1, but possesses a silent function rather than the standby function present in the TCAN1042.

4.1.3 SN65HVD267

The SN65HVD267 transceiver supports half-duplex operation and is designed for CAN data bus networks in demanding industrial applications. The SN65HVD267 device is powered by a 5-V supply, supports CAN FD data rates up to 2 Mbps, and is fully compliant to the ISO11898-2 standard. The SN65HVD267 is feature-rich with under voltage protection (UVLO) on the supply pins, –27 to 40 V bus fault protection, receiver dominant state timeout (RXD DTO), driver dominant state timeout (RXD DTO), thermal shutdown protection, and a fault pin output redundancy. The bus pins, CANH and CANL, have integrated ESD protection making them robust to ESD events with high levels of protection against HBM, CDM, IEC 61000-4-2 and ISO7637. The SN65HVD267 supports ±8 kV of IEC 61000-4-2 ESD protection, ±12 kV HBM protection, and ±4kV IEC EFT protection on die.

4.1.4 SN65HVD257

The SN65HVD257 transceiver compliments the SN65HVD267 described in Section 4.1.3, but is optimized for data rates up to 1 Mbps rather than 2 Mbps.



System Design Theory www.ti.com

5 System Design Theory

This TI Design features four robust protection schemes; a TVS diode, a transient blocking unit (TBU), a metal oxide varistor (MOV), a thyristor, and a gas discharge tube. The board contains a pad site for an 8-pin SOIC CAN transceiver with the SN65HVD267 installed, and banana jacks for injecting the ESD, EFT, and surge test pulses. The concept behind the design is to protect the CAN transceiver from lethal transients caused by electrostatic discharge during handling, interruption of inductive loads, relay contact bounce, and/or lightning strikes. Without protection, energy that is delivered during one of these transient events can be large enough in amplitude to permanently damage the device.

The TVS is used to provide protection against voltage transients. It acts as a clamping circuit to redirect any high energy pulses to ground and away from the transceiver. The diode needs to be rated for the type of energy levels that are expected per the design. This design was done with the IEC 61000-4-2 standard in mind, and uses the CDSOT23-SM712 as it is rated for this type of application.

The TBU high speed protector is used to shield the TVS diode and the CAN transceiver from AC power cross events or large transients, as well as over current conditions. When the transient current exceeds the trigger current level on the TBU device, the TBU clamps or crowbars the current to a safe level by transitioning to a high impedance state.

The MOV, thyristor, and GDT protect the TBU device from high voltage surges caused by lightning strikes, power contact, and power induction. The MOV, thyristor, and GDT devices have fast turn on times and high current handling capability to protect the TBU, TVS, and CAN transceiver. The reason behind providing separate circuits for the MOV, thyristor, and GDT is that they each provide a different level of protection. Table 4 lists the level of protection provide by each device.

Table 4. Overvoltage Protection Levels

DEVICE	PROTECTION LEVEL
Metal Oxide Varistor (MOV-10D201K)	185 V
Thyristor (TISP424M3BJR-S)	240 V
Gas Discharge Tube (2031-42T-SM- RPLF)	360 V



www.ti.com Getting Started Hardware

6 Getting Started Hardware

The TIDUB36 design includes a CDSOT23-SM712 TVS diode from Bourns, a TBU-CA0065-200-WH from Bourns, a MOV-14D561KTR from Bourns, a TISP4240M3BJR-S from Bourns, a 2031-42T-SM-RPLF from Borns, and a TCAN1042 CAN transceiver from TI. The device is placed into normal operating mode by pulling pin 8 of the transceiver low through JMP1 for circuit one, JMP7 for circuit 2, JMP13 for circuit 3, and JMP19. Once the proper mode is enabled, the device functionality can be checked via the two pin berg header labeled TXD which is the driver pin, the two pin berg header labeled RXD which is the receiver pin, and the bus pins via the four pin berg header labeled CANH and CANL.

Once device functionality is verified, the transient testing can be done via the two banana jacks connected to the bus pins. The IEC ESD contact test pulses may be injected onto the bus pins by directly touching the banana jacks to discharge the pulses. The IEC ESD air test pulses can be injected on the bus pins by approaching the banana jack slowly until the ESD gun discharges. Care must be taken to ensure that the appropriate bus pin is struck during the air testing as the ESD pulse can jump from location to location on the board. The EFT test can be performed by connecting a bus wire to the CANH and CANL pins and inserting the wire into the capacitive clamp defined by the IEC 61000-4-4 standard. The surge generator uses shrouded banana jacks to couple the energy onto the bus pins directly.

When performing these types of compliance tests, the test methods should be followed as they are laid out in the standards documentation. After each test level is completed the leakage current should be observed and verified with the leakage current prior to the test, as this may be an indication that something has been broken in the device. The device should be checked for general functionality in both the driver and receiver directions. Figure 5 shows an overview of the board with descriptions of each point.



Figure 5. RS-485 Transient EVM Overview



Test Setup www.ti.com

7 Test Setup

Figure 6, Figure 7, and Figure 8 show the test setups used in the IEC immunity compliance testing for this CAN design. Figure 6 shows the IEC ESD setup. The setup used for this testing is fully compliant to the IEC ESD specification. Figure 7 shows the EFT and surge generator box. The EFT/surge generator box is made by EMC-Partner and is model number CDN-UTP. Figure 8 shows the complete test setup with the capacitive clamp defined in the IEC 61000-4-4 standard as well as the protective cases used to encase the DUTs during testing. Figure 9 shows a close up image of the capacitive clamp used to couple the EFT pulses onto the bus cable.



Figure 6. IEC ESD Compliant Test Setup



www.ti.com Test Setup

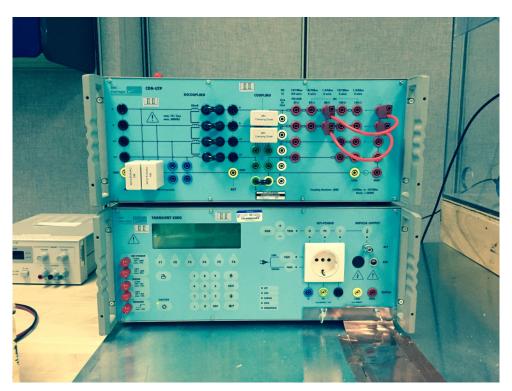


Figure 7. Electrical Fast Transient (EFT) and Surge Generator

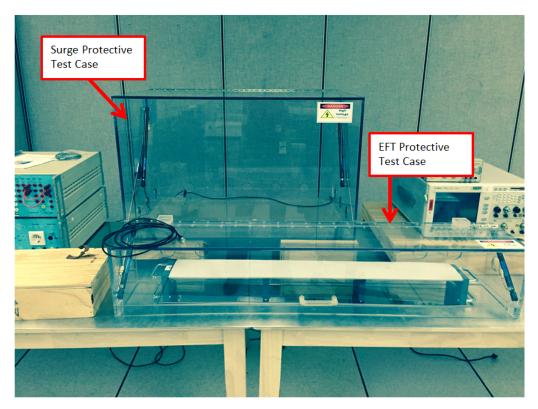


Figure 8. EFT and Surge Test Setup



Test Setup www.ti.com

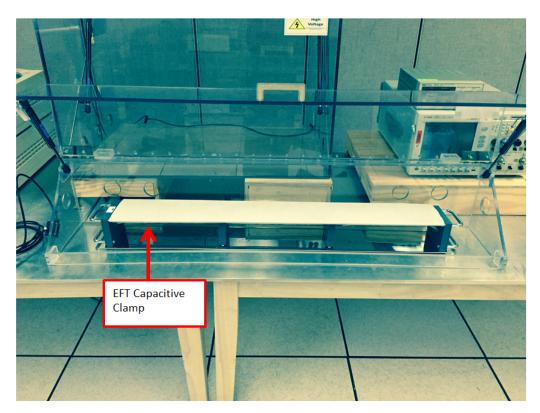


Figure 9. EFT Capacitive Clamp



www.ti.com Test Data

8 Test Data

Table 5 and Table 6 summarize the test results of the TCAN1042 and the TCAN1051 respectively for the IEC 61000–4-2 ESD immunity test, the IEC 61000–4-4 immunity test, and the IEC 61000–4-5 surge immunity test.

Table 5. Summary of TCAN1042 Test Results

PROTECTION SCHEME	PROTECTION SCHEME IEC ESD (kV)		IEC Surge (kv)
TVS	± 30 Contact	± 4	±2
175	± 30 Air	±4	±2
TV/C/TDLI/MOV/	± 30 Contact	± 4	± 6
TVS/TBU/MOV	± 30Air	±4	± 0
TVS/TBU/TISP	± 30 Air	± 4	± 6
TVS/TBU/GDT	±30 Contact	± 4	± 6
1 43/100/001	±30 Air	±4	± 0

Table 6. Summary of TCAN1051 Test Results

PROTECTION SCHEME	IEC ESD (kV)	IEC EFT (kV)	IEC SURGE (kV)
TVS	± 30 Contact	± 4	±2
173	± 30 Air	±4	±2
TVS/TBU/MOV	± 30 Contact	± 4	± 6
I V S/ I BU/IVIO V	± 30 Air	±4	± 0
TVS/TBU/TISP	± 30 Contact	± 4	± 6
179/180/1195	± 30 Air	±4	± 0
TVS/TBU/GDT	± 30 Contact		. 6
	±30 Air	± 4	± 6

Table 7 shows the summary of the SN65HVD267 test results.

Table 7. Summary of SN65HVD267 Test Results

PROTECTION SCHEME	IEC ESD (kV)	IEC EFT (kV)	IEC SURGE (kV)
TVS	± 30 Contact	± 4	±2
175	± 30 Air	14	±2
TVS/TBU/MOV	± 30 Contact	± 4	± 6
1 A 2/ 1 BO\INIO A	± 30 Air	±4	Ξ0
TVS/TBU/TISP	± 30 Contact	± 4	± 6
	± 30 Air	±4	Ξ0
TVS/TBU/GDT	± 30 Contact	±4 ±6	
	± 30 Air	±4	Ξ 0



Table 8 shows the summary of the SN65HVD257 test results.

Table 8. Summary of SN65HVD257 Test Results

PROTECTION SCHEME	IEC ESD (kV)	IEC EFT (kV)	IEC SURGE (kV)
TVS	± 30 Contact	± 4	±2
173	± 30 Air	±4	Ξ2
TVS/TBU/MOV	± 30 Contact	± 4	. 6
	± 30 Air	±4	± 6
TVC/TDLI/TICD	± 30 Contact	± 4	. 6
TVS/TBU/TISP	± 30 Air	±4	± 6
TVS/TBU/TISP	± 30 Contact	± 4	±6
	± 30 Air	<u> </u>	± 0

Table 9 shows the table key for tables 9 - 16.

Table 9. Table Key for Tables 9 - 16

SYMBOL	MEANING
$\sqrt{}$	Passing
×	Failing
NT	Not Tested



Table 10 shows the TCAN10xx IEC ESD contact test results.

Table 10. TCAN10xx IEC ESD Contact Test Results

		C	AN IEC ESD TEST R	RESULTS		
			Positive Contact ESD			
ICE ESD LEVEL	TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
+ 4 kV	√	√	V	√	√	V
+ 5 kV	V	√	V	V	√	V
+ 6 kV	V	√	V	√	√	V
+ 7 kV	V	√	V	√	√	V
+ 8 kV	√	√	V	√	√	√
+ 9 kV	√	√	V	√	√	V
+ 10 kV	√	√	V	√	√	√
+ 11 kV	√	√	√	√	√	√
+ 12 kV	√	√	√	√	√	√
+ 13 kV	√	√	√	√	√	√
+ 14 kV	V	√	V	V	√	√
+ 15 kV	V	√	V	V	√	V
+ 16 kV	V	√	V	V	√	V
+ 17 kV	√	√	V	V	√	V
+ 18 kV	√ ·		√ V	√ V	√	√ V
+ 19 kV	√ √		√ √	· √	· √	√ √
+ 20 kV	√ √		√ √	· √	· √	· √
+ 21 kV	√ √		√ √	· √	· √	√ √
+ 22 kV	√ √		√ √	· √	· √	√ √
+ 23 kV	, √		√ √	\ √	, √	√ √
+ 24 kV	√	√	√ √	\ \ \	√	√ √
+ 25 kV	· √		√ √	, , , , , , , , , , , , , , , , , , ,	, √	, ,
+ 26 kV	· √		√ √	, , , , , , , , , , , , , , , , , , ,	· √	√ √
+ 27 kV	· √		√ √	, , , , , , , , , , , , , , , , , , ,	· √	√ √
+ 28 kV	√ √		√ √	\ \ \ \	· √	√
+ 29 kV	√	√	v v	\ \J	√	√ √
+ 30 kV	√	√	1	7	√ √	√
+ 30 KV	,	<u> </u>	v Negative Contact ESI) Strikes	V	,
– 4 kV	V	√	Negative Contact Loc	Journes	√	V
– 4 KV	v V	<u> </u>	N al	N 2/	N 2/	N 2/
	V	- V	N al	N 2/	N 2/	N 2/
- 6 kV	√ √		N al	N al	N al	N al
	√ √		N al	N al	N al	N al
- 8 kV	√ √	- V	N al	N al	N al	N al
- 9 kV	√ √	V	V	N	N el	N ./
- 10 kV		- V	N al	N al	N al	N al
- 11 kV	√ 1	./	V	N	N .1	N
– 12 kV	√ 1	V	V	N	V	N
– 13 kV	V	V	V	N I	N	V
– 14 kV	√	√	V	V	V	√
– 15 kV	√ /	<u> </u>	√	V	√	٧
– 16 kV	√ /	<u> </u>	√	V	√	٧,
– 17 kV	V	V	√	٧	√	√
– 18 kV	\checkmark	$\sqrt{}$	√	√	√	√



Table 10. TCAN10xx IEC ESD Contact Test Results (continued)

	CAN IEC ESD TEST RESULTS						
– 19 kV	√	V	√	√	√	√	
– 20 kV	√	V	√	√	√	√	
– 21 kV	√	V	√	√	√	√	
– 22 kV	√	V	√	√	√	√	
– 23 kV	√	V	√	√	√	√	
– 24 kV	√	V	√	√	√	√	
– 25 kV	√	\checkmark	√	√	V	√	
– 26 kV	√	V	√	√	√	√	
– 27 kV	V	V	√	√	√	√	
– 28 kV	V	V	√	√	√	√	
– 29 kV	√	V	√	√	√	√	
- 30 kV	√	V	√	√	√	√	



Table 11 shows the TCAN10xx IEC ESD air discharge test results.

Table 11. TCAN10xx IEC ESD Air Discharge Test Results

			N IEC ESD TEST RE			
		0.1	Positive AIR ESD St			
ICE ESD LEVEL	TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
+ 4 kV	√	√	√	√	√	√
+ 5 kV	√	√	√	√	V	V
+ 6 kV	√	√	√	√	√	√
+ 7kV	√	√	√	√	√	√
+ 8 kV	√	√	√	√	√	√
+ 9 kV	√	√	√	√	√	√
+ 10 kV	√	√	√	√	√	√
+ 11 kV	√	√	√	√	√	V
+ 12 kV	√	√	√	√	√	√
+ 13 kV	√	√	√	√	√	√
+ 14 kV	√	√	√	√	√	√
+ 15 kV	√	√	√	√	√	√
+ 16 kV	√	√	√	√	√	√
+ 17 kV	√	√	√	√	√	√
+ 18 kV	√	√	√	√	√	√
+ 19 kV	√	√	V	√	V	√
+ 20 kV	√	√ ×	√	√	√	√
+ 21 kV	√	√ ×	V	√ ×	V	√
+ 22 kV	√	√	√ V	√ ·	√ V	
+ 23 kV	√ V	√	√ ·	√ V	√ ·	
+ 24 kV	· √	· √	√ √	· √	· √	
+ 25 kV	√	√	√ ×	√ V	√ V	
+ 26 kV	· √	· √	√ √	· √	· √	
+ 27 kV	√	√	√ V	√ ·	√ V	
+ 28 kV	· √	· √	√ √	· √	\ \ \ \ \	
+ 29 kV	· √	· √	· √	· √	\ \ \ \ \ \	
+ 30 kV	√	√	\ \ \ \ \	√	√	
1 00 KV	,	•	Negative Air ESD St	The state of the s	,	· · · · · · · · · · · · · · · · · · ·
– 4 kV	√	√	√ V	√	V	√
– 4 KV – 5 kV	√ √	1	√ √	√ √	V	√
- 6 kV	√ √	√ √	√	√ √	√	√
– 7 kV	√	√ √	√ √	√ √	√	√
- 7 kV - 8 kV	√	√ √	√ √	√ √	√	√
- 9 kV	V √	√ √	√	√ √	√	√
– 9 kV – 10 kV	\ √	√ √	√ √	\ √	√	√
– 10 kV – 11 kV	V √	√ √	√ √	√ √	\ √	√
	√ √	√ √	√ √	√ √	√ √	
- 12 kV	V √	1		1	,	1
- 13 kV		ν 2	√ √	√ √	√ √	<u>۷</u>
- 14 kV	√ ./	√ 	√ 	√ 1	√	- V
– 15 kV	√ ./	√ ./	√ ./	√ ./	√ ./	√
- 16 kV	√ 	√ 	√ 	√ 	√ ./	√
– 17 kV	√ 	√ /	√ /	√ /	√ /	√
– 18 kV	√	√	√	V	V	٧



Table 11. TCAN10xx IEC ESD Air Discharge Test Results (continued)

CAN IEC ESD TEST RESULTS							
– 19 kV	√	√	√	√	√	√	
– 20 kV	√	√	√	√	√	√	
– 21 kV	√	√	√	√	√	√	
– 22 kV	√	√	√	√	√	√	
– 23 kV	√	√	√	√	V	V	
– 24 kV	√	√	√	√	√	√	
– 25 kV	√	√	√	\checkmark	\checkmark	√	
– 26 kV	√	√	√	√	V	V	
– 27 kV	√	√	√	√	V	V	
– 28 kV	√	√	√	√	√	√	
– 29 kV	√	√	√	√	√	√	
– 30 kV	√	√	√	√	√	√	



Table 12 shows the IEC electrical fast transient test results.

Table 12. TCAN10xx IEC Electrical Fast Transient Test Results

Level Board 1 Board 2 Board 3 Board 1 Board 2 Board 2 + 0.5 kV √ <td< th=""><th></th><th></th><th></th><th></th><th>EST RESULTS</th><th></th><th></th></td<>					EST RESULTS		
Positive EFT Strikes			CANTE				
EC EFT							
Level Board 1 Board 2 Board 3 Board 1 Board 2 Board 2 0.5 kV √	IEC EET	TCAN1042	TCAN1042	T	T	TCAN1051	TCAN1051
+ 1 kV							Board 3
+ 2 kV	+ 0.5 kV	√	√	√	√	√	√
Head	+ 1 kV	√	√	√	√	√	√
Negative EFT Strikes	+ 2 kV	\checkmark	√	√	√	√	V
TCAN1042 Board 1 Board 2 Board 3 Board 1 Board 2 Board 3 Month of the provided	+ 4 kV	\checkmark	√	√	V	√	V
Level Board 1 Board 2 Board 3 Board 1 Board 2 Board 2 -0.5 kV √				Negative EFT Str	rikes		
- 1 kV	IEC EFT Level						TCAN1051 Board 3
- 2 kV NT	– 0.5 kV	V	√	√	V	√	V
Text	– 1 kV	V	√	√	V	√	√
TVS/TBU/MOV Positive EFT Strikes	– 2 kV	NT	NT	NT	NT	NT	NT
Positive EFT Strikes	– 4 kV	NT	NT	NT	NT	NT	NT
Level Board 1 Board 2 Board 3 Board 1 Board 2 Board 2 + 0.5 kV √ √ √ √ √ √ √ + 1 kV √ √ √ √ √ √ √ + 2 kV √ √ √ √ √ √ √ + 4 kV √ √ √ √ √ √ √ Negative EFT Strikes EC EFT TOAN1042 Board 2 TCAN1042 TCAN1042 Board 3 TCAN1051 Board 1 TCAN1051 Board 2 TCAN1042 Board 1 TCAN1042 TCAN1042 TCAN1042 Board 2 TCAN1042 Board 3 TCAN1051 Board 1 TCAN1051 Board 2 TCAN1042 Board 3 TCAN1051 Board 3			<u>I</u>			1	
+ 1 kV	IEC EFT Level						TCAN1051 Board 3
+ 2 kV	+ 0.5 kV	√	√	√	√	√	√
+ 4 kV	+ 1 kV	√	√	√	√	√	√
Negative EFT Strikes	+ 2 kV	V	√	√	√	√	√
C	+ 4 kV	V	√	√	√	√	√
Level Board 1 Board 2 Board 3 Board 1 Board 2 Board 2 - 0.5 kV √ √ √ √ √ √ - 1 kV √ √ √ √ √ √ - 2 kV √ √ √ √ √ √ - 4 kV √ √ √ √ √ √ TVS/TBU/TISP Protection Circuit Positive EFT Strikes EC EFT TCAN1042 Board 1 TCAN1051 Board 2 TCAN1051 Board 3				Negative EFT Str	rikes		
- 1 kV	IEC EFT Level						TCAN1051 Board 3
- 2 kV	– 0.5 kV	V	√	√	V	√	√
- 4 kV	– 1 kV	V	√	√	V	√	V
TVS/TBU/TISP Protection Circuit Positive EFT Strikes EC EFT TCAN1042 TCAN1042 TCAN1042 TCAN1051 TCAN1051 Board 2	– 2 kV	V	√	√	V	√	√
Can	– 4 kV	V	√	√	V	√	√
Level Board 1 Board 2 Board 3 Board 1 Board 2 Board 2 + 0.5 kV √ √ √ √ √ √ + 1 kV √ √ √ √ √ √ + 2 kV √ √ √ √ √ √ + 4 kV √ √ √ √ √ √	-		TV			+	+
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	IEC EFT Level						TCAN1051 Board 3
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	+ 0.5 kV	V	√	√	V	√	V
+ 4 kV	+ 1 kV	V	√	√	√	√	√
	+ 2 kV	V	√	√	V	√	V
	+ 4 kV	V	√	√	V	√	√
Negative EFT Strikes			1	Negative EFT Str	rikes	-1	+
EC EFT TCAN1042 TCAN1042 TCAN1051 TC	IEC EFT Level			TCAN1042	TCAN1051		TCAN1051 Board 3
- 0.5 kV	– 0.5 kV	V	√	√	V	√	√
-1 kV √ √ √ √	– 1 kV	V	√	√	V	√	√
- 2 kV	– 2 kV	V	√	√	√	√	V
-4 kV √ √ √ √	– 4 kV	V	√	√	V	√	√
TVS/TBU/GDT Protection Circuit Positive EFT Strikes			TV			•	



Table 12. TCAN10xx IEC Electrical Fast Transient Test Results (continued)

	CAN IEC 61000-4-5 EFT TEST RESULTS								
IEC EFT Level	TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3			
+ 0.5 kV	√	√	√	√	√	√			
+ 1 kV	√	√	√	V	√	√			
+2 kV	√	√	√	V	√	√			
+ 4 kV	√	√	√	V	√	√			
			Negative EFT Str	ikes					
– 0.5 kV	TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3			
– 1 kV	√	√	√	V	√	√			
– 2 kV	√	√	√	V	√	√			
– 4 kV	√	√	√	V	√	√			



Table 13 shows the TCAN10xx IEC surge test results.

Table 13. TCAN10xx IEC Surge Test Results

	CANIECE	61000-4-5 SURGE TI	EST RESULTS		
	CAN IEC (
TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
√	V	V	√	√	√
√	√	√	√	√	√
×	×	×	×	×	×
NT	NT	NT	NT	NT	NT
NT	NT	NT	NT	NT	NT
		Negative Surge Strik	ces	1	
TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
V	V	√	√	√	√
√	V	V	√	√	√
NT	NT	NT	NT	NT	NT
NT	NT	NT	NT	NT	NT
NT	NT	NT	NT	NT	NT
		TVS/TBU/MOV Positive Surge Strik	es		
TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
\checkmark	√	\checkmark	√	√	√
V	√	√	√	√	√
\checkmark	√	\checkmark	V	√	√
\checkmark	\checkmark	\checkmark	\checkmark	√	√
NT	NT	NT	NT	NT	NT
		Negative Surge Strik	es		
TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
V	V	√	√	√	√
V	V	√	V	√	√
V	√	V	V	√	√
V	V	V	V	√	√
NT	NT	NT	NT	NT	NT
	TVS			·	,
TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3
V	√	$\sqrt{}$	√	√	V
V	√	V	√	√	√
V	√	V	√	√	√
√	√	V	√	√	√
	i e		1	1	+
	Board 1	Board 1	Positive Surge Strike TCAN1042 Board 1 Board 2 TCAN1042 Board 3	Board 1	Positive Surge Strikes



Table 13. TCAN10xx IEC Surge Test Results (continued)

	CAN IEC 61000-4-5 SURGE TEST RESULTS									
IEC Surge Level	TCAN1042 Board 1	TCAN1042 Board 2	TCAN1042 Board 3	TCAN1051 Board 1	TCAN1051 Board 2	TCAN1051 Board 3				
- 0.5 kV	√	V	√	√	√	√				
– 1 kV	√	V	√	√	√	√				
– 2 kV	√	V	√	√	√	√				
– 4 kV	√	V	√	√	√	√				
– 6 kV	NT	NT	NT	NT	NT	NT				



Table 14 shows the SN65HVD2xx IEC ESD contact discharge test results.

Table 14. SN65HVD2xx IEC ESD Contact Discharge Test Results

		C	AN IEC ESD TEST RE	SULTS				
Positive Contact ESD Strikes								
IEC ESD Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3		
+ 4 kV	√	√	V	√	√	√		
+ 5 kV	√	V	V	√	√	√		
+ 6 kV	√	V	V	√	√	√		
+ 7 kV	√	√	V	√	√	√		
+ 8 kV	√	√	V	√	√	√		
+ 9 kV	√	√	V	V	√	√		
+ 10 kV	√	√	V	√	V	V		
+ 11 kV	√	√	V	√	V	V		
+ 12 kV	√	√	V	√	√	√		
+ 13 kV	√	√	V	√	√	√		
+ 14 kV	√	V	V	√	√	√		
+ 15 kV	√	√	V	√	√	√		
+ 16 kV	√	√	V	√	√	√		
+ 17 kV	√	√	V	√	√	√		
+ 18 kV	√	√	V	√	√	√		
+ 19 kV	√	√	V	√	√	√		
+ 20 kV	√	√	V	√	√	√		
+ 21 kV	√	√	V	√	√	√		
+ 22 kV	√	√	V	√	√	√		
+ 23 kV	√	√	V	√	√	√		
+ 24 kV	√	√	V	√	√	√		
+ 25 kV	√	√	V	√	√	√		
+ 26 kV	√	√	V	√	√	√		
+ 27 kV	√	√	V	√	√	√		
+ 28 kV	√	√	V	√	√	√		
+ 29 kV	√	√	V	√	√	√		
+ 30 kV	√	√	V	√	√	√		
		N	legative Contact ESD	Strikes				
– 4 kV	√	√	√	√	√	√		
– 5 kV	√	√	V	√	√	√		
– 6 kV	V	√	V	√	√	√		
– 7 kV	√	V	V	√	√	√		
– 8 kV	√	V	V	√	√	√		
– 9 kV	√	√	V	√	V	√		
– 10 kV	√	√	V	√	√	√		
– 11 kV	√	V	V	√	√	√		
– 12 kV	√	V	V	√	√	√		
– 13 kV	√	V	V	√	√	√		
– 14 kV	V	√	V	√	√	√		
– 15 kV	√	√	V	√	√	√		
– 16 kV	√ ·	√	√ V	√ V	√	√ ·		
– 17 kV	√	V	V	√	√	√		
– 18 kV	√ ·	√ ·	√ V	√ V	√ V	√ ·		



Table 14. SN65HVD2xx IEC ESD Contact Discharge Test Results (continued)

	CAN IEC ESD TEST RESULTS									
– 19 kV	√	V	√	√	√	√				
– 20 kV	√	V	√	√	√	√				
– 21 kV	V	V	√	V	√	√				
– 22 kV	V	V	√	V	√	√				
– 23 kV	V	V	√	V	√	√				
– 24 kV	√	V	√	√	√	√				
– 25 kV	~	\checkmark	V	\checkmark	V	√				
– 26 kV	V	V	√	V	√	√				
– 27 kV	V	V	√	V	√	√				
– 28 kV	V	V	V	V	√	V				
– 29 kV	√	V	√	√	√	√				
- 30 kV	√	V	√	√	√	√				



Table 15 shows the SN65HVD2xx IEC ESD air discharge test results.

Table 15. SN65HVD2xx IEC ESD Air Discharge Test Results

		C	AN IEC ESD TEST RE	SULTS					
Positive AIR ESD Strikes									
IEC ESD Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3			
+ 4 kV	√	√	√	√	V	√			
+ 5 kV	V	√	√	√	V	√			
+ 6 kV	√	√	√	√	V	√			
+ 7 kV	√	√	√	√	√	√			
+ 8 kV	V	√	√	√	V	√			
+ 9 kV	V	√	√	√	V	√			
+ 10 kV	V	√	√	√	V	√			
+ 11 kV	V	√	√	√	V	√			
+ 12 kV	V	√	√	√	V	√			
+ 13 kV	V	√	√	√	V	√			
+ 14 kV	V	√	√ ×	√	V	√			
+ 15 kV	√ ·		√ ·	√ ·	√ V	√ V			
+ 16 kV	√ ·	√	√ ·	√ ·	√ V	√ V			
+ 17 kV	√ ·		√ √	√	√ V	√ ×			
+ 18 kV	· √	` √	· √	· √	· √	, √			
+ 19 kV	· √	`	· √	· √	· √	, √			
+ 20 kV	· √	`	· √	· √	· √	, √			
+ 21 kV	· √	`	· √	· √	· √	, √			
+ 22 kV	√	\	√ √	√	√	√			
+ 23 kV	√	<u> </u>	√ √	√	√	√			
+ 24 kV	√	` √	√ √	√	√ √	√			
+ 25 kV	√	` √	√ √	√	√	√			
+ 26 kV	√		√ √	√	v v	1			
+ 27 kV	√	\	√ √	√ √	√	√			
+ 28 kV	√	√	√		√ √	√			
+ 29 kV	√	√	√	√ √	√ √	√			
+ 30 kV	√	√	√ √	√ √	√ √	√ √			
+ 30 KV	٧	v	Negative AIR ESD St		V	V			
IEC ESD Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3			
– 4 kV	√	√	√	√	V	√			
– 5 kV	√	<u> </u>	√ √	√ √	N N	√			
- 6 kV	√		√ √	√ √	N N	√			
	√	√	√ √	√ √	1	√			
- 7 kV	N 2/	√		√ √	N al	√ √			
- 8 kV	√ √	√	V √	√ √	N al	√ √			
- 9 kV	√ √	√	V √	√ √	√ √	√ √			
- 10 kV	1	-		,	,	,			
- 11 kV	V	V	√ -/	√ ./	V	√ ./			
– 12 kV	√ 	√ 	√ 	√ /	V	√			
– 13 kV	√	<u>√</u>	√ /	√ /	√ /	√ 			
– 14 kV	√	<u>√</u>	√ ,	√ /	V	√ 			
– 15 kV	V	√	√ 	√ 	V	√			
– 16 kV	\checkmark	$\sqrt{}$	√	√	√	V			



Table 15. SN65HVD2xx IEC ESD Air Discharge Test Results (continued)

	CAN IEC ESD TEST RESULTS									
– 17 kV	√	√	√	√	√	√				
– 18 kV	√	V	√	V	√	√				
– 19 kV	√	V	√	V	√	√				
– 20 kV	√	V	V	V	√	√				
– 21 kV	V	V	V	V	√	√				
– 22 kV	√	V	√	V	√	√				
– 23 kV	√	V	√	V	√	√				
– 24 kV	√	V	V	V	√	√				
– 25 kV	√	V	V	V	√	√				
– 26 kV	√	V	V	V	√	√				
– 27 kV	√	V	√	V	√	√				
– 28 kV	√	V	√	V	√	√				
– 29 kV	√	V	V	V	√	√				
– 30 kV	√	V	V	V	√	√				



Table 16 shows the SN65HVD2xx IEC electrical fast transient test results.

Table 16. SN65HVD2xx IEC Electrical Fast Transient Test Results

		CANTE	EC 61000-4-5 EFT TEST			
			TVS Protection Circu			
			Positive EFT Strike	S		
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
+ 0.5 kV	√	√	√	V	√	√
+ 1 kV	√	√	√	V	√	√
+ 2 kV	√	√	√	√	√	√
+ 4 kV	√	√	√	V	√	√
			Negative EFT Strike	3		•
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
– 0.5 kV	√	V	√	V	√	√
– 1 kV	√	V	√	V	√	√
– 2 kV	√	V	√	V	√	√
– 4 kV	√	V	√	V	√	√
	<u> </u>		TVS/TBU/MOV Positive EFT Strikes	1		
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
+ 0.5 kV	√	√	√	V	√	√
+ 1 kV	√	√	√	V	√	√
+ 2 kV	√	√	√	V	√	√
+ 4 kV	V	√	√	V	V	√
			Negative EFT Strike	 S		
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
– 0.5 kV	√	V	√	V	√	√
– 1 kV	√	V	√	V	√	√
– 2 kV	√	V	√	V	√	√
– 4 kV	V	V	√	V	V	V
	+	יד	VS/TBU/TISP Protection Postive EFT Strikes		-1	-1
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD25 Board 3
+ 0.5 kV	√	√	√	V	√	√
+ 1 kV	V	√	√	V	V	V
+ 2 kV	V	√	√	V	V	V
+ 4 kV	V	√	√	V	V	V
			Negative EFT Strike	3	1	1
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD25 Board 3
– 0.5 kV	V	√	√	V	√	√
– 1 kV	V	√	√	V	√	√
– 2 kV	√	√	√	V	√	√
– 4 kV	V	√	√	V	V	V



Table 16. SN65HVD2xx IEC Electrical Fast Transient Test Results (continued)

	CAN IEC 61000-4-5 EFT TEST RESULTS								
	TVS Protection Circuit								
			Positive EFT Strike	s					
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3			
+ 0.5 kV	√	√	√	V	√	√			
+ 1 kV	√	V	√	√	√	√			
+ 2 kV	√	√	√	√	√	√			
+ 4 kV	√	√	√	√	√	√			
			Negative EFT Strike	S					
IEC EFT Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3			
– 0.5 kV	√	V	√	V	√	√			
– 1 kV	√	V	√	√	√	√			
– 2 kV	√	V	√	√	√	√			
– 4 kV	√	V	√	√	√	√			



Table 17 shows the SN65HVD2xx IEC surge test results.

Table 17. SN65HVD2xx IEC Surge Test Results

		CAN IEC	61000-4-5 SURGE TE	ST RESULTS		
			TVS Protection Circu			
			Positive Surge Strike			
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
+ 0.5 kV	√	V	V	V	√	√
+ 1 kV	√	V	√	V	√	V
+ 2 kV	×	×	×	×	×	×
+ 4 kV	NT	NT	NT	NT	NT	NT
+ 6 kV	NT	NT	NT	NT	NT	NT
U.	<u>'</u>		Negative Surge Strik	es		1
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
– 0.5 kV	√	√	√	\checkmark	√	√
– 1 kV	√	√	√	V	√	√
– 2 kV	NT	NT	NT	NT	NT	NT
– 4 kV	NT	NT	NT	NT	NT	NT
– 6 kV	NT	NT	NT	NT	NT	NT
·	,		TVS/TBU/MOV Positive Surge Strike	es		
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
+ 0.5 kV	√	V	√	V	√	√
+ 1 kV	√	V	√	V	√	√
+ 2 kV	√	V	√	V	√	√
+ 4 kV	√	V	√	V	√	√
+ 6 kV	\checkmark	$\sqrt{}$	√	\checkmark	√	√
			Negative Surge Strik	es		
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
– 0.5 kV	√	V	V	V	√	√
– 1 kV	\checkmark	$\sqrt{}$	V	\checkmark	√	V
– 2 kV	\checkmark	$\sqrt{}$	V	\checkmark	√	\checkmark
– 4 kV	√	V	V	V	√	V
– 6 kV	√	√	\checkmark	V	√	\checkmark
		Protec	TVS/TBU/TISP tion Circuit Positive Su	rge Strikes		
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
+ 0.5 kV	V	V	√	√	√	√
+ 1 kV	√	V	V	√	√	√
+ 2 kV	√	V	V	V	V	√
+ 4 kV	√	√	√	V	√	√
+6 kV	√	√	√	V	√	√
			Negative Surge Strik	es		
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3
– 0.5 kV	√	V	V	V	√	V
– 1 kV	√	√	√	√	√	√



Table 17. SN65HVD2xx IEC Surge Test Results (continued)

CAN IEC 61000-4-5 SURGE TEST RESULTS										
– 2 kV	√	√	√	\checkmark	√	√				
– 4 kV	√	√	√	√	√	√				
– 6 kV	√	V	V	√	√	√				
	TVS/TBU/GDT Protection Circuit Positive Surge Strikes									
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3				
+ 0.5 kV	√	√	√	√	√	√				
+ 1 kV	√	√	√	√	√	√				
+ 2 kV	√	V	V	√	√	√				
+ 4 kV	√	V	V	√	√	√				
+ 6 kV	√	V	V	√	√	√				
			Negative Surge Strik	es	•					
IEC Surge Level	SN65HVD267 Board 1	SN65HVD267 Board 2	SN65HVD267 Board 3	SN65HVD257 Board 1	SN65HVD257 Board 2	SN65HVD257 Board 3				
– 0.5 kV	√	V	V	$\sqrt{}$	√	√				
– 1 kV	√	V	V	√	√	√				
– 2 kV	√	V	V	√	√	√				
– 4 kV	√	√	√	\checkmark	√	√				
– 6 kV	√	√	V	√	√	√				

8.1 Test Results

The test results show that by adding the TVS diode, the transient blocking unit, the metal oxide varistor, the thyristor and the gas discharge tube to the CANH and CANL bus lines of the TCAN1042, TCAN1051, SN65HVD267 and SN65HVD257 transceivers, the transient immunity increases significantly. The design passes IEC ESD level 4 criteria, IEC EFT level 4 criteria, and IEC surge level 4 criteria. The four transceivers also fall into the *special* characteristic per the IEC ESD standard as they pass up to ±30 kV IEC ESD, surpassing the level 4 ESD voltage.



Design Files www.ti.com

9 **Design Files**

Schematics 9.1

To download the schematics for each board, see the design files at http://www.ti.com/tool/TIDA-00629.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00629. Table 18 lists the BOM required for this design.

Table 18. Bill of Materials

ITEM	QUANTITY	REFERENCE	VALUE	MANUFACTU RER	MANUFACTURER PART #	PCB FOOTPRINT
1	8	C1, C4, C6, C11, C14, C16, C20	68 pF	Any	Any (5V+ Rated)	0603
2	4	C2, C7, C12, C17	0.1 μF	Any	Any (5V+ Rated)	0402
3	4	C3, C8, C13, C18	4.7 nF_DNI	Any	Any (5V+ Rated)	0402
4	4	C5, C10, C15, C19	15 pF_DNI	Any	Any (5V+ Rated)	0402
5	1	C21	47 μF	Any	Any (5V+ Rated)	7343
6	1	C22	22 µF	Any	Any (5V+ Rated)	7343
7	1	C23	68 µF	Any	Any (5V+ Rated)	1210
8	1	C24	10 μF	Any	Any (5V+ Rated)	0805
9	1	C25	1 μF	Any	Any (5V+ Rated)	1206
10	1	C26	0.1 μF	Any	Any (5V+ Rated)	1206
11	1	C27	0. 01 µF	Any	Any (5V+ Rated)	0805
12	4	C28, C29, C30, C31	0.01 μF	Any	Any (5V+ Rated)	0603
13	8	JMP1, JMP5, JMP7, JMP11, JMP13, JMP17, JMP19, JMP23	Header 2 x 3 Tee	Samtec™	HTSW-150-08-G-S	berg 2 × 3 tree
14	12	JMP2, JMP3, JMP6, JMP8, JMP9, JMP12, JMP14, JMP15, JMP18, JMP20, JMP21, JMP24, JMP25	Header 1 x	Samtec	HTSW-150-08-G-S	berg 1 × 2
15	4	JMP4, JMP10, JMP16, JMP22	Header 1 x	Samtec	HTSW-150-08-G-S	berg 1 x 4
16	4	L1, L2. L3, L4	ACT45B Choke	Any	ACT45B-101-2P- TL003	IND_ACT45B_SM T_4p5 × 3 p 2 mm
17	4	R1, R17, R33, R49	4.7 k	Any	Any (1% tolerance)	0603
18	4	R2, R19, R35, R51	0	Any	Any (1% tolerance)	0603
19	4	R3, R20, R36, R52	10 l	Any	Any (1% tolerance)	0603
20	8	R4, R14, R18, R32, R34, R48, R50, R64	0	Any	Any (1% tolerance)	0603
21	8	R5, R16, R21, R31, R37, R47, R53	49.9	Any	Any (1% tolerance)	0603
22	8	R6, R10, R22, R26, R38, R42, R54, R58	0_DNI	Any	Any (1% tolerance)	0603
23	8	R7, R12, R23, R28, R39, R44, R55, R60	49.9_DNI	Any	Any (1% tolerance)	0603
24	2	R8, R11	60.4_DNI	Any	Any (1% tolerance)	0603
25	4	R9, R25, R41, R57	120	Any	Any (1% tolerance)	0603
26	4	R13, R29, R45, R61	10k_DNI	Any	Any (1% tolerance)	0603
27	4	R15, R30, R46, R62	453	Any	Any (1% tolerance)	0603
28	6	R24, R27, R40, R43, R56, R59	60_DNI	Any	Any (1% tolerance)	0603
29	16	U1, U2, U4, U5, U6, U7, U12, U14, U15, U16, U22, U23, U24, U26, U30, U32	SM712	Any	SM712-TP	SOT_23_321
30	4	U3, U10, U19, U28	CAN Transceiver	TI	SN65HVD1042D	SOIC 8 Pin



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Table 18. Bill of Materials (continued)

ITEM	QUANTITY	REFERENCE	VALUE	MANUFACTU RER	MANUFACTURER PART #	PCB FOOTPRINT
31	6	U8, U13, U17, U21, U25/ U31	Surge Supp TBU 200 MA 850 VIMP SMD	Bourns	TBU-CA085-200- WH	DFN_3_157 × 256
32	2	U9, U11	Varistor 185 V 2.5 KA disc 10 mm	Bourns	MOV-10D201K	VAR_DOSC_3p8 × 12p5 mm
33	2	U18, U20	Protector single bidirect 240 V	Bourns	TISP4240M3BJR-s	do-214aa
34	2	U27. U29	GDT 360 V 1 KA surface mount	Bourns	2031-42T-SM- RPLF	GDT_SM_2031- xxT



www.ti.com Design Files

9.3 PCB Layout Recommendations

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. On-chip IEC ESD protection is good for laboratory and portable equipment, but is not sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents harsh transient events from propagating further into the PCB and system. Use $V_{\rm CC}$ and ground planes to provide low inductance.

NOTE: High-frequency current follows the path of least inductance and not the path of least resistance.

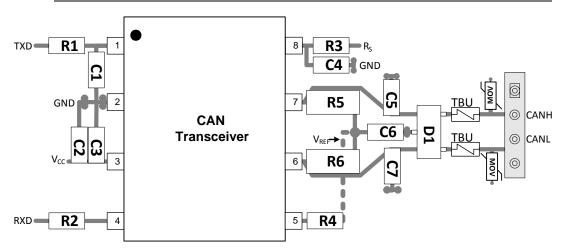


Figure 10. Layout Example

Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device. An example placement of the Transient Voltage Suppression (TVS) device is indicated as D1 (either bidirectional diode or varistor solution) and bus filter capacitors C5 and C7 are shown in Figure 10.

The bus transient protection and filtering components should be placed as close to the bus connector, J1, as possible. This prevents transients, ESD, and noise from penetrating onto the board and disturbing other devices.

Bus Termination; Figure 10 shows split termination. This is where the termination is split into two resistors, R5 and R6, with the center or split tap of the termination connected to ground through capacitor C6. Split termination provides common-mode filtering for the bus. When termination is placed on the board instead of directly on the bus, care must be taken to ensure the terminating node is not removed from the bus as signal integrity issues may arise if the bus is not properly terminated on both ends.

Bypass and bulk capacitors must be placed as close as possible to the supply pins of transceiver. Examples include C2 and C3 ($V_{\rm CC}$).

Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

To limit current of digital lines, serial resistors may be used. Examples are R1, R2, R3, and R4.

To filter noise on the digital I/O lines, a capacitor may be used close to the input side of the IO as shown by C1 and C4.

Because the internal pull-up and pull-down biasing of the device is weak for floating pins, an external $1-k\Omega$ to $10-k\Omega$ pull-up or pull-down resistor must be used to bias the state of the pin more strongly against noise during transient events.

Pin 1: If an open-drain host processor is used to drive the TXD pin of the device, an external pull-up resistor between $1-k\Omega$ and $10-k\Omega$ should be used to drive the recessive input state of the device.



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Pin 5: SPLIT must be connected to the center point of a split termination scheme to help stabilize the common-mode voltage to $V_{\rm CC}/2$. If SPLIT is unused it should be left floating.

Pin 8: Is shown assuming the mode pin, STB, is used. If the device is only used in normal mode, R3 is not required, and the pads of C4 may be used for the pull-down resistor to GND.

9.3.1 Layout Prints

To download the layout prints for each board, see the design files at http://www.ti.com/tool/TIDA-00629.

9.4 Layout Guidelines

Figure 11 shows the layout guidelines.

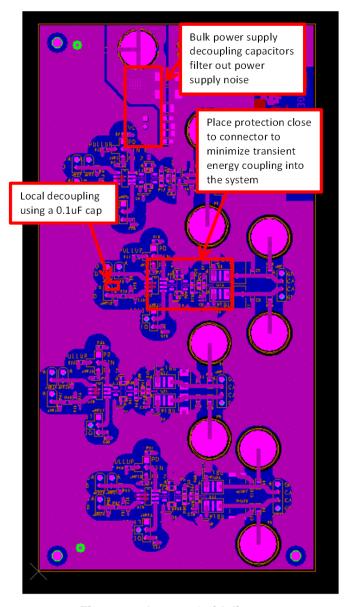


Figure 11. Layout Guidelines

9.5 Gerber Files

To download the Gerber files for each board, see the design files at http://www.ti.com/tool/TIDA-00629.



www.ti.com Design Files

9.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at http://www.ti.com/tool/TIDA-00629.

10 Related Documentation

1. Introduction to the Controller Area Network (CAN), (SLOA101A)

10.1 Trademarks

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11 About the Author

MICHAEL PEFFERS is an applications engineer at TI supporting the RS-485, LVDS, PECL, CAN, LIN, IO-Link, and Profibus interface products. Michael is responsible for developing reference designs solutions for the industrial segment and direct customer support including onsite support as well as onsite training. Michael is also responsible for producing technical content such as application notes, datasheets, white papers, and is the author of a recurring blog on the TI E2E forum called Analog Wire: Get Connected. Michael brings to this role his experience in high-speed SERDES applications as well as experience in the optical transceiver space. Michael earned his Bachelors of Science in Electrical Engineering (BSEE) from the University of Central Florida (UCF).



Revision B History www.ti.com

Revision B History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Cł	Changes from A Revision (March 2016) to B Revision				
•	Changed link for TIDA-00629.	1			
•	Changed link for TCAN1042.	1			
	Changed link for TCAN1051.				
	Changed link for SLOA101				
	· ·				

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