ISL3259E

±15kV ESD Protected, 100Mbps, 5V, PROFIBUS, Full Fail-Safe, RS-485/RS-422 Transceiver

FN6587
Rev.2.00
Aug 31, 2017

The ISL3259E is a ±15kV IEC61000 ESD Protected, 5V powered, single transceiver that meets both the RS-485 and RS-422 standards for balanced communication. It also features the larger output voltage and higher data rate (up to 100Mbps) required by high speed PROFIBUS applications. The low bus currents (+220µA/-150µA) present a 1/5 unit load to the RS-485 bus. This allows up to 160 transceivers on the network without violating the RS-485 specification's load limit, and without using repeaters.

This transceiver requires a 5V supply, and delivers at least a 2.1V differential output voltage. This translates into better noise immunity (data integrity), longer reach, or the ability to drive up to six 120Ω terminations in "star" or other non-standard bus topologies.

SCSI applications benefit from the ISL3259E's low receiver and transmitter part-to-part skews. The ISL3259E is perfect for high speed parallel applications requiring simultaneous capture of large numbers of bits. The low bit-to-bit skew eases the timing constraints on the data latching signal.

Receiver (Rx) inputs feature a "Full Fail-Safe" design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven. Rx outputs feature high drive levels (typically >30mA @ V_{OL} = 1V) to ease the design of optically isolated interfaces.

Hot plug circuitry ensures that the Tx and Rx outputs remain in a high impedance state while the power supply stabilizes.

Driver (Tx) outputs are short-circuit protected, even for voltages exceeding the power supply voltage. Additionally, on-chip thermal shutdown circuitry disables the Tx outputs to prevent damage if power dissipation becomes excessive.

Related Literature

- For a full list of related documents, refer to our website
  - ISL3259E product page

Features

- IEC61000 ESD protection on RS-485 I/O pins . . . . . ±15kV
  - Class 3 HBM ESD level on all other pins . . . . . >9kV
- Large differential V_{OUT} . . . . . 2.8V into 54Ω
  Better noise immunity, or drive up to 6 terminations
- Very high data rate. . . . . up to 100Mbps
- 11/13ns (maximum) Tx/Rx propagation delays; 1.5ns (maximum) skew
- 1/5 unit load allows up to 160 devices on the bus
- Full fail-safe (open, shorted, terminated/undriven) receiver
- High Rx I_{OL} to drive opto-couplers for isolated applications
- Hot plug - Tx and Rx outputs remain three-state during power-up
- Low quiescent supply current. 4mA
- Low current shutdown mode 1µA
- -7V to +12V common mode input voltage range
- Three-State Rx and Tx outputs
- Operates from a single +5V supply
- Current limiting and thermal shutdown for driver overload protection
- Pb-free (RoHS compliant)

Applications

- PROFIBUS® DP and FMS networks
- SCSI "fast 40" drivers and receivers
- Motor controller/position encoder systems
- Factory automation
- Field bus networks
- Security networks
- Building environmental control systems
- Industrial/process control networks

Ordering Information

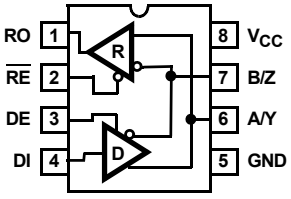
PART NUMBER (Note 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL3259EIBZ (Note 1)	3259 EIBZ	-40 to +85	8 Ld SOIC	M8.15
ISL3259EIUZ (Note 1)	3259Z	-40 to +85	8 Ld MSOP	M8.118
ISL3259EIRZ (Note 2)	3259	-40 to +85	10 Ld 3x3 DFN	L10.3x3C

NOTES:

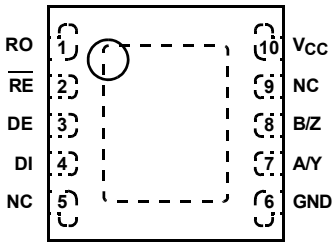
1. Add “-T” suffix for 2.5k unit tape and reel options. Refer to TB347 for details on reel specifications.
2. Add “-T” suffix for 6k unit tape and reel options. Refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

ISL3259E
(8 LD MSOP, SOIC)
TOP VIEW



ISL3259E
(10 LD DFN)
TOP VIEW



Truth Table

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B/Z	A/Y
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z*	High-Z*

NOTE: *Shutdown Mode

Truth Table

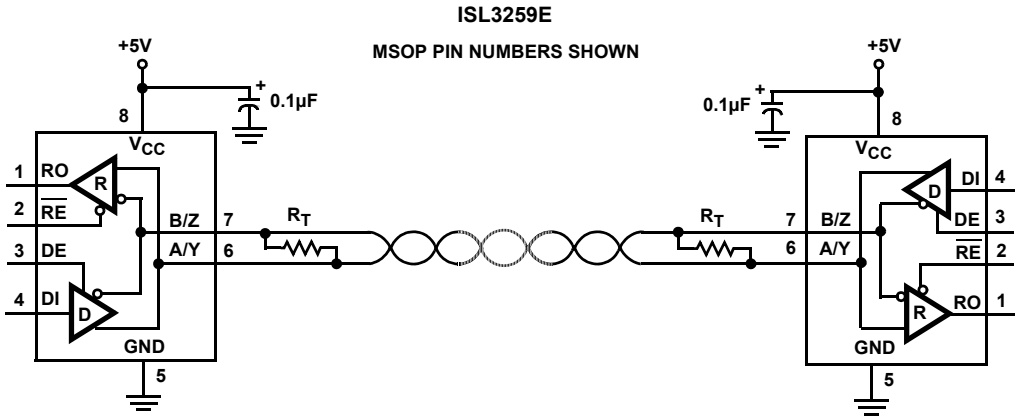
RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	0	$V_{AB} \geq -0.05V$	1
0	0	$-0.05V > V_{AB} > -0.2V$	Undetermined
0	0	$V_{AB} \leq -0.2V$	0
0	0	Inputs Open/Shorted	1
1	1	X	High-Z
1	0	X	High-Z*

NOTE: *Shutdown Mode

Pin Descriptions

PIN	FUNCTION
RO	Receiver output: If A - B ≥ -50mV, RO is high. If A - B ≤ -200mV, RO is low. If A and B are unconnected (floating) or shorted, or connected to a terminated bus that is undriven, RO is high.
$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low. RO is high impedance when $\overline{RE}$ is high. If the Rx enable function isn't required, connect $\overline{RE}$ directly to GND.
DE	Driver output enable. The driver outputs, Y and Z, are enabled by bringing DE high. They are high impedance when DE is low. If the Tx enable function isn't required, connect DE to V_{CC} through a 1kΩ or greater resistor.
DI	Driver input. A low on DI forces output Y low and output Z high. Similarly, a high on DI forces output Y high and output Z low.
GND	Ground connection. This is also the potential of the DFN thermal pad.
A/Y	±15kV IEC61000 ESD Protected RS-485, RS-422 level, noninverting receiver input and noninverting driver output. Pin is an input (A) if DE = 0; pin is an output (Y) if DE = 1.
B/Z	±15kV IEC61000 ESD Protected RS-485, RS-422 level, inverting receiver input and inverting driver output. Pin is an input (B) if DE = 0. Pin is an output (Z) if DE = 1.
V_{CC}	System power supply input (4.75V to 5.25V).
NC	No Connection.

Typical Operating Circuit



Absolute Maximum Ratings

VCC to GND 7V
Input Voltages
DI, DE, $\overline{RE}$ . . . . . -0.3V to 7V
Input/Output Voltages
A/Y, B/Z . . . . . -9V to +13V
RO . . . . . -0.3V to (V_{CC} +0.3V)
Short-circuit Duration
Y, Z . . . . . Continuous
ESD Rating . . . . . Refer to "Electrical Specifications"

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)
8 Ld SOIC Package (Note 4)	105
8 Ld MSOP Package (Note 4)	140
10 Ld DFN Package (Note 5)	75

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. Refer to TB379 for details.
5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. Refer to TB379 for details.

Electrical Specifications

Test Conditions: V_{CC} = 4.75V to 5.25V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, (Note 6).

PARAMETER	SYMBOL	TEST CONDITIONS		TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNITS
DC CHARACTERISTICS								
Driver Differential V_{OUT}	V_{OD}	No Load		Full	-	-	V_{CC}	
		R_L = 100Ω (RS-422) (Figure 1A)		Full	2.6	3.4	-	V
		R_L = 54Ω (RS-485) (Figure 1A)		Full	2.1	2.8	V_{CC}	V
		R_L = 60Ω, -7V ≤ V_{CM} ≤ 12V (Figure 1B)		Full	1.9	2.7	-	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	2	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 54Ω or 100Ω (Figure 1A)		Full	-	0.01	0.2	V
Logic Input High Voltage	V_{IH}	DI, DE, $\overline{RE}$		Full	2	-	-	V
Logic Input Low Voltage	V_{IL}	DI, DE, $\overline{RE}$		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DI = DE = $\overline{RE}$ = 0V or V_{CC}		Full	-2	-	2	µA
Input Current (A/Y, B/Z)	I_{IN2}	DE = 0V, V_{CC} = 0V or 5.25V	V_{IN} = 12V	Full	-	-	220	µA
			V_{IN} = -7V	Full	-160	-	-	µA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	DE = V_{CC}, -7V ≤ V_Y or V_Z ≤ 12V (Note 8)		Full	-	-	±250	mA
Differential Capacitance	C_D	A/Y to B/Z		25	-	9	-	pF
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ V_{CM} ≤ 12V		Full	-200	-	-50	mV
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0V		25	-	28	-	mV
Receiver Output High Voltage	V_{OH}	I_O = -8mA, V_{ID} = -50mV		Full	V_{CC} - 0.5	-	-	V
Receiver Output Low Voltage	V_{OL}	I_O = +10mA, V_{ID} = -200mV		Full	-	-	0.4	V
Receiver Output Low Current	I_{OL}	V_{OL} = 1V, V_{ID} = -200mV		Full	25	40	-	mA
Three-State (High Impedance) Receiver Output Current	I_{OZR}	0.4V ≤ V_O ≤ 2.4V		Full	-1	0.015	1	µA

Electrical Specifications Test Conditions: V_{CC} = 4.75V to 5.25V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNITS
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ 12V	Full	54	80	-	kΩ
Receiver Short-Circuit Current	I_{OSR}	0V ≤ V_O ≤ V_{CC}	Full	±20	-	±110	mA
SUPPLY CURRENT							
No-Load Supply Current (Note 7)	I_{CC}	DI = DE = 0V or V_{CC}	Full	-	2.6	4	mA
Shutdown Supply Current	I_{SHDN}	DE = 0V, $\overline{RE}$ = V_{CC}, DI = 0V or V_{CC}	Full	-	0.05	1	µA
ESD PERFORMANCE							
RS-485 Pins (A/Y, B/Z)		IEC61000-4-2, Air-Gap Discharge Method	25	-	±15	-	kV
		IEC61000-4-2, Contact Discharge Method	25	-	±8	-	kV
		Human Body Model, From Bus Pins to GND	25	-	±16.5	-	kV
All Pins		HBM, per MIL-STD-883 Method 3015	25	-	> ±9	-	kV
		Machine Model	25	-	> ±400	-	V
DRIVER SWITCHING CHARACTERISTICS							
Maximum Data Rate	f_{MAX}	V_{OD} ≥ ±1.5V, R_D = 54Ω, C_L = 100pF (Figure 4)	Full	100	-	-	Mbps
Driver Differential Output Delay	t_{DD}	R_D = 54Ω, C_D = 50pF (Figure 2)	Full	-	8	12	ns
Driver Differential Output Skew	t_{SKEW}	R_D = 54Ω, C_D = 50pF (Figure 2)	Full	-	0.5	1.5	ns
Prop Delay Part-to-Part Skew	t_{SKP-P}	R_D = 54Ω, C_D = 50pF (Figure 2), (Note 14)	Full	-	-	4	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_D = 54Ω, C_D = 50pF (Figure 2)	Full	2	5	8	ns
Driver Enable to Output High	t_{ZH}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 3), (Note 9)	Full	-	13	20	ns
Driver Enable to Output Low	t_{ZL}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 3), (Note 9)	Full	-	11	20	ns
Driver Enable Time Skew	t_{ENSKEW}	|t_{ZH} (Y or Z) - t_{ZL} (Z or Y)|	Full	-	2.5	-	ns
Driver Disable from Output High	t_{HZ}	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 3)	Full	-	14	20	ns
Driver Disable from Output Low	t_{LZ}	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 3)	Full	-	12	20	ns
Driver Disable Time Skew	$t_{DISSKEW}$	|t_{HZ} (Y or Z) - t_{LZ} (Z or Y)|	Full	-	3	-	ns
Time to Shutdown	t_{SHDN}	(Note 11)	Full	60	-	600	ns
Driver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = GND (Figure 3), (Notes 11, 12)	Full	-	-	1000	ns
Driver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 110Ω, C_L = 50pF, SW = V_{CC} (Figure 3), (Notes 11, 12)	Full	-	-	1000	ns
RECEIVER SWITCHING CHARACTERISTICS							
Maximum Data Rate	f_{MAX}	V_{ID} = ±1.5V	Full	100	-	-	Mbps
Receiver Input to Output Delay	t_{PLH}, t_{PHL}	(Figure 5)	Full	-	9	13	ns
Receiver Skew | t_{PLH} - t_{PHL} |	t_{SKD}	(Figure 5)	Full	-	0	1.5	ns
Prop Delay Part-to-Part Skew	t_{SKP-P}	(Figure 5), (Note 14)	Full	-	-	4	ns
Receiver Enable to Output High	t_{ZH}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6), (Note 10)	Full	-	-	12	ns
Receiver Enable to Output Low	t_{ZL}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6), (Note 10)	Full	-	-	12	ns
Receiver Disable from Output High	t_{HZ}	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6)	Full	-	-	12	ns
Receiver Disable from Output Low	t_{LZ}	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6)	Full	-	-	12	ns

Electrical Specifications Test Conditions: V_{CC} = 4.75V to 5.25V; unless otherwise specified. Typical values are at V_{CC} = 5V, T_A = +25°C, (Note 6). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP (°C)	MIN (Note 15)	TYP	MAX (Note 15)	UNITS
Time to Shutdown	t_{SHDN}	(Notes 11)	Full	60	-	600	ns
Receiver Enable from Shutdown to Output High	$t_{ZH(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = GND (Figure 6), (Notes 11, 13)	Full	-	-	1000	ns
Receiver Enable from Shutdown to Output Low	$t_{ZL(SHDN)}$	R_L = 1kΩ, C_L = 15pF, SW = V_{CC} (Figure 6), (Notes 11, 13)	Full	-	-	1000	ns

NOTES:

6. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
7. Supply current specification is valid for loaded drivers when DE = 0V.
8. Applies to peak current. See "Typical Performance Curves" starting on page 11 for more information.
9. Because of the shutdown feature, keep $\overline{RE}$ = 0 to prevent the device from entering SHDN.
10. Because of the shutdown feature, the $\overline{RE}$ signal high time must be short enough (typically <100ns) to prevent the device from entering SHDN.
11. These ICs are put into shutdown by bringing $\overline{RE}$ high and DE low. If the inputs are in this state for less than 60ns, the parts are guaranteed not to enter shutdown. If the inputs are in this state for at least 700ns, the parts are guaranteed to have entered shutdown. See "Low Power Shutdown Mode" on page 10.
12. Keep $\overline{RE}$ = VCC, and set the DE signal low time >700ns to ensure that the device enters SHDN.
13. Set the $\overline{RE}$ signal high time >700ns to ensure that the device enters SHDN.
14. This is the part-to-part skew between any two units tested with identical test conditions (Temperature, V_{CC}, etc.).
15. Parts are 100% tested at +25°C. Over-temperature limits are established by characterization and are not production tested.

Test Circuits and Waveforms

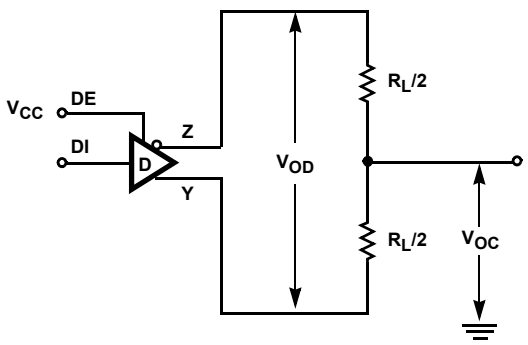


FIGURE 1A. V_{OD} AND V_{OC}

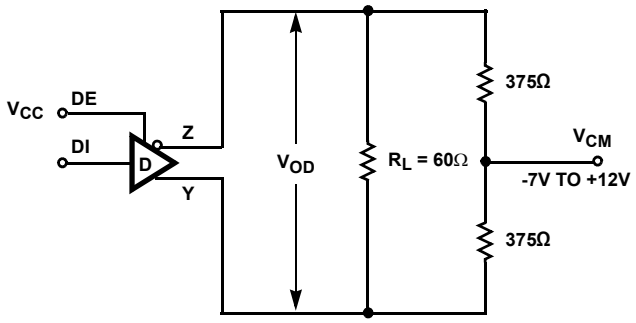


FIGURE 1B. V_{OD} WITH COMMON MODE LOAD

FIGURE 1. DC DRIVER TEST CIRCUITS

Test Circuits and Waveforms (Continued)

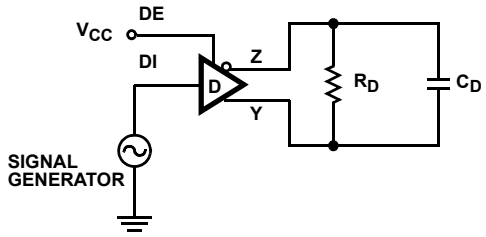


FIGURE 2A. TEST CIRCUIT

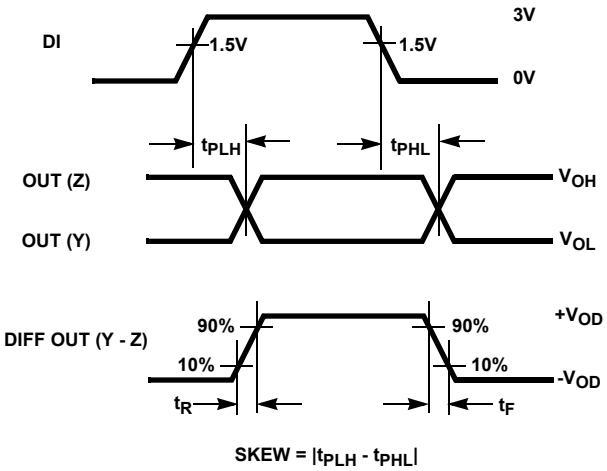
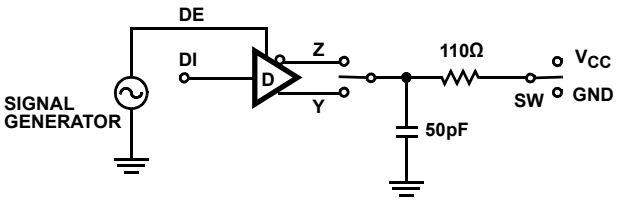


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. DRIVER PROPAGATION DELAY AND DIFFERENTIAL TRANSITION TIMES



PARAMETER	OUTPUT	$\overline{RE}$	DI	SW
t_{HZ}	Y/Z	X	1/0	GND
t_{LZ}	Y/Z	X	0/1	V_{CC}
t_{ZH}	Y/Z	0 (Note 9)	1/0	GND
t_{ZL}	Y/Z	0 (Note 9)	0/1	V_{CC}
$t_{HZ(SHDN)}$	Y/Z	1 (Note 12)	1/0	GND
$t_{LZ(SHDN)}$	Y/Z	1 (Note 12)	0/1	V_{CC}

FIGURE 3A. TEST CIRCUIT

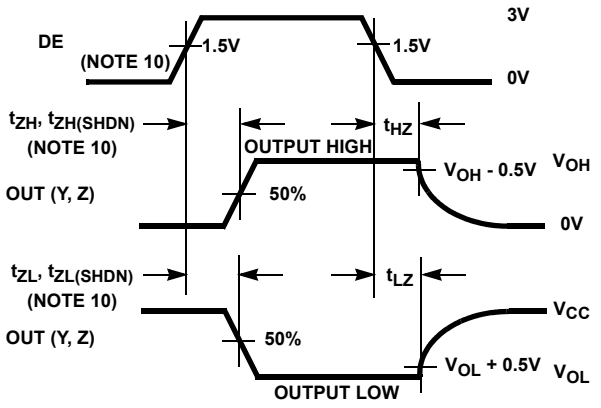


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. DRIVER ENABLE AND DISABLE TIMES

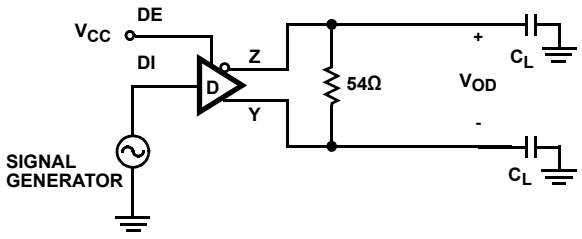


FIGURE 4A. TEST CIRCUIT

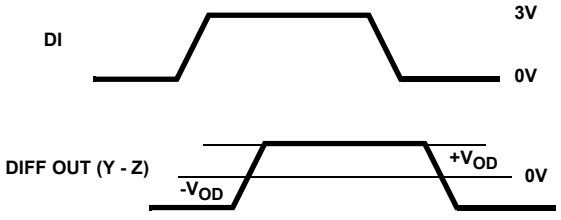


FIGURE 4B. MEASUREMENT POINTS

FIGURE 4. DRIVER DATA RATE

Test Circuits and Waveforms (Continued)

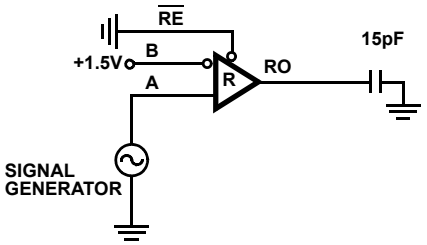


FIGURE 5A. TEST CIRCUIT

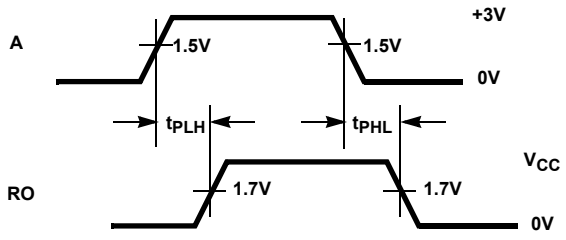
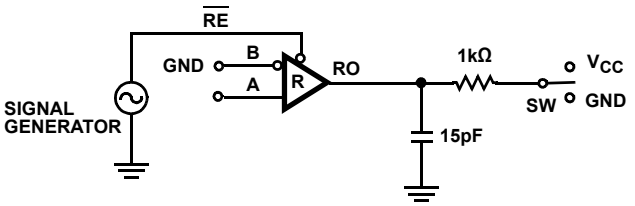


FIGURE 5B. MEASUREMENT POINTS

FIGURE 5. RECEIVER PROPAGATION DELAY



PARAMETER	DE	A	SW
t_{HZ}	0	+1.5V	GND
t_{LZ}	0	-1.5V	V_{CC}
t_{ZH} (Note 10)	0	+1.5V	GND
t_{ZL} (Note 10)	0	-1.5V	V_{CC}
$t_{HZ(SHDN)}$ (Note 13)	0	+1.5V	GND
$t_{LZ(SHDN)}$ (Note 13)	0	-1.5V	V_{CC}

FIGURE 6A. TEST CIRCUIT

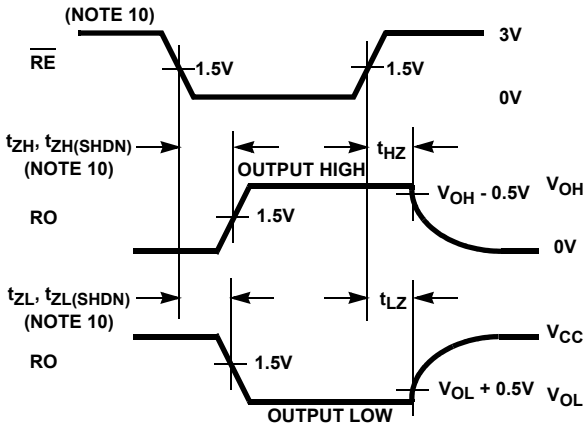


FIGURE 6B. MEASUREMENT POINTS

FIGURE 6. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 receivers on each bus, assuming one unit load devices. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any mix of drivers and receivers) on each bus. To allow for multipoint operation, the RS-485 specification requires that drivers must handle bus contention without sustaining any damage.

Another important advantage of RS-485 is the extended Common Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for cable lengths as long as 4000ft (~1200m), so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver (Rx) Features

This transceiver uses a differential input receiver for maximum noise immunity and common mode rejection. Input sensitivity is ±200mV, as required by the RS-422 and RS-485 specifications. Receiver inputs function with common mode voltages as great as 7V outside the power supplies (that is, +12V and -7V), making them ideal for long networks, or industrial environments, where induced voltages are a realistic concern.

The receiver input resistance of 50kΩ surpasses the RS-422 specification of 4kΩ, and is five times the RS-485 “Unit Load” (UL) requirement of 12kΩ minimum. Thus, the ISL3259E is known as a “one-fifth UL” transceiver, and there can be up to 160 devices on the RS-485 bus while still complying with the RS-485 loading specification.

The receiver is a “full fail-safe” version that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated bus with all the transmitters disabled (terminated/undriven).

Rx outputs deliver large low state currents (typically >30mA) at V_{OL} = 1V, to ease the design of optically coupled isolated networks.

Receivers easily meet the 100Mbps data rate supported by the driver, and the receiver output is tri-statable using the active low $\overline{RE}$ input.

Driver (Tx) Features

The RS-485/RS-422 driver is a differential output device that delivers at least 2.1V across a 54Ω load (RS-485/PROFIBUS), and at least 2.6V across a 100Ω load (RS-422) even with V_{CC} = 4.75V. The drivers feature low propagation delay skew to maximize bit width, and to minimize EMI.

Driver outputs are not slew rate limited, so faster output transition times allow data rates up to 100Mbps. Driver outputs are tri-statable using the active high DE input.

For parallel applications, bit-to-bit skews between any two ISL3259E transmitter and receiver pairs are guaranteed to be no worse than 8ns (4ns maximum for any two Tx, 4ns maximum for any two Rx).

High V_{OD} Improves Noise Immunity and Flexibility

The ISL3259E driver design delivers larger differential output voltages (V_{OD}) than the RS-485 standard requires, or than most RS-485 transmitters can deliver. The minimum ±2.1V V_{OD} guarantees at least ±600mV more noise immunity than networks built using standard 1.5V V_{OD} transmitters.

Another advantage of the large V_{OD} is the ability to drive more than two bus terminations, which allows for use of the ISL3259E in “star” and other multi-terminated, non-standard network topologies. Figure 8 on page 11 details the transmitter’s V_{OD} vs I_{OUT} characteristic, and includes load lines for four (30Ω) and six (20Ω) 120Ω terminations. The figure shows that the driver typically delivers 1.9/1.5V into 4/6 terminations, even at +85°C. The RS-485 standard requires a minimum 1.5V V_{OD} into two terminations, but the ISL3259E typically delivers RS-485 voltage levels with 2x to 3x the number of terminations.

ESD Protection

All pins on the ISL3259E include Class 3 (>9kV) Human Body Model (HBM) ESD protection structures, but the RS-485 pins (driver outputs and receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±16.5kV HBM and ±15kV IEC61000-4-2. The RS-485 pins are particularly vulnerable to ESD strikes because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that can destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common mode range of -7V to +12V. This built-in ESD protection eliminates the need for board level protection structures (for example, transient suppression diodes), and the associated, undesirable capacitive load they present.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case), and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The IEC61000 standard’s lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device’s RS-485 pins allows the design of equipment meeting Level 4 criteria without the need for additional board level protection on the RS-485 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc, so it is more difficult to obtain repeatable results. The ISL3259E RS-485 pins withstand ±15kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The RS-485 pins of the ISL3259E survive ±8kV contact discharges.

Hot Plug Function

When a piece of equipment powers up, a period of time occurs in which the processor or ASIC driving the RS-485 control lines (DE, $\overline{RE}$) is unable to ensure that the RS-485 Tx and Rx outputs are kept disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up may crash the bus. To avoid this scenario, the ISL3259E incorporates a hot plug function. Circuitry monitoring V_{CC} ensures that, during power-up and power-down, the Tx and Rx outputs remain disabled, regardless of the state of DE and $\overline{RE}$, if V_{CC} is less than ~3.2V. This gives the processor/ASIC a chance to stabilize and drive the RS-485 control lines to the proper states.

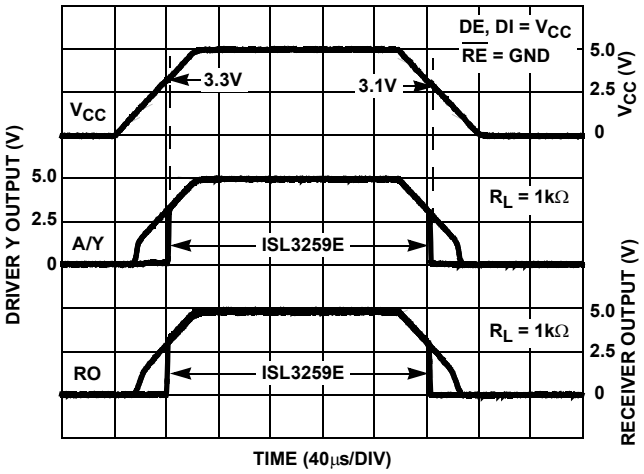


FIGURE 7. HOT PLUG PERFORMANCE (ISL3259E) vs ISL83088E WITHOUT HOT PLUG CIRCUITRY

Data Rate, Cables, and Terminations

Twisted pair is the cable of choice for RS-485, RS-422, and PROFIBUS networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common mode signals, which are effectively rejected by the differential receivers in these ICs.

According to guidelines in the RS-422 and PROFIBUS specifications, networks operating at data rates in excess of 3Mbps should be limited to cable lengths of 100m (328 ft) or less, and the PROFIBUS specification recommends that the more expensive "Type A" (22AWG) cable be used. The ISL3259E's large differential output swing, fast transition times, and high drive-current output stages allow operation even at 100Mbps over standard "CAT-5" cables up to 31m (100ft). Figures 16 and 17 detail the ISL3259E performance at this condition, with a 120Ω termination resistor at both the driver and the receiver ends. Note that the differential signal delivered to the receiver at the end of the cable (A - B) still exceeds 1V, so even longer cables could be driven if lower noise margins are acceptable. Of course, jitter or some other criteria may limit the network to shorter cable lengths than those discussed here. If more noise margin is desired, shorter cables may produce a larger receiver input signal. Performance should be even better if using the "Type A" cable.

The ISL3259E can also be used at slower data rates over longer cables, but some limitations apply. The Rx is optimized for high speed operation, so its output may glitch if the Rx input differential transition times are too slow. Keeping the transition times below 500ns, (which equates to the Tx driving a 1000ft (305m) CAT-5 cable) yields excellent performance over the full operating temperature range.

To minimize reflections, proper termination is imperative when using this high data rate transceiver. In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω for "CAT-5", and 220Ω for "Type A") at the end farthest from the driver. In multi-receiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multi-driver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transceiver to the main cable should be kept as short as possible.

Built-In Driver Overload Protection

As stated previously, the RS-485 specification requires that drivers survive worst case bus contentions undamaged. These transmitters meet this requirement using driver output short circuit current limits, and on-chip thermal shutdown circuitry.

The driver output stages incorporate short circuit current limiting circuitry, which ensures that the output current never exceeds the RS-485 specification, even at the common mode voltage range extremes. In the event of a major short circuit condition, the device also includes a thermal shutdown feature that disables the drivers whenever the die temperature becomes excessive. This eliminates the power dissipation, allowing the die to cool. The drivers automatically reenable after the die temperature drops about +15 degrees. If the contention persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared. Receivers stay operational during thermal shutdown.

Low Power Shutdown Mode

This BiCMOS transceiver uses a fraction of the power required by its bipolar counterparts, but it also includes a shutdown feature that reduces the already low quiescent I_{CC} to a 50nA trickle. It enters shutdown whenever the receiver and driver are *simultaneously* disabled ($\overline{RE}$ = V_{CC} and DE = GND) for a period of at least 600ns. Disabling both the driver and the receiver for less than 60ns guarantees that the transceiver will not enter shutdown.

Note that receiver and driver enable times increase when the transceiver enables from shutdown. Refer to Notes 9, 10, 11, 12, and 13 in the "Electrical Specifications" section for more information.

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified

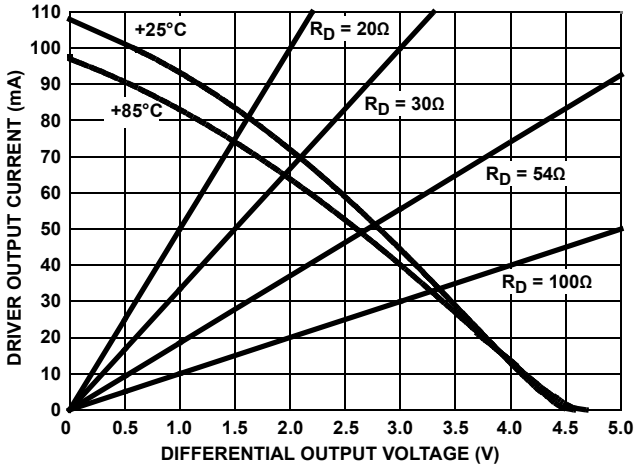


FIGURE 8. DRIVER OUTPUT CURRENT vs DIFFERENTIAL OUTPUT VOLTAGE

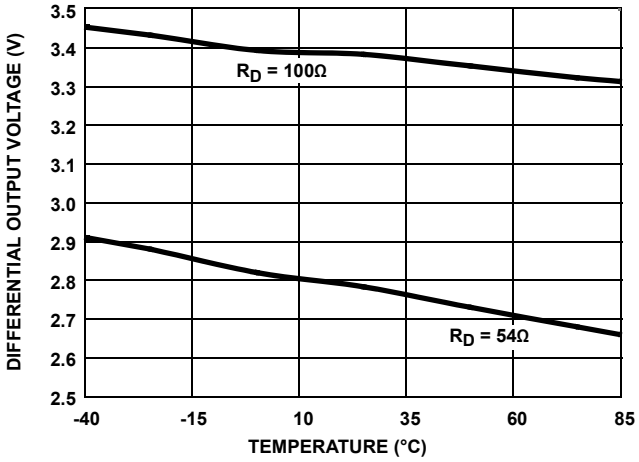


FIGURE 9. DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs TEMPERATURE

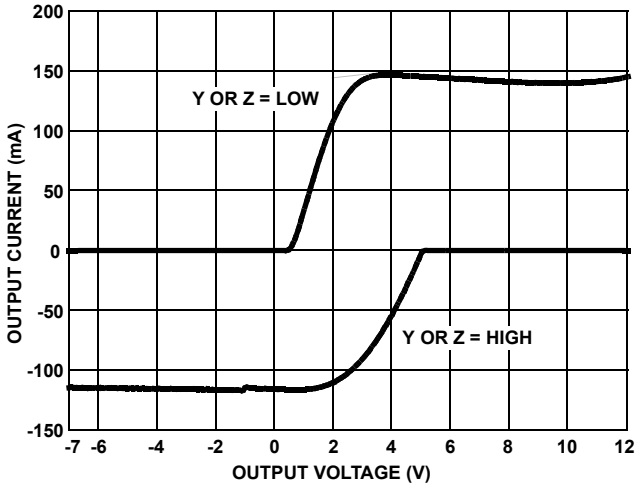


FIGURE 10. DRIVER OUTPUT CURRENT vs SHORT CIRCUIT VOLTAGE

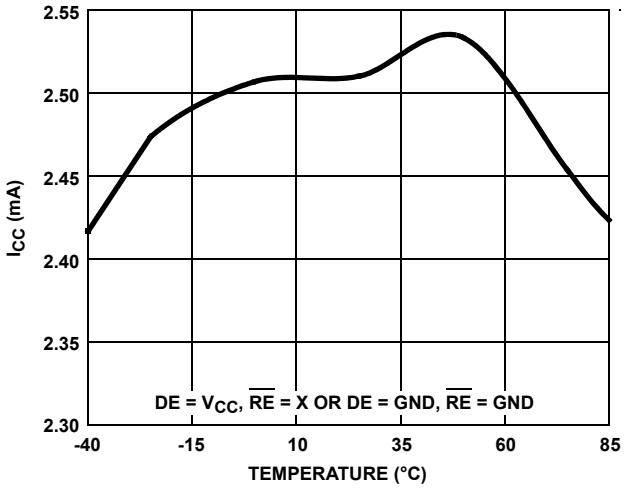


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

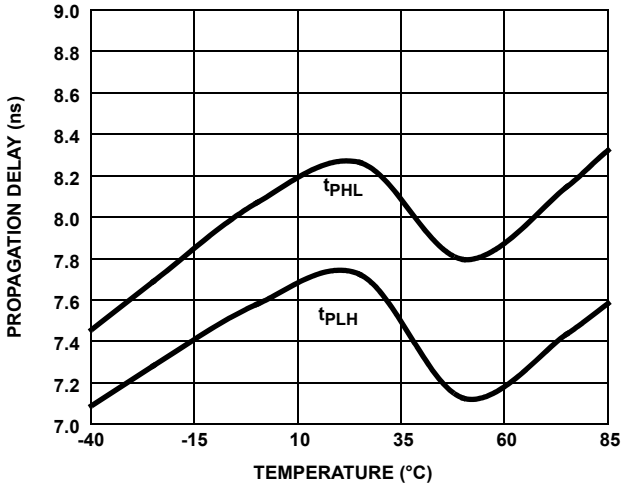


FIGURE 12. DRIVER DIFFERENTIAL PROPAGATION DELAY vs TEMPERATURE

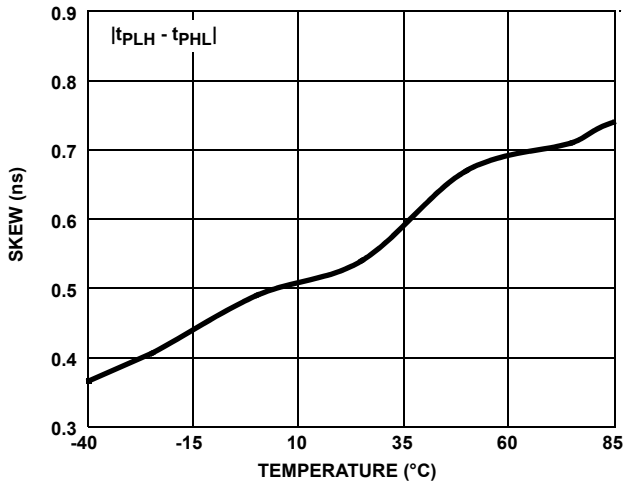


FIGURE 13. DRIVER DIFFERENTIAL SKEW vs TEMPERATURE

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified

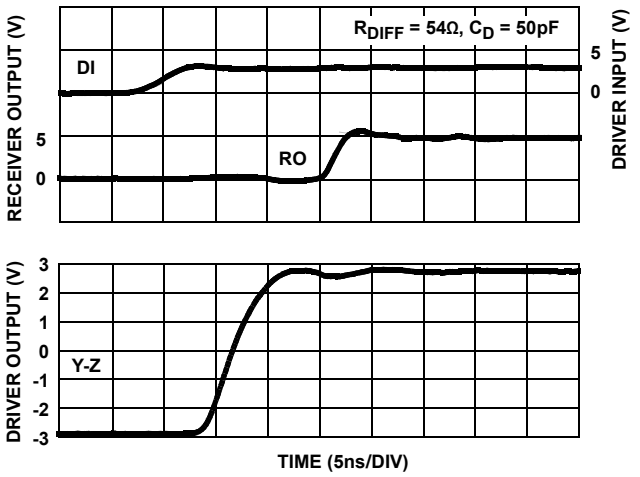


FIGURE 14. DRIVER AND RECEIVER WAVEFORMS

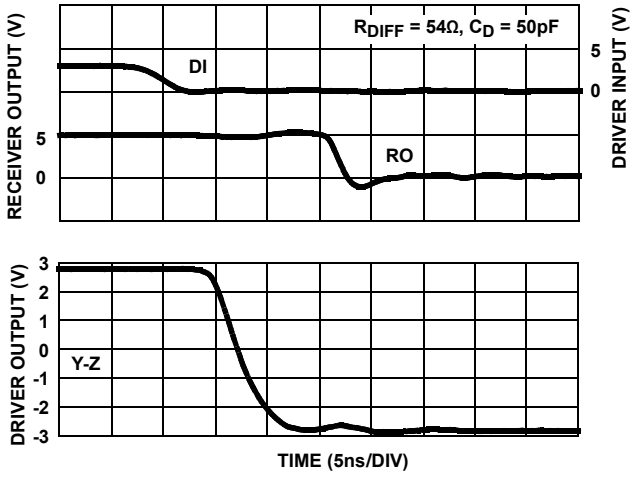


FIGURE 15. DRIVER AND RECEIVER WAVEFORMS

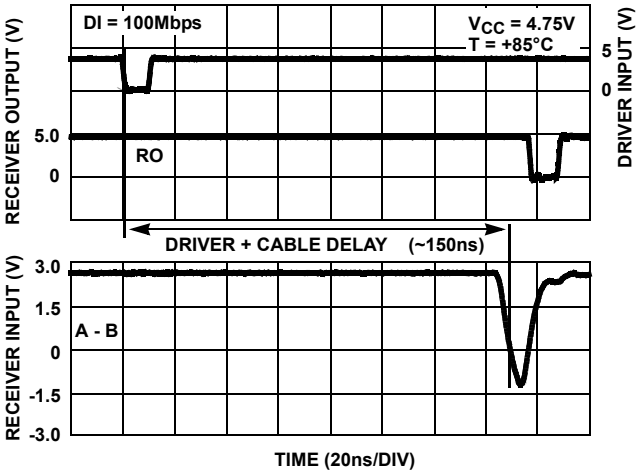


FIGURE 16. WORST CASE (NEGATIVE) SINGLE PULSE DRIVER AND RECEIVER WAVEFORMS DRIVING 100 FEET (31 METERS) OF CAT5 CABLE (DOUBLE TERMINATED WITH 120Ω)

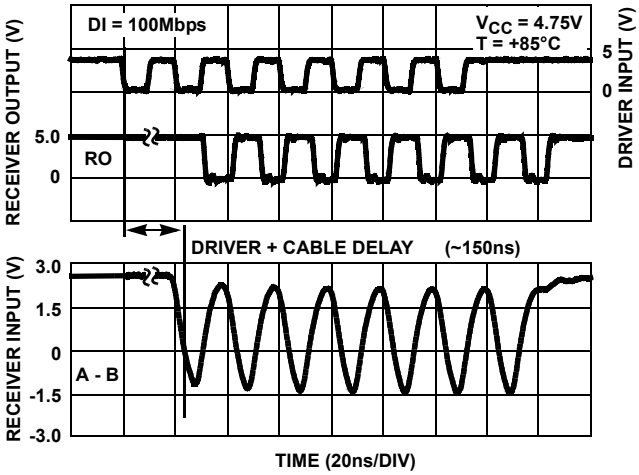


FIGURE 17. DRIVER AND RECEIVER SEVEN PULSE WAVEFORMS DRIVING 100 FEET (31 METERS) OF CAT5 CABLE (DOUBLE TERMINATED WITH 120Ω)

Typical Performance Curves V_{CC} = 5V, T_A = +25°C; Unless Otherwise Specified

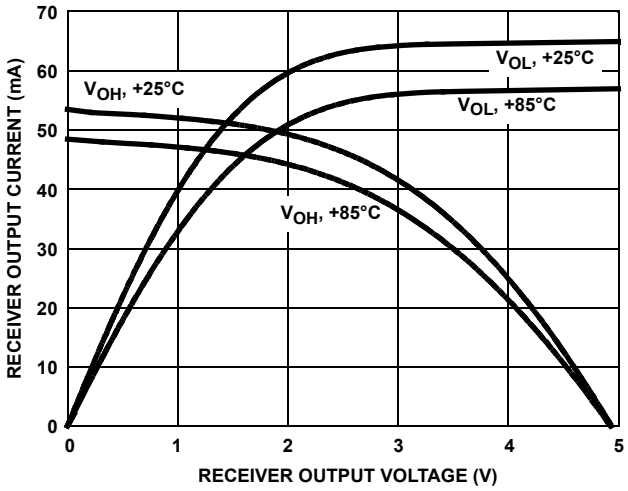


FIGURE 18. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Die Characteristics

SUBSTRATE AND DFN THERMAL PAD POTENTIAL (POWERED UP)

GND

TRANSISTOR COUNT

768

PROCESS

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Aug 31, 2017	FN6587.2	Added Related Literature section. Added V_{AB} information to Receiving Truth Table on page 2. Applied new header/footer.
Feb 18, 2008	FN6587.1	Initial release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

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You can report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

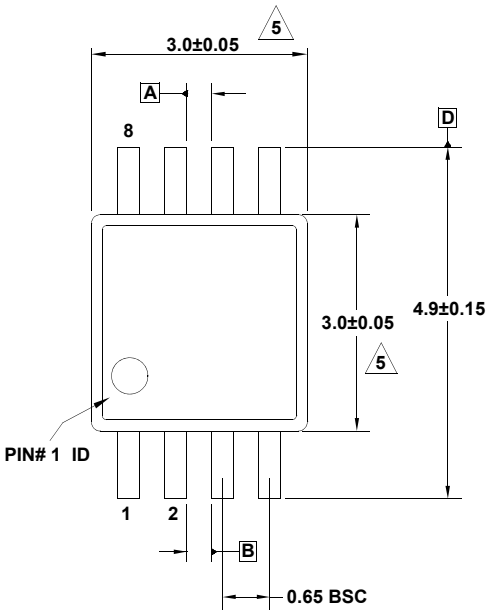
Package Outline Drawing

For the most recent package outline drawing, see M8.118.

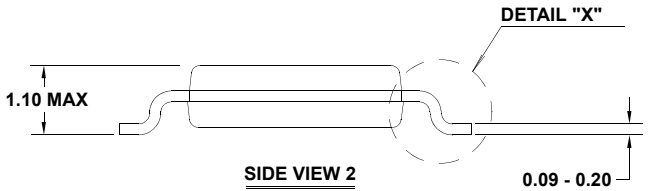
M8.118

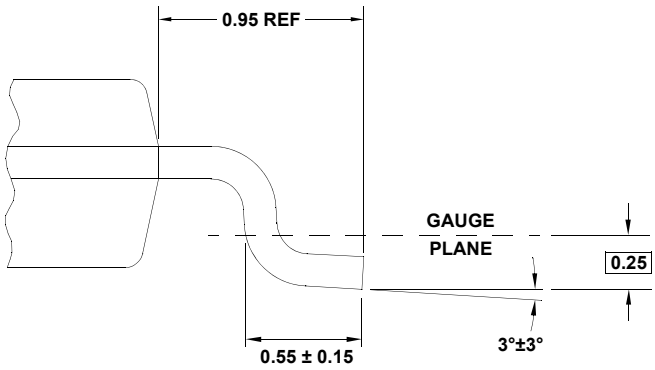
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

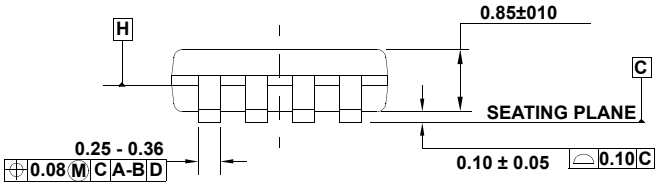


TOP VIEW

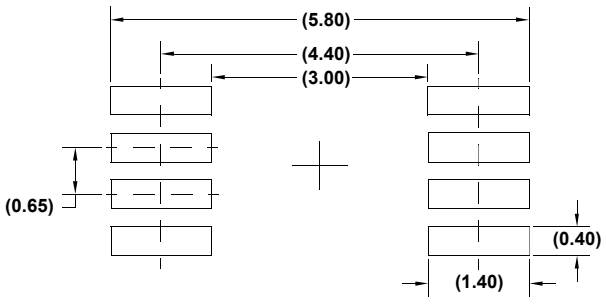




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.

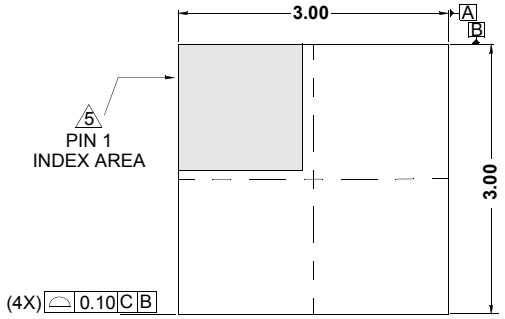
Package Outline Drawing

For the most recent package outline drawing, see L10.3x3C.

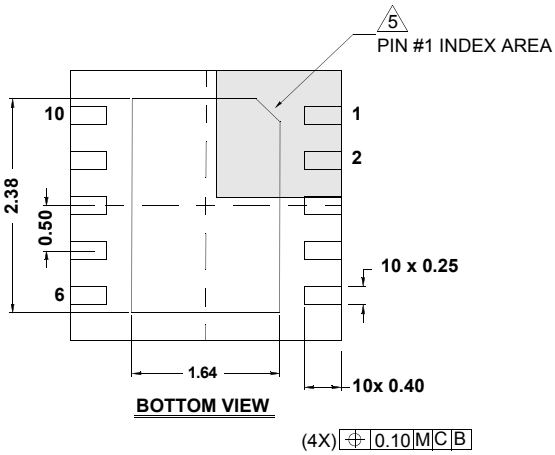
L10.3x3C

10 LEAD DUAL FLAT PACKAGE (DFN)

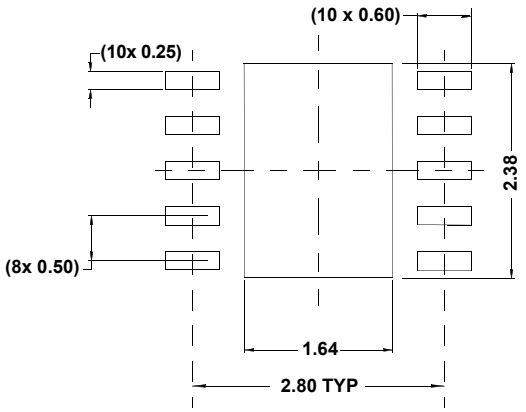
Rev 4, 3/15



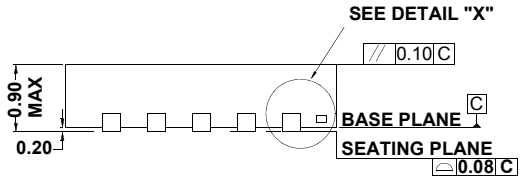
TOP VIEW



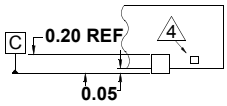
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Compliant to JEDEC MO-229-WEED-3 except for E-PAD dimensions.

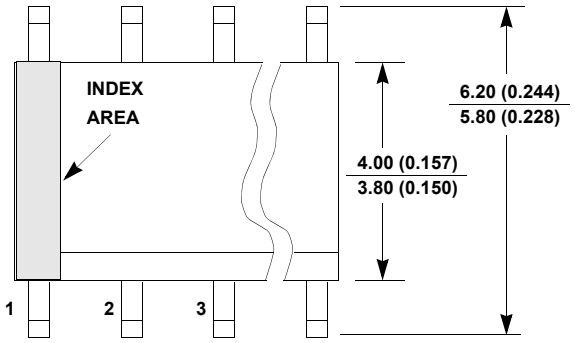
Package Outline Drawing

For the most recent package outline drawing, see M8.15.

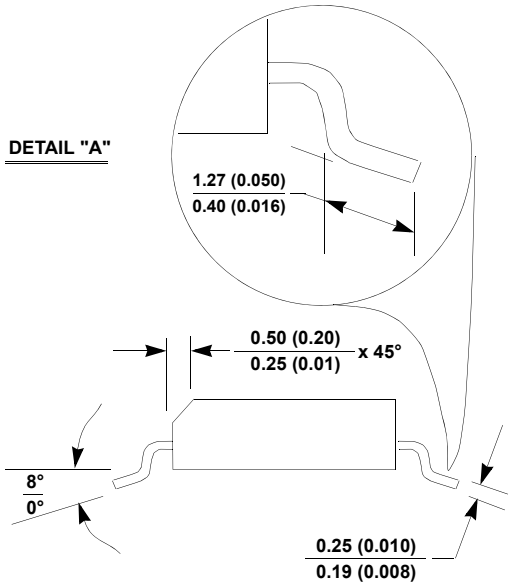
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

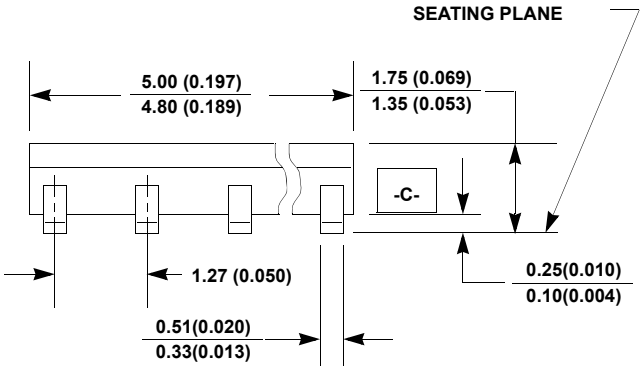
Rev 4, 1/12



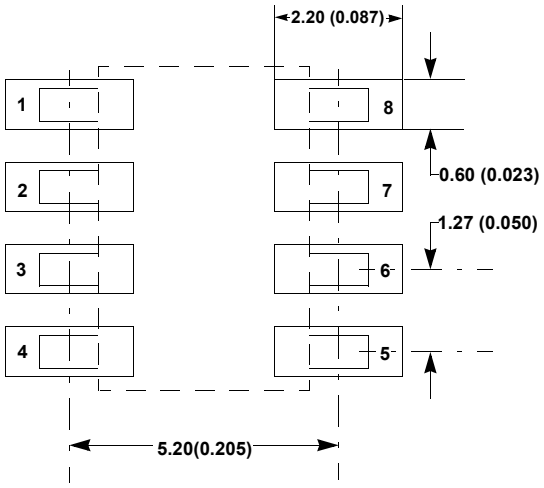
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

16. Dimensioning and tolerancing per ANSI Y14.5M-1994.
17. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
18. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
19. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
20. Terminal numbers are shown for reference only.
21. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
22. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
23. This outline conforms to JEDEC publication MS-012-AA ISSUE C.