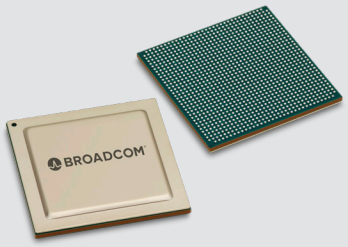
BROADCOM®

Product Brief

BCM87580

7-nm 400GbE PAM-4 PHY (8:8) for Transceiver Applications



Applications

- 400GbE SR8/AOC
- Supports breakout applications for SR8 to 8 × SR1, 4 × SR2, and 2 × SR4
- 400GbE (8 × 50G PAM-4), 2 × 200GbE (4 × 50G PAM-4), 4 × 100GbE (2 × 50G PAM-4), and 8 × 50GbE (1 × 50G PAM-4) transceivers
- 1 × 200GbE (8 × 25G NRZ), 2 × 100GbE (4 × 25G NRZ), 4 × 50GbE (2 × 25G NRZ), and 8 × 25GbE (1 × 25G NRZ) transceivers

Overview

The Broadcom® BCM87580 is a single-chip, low-power, low-latency PAM-4 PHY that integrates retimer and equalizer functions to support 400GbE, 2 × 200GbE, 4 × 100GbE, and 8 × 50GbE applications. In these modes, the BCM87580 retimes, adds FEC (optional), and equalizes n × 50G PAM-4 host-side signals into n × 50G PAM-4 line-side signals, which drive the optical PAM-4 links inside the next-generation modules, including QSFPDD and OSFP modules.

The BCM87580 is compliant with the IEEE 400G AUI-C2M and 200G AUI-C2M standards with KP4 FEC and FEC bypass capabilities.

The BCM87580 also supports 1 × 200GbE, 2 × 100GbE, 4 × 50GbE, and 8 × 25GbE modes. In these modes, the device retimes and equalizes the incoming data from the both host and line sides at n × 25G NRZ rate.

On-chip clock synthesis is performed by a low-cost 156.25-MHz reference clock using high-frequency, low-jitter phase-locked loops (PLLs).

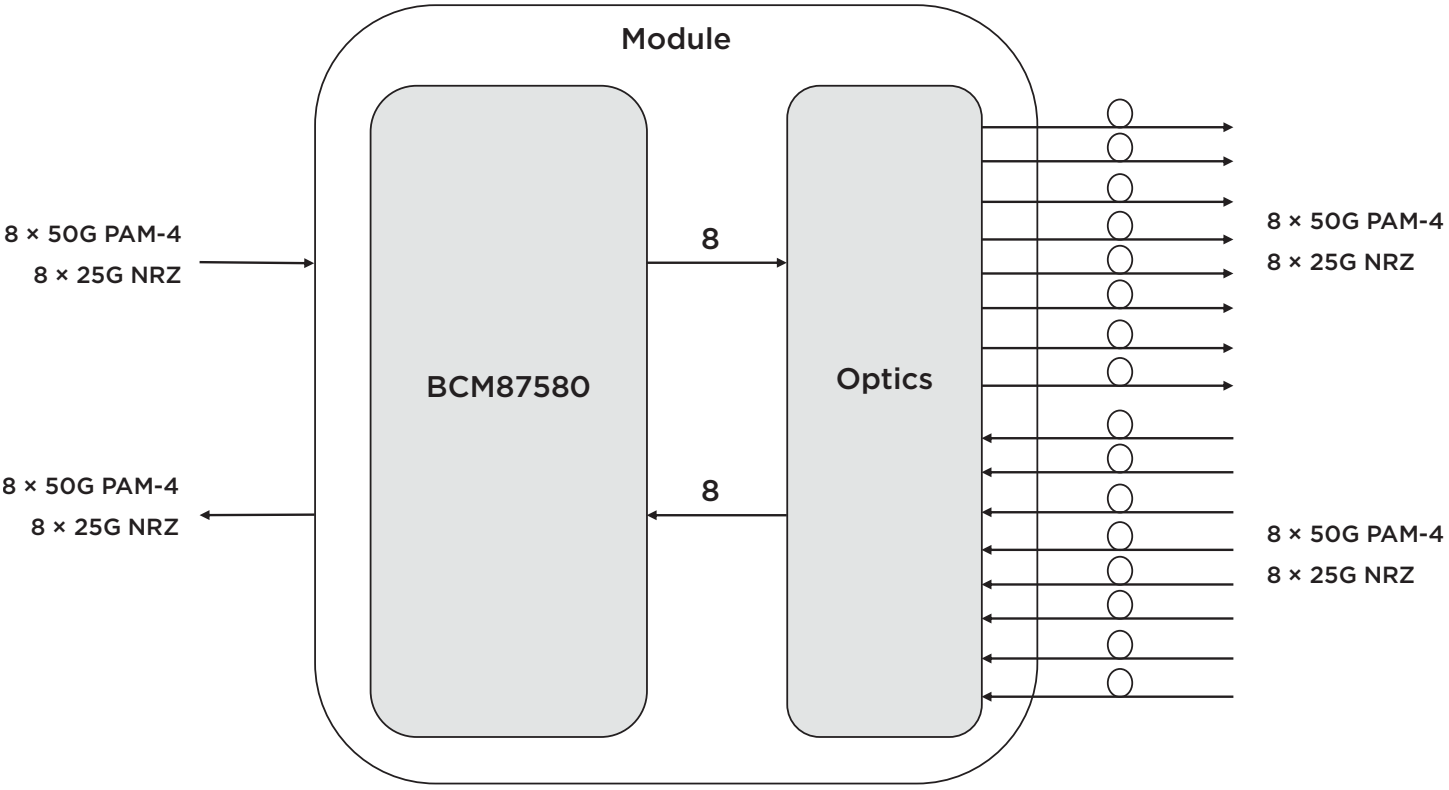
The BCM87580 is fabricated in advanced low-power 7-nm CMOS technology.

The BCM87580 is available in a 12.5 mm × 11 mm, 0.5-mm pitch, 504-ball BGA, RoHS-compliant package.

Features

- Single-chip 8 × 50G PHY drives 1 × 400GbE, 2 × 200GbE, 4 × 100GbE, and 8 × 50GbE transceivers
  - Client side: 8 × 50G PAM-4
  - Line side: 8 × 50G PAM-4
- Single-chip 8 × 25G drives 1 × 200GbE, 2 × 100GbE, 4 × 50GbE, and 8 × 25GbE transceivers
  - Client side: 8 × 25G NRZ
  - Line side: 8 × 25G NRZ
- Client-side interface is compliant with the IEEE 400GAUI-8 PAM-4 C2M and 200GAUI-8 NRZ C2M specification supporting VSR channels
- Data path supports mixed mode of operation
- All eight channels are independent and can be programmed independently
- Supports both QSFPDD and OSFP transceivers
- Low-power 7-nm CMOS design
- Integrated AC-coupling capacitors for the client RX side
- Line-side and client-side loopbacks

Block Diagram



Ordering Information

Part Number	Package
BCM87580A0KFEBG	A0 Silicon, 12.5 mm × 11 mm, 0.5-mm pitch, 504-ball BGA, RoHS-compliant

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87580-PB100 May 3, 2021