Circuit Note
CN-0278

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0278.

Devices Connected/Referenced	
AD5700, AD5700-1	Low Power HART Modem
AD5422	16-Bit Current and Voltage Output DAC

Complete 4 mA to 20 mA HART Solution with Additional Voltage Output Capability

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

AD5422 Circuit Evaluation Board (EVAL-AD5422EBZ, LFCSP version)
AD5700-1/AD5700 Evaluation Board (EVAL-AD5700-1EBZ)

Design and Integration Files

Schematics, Layout Files, Bill of Materials

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 uses the AD5700, the industry's lowest power and smallest footprint HART®[1]-compliant IC modem, and the AD5422, a 16-bit current output and voltage output DAC, to form a complete HART-compatible 4 mA to 20 mA solution. The use of the OP184 in the circuit allows the I_{OUT} and V_{OUT} pins to be shorted together, thus reducing the number of screw connections required in programmable logic control (PLC) module applications. For additional space savings, the AD5700-1 offers a 0.5% precision internal oscillator.

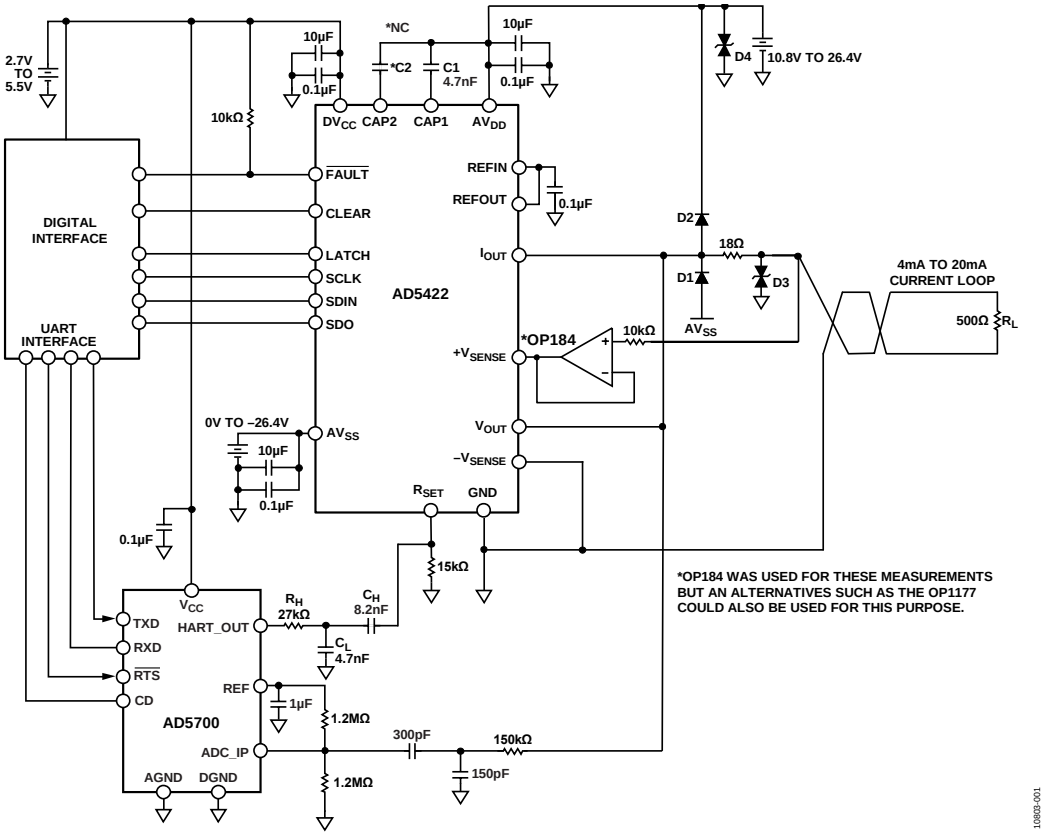

Figure 1. AD5422 HART-Enabled Circuit Simplified Schematic

[1] HART is a registered trademark of the HART Communication Foundation.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

Application Note AN-1065 describes a manner in which the AD5420 I_{OUT} DAC can be configured for HART communication compliance. AN-1065 outlines how the AD5700 HART modem output can be attenuated and ac coupled into the AD5420 via the CAP2 pin. The same is true of the AD5422. However, if the application involves a particularly harsh environment, an alternative circuit configuration can be used which offers better power supply rejection characteristics. This alternative circuit requires the use of the external R_{SET} resistor and involves coupling the HART signal into the R_{SET} pin of the AD5420 or AD5422. The CN-0270 describes this solution for the AD5420, typical of line-powered transmitter applications. The current circuit note is relevant to the AD5422, which, unlike the AD5420, offers both a voltage and a current output pin, and so is particularly useful in PLC/distributed control system (DCS) applications. The AD5422 is available in both 40-lead LFCSP and 24-lead TSSOP packages and the relevance of this, to the circuit characteristics, is examined in the Circuit Description section.

This circuit adheres to the HART physical layer specifications as defined by the HART Communication Foundation, for example, the output noise during silence and the analog rate of change specifications.

For many years, 4 mA to 20 mA communication has been used in process control instrumentation. This communication method is reliable and robust, and offers high immunity to environmental interference over long communication distances. A limitation, however, is that only 1-way communication of one process variable at a time is possible.

The development of the highway addressable remote transducer (HART) standard provided highly capable 2-way digital communication, simultaneously with the 4 mA to 20 mA analog signaling used by traditional instrumentation equipment. This allows for features such as remote calibration, fault interrogation, and transmission of additional process variables. Put simply, HART is a digital two-way communication in which a 1 mA peak-to-peak, frequency-shift-keyed (FSK) signal is modulated on top of the 4 mA to 20 mA analog current signal.

CIRCUIT DESCRIPTION

Figure 1 shows the manner in which the AD5422 can be combined with the AD5700 HART modem and a UART interface to construct a HART-capable 4 mA to 20 mA current output, typical of PLC and DCS systems. The buffer connected to the $+V_{SENSE}$ pin is not necessary if the application does not require the I_{OUT} and V_{OUT} pins to be shorted. The HART_OUT signal from the AD5700 is attenuated and ac-coupled into the R_{SET} pin of the AD5422. If the external R_{SET} resistor is not being used, an alternative method of connecting the AD5422 and the AD5700 via the CAP2 pin can be found in Application Note AN-1065, as previously described. This method is only relevant to the 40-lead LFCSP package option of the AD5422 because the lower pin-count 24-lead TSSOP package does not contain a CAP2 pin.

While the method described in the current circuit note requires the use of the external R_{SET} resistor, in return, it provides better power supply rejection performance than the alternative application note solution. The use of either solution results in the AD5700 HART modem output modulating the 4 mA to 20 mA analog current (as shown in Figure 2) without affecting the dc level of the current. The diode protection circuitry (D1 to D4) is discussed in more detail in the Transient Voltage Protection section.

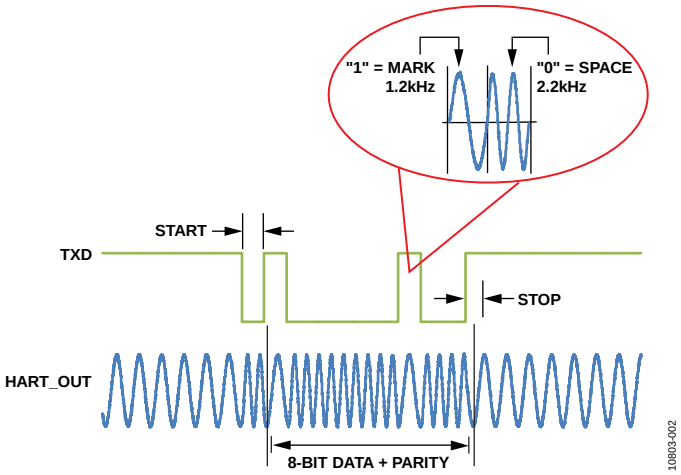

Figure 2. AD5700/AD5700-1 Sample Modulator Waveform

Determining the Values of the External Components

Capacitors, C1 and C2, can be used in conjunction with the digital slew rate control functionality of the part to control the slew rate of the I_{OUT} signal of the AD5422. In determining the absolute values of the capacitors, ensure that the FSK output from the modem is passed undistorted. Thus, the bandwidth presented to the modem output signal must pass the 1200 Hz and 2200 Hz frequencies. Figure 3 shows a circuit that achieves this requirement. In this case, C2 (shown in Figure 1) is left open-circuit.

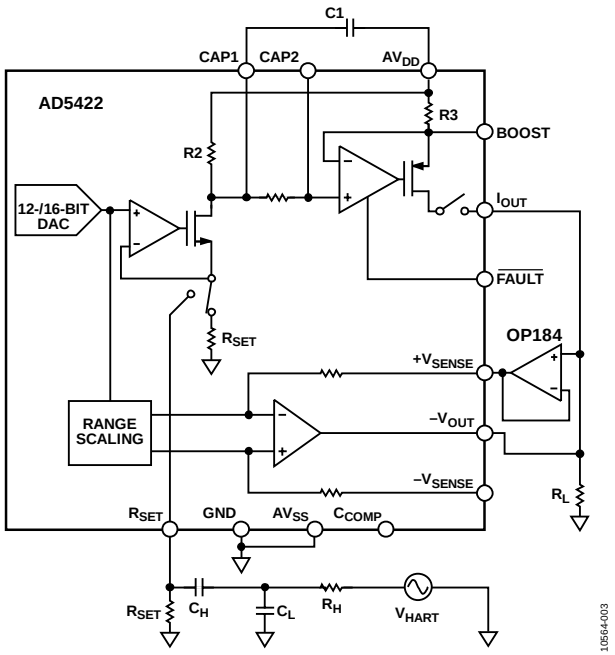

Figure 3. AD5422 and AD5700 HART Modem Connection

The low-pass and high-pass filter circuitry is formed through the interaction of R_H, C_L, C_H, and C1, along with some internal circuitry in the AD5422. In calculating the values of these components, the low-pass and high-pass frequency cutoff point targets were >10 kHz and <500 Hz, respectively. Figure 4 shows a plot of the simulated frequency response, while Table 1 shows the effect on the frequency response of increasing each component while the remaining component values are kept constant.

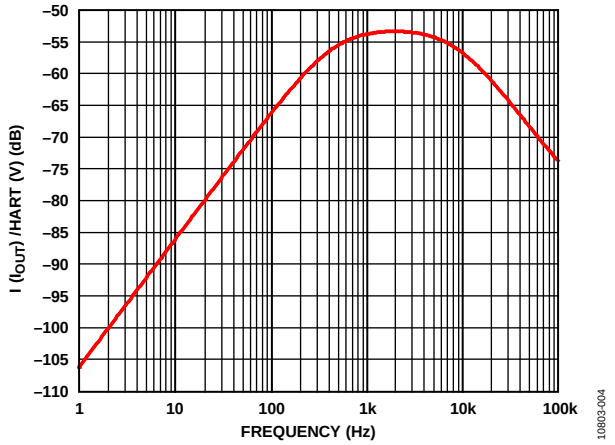

Figure 4. Simulated Frequency Response

Table 1. Effect on Frequency Response of Individual Component Value Increase

Component	C1	C_H	C_L	R_H
f_L (Hz)	↓	↓	↓	↓
f_H (kHz)	↓	No change	No change	No change
G (dB)	↓	↑	↓	↓

The output of the modem is an FSK signal consisting of 1200 Hz and 2200 Hz shift frequencies. This signal must translate to a 1 mA p-p current signal. To achieve this, the signal amplitude at the R_{SET} pin must be attenuated. This is due to the internal current gain configuration in the AD5422 design. Assuming that the modem output amplitude is 500 mV p-p, its output must be attenuated by 500/150 = 3.33. This attenuation is achieved by means of R_H and C_L.

The measurements in this circuit note were completed using the following component values:

- C1 = 4.7 nF
- R_H = 27 kΩ
- C_L = 4.7 nF
- C_H = 8.2 nF

Figure 5 shows the individual 1200 Hz and 2200 Hz shift frequencies measured across a 500 Ω load resistor. Channel 1 shows the modulated HART signal coupled into the AD5422 output (set to output 4 mA), while Channel 2 shows the AD5700 TXD signal.

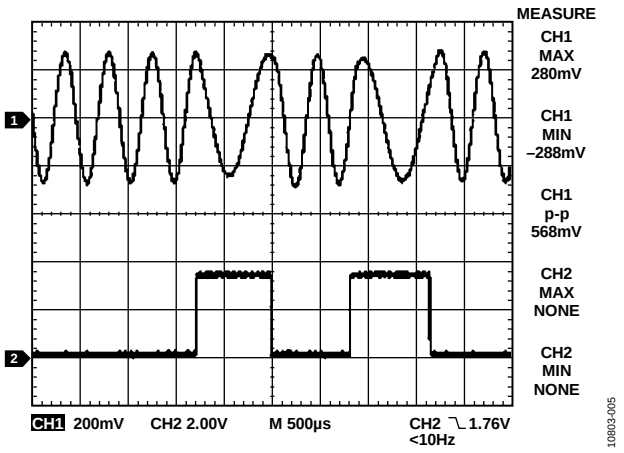

Figure 5. FSK Waveforms Measured Across a 500 Ω Load

HART Compliance

For the circuit in Figure 1 to be HART-compliant, it must meet the HART physical layer specifications. There are numerous physical layer specifications included in the HART specification documents. The two that are most important in this case are the output noise during silence and the analog rate of change.

Output Noise During Silence

When a HART device is not transmitting (silent), it should not couple noise onto the network in the HART extended frequency band. Excessive noise may interfere with reception of HART signals by the device itself or other devices on the network.

The voltage noise measured across a 500 Ω load must contain no more than 2.2 mV rms of combined broadband and correlated noise in the extended frequency band. This noise was measured by connecting the HCF_TOOL-31 filter (available from the HART Communication Foundation) across the 500 Ω load and by connecting the output of the filter to a true rms meter (see Figure 6). An oscilloscope was also used to examine the output waveform peak-to-peak voltage.

The AD5422 output current was set to 4 mA, 12 mA, and 20 mA. Results with the band-pass filter in place were very similar for all three output current values, while the wide bandwidth noise increased slightly as the current output value increased. The rms values measured, with and without the HCF_TOOL-31 band-pass filter in the case of 4 mA output current, were 143 µV rms and 1.4 mV rms, respectively. Both of these values are well within the required specifications of 2.2 mV rms (with HART filter) and 138 mV rms (broadband noise without HART filter). For 12 mA output current, the rms values measured, with and without the HCF_TOOL-31 band-pass filter were 158 µV rms and 2.1 mV rms, respectively, again, both well within HART protocol specifications.

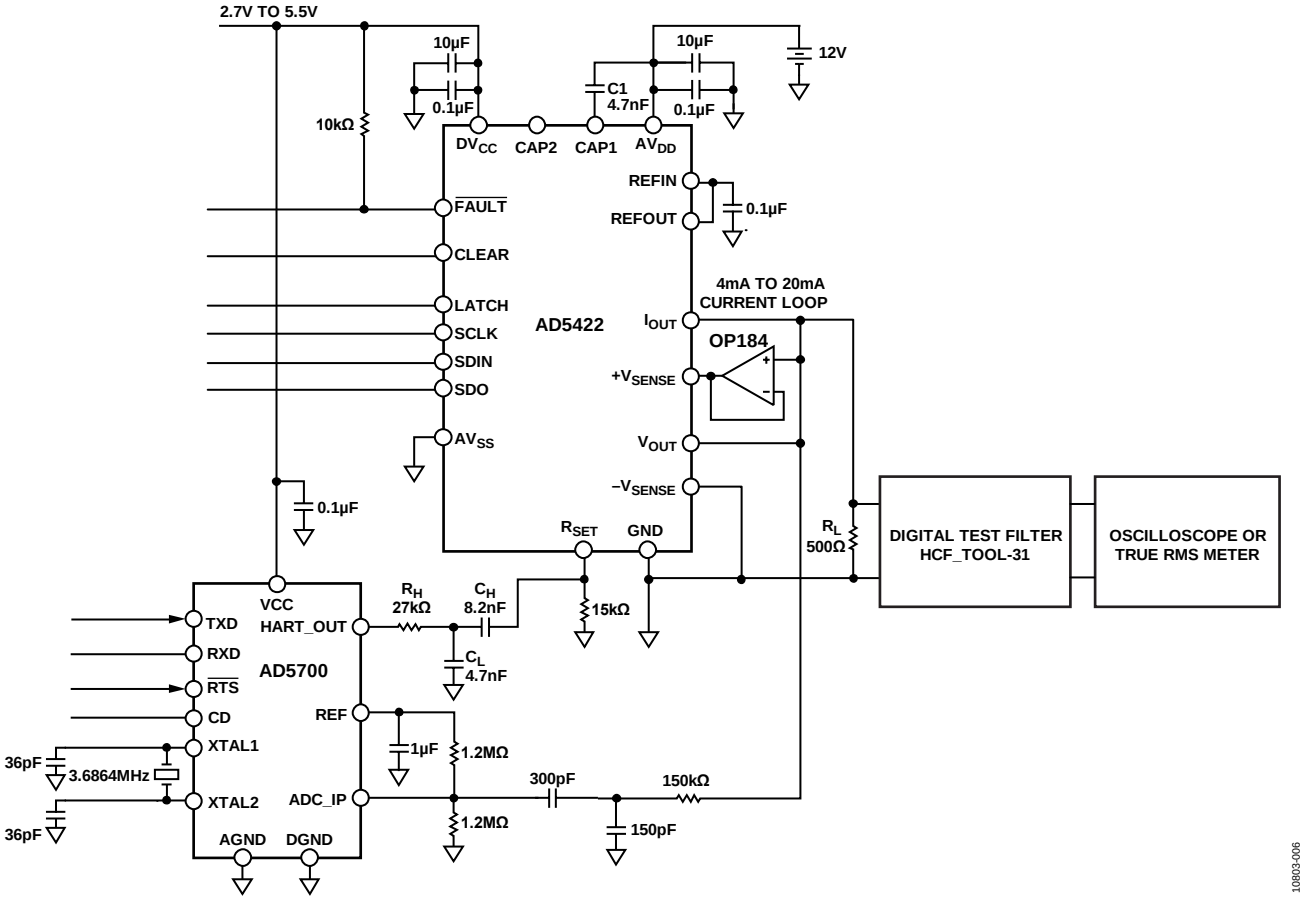

Figure 6. HART Specifications Test Circuit

Figure 7 and Figure 8 show the oscilloscope plots for 4 mA and 12 mA output current, respectively. Note that the filter has a pass-band gain of 10. Channel 1 and Channel 2 on each plot show the input and output of the filter, respectively.

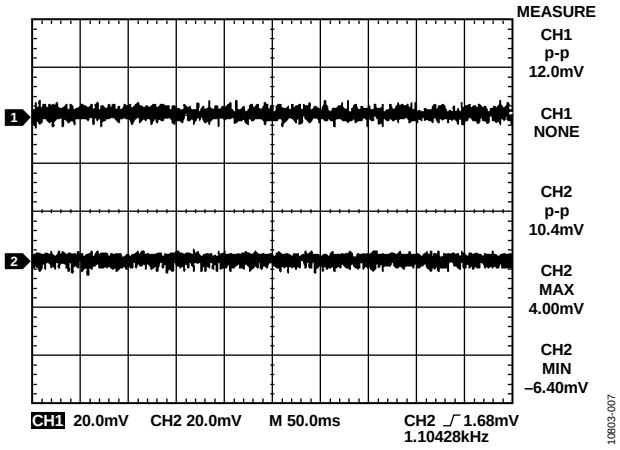

Figure 7. Noise at Input (CH1) and Output (CH2) of HART Filter with 4 mA Output Current

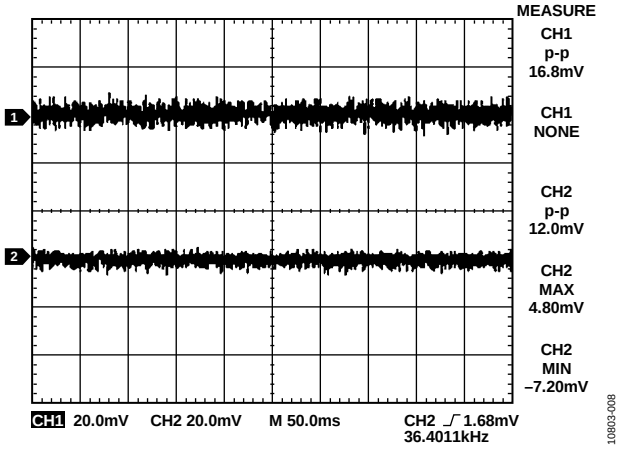

Figure 8. Noise at Input (CH1) and Output (CH2) of HART Filter with 12 mA Output Current

Analog Rate of Change

This specification ensures that when a device regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling. The same test circuit shown in Figure 6 was used. For this test, the AD5422 was programmed to output a cyclic waveform, switching from 4 mA to 20 mA with no delay at either value, to ensure the maximum rate of change. To meet the HART specifications, the waveform at the output of the filter must not exhibit a peak voltage greater than 150 mV. Meeting this requirement ensures that the maximum bandwidth of the analog signaling is within the specified dc to 25 Hz frequency band.

The normal time for the output of the AD5422 to change from 4 mA to 20 mA is about 10 µs. This is obviously too fast and can cause major disruption to a HART network. To reduce the rate of change, the AD5422 employs two features: connecting capacitors at the CAP1 and CAP2 pins, and an internal linear digital slew rate control function (refer to the AD5422 data sheet for details). For faster slew rates, a nonlinear digital ramp can be implemented on the controller/FPGA communicating with the AD5422.

It requires very large capacitor values at CAP1 and CAP2 to reduce the bandwidth below 25 Hz. The optimum solution is to use a combination of the external capacitors and the digital slew rate control function of the AD5422. The two capacitors, C1 and C2, have the effect of reducing the rate of change of the analog signal; however, not sufficiently enough to meet the specification. Enabling the slew rate control feature offers the flexibility to set the rate of change.

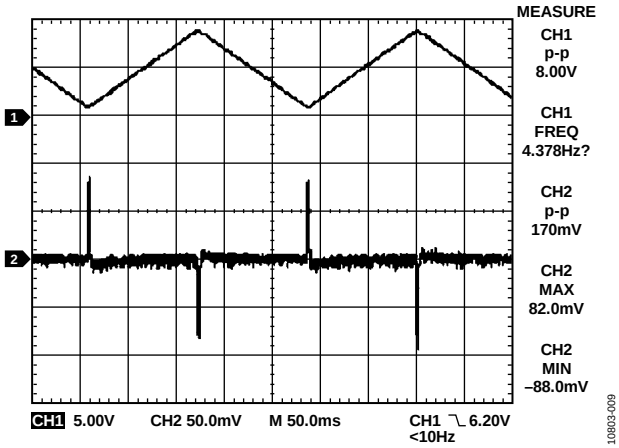

Figure 9. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 3, SR Step = 2, C1 = 4.7 nF, C2 = NC

Figure 9 shows the output of the AD5422 and the output of the HART filter. The peak voltage at the output of the filter is within specification at 82 mV. The slew rate settings are SR clock = 3 and SR step = 2, setting the transition time from 4 mA to 20 mA at approximately 120 ms. C1 is 4.7 nF and C2 is unconnected. If this rate of change is too slow, the slew time can be reduced. With this circuit configuration of C1 = 4.7 nF and C2 unconnected, it was found that setting up an 80 ms slew time (SR clock = 1, SR step = 2) gave an analog rate of change result inside the HART specification. However, reducing the slew time further, to 60 ms (SR clock = 0, SR step = 2), pushed the result just outside of the 150 mV specification. The capacitor connected from CAP1 to AV_{DD} can be used to counteract the effect of the increased peak voltage at the output of the filter due to faster slew times. However, care must be taken when choosing this value because it has an effect on the low-pass filter frequency cutoff discussed in the Determining the Values of the External Components section.

Figure 10 shows the results of changing the slew rate control settings to SR clock = 5 and SR step = 2, while leaving the C1 capacitor value unchanged at 4.7 nF. This results in a transition time of approximately 240 ms. The peak amplitude at the output of the filter can be reduced further by increasing the value of C1, configuring a slower slew rate, or a combination of both.

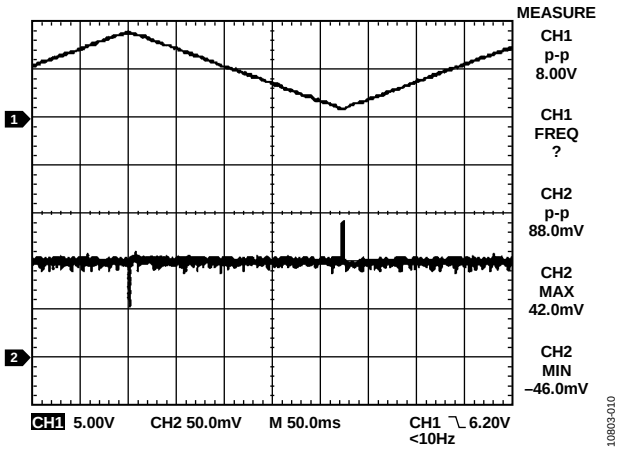

Figure 10. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 5, SR Step = 2, C1 = 4.7 nF, C2 = NC

Transient Voltage Protection

The AD5422 contains ESD protection diodes that prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. To protect the AD5422 from excessively high voltage transients, external power diodes and a surge current limiting resistor may be required, as shown in Figure 1. The constraint on the resistor value, shown in Figure 1 as 18 Ω, is that during normal operation the output level at I_{OUT} must remain within its voltage compliance limit of AV_{DD} – 2.5 V, and the two protection diodes and resistor must have the appropriate power ratings. With 18 Ω, for a 4 mA to 20 mA output, the compliance limit at the terminal is decreased by $V = I_{MAX} \times R = 0.36$ V. There is also a 10 kΩ resistor shown at the positive input of the OP184 buffer. This protects the amplifier by limiting the current during a transient event. Further protection can be provided with transient voltage suppressors (TVS) or transorbs. These are available as both unidirectional and bidirectional suppressors, and in a wide range of standoff and breakdown voltage ratings. Size the TVS with the lowest breakdown voltage possible while not conducting in the functional range of the current output. It is recommended that all remotely connected nodes be protected.

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur.

The *i*Coupler family of products from Analog Devices, Inc., provides voltage isolation in excess of 2.5 kV. Further information on *i*Coupler products is available at www.analog.com/icouplers. To reduce the number of isolators required, nonessential signals, such as CLEAR, can be connected to GND; $\overline{\text{FAULT}}$ and SDO can be left unconnected, reducing the isolation requirements to only three signals. However, note that either $\overline{\text{FAULT}}$ or SDO are required to provide access to the fault detection features of the AD5422.

COMMON VARIATIONS

A common variation on the circuit shown in Figure 1 is to use the AD5420, which is similar to the AD5422, but contains only a current output. It therefore does not contain the OP184 buffer configuration at the output. This AD5420 and AD5700 HART modem circuit is described in more detail in CN-0270. Circuit Note CN-0065 provides extra information on an IEC 61000-compliant solution for a fully isolated output module using the AD5422 and the ADuM1401 digital isolator. Circuit Note CN-0233 contains information on providing power and data isolation using the ADuM3471 PWM controller and transformer driver with quad-channel isolators.

If multiple channels are required, the AD5755-1 quad voltage and current output DAC may be used. This product has innovative on-chip dynamic power control that minimizes package power dissipation in current mode. Each channel has a corresponding CHARTx pin so that HART signals can be coupled to the current output of the AD5755-1.

The AD5421 and the AD5700 HART modem can be combined if the requirement is a loop powered, 4 mA to 20 mA HART solution. Such a HART enabled smart transmitter reference demo circuit was developed by Analog Devices and uses the AD5421, the ADuCM360, and the AD5700 modem. This circuit has been compliance tested, verified, and registered as an approved HART solution by the HART Communication Foundation.

CIRCUIT EVALUATION AND TEST

To build this circuit, it requires the use of the AD5422 evaluation board (EVAL-AD5422EBZ, LFCSP version) and the AD5700-1 evaluation board (EVAL-AD5700-1EBZ), see Figure 11. As well as the two evaluation boards, the circuit also requires three external capacitors (C1, C_H, and C_L), a resistor (R_H), a load resistor (R_L), a buffer amplifier, and a UART interface.

Equipment Needed

The following equipment is needed:

- The AD5422 evaluation board (EVAL-AD5422EBZ, LFCSP version)
- The AD5700 evaluation board (EVAL-AD5700-1EBZ)
- A PC running Windows® XP with USB port
- A host controller and an UART interface (standard microcontroller, for example, ADuC7060).
- A power supply, 10.8 V to 60 V
- A digital test filter (HCF_TOOL-31 available from the HART Communication Foundation)
- A load resistor, 500 Ω
- The OP184 amplifier (on separate breadboard with connecting wires)
- External capacitors, C1 (4.7 nF), C_H (8.2 nF), and C_L (4.7 nF); and a resistor, R_H (27 kΩ)
- An oscilloscope, Tektronix DS1012B or equivalent

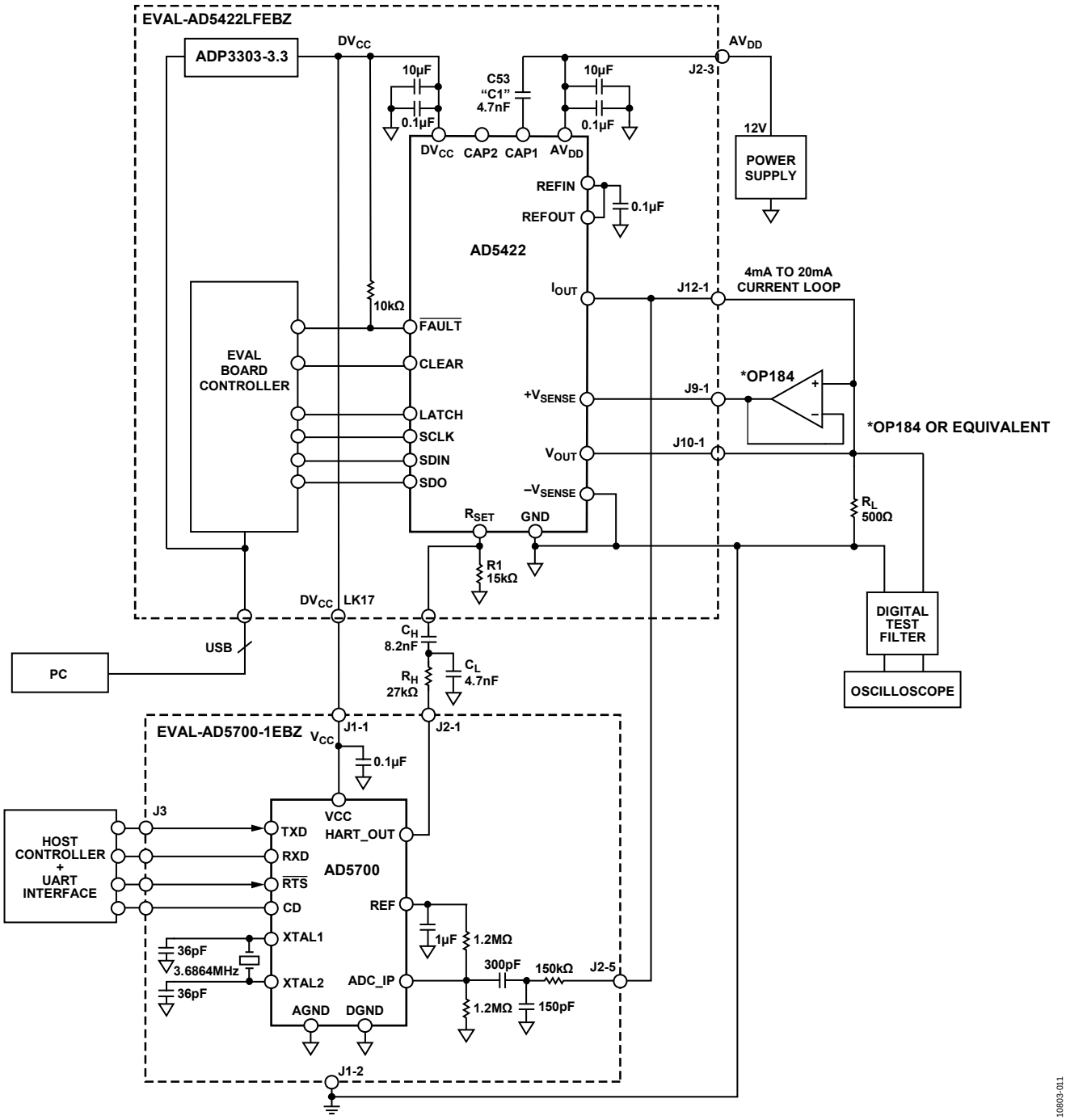

Figure 11. Test Setup Block Diagram

Noise During Silence Measurements—AD5422 LFCSP

As described previously, for the output noise during silence tests, the AD5700 modem was not transmitting (silent). The AD5422 was set to output the required current and passed through the HART Communication Foundation band-pass filter. The output noise was then measured using a Tektronix TDS1012B oscilloscope and found to be within the HART Communication Foundation protocol specifications.

Analog Rate of Change Measurements—AD5422 LFCSP

The analog rate of change specification ensures that when the AD5422 regulates current, the maximum rate of change of analog current does not interfere with HART communications. Step changes in current disrupt HART signaling. For this test, the AD5422 was programmed to output a cyclic waveform switching from 4 mA to 20 mA with no delay at either value to ensure the maximum rate of change. The slew rate settings used were SR clock = 3 and SR step = 2, with C1 set to 4.7 nF and C2 open circuit.

Measurements were also completed whereby the slew rate was reduced even further by changing the SR clock setting to 5 rather than 3, and leaving all other settings and component values unchanged, the effects of which can be seen if Figure 9 and Figure 10 are compared.

Noise During Silence Measurements—AD5422 TSSOP

Extra measurements were also taken in an effort to simulate the behavior of the AD5422 TSSOP package option in this configuration; however, without the capacitor on the CAP1 pin (C1) present (because the TSSOP version of this part does not contain a CAP1 pin).

While the results for output noise during silence tests were greater without C1 in place, than in the case of the LFCSP part with C1 in place, they were still within the HART Communication Foundation protocol specifications. Channel 2 in Figure 12 and Figure 13 shows the broadband noise results with the HCF_TOOL-31 filter in place, 530 µV rms for 4 mA I_{OUT} and 690 µV rms for 12 mA I_{OUT}. These plots can be compared with Figure 7 and Figure 8 to show the effect of the presence of C1.

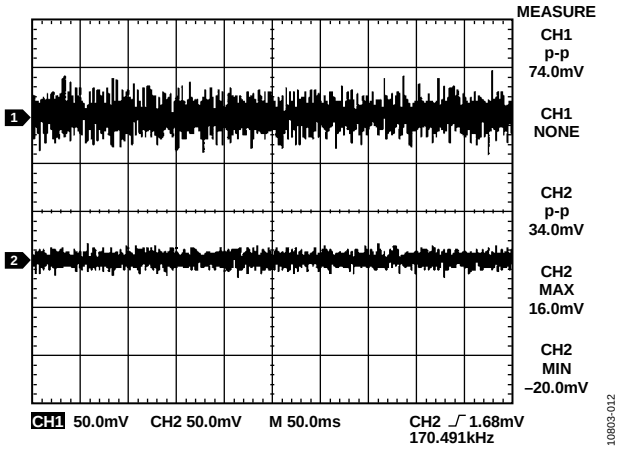

Figure 12. Noise at Input (CH1) and Output (CH2) of HART Filter with 4 mA Output Current, C1 Not in Place

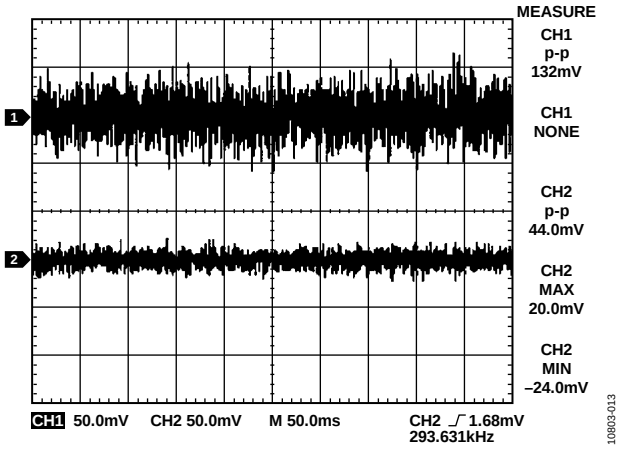

Figure 13. Noise at Input (CH1) and Output (CH2) of HART Filter with 12 mA Output Current, C1 Not in Place

Analog Rate of Change Measurements—AD5422 TSSOP

In terms of the analog rate of change test, the maximum peak result with and without C1 in place were similar. The main difference seen between the results was that without C1, the peak to peak noise floor was much larger. Figure 14 and Figure 15 show the analog rate of change plots for a slew rate of 120 ms (SR clock = 3 and SR step = 2) and 240 ms (SR clock = 5 and SR step = 2), respectively.

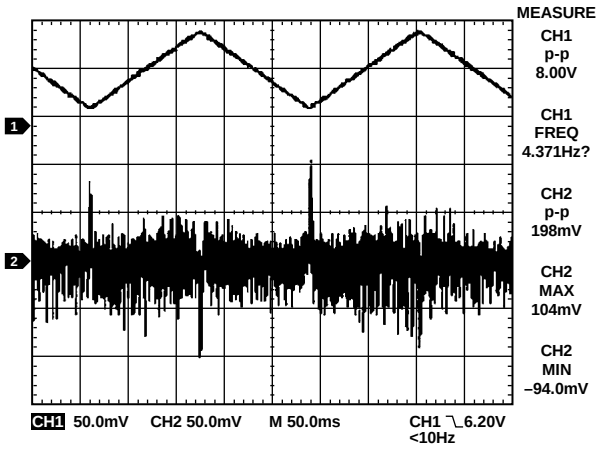

Figure 14. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 3, SR Step = 2, C1 = NC, C2 = NC

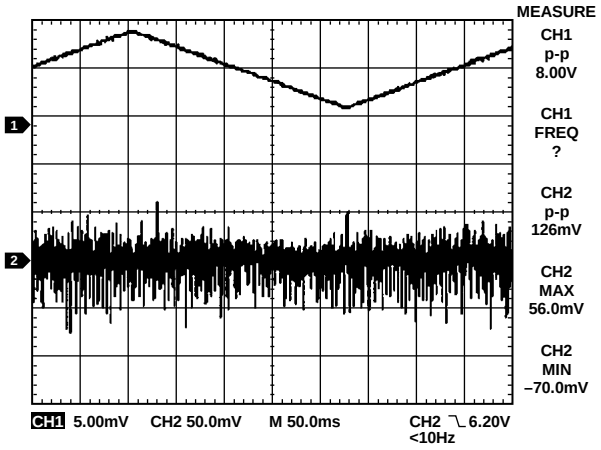

Figure 15. AD5422 Output (CH1) and HART Filter Output (CH2), SR Clock = 5, SR Step = 2, C1 = NC, C2 = NC

Again, these plots can be compared with Figure 9 and Figure 10 to show the effect of the presence of C1. While the HART-coupling technique used in this circuit configuration requires the use of the external R_{SET} resistor, note that even if the HART portion of this circuit is not implemented, the addition of the buffer causes a marginal degradation on I_{OUT} accuracy when the internal R_{SET} resistor is used. It is, therefore, recommended to use the external R_{SET} resistor when using this buffer configuration to tie the voltage and current output pins together.

LEARN MORE

CN0278 Design Support Package:
http://www.analog.com/CN0278-DesignSupport

CN-0270, *Complete 4 mA to 20 mA HART Solution*

Maurice Egan, *Configuring the AD5420 for HART Communication Compliance*, Application Note AN-1065, Analog Devices.

HART® Communication Foundation

Data Sheets and Evaluation Boards

AD5422 Data Sheet and Evaluation Boards (TSSOP and LFCSP available)

AD5700 Data Sheet and Evaluation Board

AD5700-1 Data Sheet and Evaluation Board

REVISION HISTORY

5/14—Rev. 0 to Rev. A

6/12—Revision 0: Initial Version