Reinforced, Ultra-Low-Power, 4-Channel Digital Isolators

MAX22440/MAX22441/MAX22442
MAX22840/MAX22841/MAX22842
MAX22880/MAX22881/MAX22882

Product Highlights

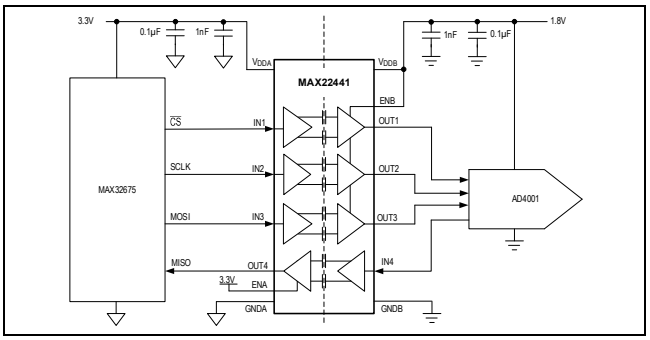
- Ultra-Low Power Consumption
  - 9.6µA per Channel at DC with V_{DD} = 3.3V
  - 13.2µA per Channel at 100kbps with V_{DD} = 3.3V
  - 47.6µA per Channel at 1Mbps with V_{DD} = 3.3V
- Wide Operating Voltage Range from 1.71V to 5.5V
- Reinforced Galvanic Isolation of Digital Signals
  - Withstands ±10kV Surge between GNDA and GNDB with 1.2µs/50µs Waveform
  - High CMTI (200kV/µs, min)
  - MAX22440-MAX22442 in 16 QSOP Package:
    - $3000V_{RMS}$ Isolation Voltage for 60s (V_{ISO})
    - $445V_{RMS}$ Continuous Working Voltage (V_{IOWM})
  - MAX22840-MAX22842 in 16 Wide SOIC Package:
    - $5000V_{RMS}$ Isolation Voltage for 60s (V_{ISO})
    - $848V_{RMS}$ Continuous Working Voltage (V_{IOWM})
  - MAX22880-MAX22882 in 20 SSOP Package:
    - $3750V_{RMS}$ Isolation Voltage for 60s (V_{ISO})
    - $784V_{RMS}$ Continuous Working Voltage (V_{IOWM})
- *Safety Regulatory Approvals*
  - UL According to UL1557 (Pending)
  - VDE 0884-11 Reinforced Insulation (Pending)
  - CSA IEC 62368-1, and IEC 61010-1 (Pending)
- Low Propagation Delay and Low Jitter
  - Maximum Data Rate Up to 10Mbps
  - Propagation Delay of 43.8ns (typ) at V_{DD} = 3.3V
  - Clock Jitter RMS of 35.0ps (typ)

Key Applications

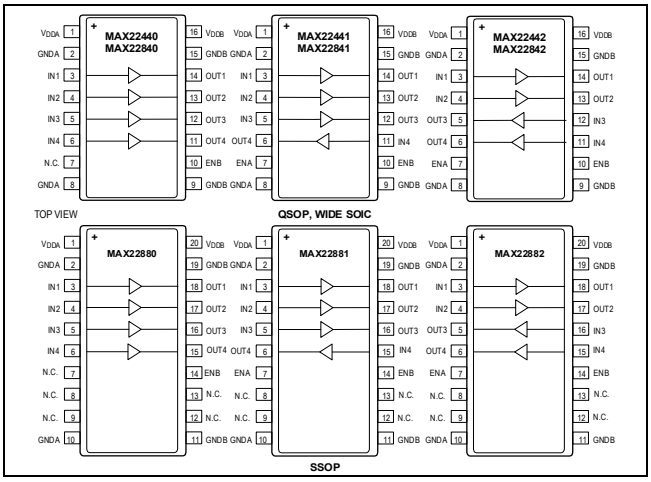
- 4-20mA Loop Process Control
- Compact Micro PLC
- Battery Management
- Parasitically Powered Applications

The MAX22440-MAX22442, MAX22840-MAX22842, and MAX22880-MAX22882 are a family of 4-channel, reinforced, ultra-low-power digital galvanic isolators using Analog Devices proprietary process technology. The MAX22440-MAX22442 are in a 16-QSOP package with a withstand voltage rating of $3kV_{RMS}$ for 60 seconds, the MAX22840-MAX22842 are in a 16 wide SOIC package with a withstand voltage rating of $5kV_{RMS}$ for 60 seconds, and the MAX22880-MAX22882 are in a 20-SSOP package with a withstand voltage rating of $3.75kV_{RMS}$ for 60 seconds. Devices are rated for operation at ambient temperatures from -40°C to +125°C.

Simplified Application Diagram



Pin Description



The devices transfer digital signals between circuits with different power domains, using as little as 77.04µW per channel at 1Mbps (1.8V supply). The ultra-low-power feature reduces system dissipation, increases reliability, and enables compact designs. Devices are available with a maximum data rate of 10Mbps and with default-high or default-low outputs. The devices feature low propagation delay and low clock jitter, which reduces system latency. Independent 1.71V to 5.5V supplies on each side also make the devices suitable for use as level translators. All four channels of the MAX22440/840/880 transfer data in the same direction. Three out of four channels of the MAX22441/841/881 transfer data in one direction while the other one transfers data in the opposite direction. Two channels of the MAX22442/842/882 transfer data in one direction and the other two in the opposite direction.

Ordering Information ***appears at end of data sheet.***

19-101556; Rev 5; 1/24

Absolute Maximum Ratings

V_{DDA} to GNDA ..... -0.3V to +6V

V_{DDB} to GNDB ..... -0.3V to +6V

ENA, IN_ on Side A to GNDA ..... -0.3V to +6V

ENB, IN_ on Side B to GNDB ..... -0.3V to +6V

OUT_ on Side A to GNDA ..... -0.3V to (V_{DDA} + 0.3)V

OUT_ on Side B to GNDB ..... -0.3V to (V_{DDB} + 0.3)V

Short-Circuit Continuous Current

OUT_ On Side A to GNDA ..... ±30mA

OUT_ On Side B to GNDB ..... ±30mA

Continuous Power Dissipation (T_A = +70°C)

QSOP (derate 9.60mW/°C above +70°C) 771.50mW

Wide SOIC (derate 14.1mW/°C above +70°C).... 1126.8mW

SSOP (derate 10.60mW/°C above +70°C)..... 848.36mW

Temperature Ratings

Operating Temperature Range ..... -40°C to +125°C

Maximum Junction Temperature ..... +150°C

Storage Temperature Range..... -60°C to +150°C

Lead Temperature (soldering, 10s) ..... +300°C

Soldering Temperature (reflow)..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 QSOP

Package Code	E16MS+1F
Outline Number	21-0055
Land Pattern Number	90-0167
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	103.70°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	37°C/W

16 Wide SOIC

Package Code	W16MS+12A
Outline Number	21-0042
Land Pattern Number	90-0107
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	71°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	24°C/W

20 SSOP

Package Code	A20MS+7
Outline Number	21-0056
Land Pattern Number	90-0094
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	94.30°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	43.70°C/W

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (*Note 1*, *Note 3*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER							
Supply Voltage	V_{DDA}	Relative to GNDA		1.71		5.5	V
	V_{DDB}	Relative to GNDB		1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO\_}$	$V_{DD\_}$ rising		1.5	1.6	1.69	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}				30		mV
MAX22440/MAX22840/MAX22880 SUPPLY CURRENT (*NOTE 2*)							
Supply Current Side A	I_{DDA}	DC, C_L = 0pF	V_{DDA} = 5V		6.9	18.8	µA
			V_{DDA} = 3.3V		6.7	18.2	
			V_{DDA} = 2.5V		6.7	18.0	
			V_{DDA} = 1.8V		6.5	17.5	
		5kHz square wave, C_L = 0pF	V_{DDA} = 5V		6.9	18.8	
			V_{DDA} = 3.3V		6.7	18.2	
			V_{DDA} = 2.5V		6.7	18.0	
			V_{DDA} = 1.8V		6.5	17.5	
		50kHz square wave, C_L = 0pF	V_{DDA} = 5V		15.7	28.4	
			V_{DDA} = 3.3V		15.5	27.6	
			V_{DDA} = 2.5V		15.2	27.2	
			V_{DDA} = 1.8V		14.9	26.3	
		500kHz square wave, C_L = 0pF	V_{DDA} = 5V		102.3	124.2	
			V_{DDA} = 3.3V		100.3	122.2	
			V_{DDA} = 2.5V		100.8	121.2	
			V_{DDA} = 1.8V		95.4	113.9	
Supply Current Side B	I_{DDB}	DC, C_L = 0pF	V_{DDB} = 5V		31.8	45.1	µA
			V_{DDB} = 3.3V		31.7	44.3	
			V_{DDB} = 2.5V		31.6	44.1	
			V_{DDB} = 1.8V		31.4	43.4	
		5kHz square wave, C_L = 0pF	V_{DDB} = 5V		31.8	45.1	
			V_{DDB} = 3.3V		31.7	44.3	
			V_{DDB} = 2.5V		31.6	44.1	
			V_{DDB} = 1.8V		31.4	43.4	
		50kHz square wave, C_L = 0pF	V_{DDB} = 5V		38.6	52.2	
			V_{DDB} = 3.3V		37.2	50.2	
			V_{DDB} = 2.5V		36.4	49.1	
			V_{DDB} = 1.8V		35.6	47.7	
		500kHz square wave, C_L = 0pF	V_{DDB} = 5V		104.1	121.2	
			V_{DDB} = 3.3V		89.9	106.6	
			V_{DDB} = 2.5V		84.7	99.9	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (*Note 1*, *Note 3*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{DDB} = 1.8V		75.8	89.9	
MAX22441/MAX22841/MAX22881 SUPPLY CURRENT (*NOTE 2*)							
Supply Current Side A	I_{DDA}	DC, C_L = 0pF	V_{DDA} = 5V		13.1	25.4	µA
			V_{DDA} = 3.3V		13.0	24.7	
			V_{DDA} = 2.5V		12.9	24.5	
			V_{DDA} = 1.8V		12.7	24.0	
		5kHz square wave, C_L = 0pF	V_{DDA} = 5V		13.1	25.4	
			V_{DDA} = 3.3V		13.0	24.7	
			V_{DDA} = 2.5V		12.9	24.5	
			V_{DDA} = 1.8V		12.7	24.0	
		50kHz square wave, C_L = 0pF	V_{DDA} = 5V		21.3	34.2	
			V_{DDA} = 3.3V		20.8	33.1	
			V_{DDA} = 2.5V		20.4	32.6	
			V_{DDA} = 1.8V		20.0	31.6	
		500kHz square wave, C_L = 0pF	V_{DDA} = 5V		101.8	122.1	
			V_{DDA} = 3.3V		97.1	117.3	
			V_{DDA} = 2.5V		96.0	115.2	
			V_{DDA} = 1.8V		90.1	107.4	
Supply Current Side B	I_{DDB}	DC, C_L = 0pF	V_{DDB} = 5V		25.6	38.5	µA
			V_{DDB} = 3.3V		25.4	37.8	
			V_{DDB} = 2.5V		25.4	37.6	
			V_{DDB} = 1.8V		25.1	36.9	
		5kHz square wave, C_L = 0pF	V_{DDB} = 5V		25.6	38.5	
			V_{DDB} = 3.3V		25.4	37.8	
			V_{DDB} = 2.5V		25.4	37.6	
			V_{DDB} = 1.8V		25.1	36.9	
		50kHz square wave, C_L = 0pF	V_{DDB} = 5V		32.8	46.2	
			V_{DDB} = 3.3V		31.7	44.4	
			V_{DDB} = 2.5V		31.0	43.6	
			V_{DDB} = 1.8V		30.4	42.3	
		500kHz square wave, C_L = 0pF	V_{DDB} = 5V		103.1	121.2	
			V_{DDB} = 3.3V		92.0	110.0	
			V_{DDB} = 2.5V		87.8	104.9	
			V_{DDB} = 1.8V		80.5	95.7	
MAX22442/MAX22842/MAX22882 SUPPLY CURRENT (*NOTE 2*)							
Supply Current Side A	I_{DDA}	DC, C_L = 0pF	V_{DDA} = 5V		19.3	31.9	µA
			V_{DDA} = 3.3V		19.2	31.3	
			V_{DDA} = 2.5V		19.1	31.1	
			V_{DDA} = 1.8V		18.9	30.4	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1, Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		5kHz square wave, C_L = 0pF	V_{DDA} = 5V		19.3	31.9	
			V_{DDA} = 3.3V		19.2	31.3	
			V_{DDA} = 2.5V		19.1	31.1	
			V_{DDA} = 1.8V		18.9	30.4	
		50kHz square wave, C_L = 0pF	V_{DDA} = 5V		26.9	40.0	
			V_{DDA} = 3.3V		26.2	38.6	
			V_{DDA} = 2.5V		25.7	37.9	
			V_{DDA} = 1.8V		25.1	36.8	
		500kHz square wave, C_L = 0pF	V_{DDA} = 5V		100.4	120.1	
			V_{DDA} = 3.3V		93.6	112.4	
			V_{DDA} = 2.5V		91.8	109.2	
			V_{DDA} = 1.8V		84.7	100.9	
Supply Current Side B	I_{DDB}	DC, C_L = 0pF	V_{DDB} = 5V		19.3	31.9	µA
			V_{DDB} = 3.3V		19.2	31.3	
			V_{DDB} = 2.5V		19.1	31.1	
			V_{DDB} = 1.8V		18.9	30.4	
		5kHz square wave, C_L = 0pF	V_{DDB} = 5V		19.3	31.9	
			V_{DDB} = 3.3V		19.2	31.3	
			V_{DDB} = 2.5V		19.1	31.1	
			V_{DDB} = 1.8V		18.9	30.4	
		50kHz square wave, C_L = 0pF	V_{DDB} = 5V		26.9	40.0	
			V_{DDB} = 3.3V		26.2	38.6	
			V_{DDB} = 2.5V		25.7	37.9	
			V_{DDB} = 1.8V		25.1	36.8	
		500kHz square wave, C_L = 0pF	V_{DDB} = 5V		100.4	120.1	
			V_{DDB} = 3.3V		93.6	112.4	
			V_{DDB} = 2.5V		91.8	109.2	
			V_{DDB} = 1.8V		84.7	100.9	
LOGIC INTERFACE (IN_, OUT_, EN_)							
Input High Voltage	V_{IH}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V		0.7 x $V_{DD\_}$			V
		1.71V ≤ $V_{DD\_}$ < 2.25V		0.75 x $V_{DD\_}$			
Input Low Voltage	V_{IL}	2.25V ≤ $V_{DD\_}$ ≤ 5.5V				0.8	V
		1.71V ≤ $V_{DD\_}$ < 2.25V				0.7	
Input Hysteresis	V_{HYS}				410		mV
Input Leakage	I_{LKG}			-1		+1	µA
Input Capacitance	C_{IN}	f_{SW} = 1MHz			2		pF
Output Voltage High	V_{OH}	I_{OUT} = -4mA source	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	$V_{DD\_}$ - 0.4			V
		I_{OUT} = -2mA source	3.0V ≤ $V_{DD\_}$ ≤ 3.6V	$V_{DD\_}$ - 0.3			

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (*Note 1*, *Note 3*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		I_{OUT} = -1mA source	2.25V ≤ $V_{DD\_}$ ≤ 2.75V	$V_{DD\_}$ - 0.2			
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	$V_{DD\_}$ - 0.2			
Output Voltage Low	V_{OL}	I_{OUT} = 4mA sink	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			0.4	V
		I_{OUT} = 2mA sink	3.0V ≤ $V_{DD\_}$ ≤ 3.6V			0.3	
		I_{OUT} = 1mA sink	2.25V ≤ $V_{DD\_}$ ≤ 2.75V			0.2	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			0.2	

Dynamic Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2, Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Common-Mode Transient Immunity	CMTI	(Note 5)		200			kV/µs
Maximum Data Rate	DR_{MAX}			10			Mbps
Minimum Pulse Width	PW_{MIN}					100	ns
Glitch Rejection				14.4	25.0	45.0	ns
Propagation Delay (Figure 1)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	28.3	42.8	67.9	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	28.8	43.9	70.3	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	29.5	45.5	74.2	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	31.8	50.6	85.7	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V	28.4	42.8	67.8	
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V	28.8	43.8	70.1	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V	29.3	45.3	73.7	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V	31.5	49.9	84.8	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	1.71V ≤ $V_{DD\_}$ ≤ 5.5V			3	ns
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				45	ns
	t_{SPHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				45	
Propagation Delay Skew Channel-to-Channel (Same Direction) (Figure 1)	t_{SCSLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				10	ns
	t_{SCSHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				10	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				30	ns
	t_{SCOHL}	1.71V ≤ $V_{DD\_}$ ≤ 5.5V				30	
Peak Eye Diagram Jitter	$t_{JIT(PK)}$	1Mbps			650		ps
Rise Time (Figure 1)	t_R	C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			8	
Fall Time (Figure 1)	t_F	C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			5	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			5	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			5	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			8	
Enable to Data Valid (Figure 2)	t_{EN}	EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			20	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			20	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			20	

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 2, Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			25	
Enable to Tristate (Figure 2)	t_{TRI}	EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD\_}$ ≤ 5.5V			20	ns
			3.0V ≤ $V_{DD\_}$ ≤ 3.6V			20	
			2.25V ≤ $V_{DD\_}$ ≤ 2.75V			20	
			1.71V ≤ $V_{DD\_}$ ≤ 1.89V			25	
Time from UVLO to Output Data Valid (Figure 3)	t_{UVLO_EN}	C_L = 15pF, $V_{DD\_}$ rising			1.1	1.7	ms
Time from Input Power Loss to Output Default (Figure 3)	t_{UVLO_DE}	C_L = 15pF, $V_{DD\_}$ falling				0.4	ms
Refresh Rate	F_R				10		kHz
ESD PROTECTION							
ESD		HBM, All Pins			±4		kV
		IEC 61000-4-2 Contact, GNDB to GNDA	Wide SOIC		±6		
			QSOP		±5		

Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

Timing Diagrams

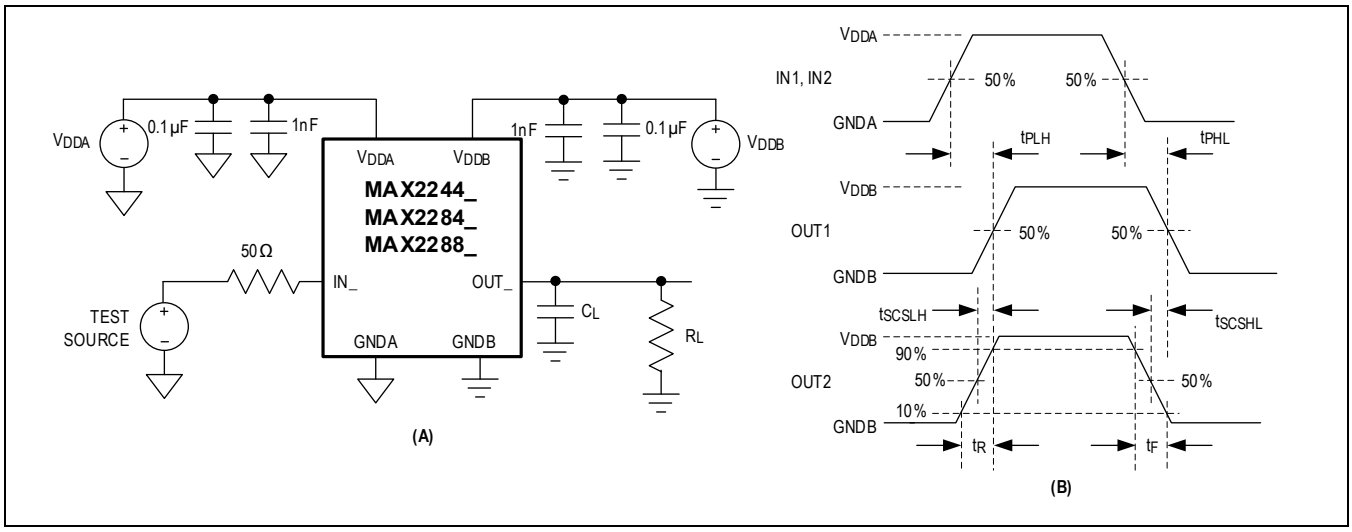


Figure 1. Test Circuit (A) and Timing Diagrams (B)

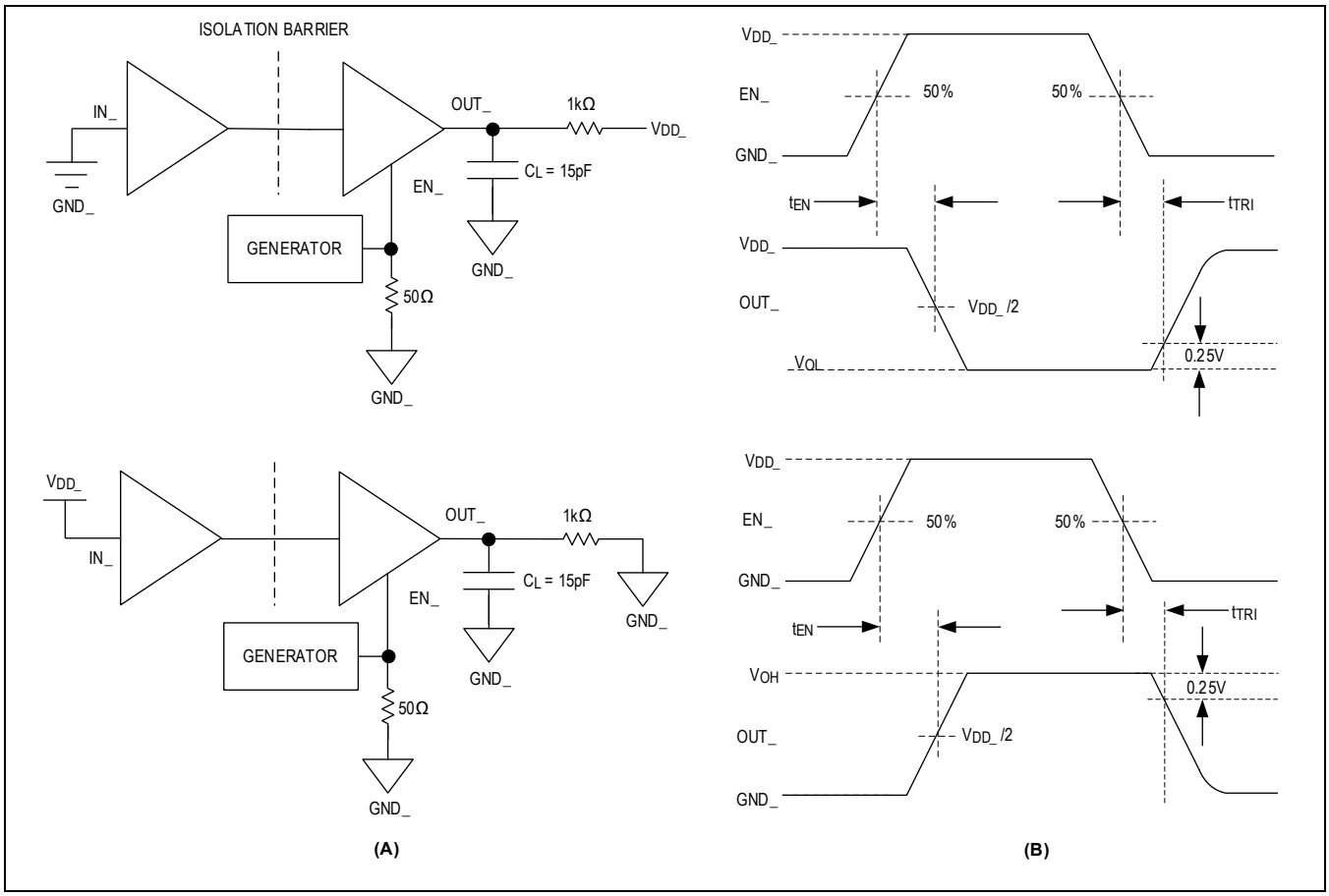


Figure 2. Enable to Output Timing Diagrams (t_{EN}, t_{TRI})

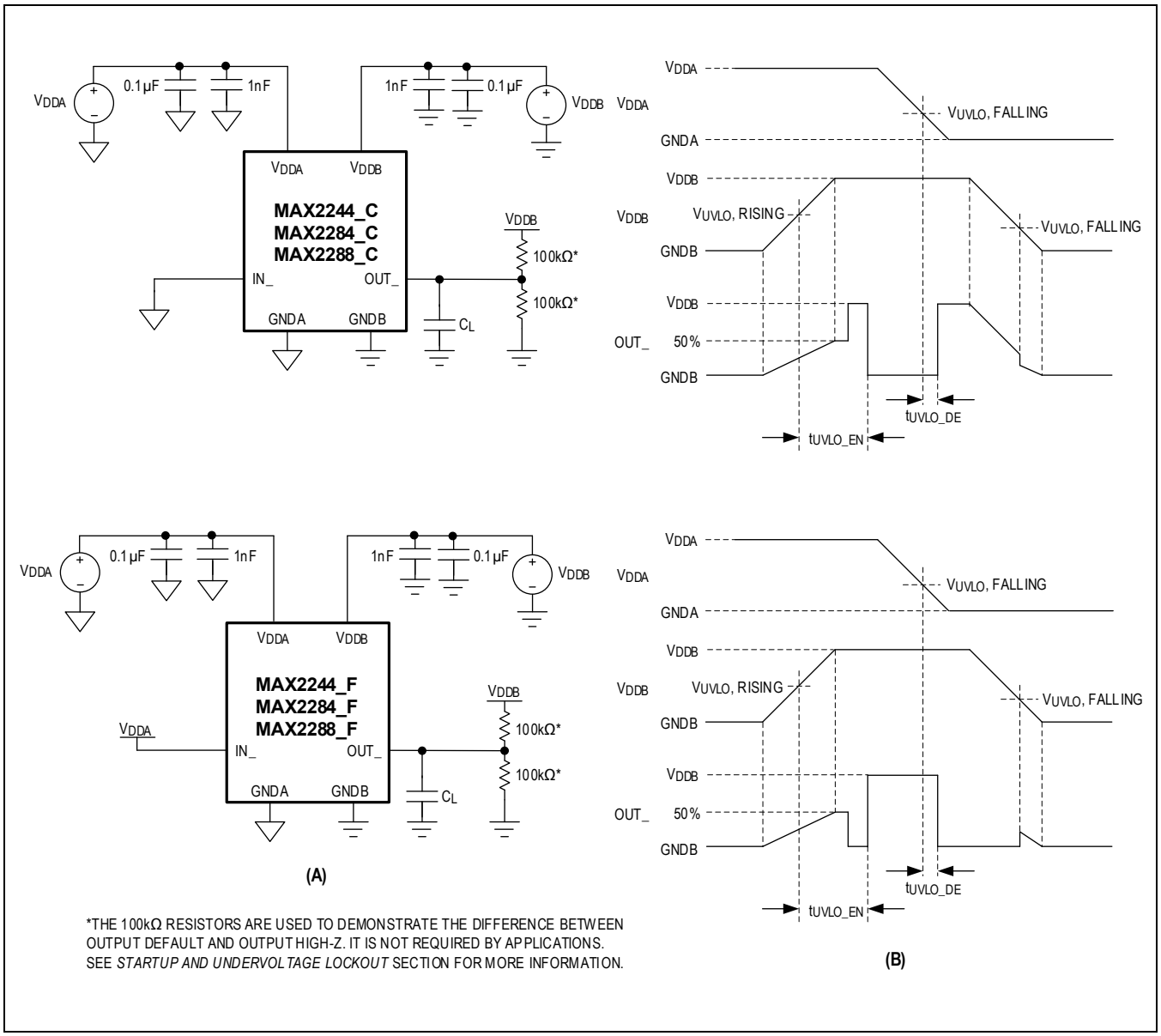


Figure 3. UVLO to Output Timing Diagrams (t_{UVLO_EN}, t_{UVLO_DE})

Table 1. Insulation Characteristics (16 QSOP)

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	1182	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(*Note 6*)	630	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 6*)	445	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 6*)	4242	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 6*, *Note 7*)	3000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 10000V_{PEAK} (*Note 6*, *Note 9*)	6250	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V, T_S = 150°C	$>10^{9}$	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (*Note 8*)	1.5	pF
Minimum Creepage Distance	CPG		3.5	mm
Minimum Clearance Distance	CLR		3.5	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	>400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Table 2. Insulation Characteristics (16 Wide SOIC)

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2250	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(*Note 6*)	1200	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 6*)	848	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 6*)	7070	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 6*, *Note 7*)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 12800V_{PEAK} (*Note 6*, *Note 9*)	8000	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V, T_S = 150°C	$>10^{9}$	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (*Note 8*)	1.5	pF
Minimum Creepage Distance	CPG		8	mm

Minimum Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group I (IEC 60112)	>600	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Table 3. Insulation Characteristics (20 SSOP)

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	2078	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(*Note 6*)	1108	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (*Note 6*)	784	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (*Note 6*)	5300	V_P
Maximum Withstanding Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (*Note 6*, *Note 7*)	3750	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 x V_{IOSM} = 10000V_{PEAK} (*Note 6*, *Note 9*)	6250	V_P
Isolation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	>10^{12}	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	>10^{11}	
		V_{IO} = 500V, T_S = 150°C	>10^9	
Barrier Capacitance Side A to Side B	C_{IO}	f_{SW} = 1MHz (*Note 8*)	1.5	pF
Minimum Creepage Distance	CPG		5.3	mm
Minimum Clearance Distance	CLR		5.3	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOTM}, V_{IOWM}, V_{IORM}, and V_{IOSM} are defined by the IEC 60747-5-5 standard.

Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.

Note 8: Capacitance is measured with all pins on field-side and logic-side tied together.

Note 9: Devices are immersed in oil during surge characterization.

Safety Regulatory Approvals (Pending)

The MAX22xxx family is approved by the organizations listed in Table 4, Table 5, and Table 6. Certifications are available at Safety and Regulatory Certifications for Digital Isolation. These couplers are suitable for safe electrical insulation only within the safety limits. Compliance with the safety limits is ensured by means of suitable protective circuits.

Table 4. MAX22440, MAX22441, MAX22442 (16 QSOP)

UL (Pending)
The devices are certified under UL1577. For more details, refer to file E351759.
The MAX22440 to MAX22442 are rated up to $3000V_{RMS}$ isolation voltage for single protection.
VDE (Pending)
The MAX22440 to MAX22442 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Repetitive Peak Isolation Voltage $630V_{PK}$, Maximum Surge Isolation Voltage $6250V_{PK}$, Maximum Transient Isolation Voltage $4242V_{PK}$, Maximum Working Isolation Voltage $445V_{RMS}$.
CSA (Pending)
CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 third edition; Basic Insulation at $350V_{RMS}$, Reinforced Insulation at $175V_{RMS}$.
CSA 61010-1-12+A1 and IEC 61010-1 third edition; Basic Insulation at $300V_{RMS}$, Reinforced Insulation at $150V_{RMS}$.

Table 5. MAX22840, MAX22841, MAX22842 (16 Wide SOIC)

UL (Pending)
The devices are certified under UL1577. For more details, refer to file E351759.
The MAX22840 to MAX22842 are rated up to $5000V_{RMS}$ isolation voltage for single protection.
VDE (Pending)
The MAX22840 to MAX22842 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Repetitive Peak Isolation Voltage $1200V_{PK}$, Maximum Surge Isolation Voltage $8000V_{PK}$, Maximum Transient Isolation Voltage $7070V_{PK}$, Maximum Working Isolation Voltage $848V_{RMS}$.
CSA (Pending)
CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 3rd edition; Basic Insulation at $800V_{RMS}$, Reinforced Insulation at $400V_{RMS}$.
CSA 61010-1-12+A1 and IEC 61010-1 third edition; Basic Insulation at $600V_{RMS}$, Reinforced Insulation at $300V_{RMS}$.

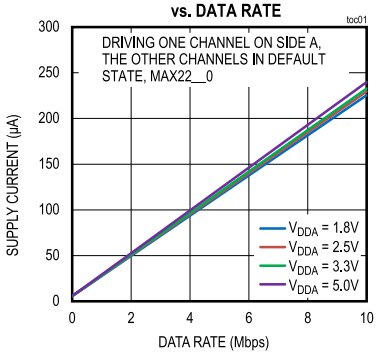
Table 6. MAX22880, MAX22881, MAX22882 (20 SSOP)

UL (Pending)
The devices are certified under UL1577. For more details, refer to file E351759.
The MAX22880-MAX22882 are rated up to $3750V_{RMS}$ isolation voltage for single protection.
VDE (Pending)
The MAX22880-MAX22882 are certified to DIN VDE V 0884-11: 2017-1. Reinforced Insulation, Maximum Repetitive Peak Isolation Voltage $1108V_{PK}$, Maximum Surge Isolation Voltage $6250V_{PK}$, Maximum Transient Isolation Voltage $5300V_{PK}$, Maximum Working Isolation Voltage $784V_{RMS}$.
CSA (Pending)
CSA 62368-1-19, EN 62368-1:2020 and IEC 62368-1:2018 3rd edition; Basic Insulation at $530V_{RMS}$, Reinforced Insulation at $265V_{RMS}$.
CSA 61010-1-12+A1 and IEC 61010-1 third edition; Basic Insulation at $300V_{RMS}$, Reinforced Insulation at $150V_{RMS}$.

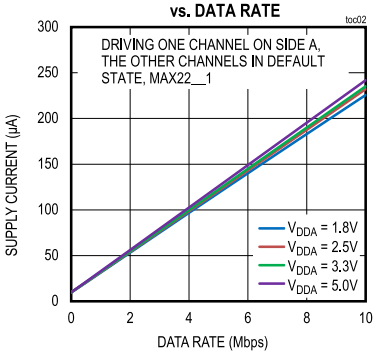
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

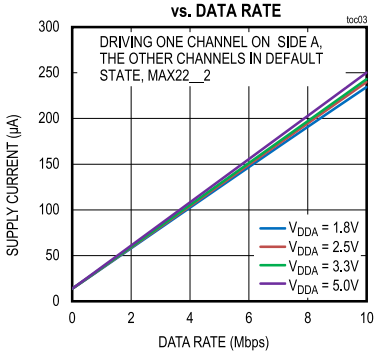
SIDE A SUPPLY CURRENT vs. DATA RATE



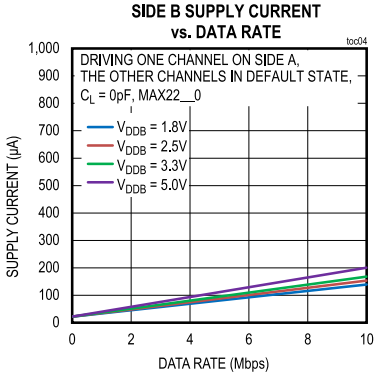
SIDE A SUPPLY CURRENT vs. DATA RATE



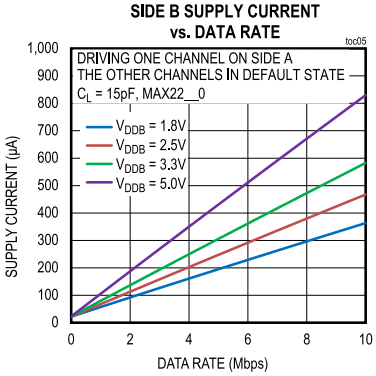
SIDE A SUPPLY CURRENT vs. DATA RATE



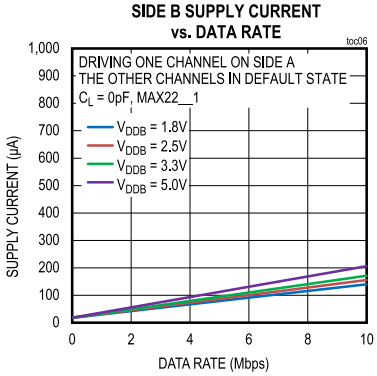
SIDE B SUPPLY CURRENT vs. DATA RATE



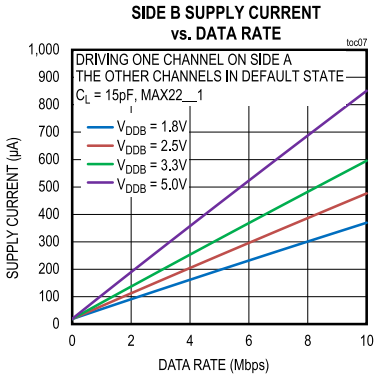
SIDE B SUPPLY CURRENT vs. DATA RATE



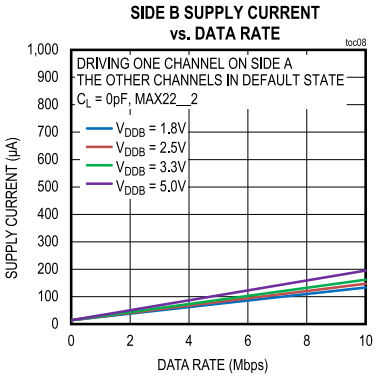
SIDE B SUPPLY CURRENT vs. DATA RATE



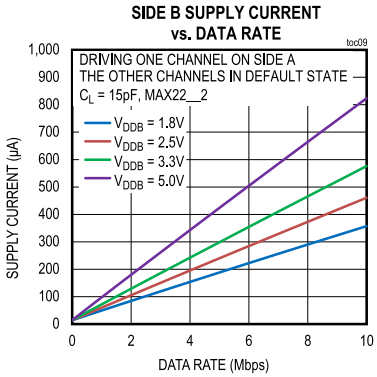
SIDE B SUPPLY CURRENT vs. DATA RATE



SIDE B SUPPLY CURRENT vs. DATA RATE

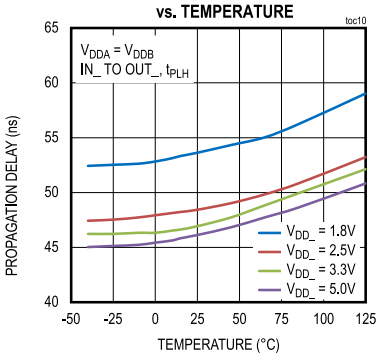


SIDE B SUPPLY CURRENT vs. DATA RATE

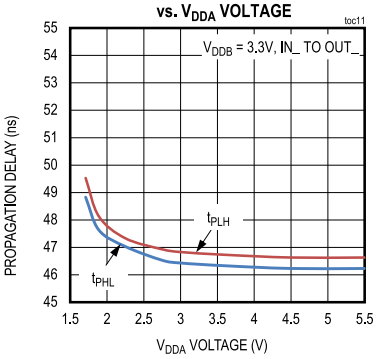


(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

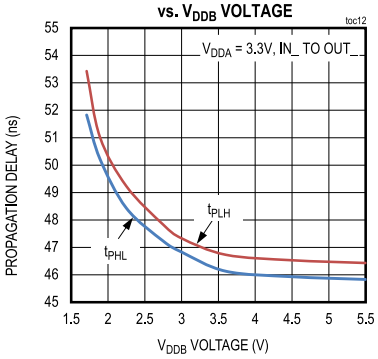
PROPAGATION DELAY vs. TEMPERATURE



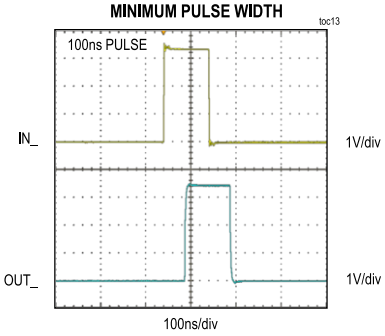
PROPAGATION DELAY vs. V_{DDA} VOLTAGE



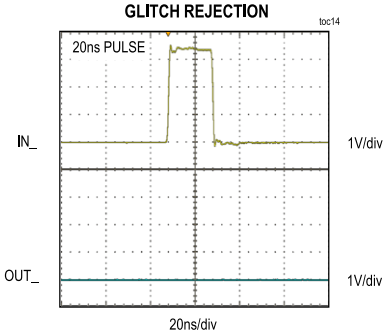
PROPAGATION DELAY vs. V_{DDB} VOLTAGE



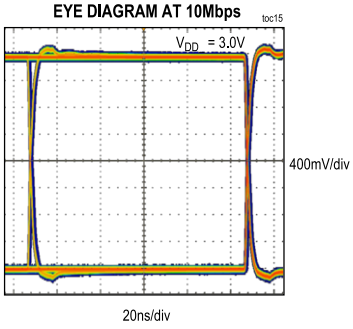
MINIMUM PULSE WIDTH



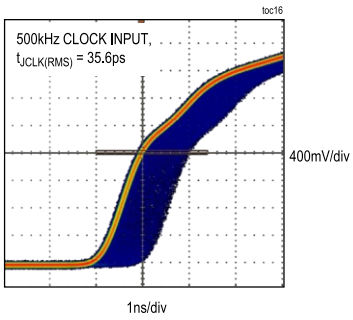
GLITCH REJECTION



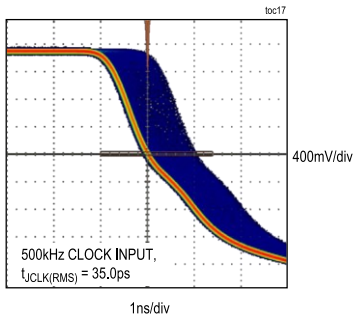
EYE DIAGRAM AT 10Mbps



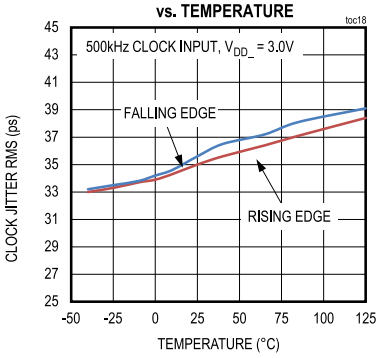
CLOCK JITTER RMS ON RISING EDGE



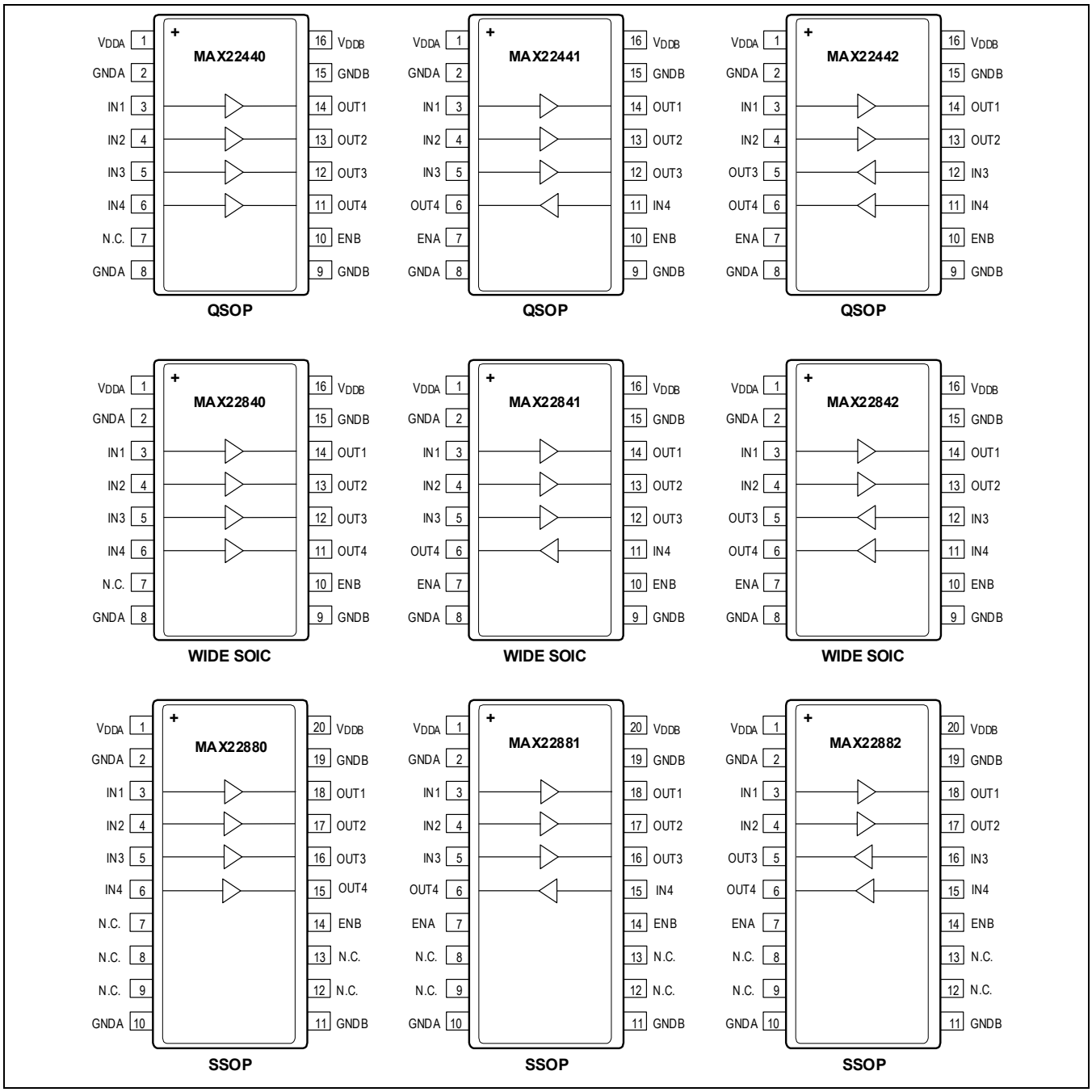
CLOCK JITTER RMS ON FALLING EDGE



CLOCK JITTER RMS vs. TEMPERATURE



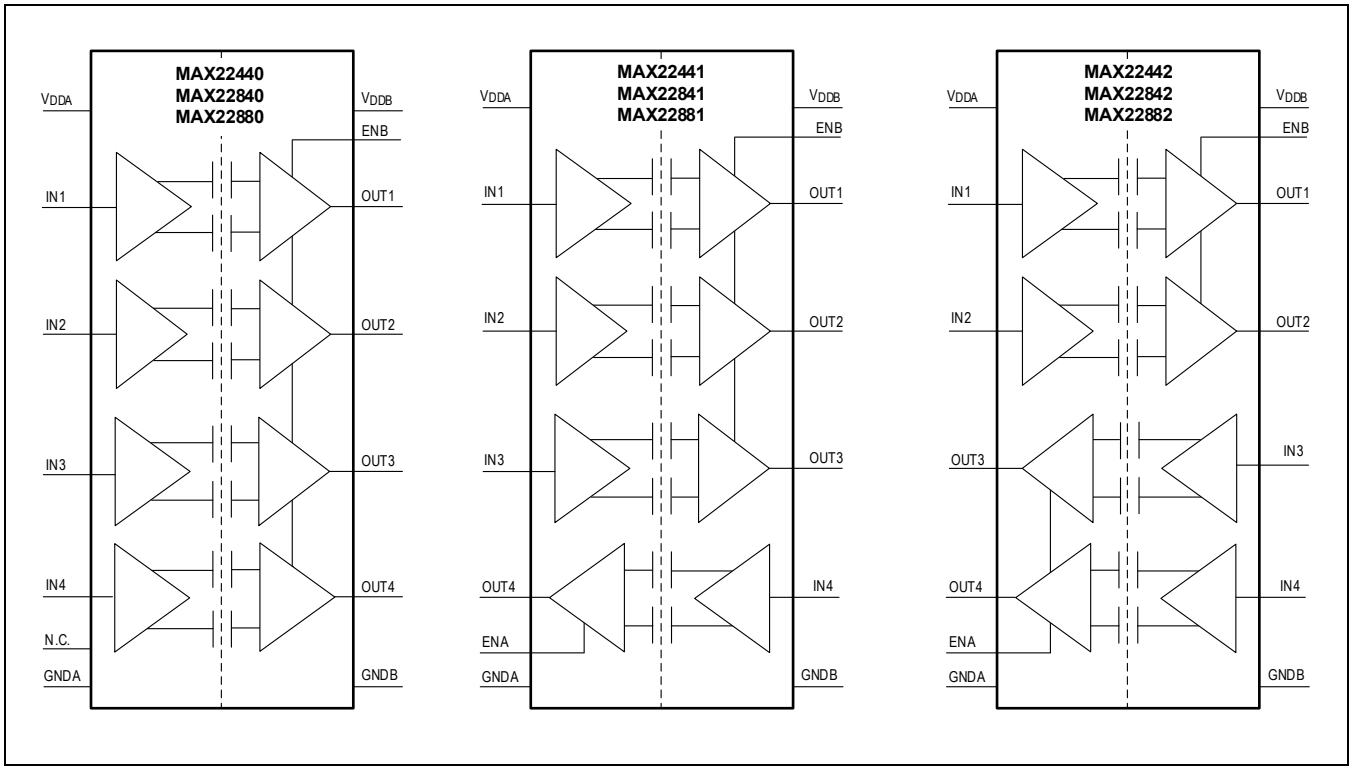
Pin Configurations



Pin Descriptions

PIN						NAME	FUNCTION
MAX22440 MAX22840	MAX22441 MAX22841	MAX22442 MAX22842	MAX22880	MAX22881	MAX22882		
1	1	1	1	1	1	V_{DDA}	Side A Power Supply. Bypass V_{DDA} to GNDA with a 1nF and a 0.1µF ceramic capacitor within 2mm to the pin.
2, 8	2, 8	2, 8	2, 10	2, 10	2, 10	GNDA	Ground Reference for Side A.
16	16	16	20	20	20	V_{DDB}	Side B power supply. Bypass V_{DDB} to GNDB with a 1nF and a 0.1µF ceramic capacitor within 2mm to the pin.
9, 15	9, 15	9, 15	11, 19	11, 19	11, 19	GNDB	Ground Reference for Side B.
3	3	3	3	3	3	IN1	Logic Input 1 on Side A, corresponds to Logic Output 1 on Side B. Tie to high or low when not used.
4	4	4	4	4	4	IN2	Logic Input 2 on Side A, corresponds to Logic Output 2 on Side B. Tie to high or low when not used.
5	5	—	5	5	—	IN3	Logic Input 3 on Side A, corresponds to Logic Output 3 on Side B. Tie to high or low when not used.
—	—	12	—	—	16		Logic Input 3 on Side B, corresponds to Logic Output 3 on Side A. Tie to high or low when not used.
6	—	—	6	—	—	IN4	Logic Input 4 on Side A, corresponds to Logic Output 4 on Side B. Tie to high or low when not used.
—	11	11	—	15	15		Logic Input 4 on Side B, corresponds to Logic Output 4 on Side A. Tie to high or low when not used.
14	14	14	18	18	18	OUT1	Logic Output 1 on Side B, corresponds to Logic Input 1 on Side A.
13	13	13	17	17	17	OUT2	Logic Output 2 on Side B, corresponds to Logic Input 2 on Side A.
12	12	—	16	16	—	OUT3	Logic Output 3 on Side B, corresponds to Logic Input 3 on Side A.
—	—	5	—	—	5		Logic Output 3 on Side A, corresponds to Logic Input 3 on Side B.
11	—	—	15	—	—	OUT4	Logic Output 4 on Side B, corresponds to Logic Input 4 on Side A.
—	6	6	—	6	6		Logic Output 4 on Side A, corresponds to Logic Input 4 on Side B.
—	7	7	—	7	7	ENA	Active-High Enable for Side A. Tie to high when not used.
10	10	10	14	14	14	ENB	Active-High Enable for Side B. Tie to high when not used.
7	—	—	7, 8, 9, 12, 13	8, 9, 12, 13	8, 9, 12, 13	N.C.	Not Connected.

Functional Diagrams



Detailed Description

The MAX22440-MAX22442, MAX22840-MAX22842, and MAX22880-MAX22882 are a family of 4-channel, reinforced, ultra-low-power digital isolators. The devices consume ultra-low power not only in DC but also across the entire operating speed range up to 10Mbps.

The MAX22440/840/880 transfer digital signals between two circuits with different power domain in one direction, which is convenient for applications such as digital I/O. The MAX22441/841/881 transfer three digital signals in one direction and one in the opposite direction, which is necessary for applications such as SPI. The MAX22442/842/882 transfer two digital signals in one direction and two in the opposite direction.

The MAX22440-MAX22442 are available in a 16-pin QSOP package with 4mm creepage and clearance, and are rated up to $3kV_{RMS}$. The MAX22840-MAX22842 are in available in a 16-pin wide SOIC package with 8mm creepage and clearance, and are rate up to $5kV_{RMS}$. The MAX22880-MAX22882 are available in a 20-pin SSOP package with 5.5mm creepage and clearance, and are rated up to $3.75kV_{RMS}$. The family of devices offers ultra-low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Analog Devices proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

The family of devices has a maximum data rate of 10Mbps and can be ordered with default-high or default-low outputs. The default is the state the output assumes when the input is open circuit. The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The family of devices also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The family of devices provides galvanic isolation for digital signals that are transmitted between two ground domains. The MAX22440-MAX22442 are in a 16-pin QSOP package and withstand differences up to $3kV_{RMS}$ for up to 60 seconds, and up to $445V_{RMS}$ of continuous isolation. MAX22840-MAX22842 are in a 16-pin wide SOIC package and withstand differences up to $5kV_{RMS}$ for up to 60 seconds, and up to $848V_{RMS}$ of continuous isolation. The MAX22880-MAX22882 are in a 20-pin SSOP package and withstand differences up to $3.75kV_{RMS}$ for up to 60 seconds, and up to $784V_{RMS}$ of continuous isolation.

Level-Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the devices to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the devices in the family is unidirectional; it only passes data in one direction, as indicated in the *Functional Diagrams*. Each device features four unidirectional channels that operate independently with guaranteed data rates from DC up to 10Mbps. The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on the output supply, the outputs go to high-Z regardless of the state of the inputs. When an undervoltage condition is detected on the input supply, the outputs go to the default regardless of the state of the inputs as seen in *Table 4*. During the output supply rises above the undervoltage (UVLO) (powered), the output transitions from high-Z to default state for a short period of time before becoming valid. During the output supply drops below the UVLO, the output transitions to high-Z immediately. *Figure 3* shows the output UVLO to output valid and input UVLO to output default timing diagrams. *Figure 4* through *Figure 7* show the behaviors of the outputs during power-up and power-down.

Table 7. Output Behavior During Undervoltage Conditions

V_{IN}	V_{DDA}	V_{DDB}	ENA, ENB	V_{OUTA}	V_{OUTB}
X	X	X	0	High-Z	High-Z
1	Powered	Powered	1	High	High
0	Powered	Powered	1	Low	Low
X	Undervoltage	Powered	1	High-Z	Default
X	Powered	Undervoltage	1	Default	High-Z

Note: X is "Don't care".

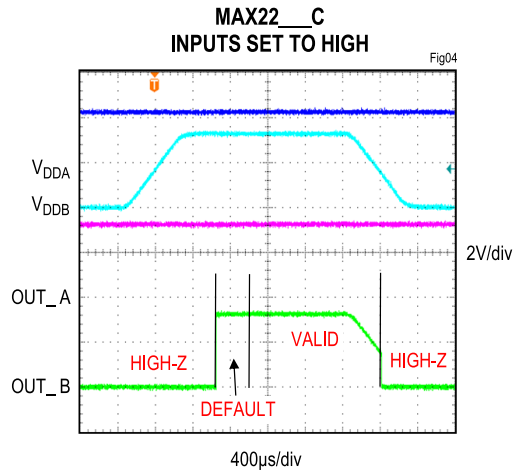


Figure 4. Undervoltage Lockout Behavior, Default High, Inputs High, Weak Outputs Pulldown to Ground

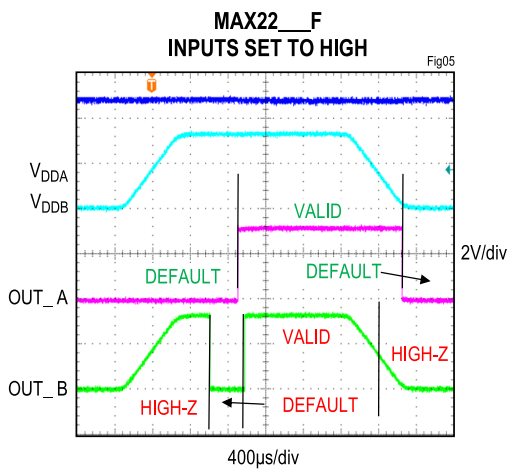


Figure 5. Undervoltage Lockout Behavior, Default Low, Inputs High, Weak Outputs Pullup to Supply

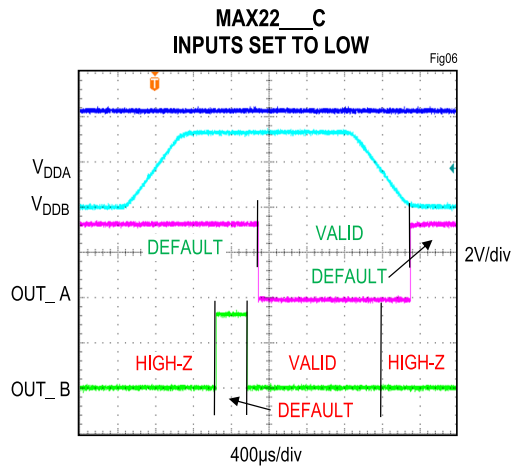


Figure 6. Undervoltage Lockout Behavior, Default High, Inputs Low, Weak Outputs Pulldown to Ground

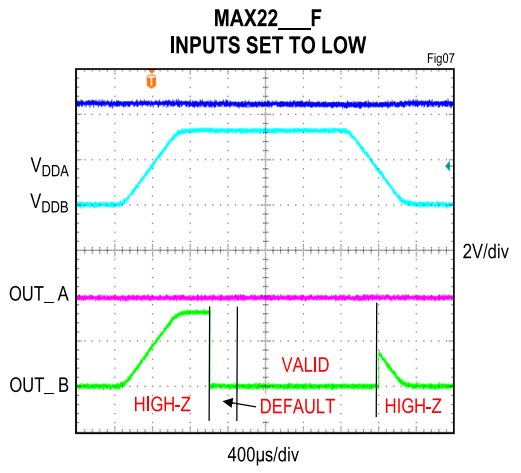


Figure 7. Undervoltage Lockout Behavior, Default Low, Inputs Low, Weak Outputs Pullup to Supply

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the devices can dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. *Table 8* shows the safety limits for the devices.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the *Absolute Maximum Ratings*. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the *Package Information* section and power dissipation calculations are discussed in the *Calculating Power Dissipation* section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 8 shows the thermal derating curves for safety limiting the power of the devices. *Figure 9* show the thermal derating curve for safety limiting the current of the devices. Ensure that the junction temperature does not exceed 150°C.

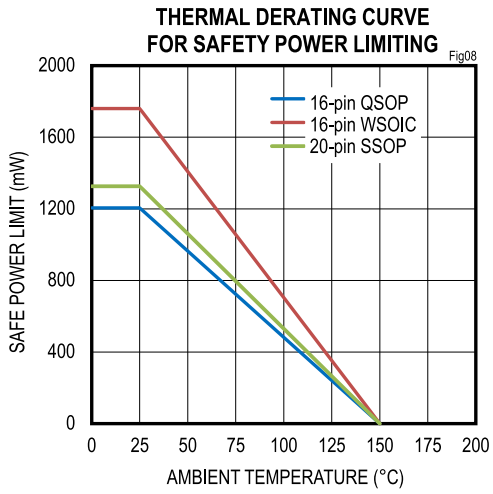


Figure 8. Thermal Derating Curve for Safety Power Limiting

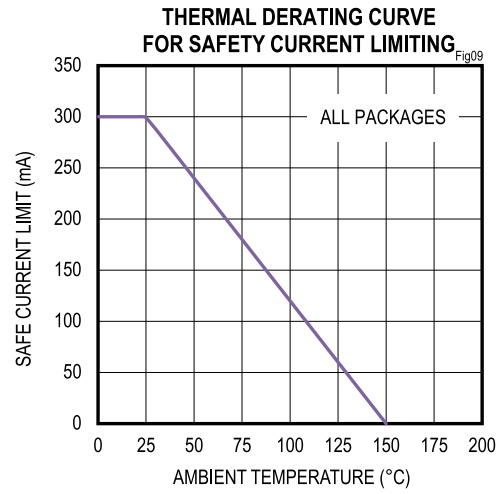


Figure 9. Thermal Derating Curve for Safety Current Limiting

Table 8. Safety Limiting Values

PARAMETER	SYMBOL	TEST CONDITIONS		MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C		300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C T_A = 25°C	16-pin QSOP	1205	mW
			16-pin Wide SOIC	1760	
			20-pin SSOP	1326	
Maximum Safety Temperature	T_S			150	°C

Applications Information

I/O Schematics

The family of devices use the I/O structures in *Figure 10* to ensure both inputs and outputs are protected for electrical static discharges (ESD).

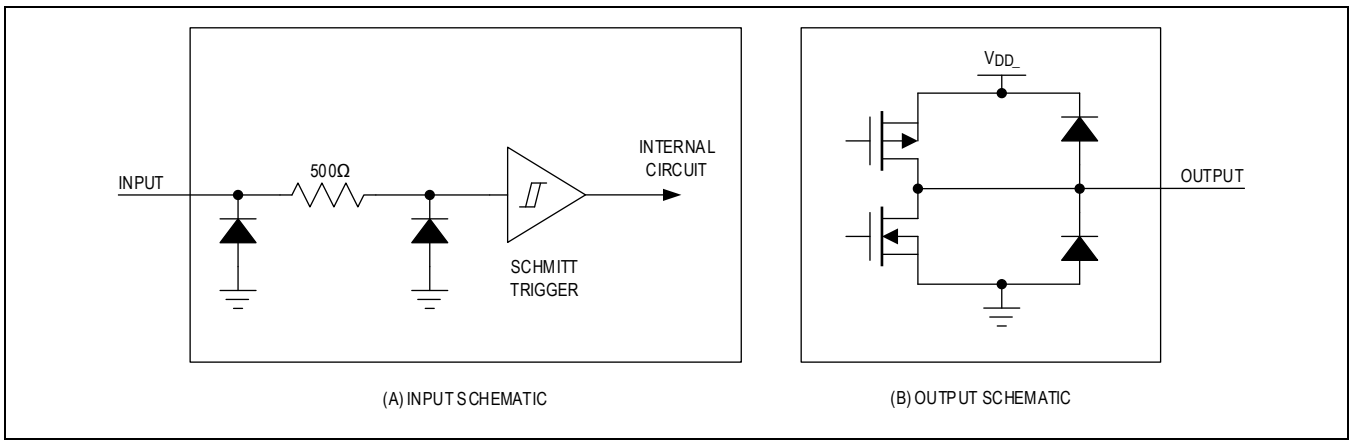


Figure 10. Device I/O Schematics

Power-Supply Sequencing

The family of devices does not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 1nF and 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close as possible with less than 2mm distance from the power supply pins.

Layout Considerations

The PCB designer should follow some critical recommendation in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias to keep the signal paths low-inductance.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the devices free from ground and signal planes. Any galvanic or metallic connection between the side A and side B defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by adding the current required for each channel.

The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in *Figure 11* and *Figure 12* Note that the data in *Figure 11* and *Figure 12* are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the no load current (shown in *Figure 11* and *Figure 12*), which is a function of voltage and data rate, and the load current, which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where:

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second/2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage, and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD}/R_L$$

where:

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in *Figure 13*)A MAX22441C is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 1Mbps with a 15pF capacitive load, channel 2 operating at 10Mbps with a 10kΩ resistive load, channel 3 operating at DC with a 15pF capacitive load, and channel 4 operating at 5Mbps with a 15pF capacitive load. See *Table 9* and *Table 10* for V_{DDA} and V_{DDB} supply-current calculation worksheets.

V_{DDA} must supply:

- Channel 1, an input channel operating at 2.5V and 1Mbps, consuming 23.64µA, estimated from *Figure 11*
- Channel 2, an input channel operating at 2.5V and 10Mbps, consuming 223.82µA, estimated from *Figure 11*
- Channel 3, an input channel connected to ground (DC), consuming 1.39µA, estimated from *Figure 11*
- Channel 4, an output channel operating at 2.5V and 5Mbps, consuming 74.36µA, estimated from *Figure 12*
- I_{CL} on channel 4 for 15pF capacitor at 2.5V and 5Mbps is 93.75µA.

Total current for side A = 416.96µA (typ)

V_{DDB} must supply:

- Channel 1, an output channel operating at 3.3V and 1Mbps, consuming 20.85µA, estimated from *Figure 12*
- Channel 2, an output channel operating at 3.3V and 10Mbps, consuming 158.81µA, estimated from *Figure 12*
- Channel 3, an output channel operating at DC, consuming 5.52µA, estimated from *Figure 12*
- Channel 4, an input channel operating at 3.3V and 5Mbps, consuming 114.13µA, estimated from *Figure 11*
- I_{CL} on channel 1 for 15pF capacitor switching at 1Mbps and 3.3V is 24.75µA.
- I_{RL} on channel 2 for 10kΩ resistor switching at 10Mbps and 3.3V is 165µA.
- I_{CL} on channel 3 for 15pF capacitor at DC and 3.3V is 0µA.

Total current for side B = 489.06µA (typ)

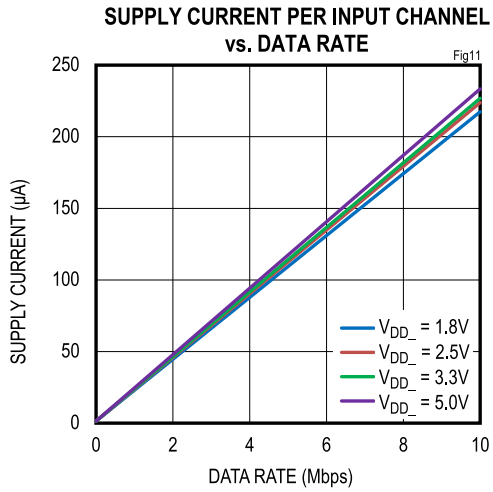


Figure 11. Supply Current per Input Channel (Estimated)

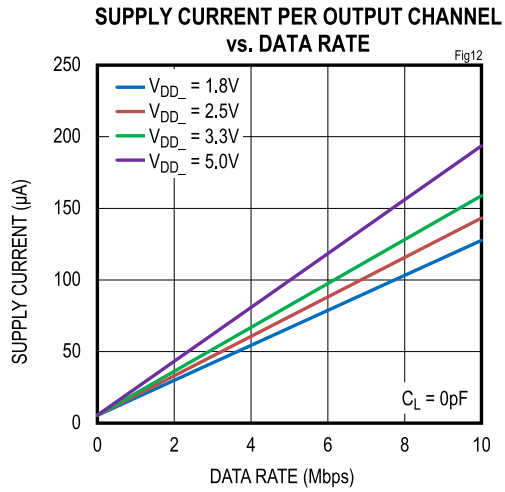


Figure 12. Supply Current per Output Channel (Estimated)

Table 9. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 2.5V					
CHANNEL	**IN/OUT**	**DATA RATE (Mbps)**	**LOAD TYPE**	**LOAD**	**NO LOAD CURRENT (µA)**	**LOAD CURRENT (µA)**
1	IN	1	—	—	23.64	—
2	IN	10	—	—	223.82	—
3	IN	DC	—	—	1.39	—
4	OUT	5	Capacitive	15pF	74.36	2.5V x 2.5MHz x 15pF = 93.75µA
Total: 416.96µA						

Table 10. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 3.3V					
CHANNEL	**IN/OUT**	**DATA RATE (Mbps)**	**LOAD TYPE**	**LOAD**	**NO LOAD CURRENT (µA)**	**LOAD CURRENT (µA)**
1	OUT	1	Capacitive	15pF	20.85	3.3V x 0.5MHz x 15pF = 24.75µA
2	OUT	10	Resistive	10kΩ	158.81	3.3V/10kΩ x 0.5 = 165µA
3	OUT	DC	Capacitive	15pF	5.52	0µA
4	IN	5	—	—	114.13	—
Total: 489.06µA						

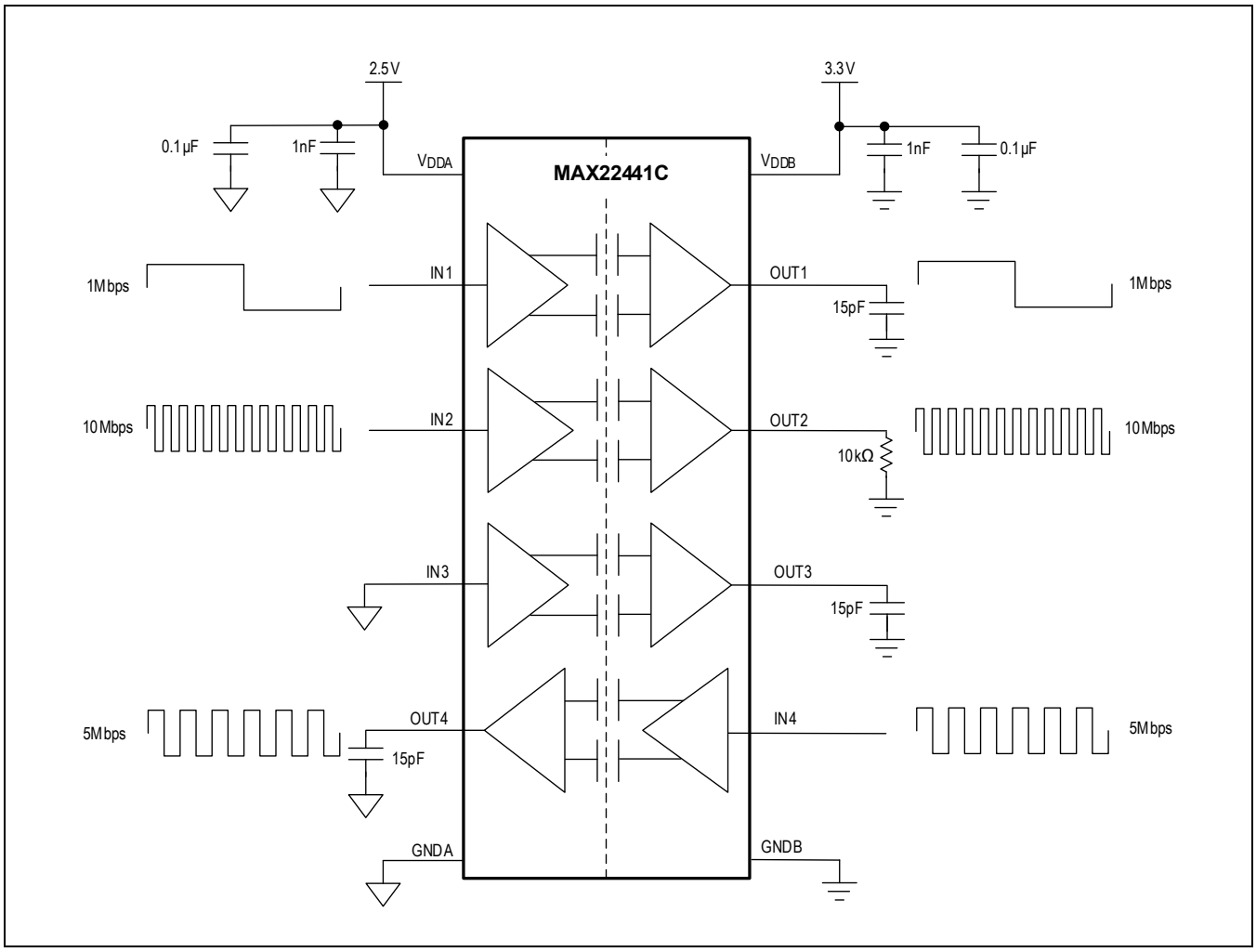
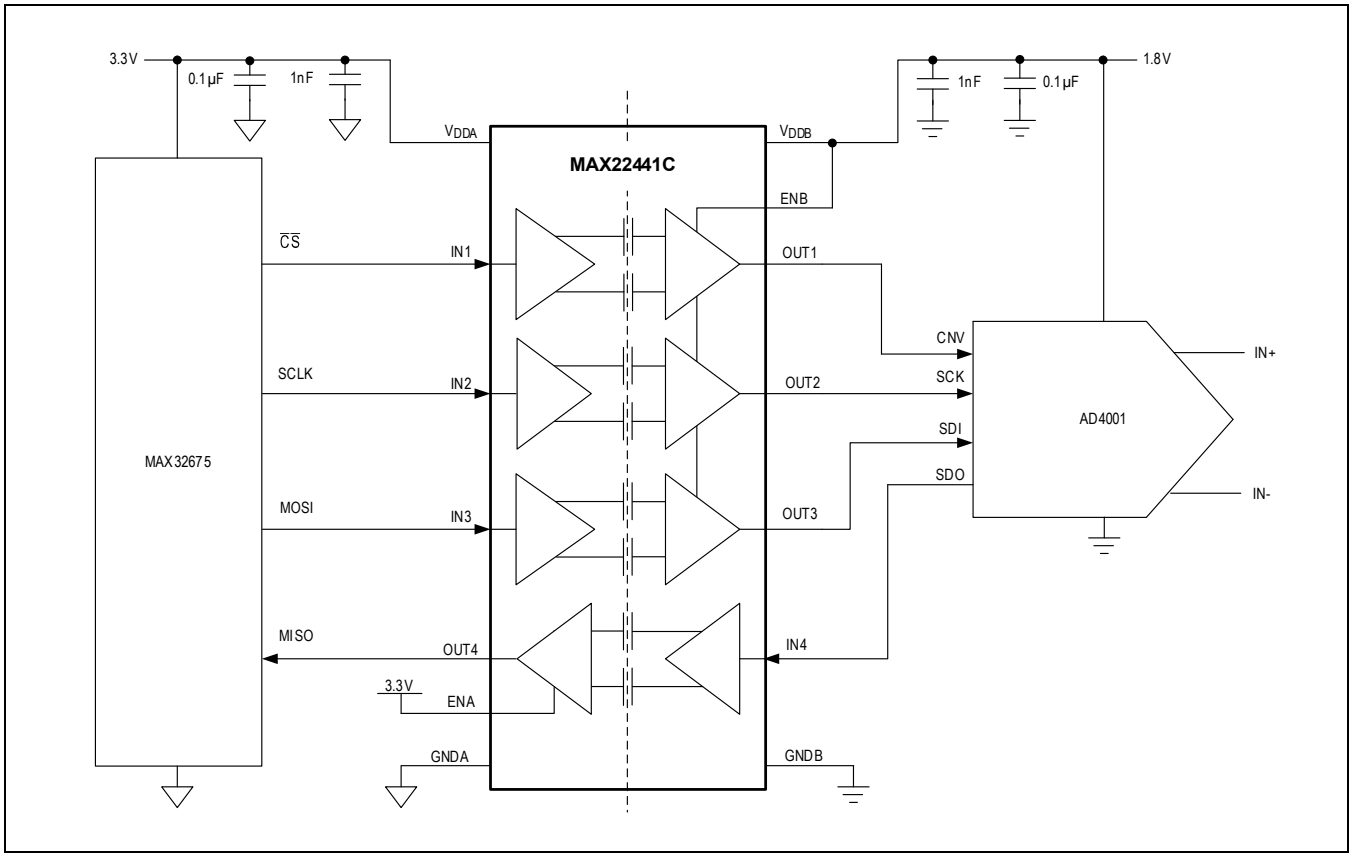


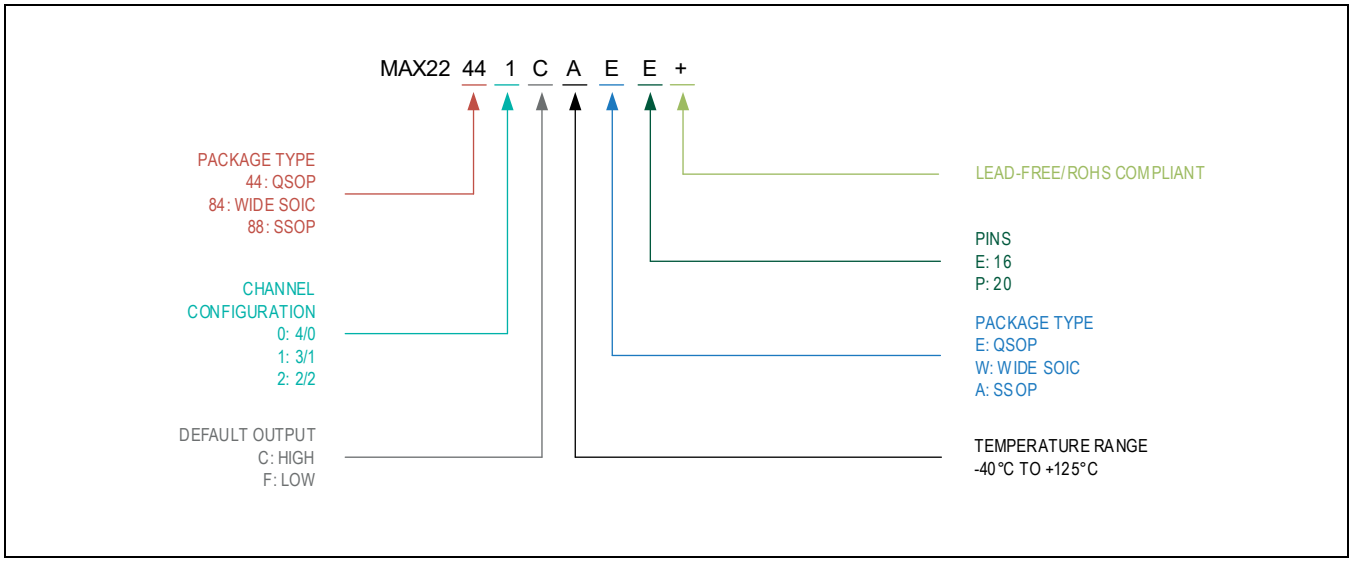
Figure 13. Example Circuit for Supply Current Calculation

Typical Application Circuits

Ultra-Low-Power ADC with Isolated SPI Control



Product Selector Guide



Ordering Information

PART NUMBER	CHANNEL CONFIGURATION	DEFAULT OUTPUT	ISOLATION VOLTAGE (kV_{RMS})	PIN-PACKAGE	TEMPERATURE RANGE
MAX22440CAEE+*	4/0	High	3	16-QSOP	-40°C to +125°C
MAX22440FAEE+*	4/0	Low	3	16-QSOP	-40°C to +125°C
MAX22441CAEE+	3/1	High	3	16-QSOP	-40°C to +125°C
MAX22441FAEE+	3/1	Low	3	16-QSOP	-40°C to +125°C
MAX22442CAEE+*	2/2	High	3	16-QSOP	-40°C to +125°C
MAX22442FAEE+*	2/2	Low	3	16-QSOP	-40°C to +125°C
MAX22840CAWE+*	4/0	High	5	16-WSOIC	-40°C to +125°C
MAX22840FAWE+	4/0	Low	5	16-WSOIC	-40°C to +125°C
MAX22841CAWE+	3/1	High	5	16-WSOIC	-40°C to +125°C
MAX22841FAWE+*	3/1	Low	5	16-WSOIC	-40°C to +125°C
MAX22842CAWE+*	2/2	High	5	16-WSOIC	-40°C to +125°C
MAX22842FAWE+*	2/2	Low	5	16-WSOIC	-40°C to +125°C
MAX22880CAAP+*	4/0	High	3.75	20-SSOP	-40°C to +125°C
MAX22880FAAP+*	4/0	Low	3.75	20-SSOP	-40°C to +125°C
MAX22881CAAP+	3/1	High	3.75	20-SSOP	-40°C to +125°C
MAX22881FAAP+*	3/1	Low	3.75	20-SSOP	-40°C to +125°C
MAX22882CAAP+*	2/2	High	3.75	20-SSOP	-40°C to +125°C
MAX22882FAAP+*	2/2	Low	3.75	20-SSOP	-40°C to +125°C

**Future product—contact factory for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/22	Release for Market Intro	—
1	11/22	Updated the Pinouts of SSOP Packages.	1, 16, 17
2	01/23	Added Future Product Designation for MAX22441FAEE+ and MAX22840FAWE+ in the Ordering Information Section.	28
3	03/23	Corrected Notes. Removed CSA notice 5A in the Safety Regulatory Approval	11, 12, 13, 16
4	8/23	Removed future product designation from MAX22881CAAP+ and MAX22841CAWE+ in the *Ordering Information* section	27
5	1/24	Removed future product designation from MAX22441FAEE+ and MAX22840FAWE+ in the *Ordering Information* section	27