Add Robust and Reliable Isolation to Your High Speed SPI Communications

Introduction

Serial Peripheral Interface (SPI) is a protocol which is commonly used for communication between a digital processor core and peripherals in industrial equipment. However, in order for it to be used safely, it is necessary that the peripherals and the core be electrically isolated. While isolation and SPI are both mature technologies, interfacing the two is not as trivial as might be expected.

Overview of SPI

The Serial Peripheral Interface (SPI) is an inter-device bus protocol that provides fast, synchronous, full-duplex communication between a master and one of several slave devices. The master device (such as an MCU or FPGA), drives the clock and selects a slave device (such as an ADC or digital output driver) to address. Every SPI device consists of a single shift register and control circuitry so that the selected device is simultaneously transmitting and receiving. There are four signals used in SPI communication as shown in Figure 1.

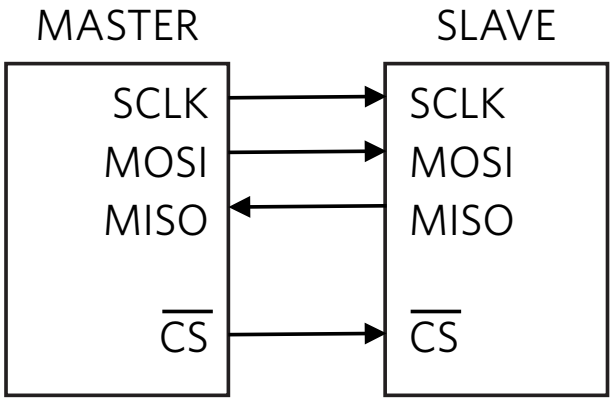

Figure 1 Master/Slave SPI connection

SCLK: The synchronous clock used by all devices. The master drives this clock and the slaves receive it. Note that SCLK can be gated and need not be driven between SPI transactions.

MOSI: Master out, slave in. Also called DO on the Master or DI on the slave. This is the main data line driven by the master to all slaves on the SPI bus. Only the selected slave clocks data from MOSI.

MISO: Master in, slave out. Also called DI on the Master and DO on the Slave. This is the main data line driven by the selected slave to the master. Only the selected slave may drive this signal.

CS: Chip Select, this signal is unique to each slave. When active (generally low) the selected slave must drive MISO based on SCLK transitions.

Challenges for Industrial Applications

For many industrial control applications, the communications pathway between the digital processor core (MCU) and the I/O module devices must be isolated. Isolation helps to minimize noise and ground loop problems, and also provides protection of expensive control units (MCUs or FPGAs) and of equipment operators. The traditional approach to signal isolation has been to use opto-couplers. However, several drawbacks make opto-couplers unsuitable for modern, high-speed, SPI data transfer applications. Opto-couplers introduce long propagation delays, have high power consumption and are bulky. Smaller, CMOS capacitive digital isolation chips have now replaced opto-couplers. However, the use of digital isolators in themselves is not a panacea. In order for digital isolators to be effectively used in high speed SPI communication, it is necessary for them to meet several challenging voltage and timing parameters, as illustrated in Figure 2.

Typically, the voltages in the analog and digital domains of the isolator are at different levels. For an isolator to be effective, it must be able to operate across the widest possible voltage range in both domains.

Additionally, since SPI is a de-facto standard rather than a formal standard, there is no clearly defined clock frequency. Although many legacy devices may use a clock frequency in the 5MHz–10MHz range, many newer devices have much higher speed data transfer requirements, using clock frequencies between 50MHz 75MHz. An effective isolator must be able to operate over this wide SPI frequency range.

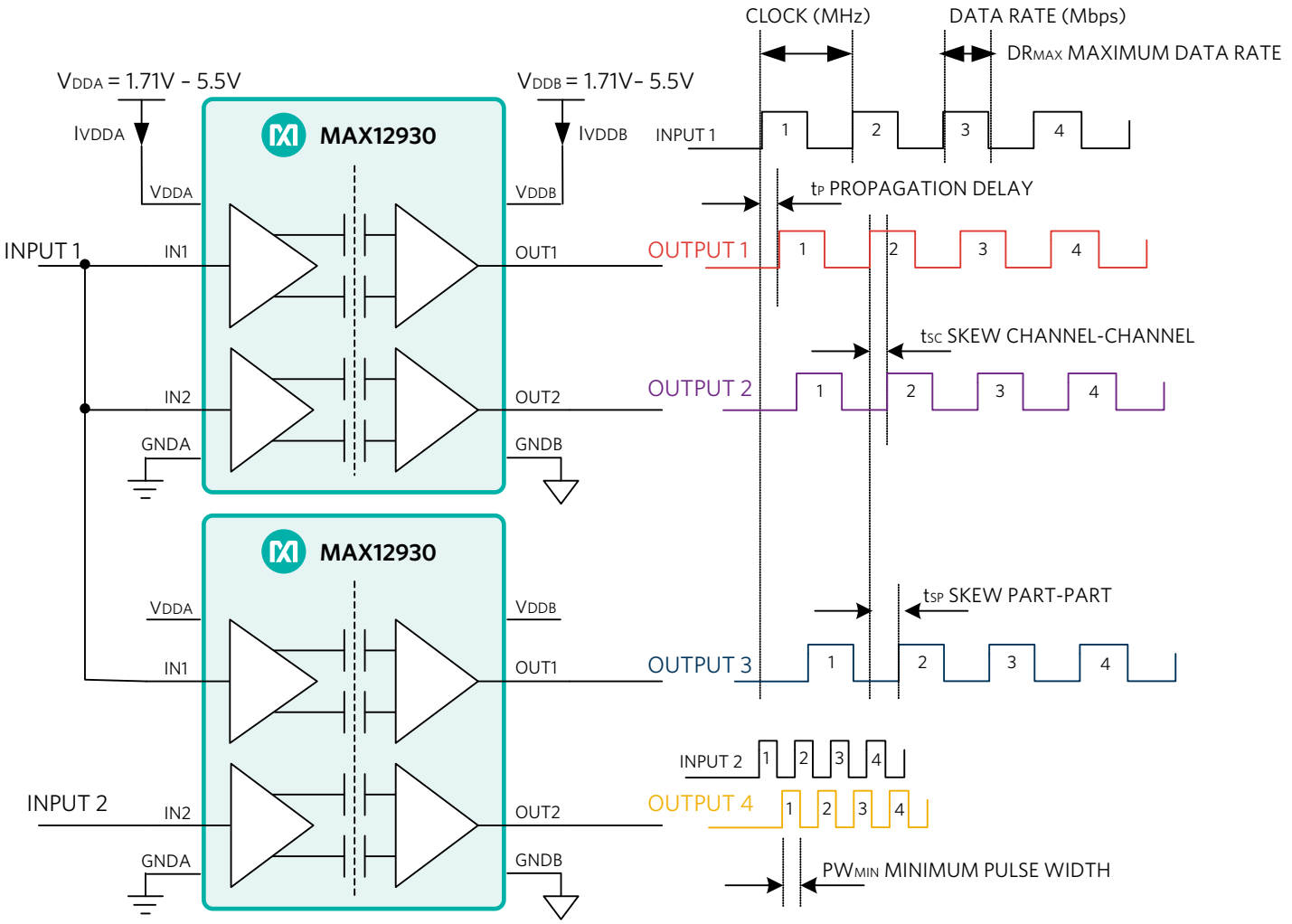

Figure 2 Critical timing parameters for high-speed SPI

By placing a digital isolator between a master and a slave device, additional signal delays are created for the SPI bus. The master uses the rising clock edge to send data (T_{PD1} for SCLK) and the falling edge to sample the data sent back from the slave (T_{PD2} for MISO). The system designer needs to check the timing budget to be sure the isolator propagation delay does not violate the master's timing requirements for sampling MISO. Otherwise, the master will lose synchronicity, or errors will be introduced into the received/transmitted data, as shown in Figure 3.

A single digital isolator part may consist of several isolation channels (typically between one and four). It is, therefore, critical that the delay is matched between isolator channels. Otherwise, a propagation delay skew may be introduced. This is important where, for example, a clock is transmitted via one channel of an isolator and data via another.

Finally, the addition of a digital isolator to the circuit will obviously cause current consumption to increase. An effective isolator should not contribute excessively to the power budget, to avoid heat dissipation in small enclosures.

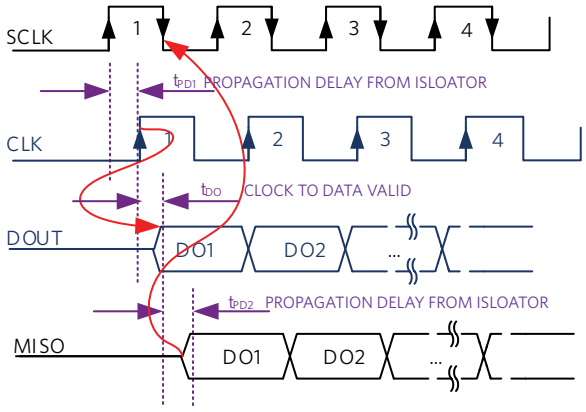

Figure 3 Timing mismatch due to isolator delays

Addressing the Voltage and Timing Challenges

Consider Figure 4, which shows a typical isolated, high-speed SPI communication circuit between an FPGA and an ADC.

The ADC is isolated from the FPGA using the MAX14935 and MAX12930 digital isolators. SCLK clocks data (MOSI) from the FPGA to the ADC. At the input to the ADC, the isolated SCLK is represented as CLK and the isolated MOSI is represented as DIN. During low-speed SPI communication, the master clock is also used to clock data (MISO) travelling in the reverse direction. In order to compensate for the fact that the master clock (SCLK) has already been delayed by the isolation in the forward direction, a copy of CLK (the isolated SCLK) is returned when clocking data in the reverse direction from the ADC to the FPGA. This ensures that the timing of CLK and DOUT are still in synch by the time they have been isolated and reach the FPGA as RETURN_SCLK and MISO, respectively.

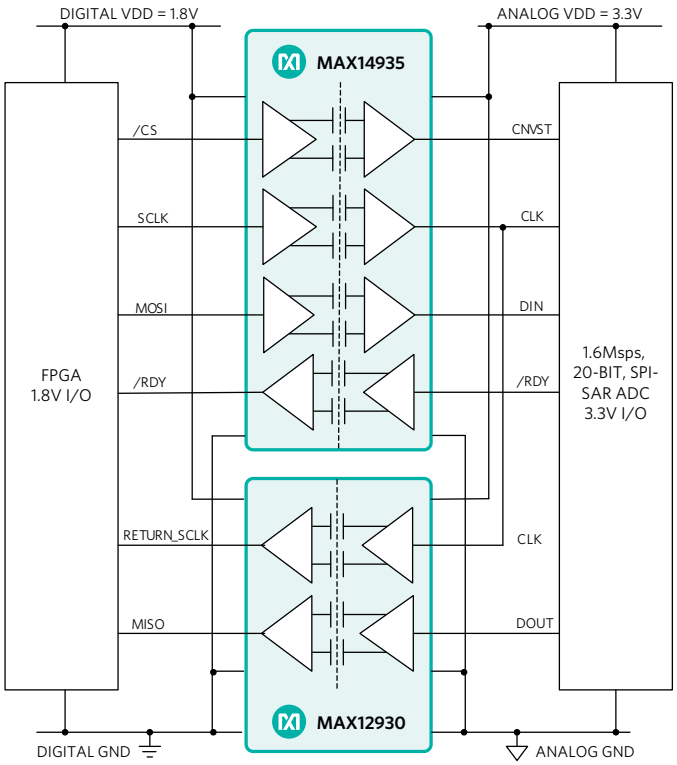

Figure 4 Typical high-speed SPI isolation circuit

In order for this arrangement to be successful, it is essential not only to have low isolator propagation delay and low channel-to-channel skew, but also low part-to-part skew. Maxim Integrated's MAX1493x and MAX1293x family of CMOS digital isolators are specifically designed to meet these requirements and ensure that the circuit arrangement can be implemented successfully, to provide isolation in high-speed SPI communications (Figure 5).

Conclusion

Based on Maxim's proprietary capacitive isolation technology,

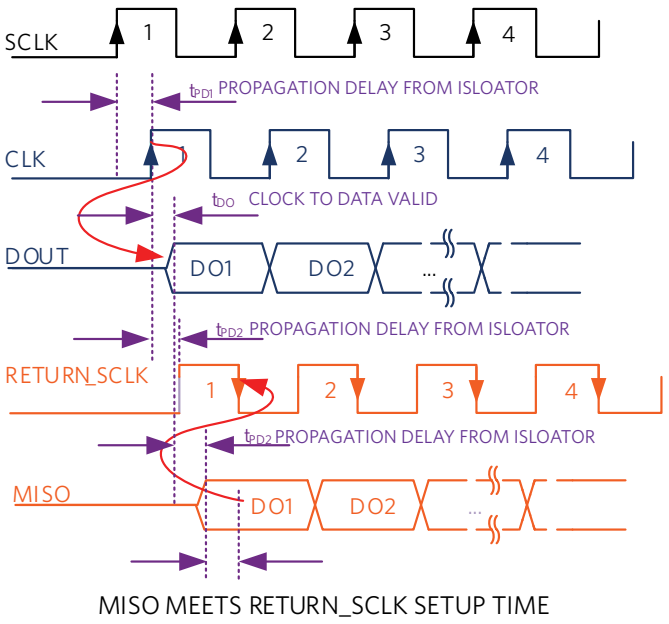

Figure 5 Timing with clock return to master

the MAX1493x and MAX1293x family of digital isolators provide system designers with the highest degree of flexibility for high-speed SPI isolation. They provide high isolation voltage protection (up to 5kVrms) while also supporting data rates up to 150Mbps. The parts operate over a wide supply voltage range (1.71V to 5.5V) with typical propagation delays of 5ns (7.5ns, max). A maximum pulse width distortion of 1ns, combined with a maximum channel-to-channel skew of 0.9ns and a maximum part-to-part skew of 3ns ensure reliable operation in high speed SPI communication circuits. Providing up to four isolation channels per part, the MAX1493x and MAX1293x are also ideal for use in programmable logic controllers (PLCs), telecommunications and medical instrumentation applications.

Learn more:

MAX14930 4-Channel, 2.75kV$_{RMS}$ /3.75kV$_{RMS}$ Digital Isolator

MAX14931 3/1-Channel, 2.75kV$_{RMS}$ /3.75kV$_{RMS}$ Digital Isolator

MAX14932 2/2-Channel, 2.75kV$_{RMS}$ /3.75kV$_{RMS}$ Digital Isolator

MAX14934 4-Channel, 5kV$_{RMS}$ Digital Isolator

MAX14935 3/1-Channel, 5kV$_{RMS}$ Digital Isolator

MAX14936 2/2-Channel, 5kV$_{RMS}$ Digital Isolator

MAX12930 2-Channel Digital Isolator

MAX12931 1/1-Channel Digital Isolator

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