User's Guide

TPS54JB20EVM-023 20-A, Buck Converter Evaluation Module

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ABSTRACT

This user's guide contains information for the TPS54JB20EVM-023 evaluation module (EVM) as well as for the TPS54JB20 DC/DC converter. Also included are the performance specifications, the schematic, and the list of materials for the TPS54JB20EVM.

Table of Contents

List of Figures

List of Tables

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1 Introduction

The TPS54JB20 is a D-CAP3™ synchronous buck converter, designed for 20-A output current, and evaluation module are designed to demonstrate the small printed-circuit-board areas that can be achieved when designing with the device. The high-side and low-side switching MOSFETs are integrated in the device package along with their gate drive circuitry. Rated input voltage and output current ranges for the evaluation module are given in Table 1-1.

1.1 Background

The EVM is set up to allow the user to evaluate the performance of the TPS54JB20 IC, and easily make changes to multiple settings. The low drain-to-source on-resistance of the MOSFETs allows the device to achieve high efficiencies and keep the junction temperature low at high output currents. There is no need for external compensation components since this device is designed with D-CAP3™ control topology. On the EVM, the switching frequency and the operation mode are externally selectable using a jumper to set the resistor from the MODE pin to AGND. An external resistor divider allows for an adjustable output voltage. Additionally, the device provides adjustable soft start, adjustable OC limit threshold, external reference input, and an open-drain power good indicator. Lastly, the TPS54JB20 device has a fixed internal VIN undervoltage lockout and externally adjustable UVLO using a resistor divider at the EN pin.

Table 1-1. Input Voltage and Output Current Summary

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS54JB20	V_{IN} = 4 V to 16 V	0 A to 20 A

Figure 1-1. Safety Warnings

1.2 Performance Specification Summary

A summary of the TPS54JB20EVM performance specifications is provided in Table 1-2. Specifications are given for an input voltage of V_{IN} = 12 V and an output voltage of 3.3 V, unless otherwise specified. The TPS54JB20EVM is designed and tested for V_{IN} = 8 V to 16 V. The ambient temperature is 25°C for all measurements, unless otherwise noted. The design can be modified to perform over 4 V to 16 V.

Table 1-2. TPS54JB20EVM Performance Specification Summary

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN} voltage range (without internal Bias)		8	12	16	V
Output voltage setpoint			3.3		V
Output current range	V_{IN} = 8 V to 16 V	0	20	20	A
Internal LDO Voltage			3.0		V
Operating frequency			600		kHz

1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54JB20. Some modifications can be made to this module.

1.3.1 Output Voltage Setpoint

To change the output voltage of the EVM, it is necessary to change the value of resistor R6 and R7. R9 is fixed at 10 kΩ. Changing the total value of R6 plus R7 can change the output voltage above the 0.9-V reference voltage V_{INTREF}. A two resistor configuration of R6 + R7 is implemented to give the exact desired output voltage setting. The value of R6 and R7 for a specific output voltage can be calculated using Equation 1.

$$R_{FB\_HS} = \frac{V_O - V_{INTREF}}{V_{INTREF}} \times R_{FB\_LS} \quad (1)$$

where

- V_{INTREF} = 0.9 V
- $R_{FB\_HS} = R_6 + R_7$
- $R_{FB\_LS} = R_9$ = 10 kΩ

1.3.2 Frequency and Operation Mode Setting

To change the frequency and operation mode of the part, the MODE pin is used. J6 and the surrounding circuitry allows for an easy change to the frequency and operation mode setting. Table 1-3 shows all six options offered by J6.

Table 1-3. TPS54JB20EVM Mode Pin Selection

SWITCHING FREQUENCY (F_{SW})	OPERATION MODE UNDER LIGHT LOAD	MODE PIN CONNECTIONS	
		CONNECTION	JUMPER SETTING
600 kHz	Skip Mode	Short to VCC	Short Pins 1 and 2
800 kHz	Skip Mode	243 kΩ ±10% to AGND	Short Pins 3 and 4
1000 kHz	Skip Mode	121 kΩ ±10% to AGND	Short Pins 5 and 6
1000 kHz	Forced CCM	60.4 kΩ ±10% to AGND	Short Pins 7 and 8
800 kHz	Forced CCM	30.1 kΩ ±10% to AGND	Short Pins 9 and 10
600 kHz	Forced CCM	Short to AGND	Short Pins 11 and 12

1.3.3 Enable Pin Selection

The converter can be enabled and disabled by J5.

Default setting: EN pin connected to VIN

Table 1-4. Enable Pin Selection

SET ON CONNECTION	ENABLE SELECTION
Pins 2-3 Shorted	EN pin connected to VIN pins through resistor divider
J3 Open	EN pin is left floating
Pins 1-2 Shorted	EN pin connected to PGND

1.3.4 Remote Sensing

The EVM is not set up for remote sensing by default. To set up remote sensing, follow these steps:

1. Replace R8 and R11 with 100-Ω resistors.
2. Connect your sense points to the Vsns+ and Vsns- test points.

1.3.5 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R2 and R9. See the *TPS54JB20 2.7-V to 16-V Input, 20-A Synchronous Step-down Converter With Differential Remote Sense Data Sheet* for detailed instructions for setting the external UVLO.

2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54JB20EVM. This section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transient, loop response, output ripple, and start-up.

2.1 Input/Output Connections

The TPS54JB20EVM is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying greater than 15 A must be connected to J1 and J2 through a pair of 20-AWG wires or better. The load must be connected to J3 and J4 through a pair of 20-AWG wires or better on each connector. The maximum load current capability is 20 A.

Wire lengths must be minimized to reduce losses in the wires. Test point VIN_SENSE+ provides a place to monitor the input voltage with Test point VIN_SENSE– providing a convenient ground reference. Test point VOUT+ is used to monitor the output voltage with VOUT– as the ground reference.

Table 2-1. TPS54JB20EVM EVM Connectors and Test Points

REFERENCE DESIGNATOR	FUNCTION
J1	VIN input voltage connector (see Table 1-1 for V_{IN} range)
J2	PGND connection for input
J3	VOUT, 3.3 V at 20 A maximum
J4	PGND connection for output
J5	3-pin header for enable. ON -> Connects EN to VIN to enable the device. OFF- > Connects EN to GND to disable device. Floating EN will prevent the part from operating.
J6	12-pin header for mode selection (see Table 1-3)
VIN_SENSE+, VIN_SENSE–	VIN voltage sensing test points
VOUT+, VOUT–	VOUT voltage sensing test points
VCC, PGND	VCC voltage forcing/sensing test points
PGOOD	PGOOD output test point (pulled up to VCC pin through a 30-kΩ resistor)
EN	EN test point
VSNS+, VSNS–	Remote sensing test points
AGND	AGND test point
BODE+, BODE–	Loop measurement test points (BODE+ is at the same net as VOUT, but is closer to FB divider and IC)
SS/REFIN	Can be used to monitor the reference voltage
SW	Switch Node test point

2.2 Start Up Procedure

1. Make sure the EN jumper (J5) is in the ON position (shorting pin 2 and pin 3) to connect the EN pin to the resistor divider from VIN.
2. (Optional) Apply appropriate external bias voltage on VCC and PGND test points. If no external bias, please go directly to step 3. The external bias range is 3.3 V to 5.3 V.
3. Apply appropriate VIN voltage to the VIN and PGND terminals at J1 and J2.

2.3 Efficiency

The efficiency of this EVM peaks at a load current of about 6 A and then decreases as the load current increases toward full load. The following images show the efficiency for the TPS54JB20EVM at an ambient temperature of 25°C. Figure 2-1 shows the efficiency over a range of Vin values Figure 2-2 shows efficiency over a range of Vcc values and how the light load efficiency is improved in DCM.

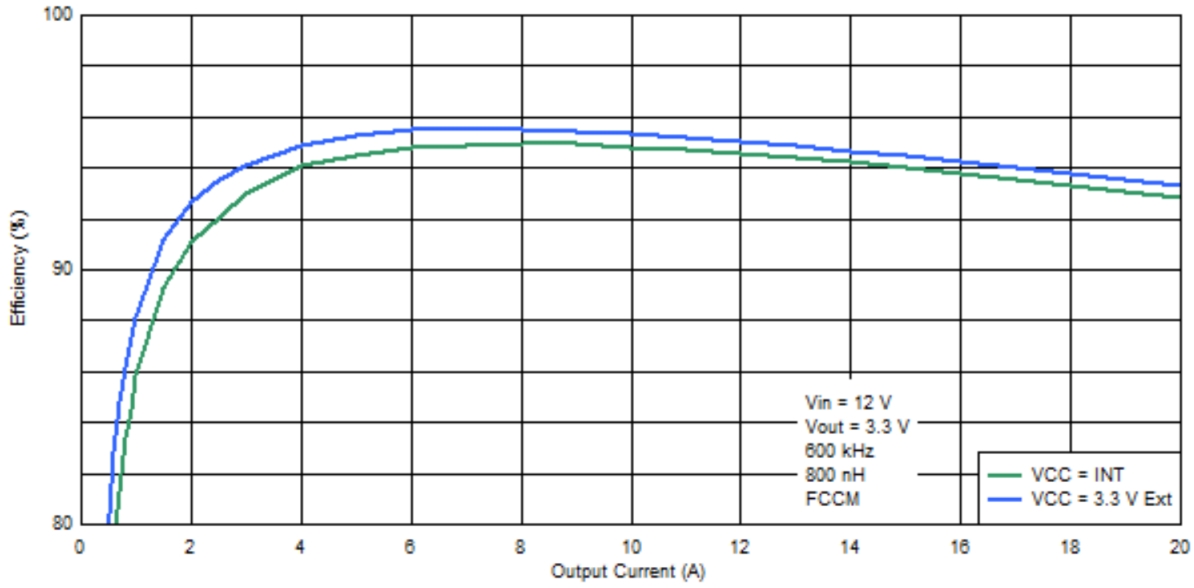

Figure 2-1. TPS54JB20 Efficiency Plot: Internal and External Bias

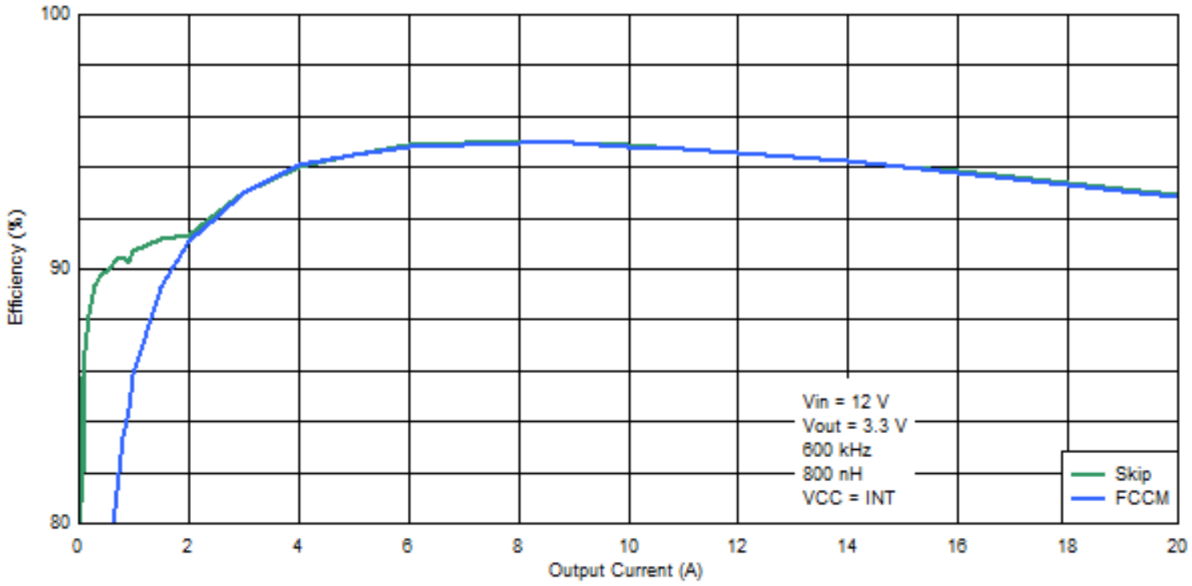

Figure 2-2. TPS54JB20 Efficiency Plot: FCCM and Skip

2.4 Load Regulation

Figure 2-3 shows the load regulation for the TPS54JB20EVM.

Measurements are given for an ambient temperature of 25°C.

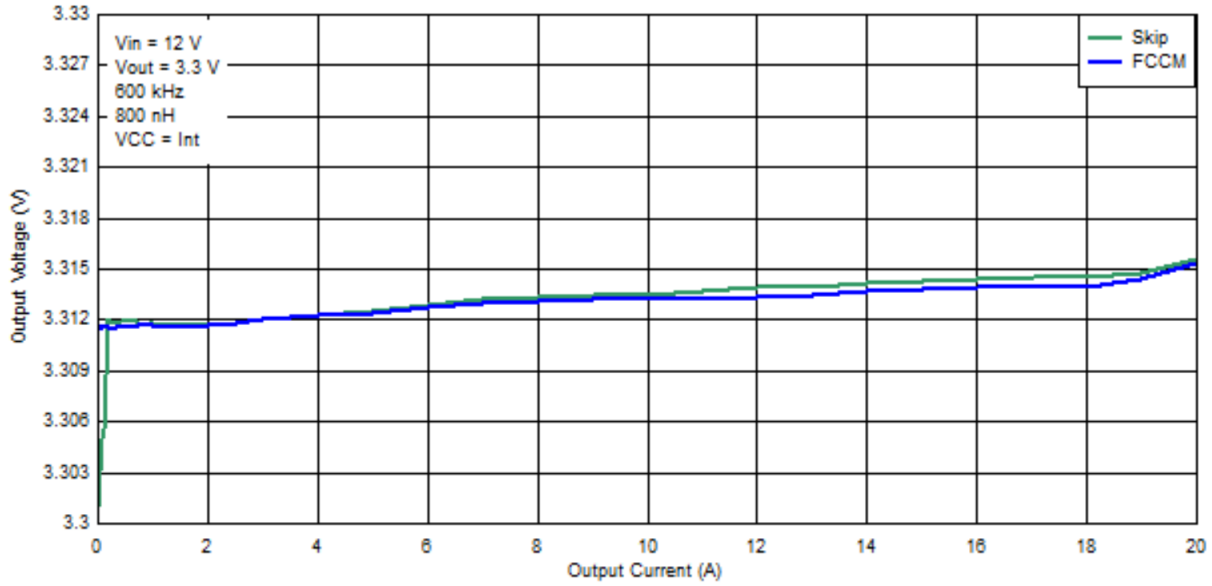

Figure 2-3. TPS54JB20 Load Regulation

2.5 Load Transients

Figure 2-4 and Figure 2-5 show how the TPS54JB20EVM response to load transients. The current step is from 25% to 75% Load. The current step slew rate is 2 A/µs. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

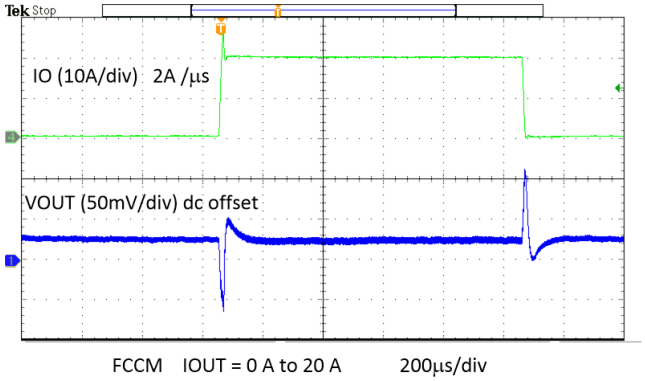

Figure 2-4. TPS54JB20 Load Transient Response

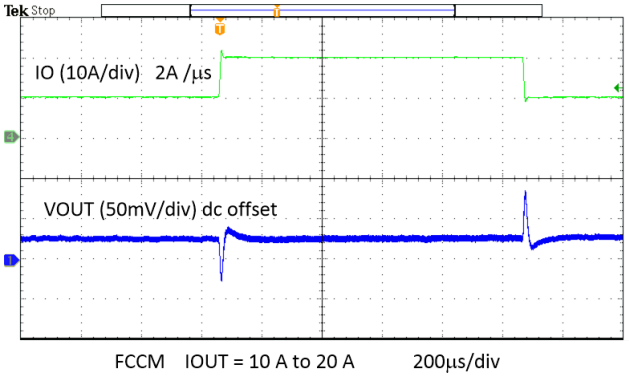

Figure 2-5. TPS54JB20 Load Transient Response

2.6 Loop Characteristics

Figure 2-6 shows the TPS54JB20EVM loop-response characteristics. Gain and phase plots are shown for V_{IN} voltage of 12 V. Load current for the measurement is 100%.

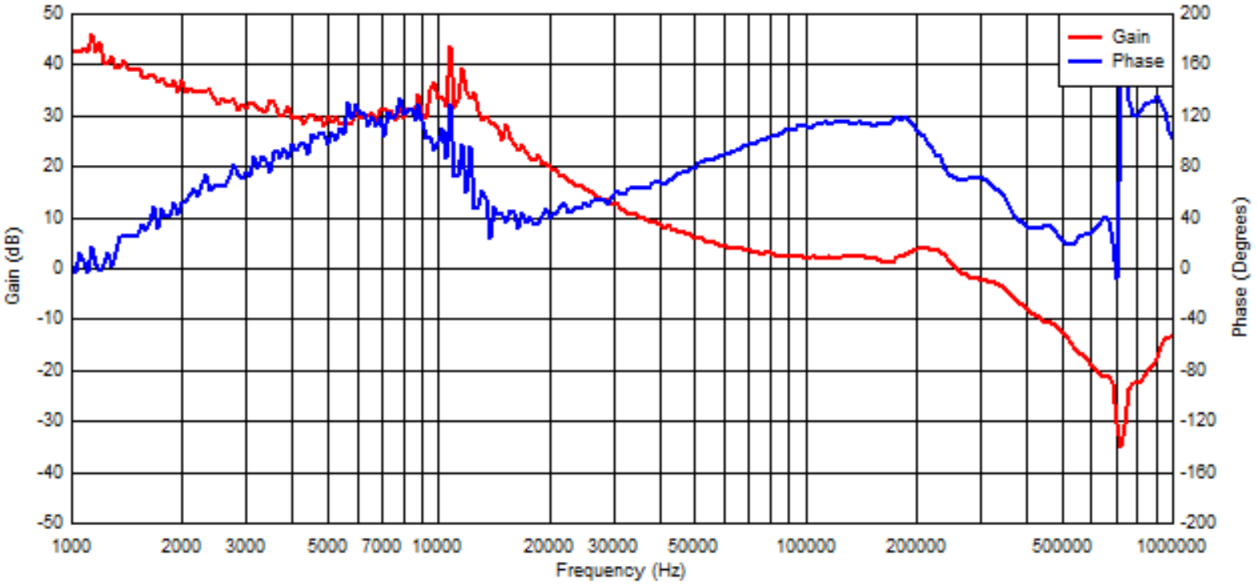

Figure 2-6. TPS54JB20 Bode Plot

2.7 Output Voltage Ripple

Figure 2-7 the TPS54JB20EVM output voltage ripple. V_{IN} = 12 V. The ripple voltage is measured directly across the last ceramic output capacitor.

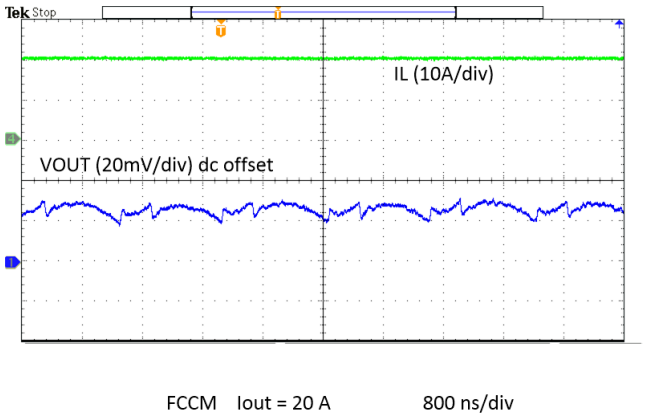

Figure 2-7. TPS54JB20 Output Ripple, 20-A Load

2.8 Powering Up

Figure 2-8 shows the start-up waveforms for the TPS54JB20EVM. This images shows that the start-up sequence begins as soon as the EN voltage is increased above the enable-threshold voltage, and the output voltage ramps up to the externally set value of 1.0 V. The input voltage for these plots is 12 V.

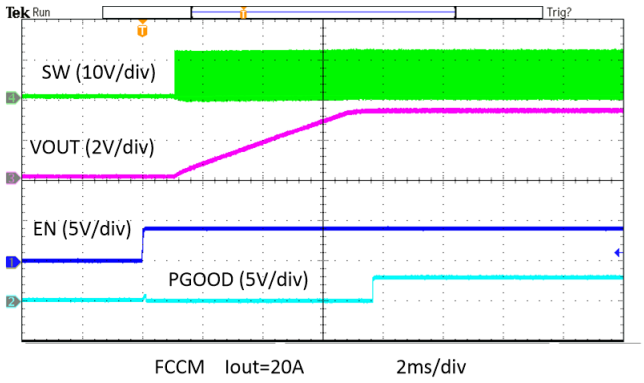

Figure 2-8. TPS54JB20 Enable Start-Up, 20-A Load

2.9 Powering Down

Figure 2-9 shows the TPS54JB20EVM shutdown. The input voltage for these plots is 12 V.

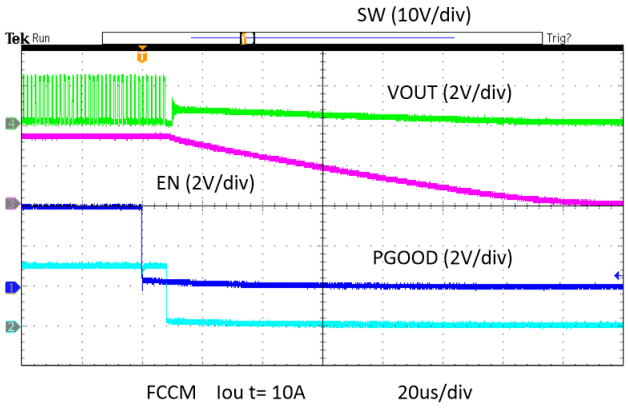

Figure 2-9. TPS54JB20 EN Shutdown, 20-A Load

3 Schematic, List of Materials, and Layout

This section provides a schematic, a description of the TPS54JB20EVM board layout, and layer illustrations.

3.1 Schematic

Figure 3-1 illustrates the schematic for the TPS54JB20EVM.

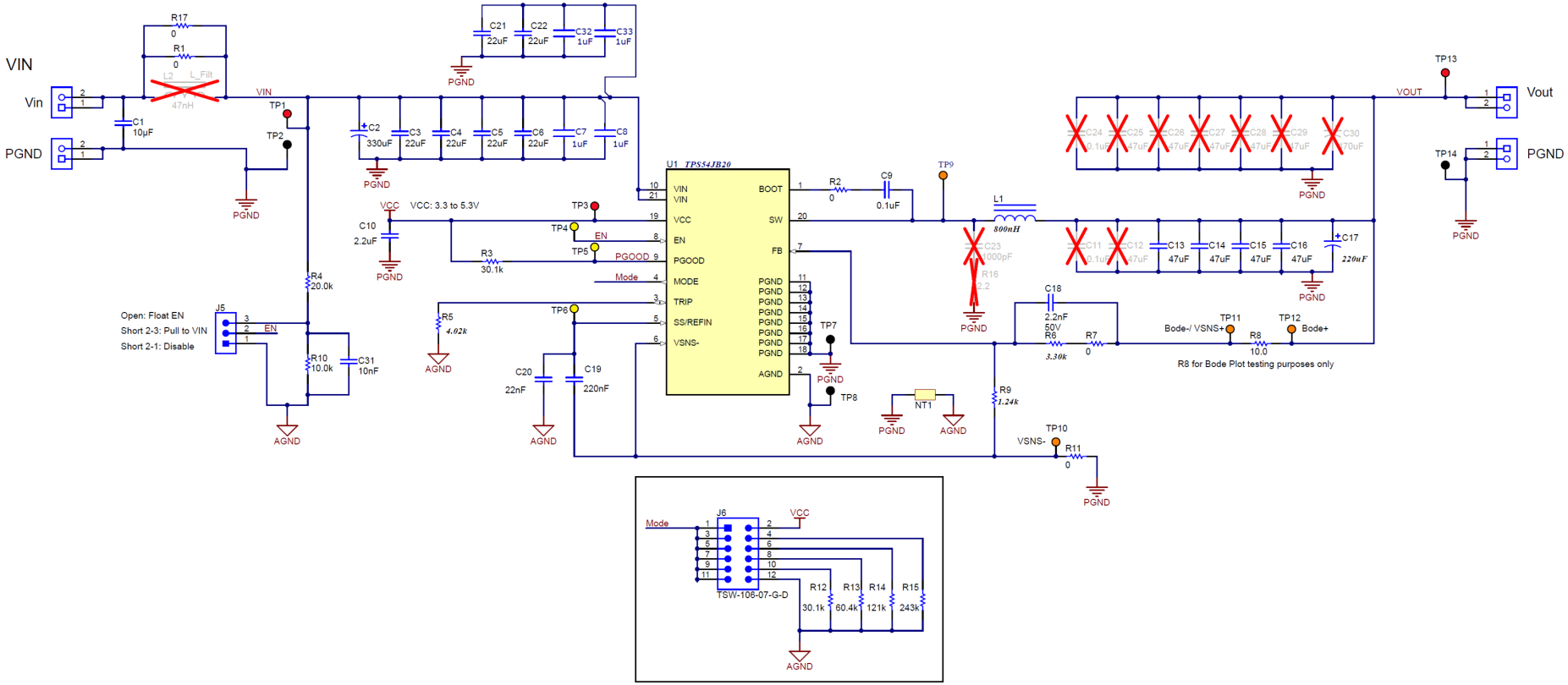

Figure 3-1. TPS54JB20EVM Schematic

3.2 List of Materials

Table 3-1 presents the list of materials for the TPS54JB20EVM.

Table 3-1. TPS54JB20EVM List of Materials

DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
C2	1	CAP, AL, 330 µF, 25 V, ±20%, 0.15 ohm, SMD, 330 µF	EEE-FC1E331P	Panasonic
C5, C6, C21, C22	4	CAP, CERM, 22 µF, 25 V, ±20%, X6S, 1206_190	GRM31CC81E226ME11L	MuRata
C7, C8, C32	3	CAP CER 1UF 25 V X6S 0402	GRM155C81E105KE11D	Murata
C9	1	CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E2X7R1H104K080AA	TDK
C10	1	CAP, CERM, 2.2 µF, 10 V, ±10%, X7R, 0603	GRM188R71A225KE15D	MuRata
C11, C24	2	CAP, CERM, 0.1 µF, 6.3 V, ±10%, X7R, 0402	GRM155R70J104KA01D	MuRata
C17	1	CAP, Tantalum Polymer, 220 µF, 10 V, ±20%, 0.025 Ω, 7343-30 SMD	10TPE220ML	Panasonic
C12, C13, C25, C26	4	CAP, CERM, 47 µF, 6.3 V, ±10%, X6S, 1206	GRM31CC80J476KE18L	MuRata
C19	1	CAP, CERM, 0.22 µF, 16 V, ±10%, X7R, 0603	C1608X7R1C224K080AC	TDK
C20	1	CAP, CERM, 0.022 µF, 16 V, ±10%, X7R, 0603	C0603C223K4RACTU	Kemet
L1	1	Inductor, Shielded, Composite, 800 nH, 25.8 A, 0.00208 Ω, SMD	XAL7070-801MEB	Coilcraft
R1, R17	2	RES, 0, 1%, 0.5 W, 1206	5108	Keystone
R2, R7, R11	3	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R3, R12	2	RES, 30.1 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060330K1FKEA	Vishay-Dale
R4	1	RES, 20.0 k, 0.1%, 0.1 W, 0603	RT0603BRD0720KL	Yageo America
R5	1	RES, 6.04 k, 1%, 0.1 W, 0603	CRCW06036K04FKEA	Vishay-Dale
R6	1	RES, 3.30 k, 1%, 0.1 W, 0603	RC0603FR-073K3L	Yageo
R8	1	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310R0FKEA	Vishay-Dale
R9	1	RES, 1.24 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW06031K24FKEA	Vishay-Dale
R10	1	RES, 10.0 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060310K0FKEA	Vishay-Dale
R13	1	RES, 60.4 k, 1%, 0.1 W, 0603	RC0603FR-0760K4L	Yageo
R14	1	RES, 121 k, 1%, 0.1 W, 0603	RC0603FR-07121KL	Yageo
R15	1	RES, 243 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW0603243KFKEA	Vishay-Dale
U1	1	4-V to 16-V Input, 20-A Single Synchronous Step-Down Converter, RWW0021A (VQFN-HR-21)	TPS54JB20RWWT	Texas Instruments

3.3 Layout

The board layout for the TPS54JB20EVM is shown in Figure 3-2 through Figure 3-5. The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper.

The top layer contains the main power traces for V_{IN}, V_{OUT}, and SW. Also on the top layer are connections for the remaining pins of the TPS54JB20 and the majority of the signal traces. The top layer has a dedicated ground plane for quiet analog ground that is connected to the main power ground plane at a single point. The internal layer-1 is a large ground plane. The internal layer-2 contains an additional large ground copper area as well as an additional V_{OUT} copper fill. The bottom layer is another ground plane with two additional traces for the output voltage feedback and various signals routed to test points and headers. There are also additional V_{IN} and V_{OUT} planes on the bottom layer. The top-side ground traces are connected to the bottom and internal ground planes with multiple via groupings placed around the board.

The input decoupling capacitors and bootstrap capacitor are all located as close to the IC as possible. Additionally, the voltage set point resistor divider components are kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation, the copper V_{OUT} trace at the TP4 test point. An additional input bulk capacitor is used to limit the noise entering the converter from the input supply. Critical analog circuits that are noise sensitive are terminated to the quiet analog ground island on the top layer.

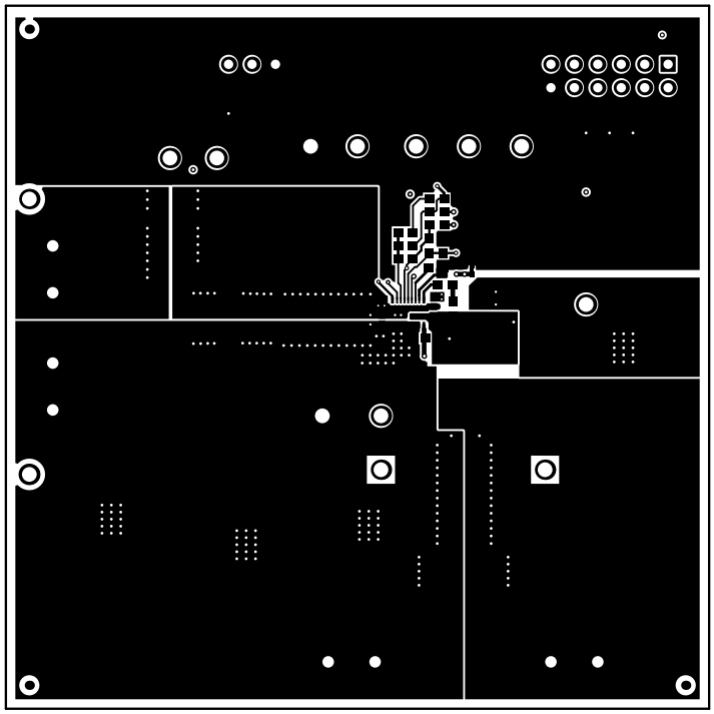

Figure 3-2. TPS54JB20EVM Top-Side Layout

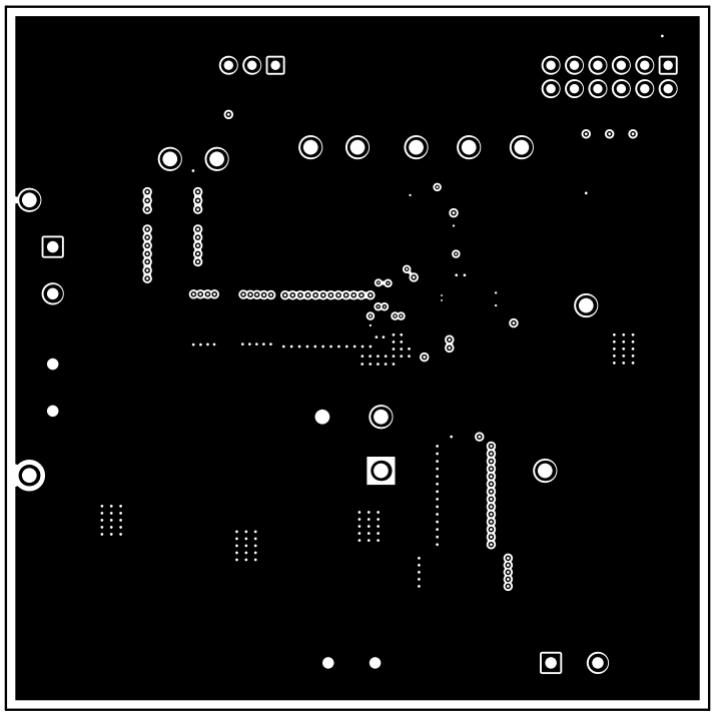

Figure 3-3. TPS54JB20EVM Internal Layer-1 Layout

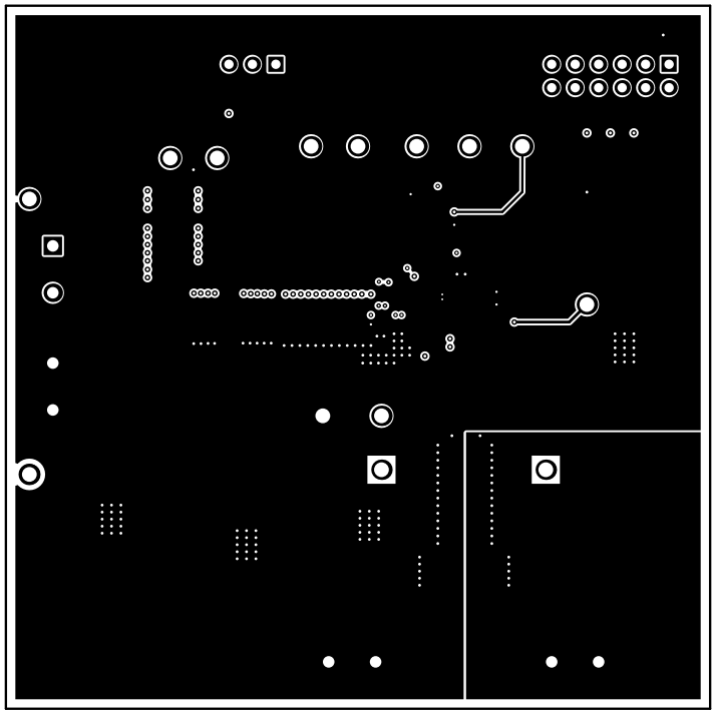

Figure 3-4. TPS54JB20EVM Internal Layer-2 Layout

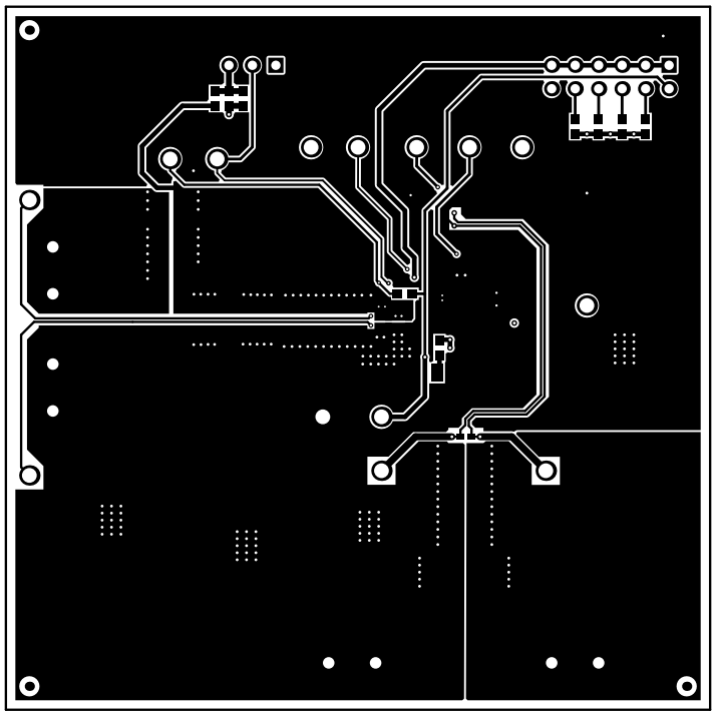

Figure 3-5. TPS54JB20EVM Bottom-Side Layout

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2020) to Revision A (October 2020)	Page
• Removed disclosure statement	1

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