SN54LS592, SN54LS593, SN74LS592, SN74LS593
8-BIT BINARY COUNTERS WITH INPUT REGISTERS

- **Parallel Register Inputs ('LS592)**

- **Parallel 3-State I/O: Register Inputs/ Counter Outputs ('LS593)**

- **Counter has Direct Overriding Load and Clear**

- **Accurate Counter Frequency: DC to 20 MHz**

description

The 'LS592 comes in a 16-pin package and consists of a parallel input, 8-bit storage register feeding an 8-bit binary counter. Both the register and the counter have individual positive-edge-triggered clocks. In addition, the counter has direct load and clear functions. A low-going $\overline{RCO}$ pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting $\overline{RCO}$ of the first stage to $\overline{CCKEN}$ of the second stage. Cascading for larger count chains can be accomplished by connecting $\overline{RCO}$ of each stage to CCK of the following stage.

The 'LS593 comes in a 20-pin package and has all the features of the 'LS592 plus 3-state I/O, which provides parallel counter outputs. The tables below show the operation of the enable (CCKEN, $\overline{CCKEN}$) inputs. A register clock enable ($\overline{RCKEN}$) is also provided.
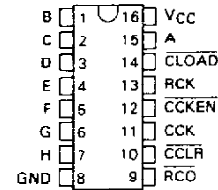
OUTPUT ENABLE CONTROL ('593 ONLY)

G	$\overline{G}$	A/Q$_A$ thru H/Q$_H$
L	L	input mode
L	H	input mode
H	L	output mode
H	H	input mode

COUNTER CLOCK ENABLE CONTROL

CCKEN	$\overline{CCKEN}$	EFFECT ON CCK
L	L	Enable
L	H	Disable
H	L	Enable
H	H	Enable

SN54LS592 . . . J OR W PACKAGE
SN74LS592 . . . N PACKAGE
(TOP VIEW)

```
        B [ 1  U 16 ] Vcc
        C [ 2    15 ] A
        D [ 3    14 ] CLOAD
        E [ 4    13 ] RCK
        F [ 5    12 ] CCKEN
        G [ 6    11 ] CCK
        H [ 7    10 ] CCLR
      GND [ 8     9 ] RCO
```

SN54LS592 . . . FK PACKAGE
(TOP VIEW)

```
          C  B  NC Vcc A
          3  2  1 20 19
      D [ 4          18 ] CLOAD
      E [ 5          17 ] RCK
     NC [ 6          16 ] NC
      F [ 7          15 ] CCKEN
      G [ 8          14 ] CCK
          9 10 11 12 13
          H GND NC RCO CCLR
```
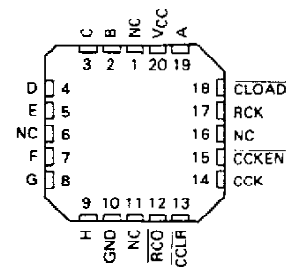
NC — No internal connection

SN54LS593 . . . J OR W PACKAGE
SN74LS593 . . . DW OR N PACKAGE
(TOP VIEW)

```
    A/QA [ 1  U 20 ] Vcc
    B/QB [ 2    19 ] G
    C/QC [ 3    18 ] G
    D/QD [ 4    17 ] RCKEN
    E/QE [ 5    16 ] RCK
    F/QF [ 6    15 ] CCKEN
    G/QG [ 7    14 ] CCKEN
    H/QH [ 8    13 ] CCK
   CLOAD [ 9    12 ] CCLR
     GND [ 10   11 ] RCO
```
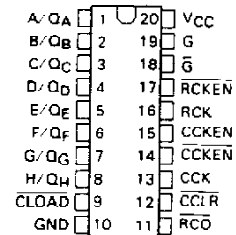
SN54LS593 . . . FK PACKAGE
(TOP VIEW)
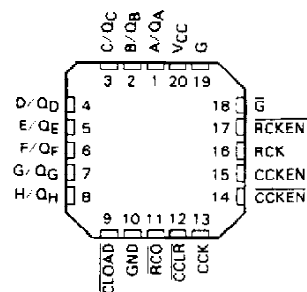
```
          C/QC B/QB A/QA Vcc G
           3   2   1  20 19
   D/QD [ 4          18 ] G
   E/QE [ 5          17 ] RCKEN
   F/QF [ 6          16 ] RCK
   G/QG [ 7          15 ] CCKEN
   H/QH [ 8          14 ] CCKEN
           9 10 11 12 13
         CLOAD GND RCO CCLR CCK
```

TEXAS INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS. TEXAS 75265

schematics of inputs and outputs

EQUIVALENT OF A THRU H INPUTS	EQUIVALENT OF 'LS592 CCK INPUT AND 'LS593 CCK AND RCK INPUTS	EQUIVALENT OF ALL OTHER INPUTS

'LS592 RCK: R_{eq} = 10 kΩ NOM
ALL OTHER: R_{eq} = 13 kΩ NOM

$\overline{RCO}$ OUTPUT	TYPICAL OF Q OUTPUTS ('LS593)

logic symbols †

'LS592

'LS593
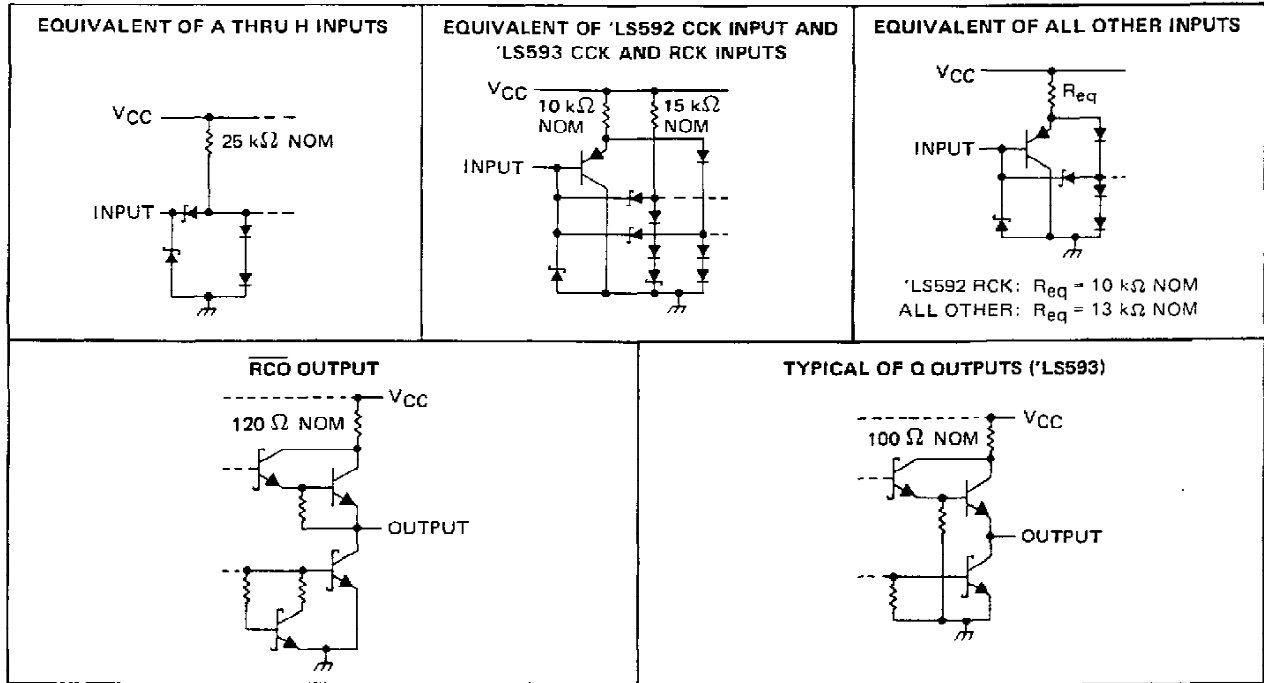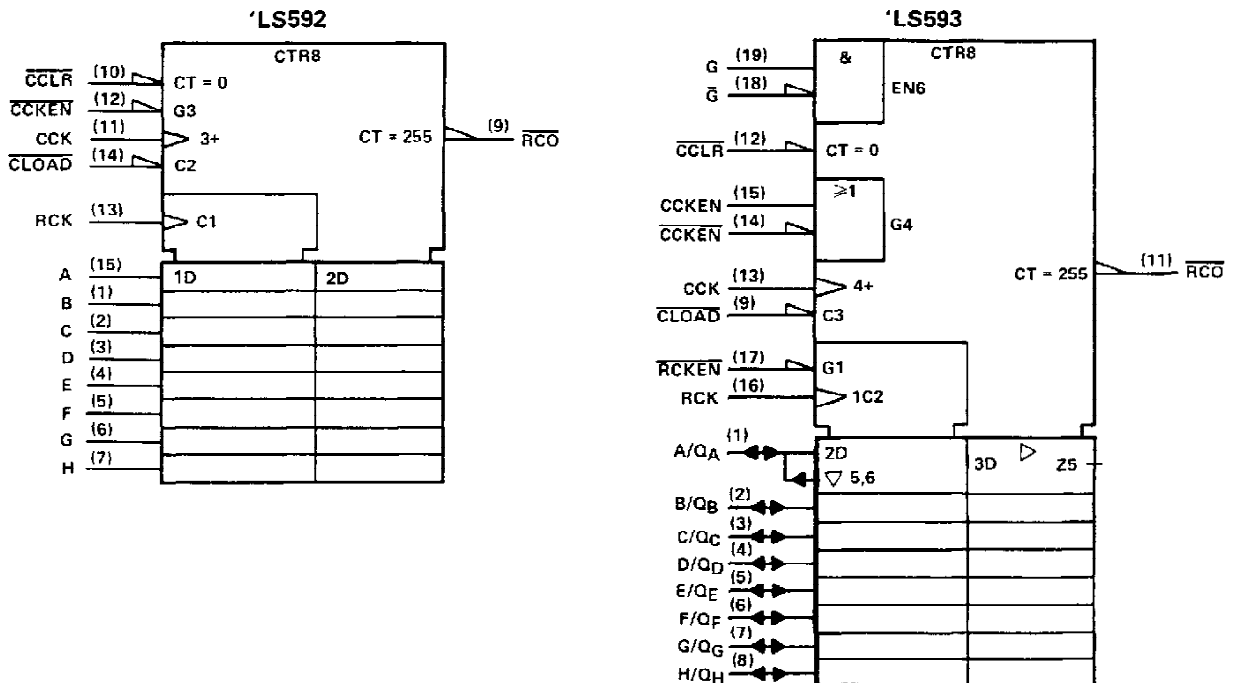
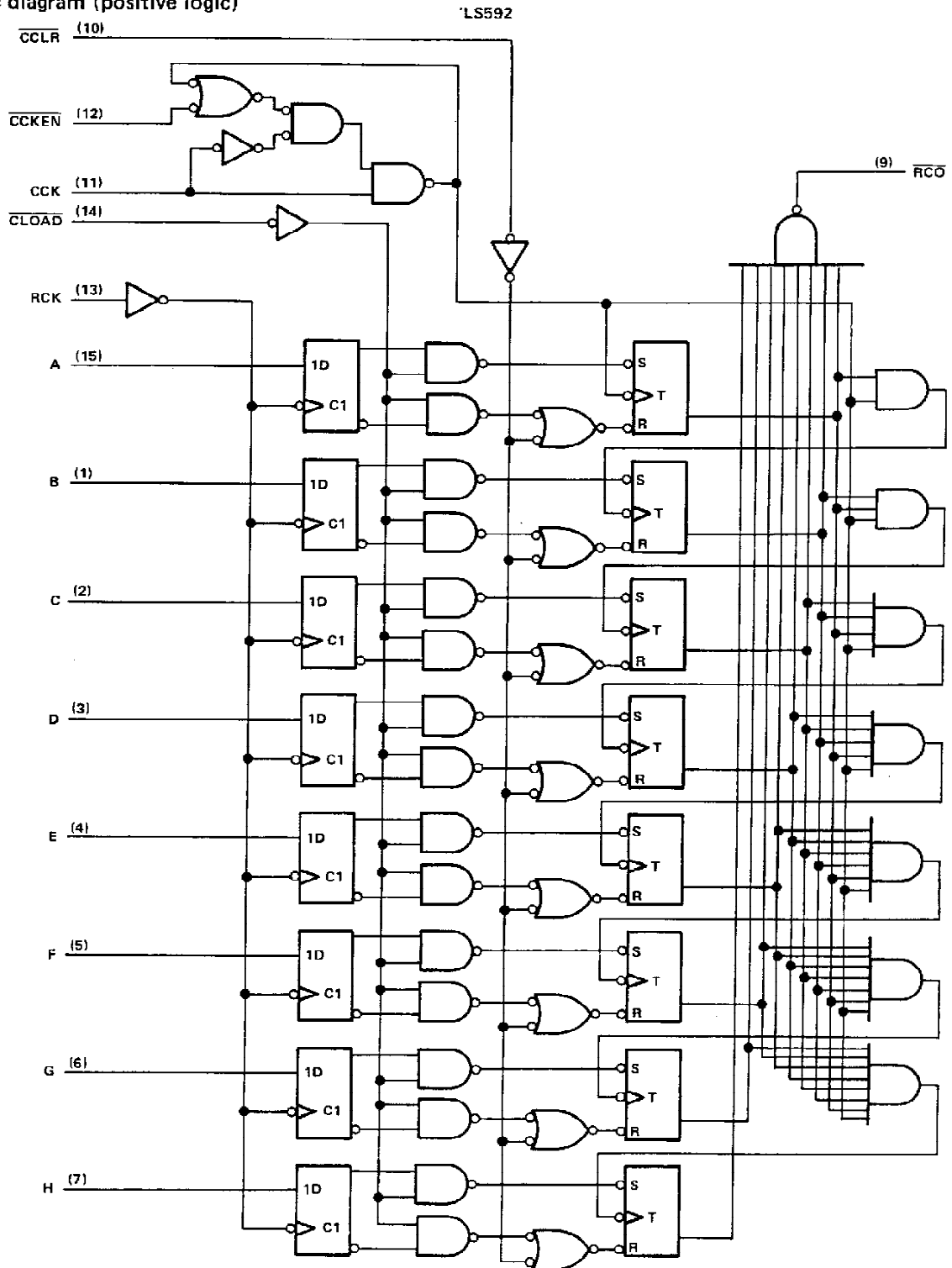† These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, J, N, and W packages.

logic diagram (positive logic)

'LS592

$\overline{CCLR}$ (10)

$\overline{CCKEN}$ (12)

CCK (11)

$\overline{CLOAD}$ (14)

RCK (13)

A (15)

B (1)

C (2)

D (3)

E (4)

F (5)

G (6)

H (7)

(9) $\overline{RCO}$

1D
C1

S
T
R

Pin numbers shown are for J, N, and W packages.

logic diagram (positive logic)

'LS593

Gating for RCK
is similar in detail
to that shown for
CCK.
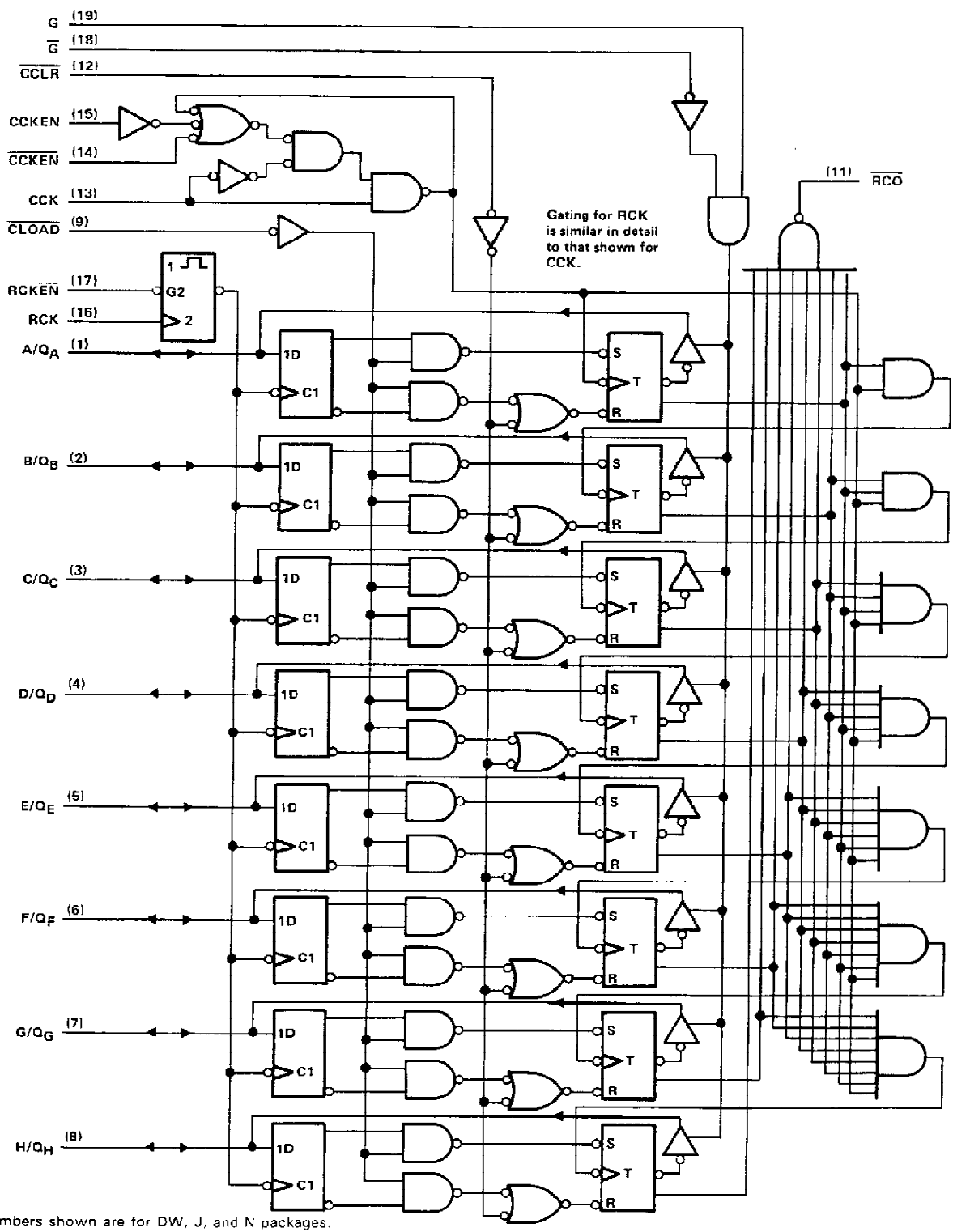
Pin numbers shown are for DW, J, and N packages.

typical operating sequences
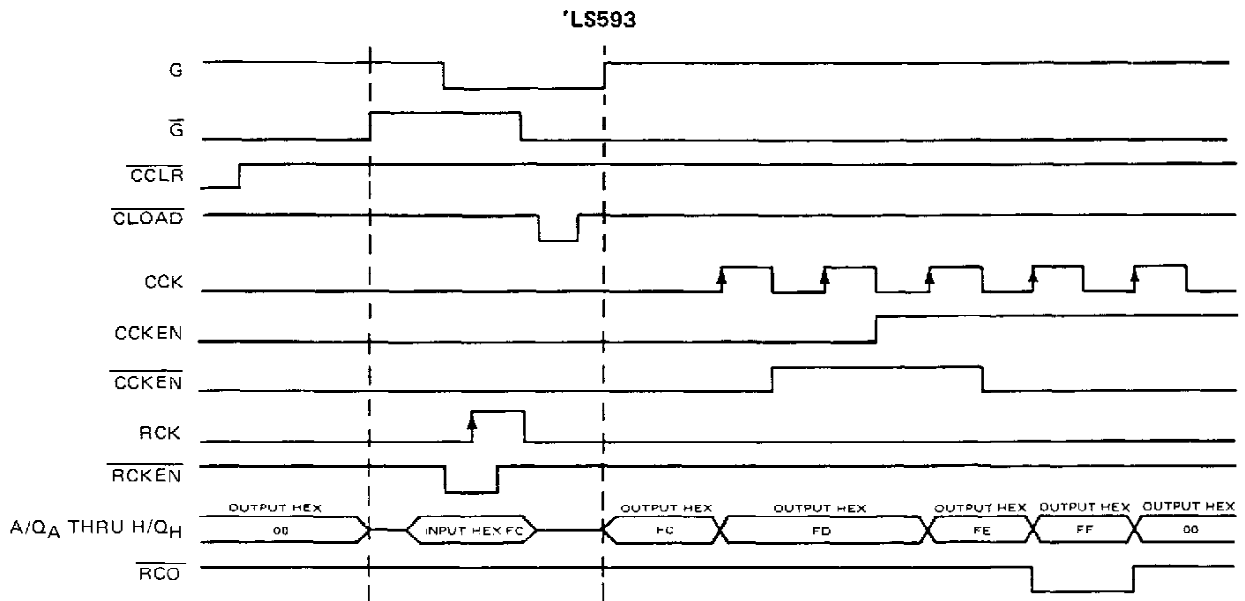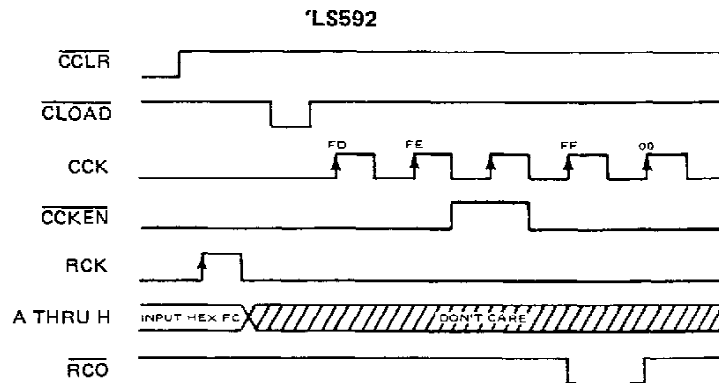
'LS592

$\overline{CCLR}$	
$\overline{CLOAD}$	
CCK	FD FE FF 00
$\overline{CCKEN}$	
RCK	
A THRU H	INPUT HEX FC / DON'T CARE
$\overline{RCO}$	

'LS593

G	
$\overline{G}$	
$\overline{CCLR}$	
$\overline{CLOAD}$	
CCK	
CCKEN	
$\overline{CCKEN}$	
RCK	
$\overline{RCKEN}$	
A/Q_A THRU H/Q_H	OUTPUT HEX 00 / INPUT HEX FC / OUTPUT HEX FC / OUTPUT HEX FD / OUTPUT HEX FE / OUTPUT HEX FF / OUTPUT HEX 00
$\overline{RCO}$	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (excluding I/O ports) .... 7 V
Off-state output voltage (including I/O ports) .... 5.5 V
Operating free-air temperature range: SN54LS592, SN54LS593 .... $-55°C$ to $125°C$
                              SN74LS592, SN74LS593 .... $0°C$ to $70°C$
Storage temperature range .... $-65°C$ to $150°C$

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

			SN54LS'			SN74LS'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
I_{OH}	High-level output current	$\overline{RCO}$			-1			-1	mA
		Q 'LS593 only			-1			-2.6	
I_{OL}	Low-level output current	$\overline{RCO}$			8			16	mA
		Q 'LS593 only			12			24	
f_{CCK}	Counter clock frequency		0		20	0		20	MHz
$t_{w (CCK)}$	Duration of counter clock pulse		25			25			ns
$t_{w (\overline{CCLR})}$	Duration of counter clear pulse		20			20			ns
$t_{w (RCK)}$	Duration of register clock pulse		20			20			ns
$t_{w (\overline{CLOAD})}$	Duration of counter load pulse		40			40			ns
t_{su}	Register enable setup time	$\overline{RCKEN}$ low to RCK ↑, 'LS593	20			20			ns
t_{su}	Counter enable setup time before CCK ↑	$\overline{CCKEN}$ low, 'LS592	30			30			ns
		$\overline{CCKEN}$ low or CCKEN high, 'LS593	30			30			
t_{su}	Setup time	$\overline{CCLR}$ inactive before CCK ↑	20			20			ns
		$\overline{CLOAD}$ inactive before CCK ↑	20			20			
		RCK ↑ before CLOAD ↑ (see Note 2)	30			30			
		Data A thru H before RCK ↑	20			20			
t_h	Hold time	Data A thru H after RCK ↑	0			0			ns
		All others	0			0			
T_A	Operating free-air temperature		-55		125	0		70	°C

NOTE 2: This time insures the data saved by RCK ↑ will also be loaded into the counter.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS' MIN	TYP‡	MAX	SN74LS' MIN	TYP‡	MAX	UNIT
V_{IK}			V_{CC} = MIN, I_I = -18 mA				-1.5			-1.5	V
V_{OH}	'LS593 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = -1 mA	2.4	3.2					V
				I_{OH} = -2.6 mA				2.4	3.1		
	$\overline{RCO}$			I_{OH} = -1 mA	2.4	3.2		2.4	3.2		
V_{OL}	'LS593 Q		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 24 mA					0.35	0.5	
	$\overline{RCO}$			I_{OL} = 8 mA		0.25	0.4		0.25	0.4	
				I_{OL} = 16 mA					0.35	0.5	
I_{OZH}	'LS593 Q		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 2.7 V				20			20	μA
I_{OZL}	'LS593 Q		V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = MAX, V_O = 0.4 V				-0.4			-0.4	mA
I_I	'LS593 Q		V_{CC} = MAX	V_I = 5.5 V			0.1			0.1	mA
	Others			V_I = 7 V			0.1			0.1	
I_{IH}			V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	CCK		V_{CC} = MAX, V_I = 0.4 V				-0.8			-0.8	mA
	RCK	'LS592					-0.2			-0.2	
		'LS593					-0.8			-0.8	
	A thru H						-0.4			-0.4	
	Others						-0.2			-0.2	
I_{OS}§	'LS593 Q		V_{CC} = MAX, V_O = 0 V		-30		-130	-30		-130	mA
	$\overline{RCO}$				-20		-100	-20		-100	
I_{CC}	'LS592	I_{CCH}	V_{CC} = MAX, All possible inputs grounded, All outputs open			40	60		40	60	mA
		I_{CCL}				40	60		40	60	
	'LS593	I_{CCH}				47	70		47	70	
		I_{CCL}				53	80		53	80	
		I_{CCZ}				57	85		57	85	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		'LS592			'LS593		UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	CCK	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF	20	35		20	35		MHz
t_{PLH}	CCK↑	Q						14	21	ns
t_{PHL}	CCK↑	Q						26	39	ns
t_{PLH}	$\overline{CLOAD}$↓	Q						34	51	ns
t_{PHL}	$\overline{CLOAD}$↓	Q						28	42	ns
t_{PHL}	$\overline{CCLR}$↓	Q	R_L = 667 Ω, C_L = 45 pF					25	38	ns
t_{PZH}	G↑	Q						31	47	ns
t_{PZL}	G↑	Q						27	40	ns
t_{PZH}	$\overline{G}$↓	Q						29	45	ns
t_{PZL}	$\overline{G}$↓	Q						31	47	ns
t_{PHZ}	G↓	Q						33	50	ns
t_{PLZ}	G↓	Q	R_L = 667 Ω, C_L = 5 pF					35	52	ns
t_{PHZ}	$\overline{G}$↑	Q						26	39	ns
t_{PLZ}	$\overline{G}$↑	Q						28	42	ns
t_{PLH}	CCK↑	$\overline{RCO}$		15	23		14	21		ns
t_{PHL}	CCK↑	$\overline{RCO}$		20	30		20	30		ns
t_{PLH}	$\overline{CLOAD}$↓	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF	31	47		31	47		ns
t_{PHL}	$\overline{CLOAD}$↓	$\overline{RCO}$		27	41		27	41		ns
t_{PLH}	$\overline{CCLR}$↓	$\overline{RCO}$		30	45		30	45		ns
t_{PLH}	RCK↑	$\overline{RCO}$	R_L = 1 kΩ, C_L = 30 pF	35	53		42	63		ns
t_{PHL}	RCK↑	$\overline{RCO}$	$\overline{CLOAD}$ = L	30	45		33	50		ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8762101EA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples
5962-8762101FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
5962-8762101FA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
SN54LS592J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS592J	Samples
SN54LS592J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS592J	Samples
SN54LS593J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS593J	Samples
SN54LS593J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54LS593J	Samples
SN74LS592D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS592	Samples
SN74LS592N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS592N	Samples
SN74LS592N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS592N	Samples
SN74LS592NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS592	Samples
SN74LS592NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS592	Samples
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS593	Samples
SN74LS593DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS593	Samples
SN74LS593N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS593N	Samples
SN74LS593N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS593N	Samples
SNJ54LS592J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54LS592J	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101EA SNJ54LS592J	Samples
SNJ54LS592W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
SNJ54LS592W	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8762101FA SNJ54LS592W	Samples
SNJ54LS593J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS593J	Samples
SNJ54LS593J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SNJ54LS593J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS592, SN54LS593, SN74LS592, SN74LS593 :

- Catalog : SN74LS592, SN74LS593

- Military : SN54LS592, SN54LS593

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS592NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LS593DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS592NSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LS593DWR	SOIC	DW	20	2000	367.0	367.0	45.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8762101FA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LS592D	D	SOIC	16	40	507	8	3940	4.32
SN74LS592N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS592N	N	PDIP	16	25	506	13.97	11230	4.32
SN74LS593N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54LS592W	W	CFP	16	25	506.98	26.16	6220	NA

C

SEATING PLANE

0.1 C

8.2 / 7.4 TYP

A

PIN 1 ID AREA

1

16

14X 1.27

10.4 / 10.0 NOTE 3

2X 8.89

8

9

16X 0.51 / 0.35

2.00 MAX

B

5.4 / 5.2 NOTE 4

⊕ 0.25 Ⓜ C A B

SEE DETAIL A

0.15 TYP

0.25

GAGE PLANE

0° - 10°

0.3 / 0.1

1.05 / 0.55

(1.25)

DETAIL A
TYPICAL

4220735/A   12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

16X (1.85)

SYMM

SEE DETAILS

1

16

16X (0.6)

SYMM

14X (1.27)

8

9

(R0.05) TYP

(7)

LAND PATTERN EXAMPLE
SCALE:7X

METAL

SOLDER MASK OPENING

SOLDER MASK OPENING

METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A   12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM

16X (1.85)

1

16X (0.6)

14X (1.27)

16

SYMM

8

9

(R0.05) TYP

(7)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A   12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0.394 (10,00)
0.386 (9,80)
⚠C

16   9

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)   ⚠D

1   8

Pin 1
Index Area

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)

⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−6/M   06/11

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         ⚠C   Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
         ⚠D   Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
         E.   Reference JEDEC MS−012 variation AC.

NS (R-PDSO-G**)   PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

PINS ** DIM	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R−GDIP−T**)   CERAMIC DUAL IN−LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°−15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. This package is hermetically sealed with a ceramic lid using glass frit.
        D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
        E. Falls within MIL STD 1835 GDIP1−T14, GDIP1−T16, GDIP1−T18 and GDIP1−T20.

W (R−GDFP−F16)   CERAMIC DUAL FLATPACK

Base and Seating Plane

0.045 (1,14)
0.026 (0,66)

0.285 (7,24)
0.245 (6,22)

0.080 (2,03)
0.055 (1,40)

0.008 (0,20)
0.004 (0,10)

0.305 (7,75) MAX

1   16

0.019 (0,48)
0.015 (0,38)

0.430 (10,92)
0.370 (9,40)

0.050 (1,27)

0.005 (0,13) MIN
4 Places

8   9

0.360 (9,14)
0.250 (6,35)

0.360 (9,14)
0.250 (6,35)

4040180−3/F 04/14

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   This package can be hermetically sealed with a ceramic lid using glass frit.
         D.   Index point is provided on cap for terminal identification only.
         E.   Falls within MIL STD 1835 GDFP2−F16

J (R—GDIP—T**)
14 LEADS SHOWN

CERAMIC DUAL IN—LINE PACKAGE

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

$\dfrac{0.065\ (1,65)}{0.045\ (1,14)}$

0.005 (0,13) MIN

$\dfrac{0.060\ (1,52)}{0.015\ (0,38)}$

A

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

$\dfrac{0.026\ (0,66)}{0.014\ (0,36)}$

0.100 (2,54)

0°—15°

$\dfrac{0.014\ (0,36)}{0.008\ (0,20)}$

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

N (R−PDIP−T**)
16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM	PINS **	14	16	18	20
A MAX		0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN		0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION		AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) /D\

0.045 (1,14)
0.030 (0,76) /D\

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option /D\

/C\

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
     /C\ Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
     /D\ The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63 / 9.97 TYP

A

PIN 1 ID
AREA

1

20

18X 1.27

13.0
12.6
NOTE 3

2X
11.43

10

11

B

7.6
7.4
NOTE 4

20X 0.51 / 0.31

⊕ 0.25Ⓜ C A B

C

SEATING PLANE

⌒ 0.1 C

2.65 MAX

SEE DETAIL A

0.33 / 0.10 TYP

0.25
GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A   05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

![Texas Instruments logo]
TEXAS INSTRUMENTS
www.ti.com

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

11

10

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.