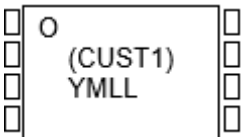
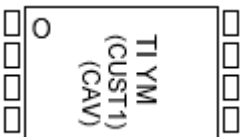


<b>PCN Number:</b>	20240510000.2			<b>PCN Date:</b>	May 13, 2024
<b>Title:</b>	Qualification of MLA as an additional Assembly & Test site for select devices				
<b>Customer Contact:</b>	Change Management team		<b>Dept:</b>	Quality Services	
<b>Proposed 1<sup>st</sup> Ship Date:</b>	November 09, 2024		<b>Sample Requests accepted until:</b>	June 12, 2024	
<b>*Sample requests received after June 12, 2024 will not be supported.</b>					
<b>Change Type:</b>					
<input checked="" type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Material
<input checked="" type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Process
<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>	Mechanical Specification	<input checked="" type="checkbox"/>	Test Site	<input type="checkbox"/>	Wafer Fab Material
<input checked="" type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input type="checkbox"/>	Wafer Fab Process
<b>PCN Details</b>					
<b>Description of Change:</b>					
Texas Instruments Incorporated is announcing the qualification of MLA as an additional Assembly & Test site for set of devices listed below. Material differences between sites as follows:					
<b>Group 1 Device:</b>					
	<b>ASESH</b>	<b>HFTF</b>	<b>TIEMA</b>	<b>UTL2</b>	<b>MLA</b>
Wire diam/type	1.0mil Au	0.8mil, 1.0mil Au 0.8mil, 1.0mil Cu	1.0mil Au	1.3mil Au	0.8mil, 1.0mil, 1.3mil Cu, 0.96mil Au
Mount compound	EY1000063	A-18	8075531	PZ0013	4147858
Mold compound	EN2000515	R-30	8096859	CZ0094	4211880
Wafer thickness	203um	190um	215.9um	203um	190um
Lead finish	NiPdAu	NiPdAu, Matte Sn	Matte Sn	NiPdAu	NiPdAu
Device marking	TI logo, pin 1 dot, backside marking*	TI logo*, pin 1 dimple, backside marking*	Pin 1 dimple	Pin 1 dimple, backside marking	TI letter, pin 1 dot, Mold cavity ID, no backside marking
MSL level	2, 1	2, 1	1	3	1
* - Not all devices have TI logo/backside marking included in the symbolization, but for the ones that do, the proposed change applies in MLA.					
<b>Group 2 Device:</b>					
	<b>ASESH</b>	<b>MLA</b>			
Wire diam/type	1.0mil Au	1.0mil Cu, 0.96mil Au			
Mount compound	EY1000063	4147858			
Mold compound	EN2000515	4226323			
Lead finish	NiPdAu	NiPdAu			
Wafer thickness	203um	190um			
Device marking	Pin1 dot, backside marking	TI letter, Mold cavity ID, pin 1 dimple, no backside marking			
MSL level	2	1			
<b>Group 3 Device:</b>					

	<b>ASESH</b>	<b>MLA</b>
Wire diam/type	1.0mil Au	1.0mil Cu
Mount compound	EY1000063	4147858
Mold compound	EN2000515	4211880
Lead finish	NiPdAu	NiPdAu
Wafer thickness	203um	190um
Device marking		
MSL level	2	1

Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ.

#### Reason for Change:

Supply continuity

- 1) To align with world technology trends and use wiring with enhanced mechanical and electrical properties
- 2) Maximize flexibility within our Assembly/Test production sites.
- 3) Cu is easier to obtain and stock

#### Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

#### Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

<b>RoHS</b>	<b>REACH</b>	<b>Green Status</b>	<b>IEC 62474</b>
<input checked="" type="checkbox"/> No Change	<input checked="" type="checkbox"/> No Change	<input checked="" type="checkbox"/> No Change	<input checked="" type="checkbox"/> No Change

#### Changes to product identification resulting from this PCN:

<b>Assembly Site</b>	<b>Assembly Site Origin (22L)</b>	<b>Assembly Country Code (23L)</b>	<b>Assembly City</b>
ASESH	ASH	CHN	Shanghai
HFTF	HFT	CHN	Hefei
TIEMA	CU6	MYS	Melaka
UTL2	NSE	THA	Bangkok
MLA	MLA	MYS	Kuala Lumpur

Sample product shipping label (not actual product label)



MADE IN: Malaysia  
2DC: 2Q:

MSL 2 / 260C/1 YEAR SEAL DT  
MSL 1 / 235C/UNLIM 03/29/04

OPT:  
ITEM: 39  
LBL: 5A (L)T0:1750



G4

(1P) SN74LS07NSR  
(Q) 2000 (D) 0336  
(31T) LOT: 3959047MLA  
(4W) TKY (1T) 7523483SI2  
(P)  
(2P) REV: (V) 003317  
(20L) CSO: SHE (21L) CCO:USA  
(22L) ASO: MLA (23L) ACO: MYS

#### Group 1 Product Affected:

OPA2170AQDGKRQ1	LM393LVQDGKRQ1	LMV822Q1MM/NOPB	LM74610QDGKTQ1
OPA2171AQDGKRQ1	TLV1702AQDGKRQ1	LMV822Q1MMX/NOPB	LM74670QDGKRQ1
OPA2313QDGKRQ1	TLV3202AQDGKRQ1	OPA2991QDGKRQ1	LM74670QDGKTQ1
OPA2316QDGKQ1	TLV7032QDGKRQ1	SN1907029QDGKRQ1	INA200AQDGKRQ1
OPA2316QDGKRQ1	TLV7042QDGKRQ1	TLV9002QDGKRQ1	INA201AQDGKRQ1
TLV2313QDGKRQ1	TLV9022QDGKRQ1	TLV9062QDGKRQ1	INA202AQDGKRQ1
TLV2316QDGKRQ1	TLV9032QDGKRQ1	TLV9152QDGKRQ1	INA2180A1QDGKRQ1
TLV2316QDGKTQ1	LM2904BAQDGKRQ1	TLV9352QDGKRQ1	INA2180A2QDGKRQ1
TLV6002QDGKRQ1	LM2904BHQDGKRQ1	TSV912AQDGKRQ1	INA2180A3QDGKRQ1
OPA2180QDGKRQ1	LM2904BQDGKRQ1	OPA2607QDGKRQ1	INA2180A4QDGKRQ1
OPA2188AQDGKRQ1	LM2904BRQDGKRQ1	OPA2836QDGKRQ1	TMP275AQDGKRQ1
OPA2197QDGKRQ1	LM2904BTQDGKRQ1	INA333QDGKRQ1	TMP75AQDGKRQ1
TLV2197QDGKRQ1	LM2904LVQDGKRQ1	LMV842QMM/NOPB	TPS61085ATDGKRQ1
TMP75BQDGKRQ1	LMV358AQDGKRQ1	LMV842QMMX/NOPB	TPS61085ATDGKTQ1
TMP75CQDGKRQ1	LMV358Q1MM/NOPB	OPA1641AQDGKRQ1	TPS560200QDGKRQ1
TMUX6219DGKRQ1	LMV358Q1MMX/NOPB	OPA1662AIDGKRQ1	TPS560200QDGKTQ1
TMUX7219DGKRQ1	LMV358Q3MM/NOPB	OPA2377QDGKRQ1	
TCA9517DGKRQ1	LMV358Q3MMX/NOPB	OPA2388QDGKRQ1	
LM2903BQDGKRQ1	LMV722QDGKRQ1	LM74610QDGKRQ1	

**Group 2 Product Affected:**

OPA2192QDGKRQ1	OPA2376QDGKRQ1
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**Group 3 Product Affected:**

INA225AQDGKRQ1	TMP175AQDGKRQ1
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# **Qualification Results** **Automotive Qualification Summary** **(As per AEC-Q100 Rev. J and JEDEC Guidelines)** Approve Date 03-May-2024

Product Attributes					
Attributes	Qual Device: LMP8278DGKZRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV842QMA/NOPB
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Logic	Logic	Logic	Signal Chain
Wafer Fab Supplier	MAINEFAB	RFAB	RFAB	RFAB	MAINEFAB
Assembly Site	MLA	MLA	MLA	MLA	TIEMA
Package Group	VSSOP	VSSOP	VSSOP	VSSOP	SOIC
Package Designator	DGK	DGS	DGS	DGS	D
Pin Count	8	20	20	20	8

QBS: Qual By Similarity - See Note which applies to Qual Device and all affected products in PCN  
 Qual Device LMP8278DGKZRQ1 is qualified at MSL1 260C

## **Qualification Results** Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: LMP8278DGKZRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV842QMA/NOPB
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	1/Pass	1/Pass	1/Pass	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	1/77/0	1/77/0	1/77/0	-
AC/uHAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	1/77/0	1/77/0	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	1/77/0	1/77/0	1/77/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	1/5/0	1/5/0	1/5/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	Note 1	1/45/0	1/45/0	1/45/0	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 2	1/77/0	-	-	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 3	-	-	-	3/2400/0
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-	-	-	-
Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: LMP8278DGKZRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV842QMA/NOPB
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 4	-	-	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDb	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

#### Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

#### E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Note 1: HAST and HSTL Package QBS is same Mold, Die attach and Wire package attributes and the manufacturing site is qualified with 3 lots.

Note 2: HTOL Process QBS is same silicon process technology family qualified with 3 lots.

Note 3: ELFR Process QBS is same wafer process technology qualified with 3 lots and generic data allowed per AEC Q100-008.

Note 4: One lot is allowed per AEC-Q100: A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

## Qualification Results

### Automotive Qualification Summary

**(As per AEC-Q100 Rev. J and JEDEC Guidelines)**

Approve Date 03-May-2024

#### Product Attributes

Attributes	Qual Device: <u>OPA2197QDGKRQ1</u>	QBS Process Reference: <u>INA301A2QDGKRQ1</u>	QBS Process Reference: <u>INA301A1QDGKRQ1</u>	QBS Process Reference: <u>INA301A3QDGKRQ1</u>	QBS Package Reference: <u>PCM1794AQDBRQ1</u>
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Signal Chain	Signal Chain	Signal Chain	Signal Chain
Wafer Fab Supplier	AIZU	AIZU	AIZU	AIZU	TSMC-WF3
Assembly Site	MLA	ASESHAT	ASESHAT	ASESHAT	MLA
Package Group	VSSOP	VSSOP	VSSOP	VSSOP	SSOP
Package Designator	DGK	DGK	DGK	DGK	DB
Pin Count	8	8	8	8	28

QBS: Qual By Similarity - See Note which applies to Qual Device and all affected products in PCN  
Qual Device OPA2197QDGKRQ1 is qualified at MSL1 260C

#### Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>OPA2197QDGKRQ1</u>	QBS Process Reference: <u>INA301A2QDGKRQ1</u>	QBS Process Reference: <u>INA301A1QDGKRQ1</u>	QBS Process Reference: <u>INA301A3QDGKRQ1</u>	QBS Package Reference: <u>PCM1794AQDBRQ1</u>
<b>Test Group A - Accelerated Environment Stress Tests</b>												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	-	-	-	3/Pass
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	-	-	-	3/231/0
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	-	-	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	-	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	1/45/0	-	-	-	-
<b>Test Group B - Accelerated Lifetime Simulation Tests</b>												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	150C	408 Hours	Note 2	1/77/0	1/77/0	1/77/0	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	150C	24 Hours	Note 3	1/800/0	1/800/0	1/800/0	-



Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	1/15/0	-	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-	-	-	-
Test Group D - Die Fabrication Reliability Tests												
EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDD8	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 4	1/30/0	1/30/0	1/30/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

#### **Ambient Operating Temperature by Automotive Grade Level:**

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

#### **E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

Note 1: HAST Package QBS is same Mold, Die attach and Wire package attributes and the manufacturing site is qualified with 3 lots.

Note 2: HTOL Process QBS is same silicon process technology family qualified with 3 lots.

Note 3: ELFR Process QBS is same wafer process technology qualified with 3 lots and generic data allowed per AEC Q100-008.

Note 4: One lot is allowed per AEC-Q100: A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.

# Qualification Results

## Automotive Qualification Summary

(As per AEC-Q100 Rev. J and JEDEC Guidelines)

Approve Date 01-May-2024

### Product Attributes

Attributes	Qual Device: TLV9032QDGKRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV393QDRQ1
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Signal Chain	Logic	Logic	Logic	Signal Chain
Wafer Fab Supplier	RFAB	RFAB	RFAB	RFAB	RFAB
Assembly Site	MLA	MLA	MLA	MLA	MLA
Package Group	VSSOP	VSSOP	VSSOP	VSSOP	SOIC
Package Designator	DGK	DGS	DGS	DGS	D
Pin Count	8	20	20	20	8

QBS: Qual By Similarity - See Note which applies to Qual Device and all affected products in PCN  
Qual Device TLV9032QDGKRQ1 is qualified at MSL1 260C

### Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: TLV9032QDGKRQ1	QBS Package Reference: SN74LV244AQDGSRQ1	QBS Package Reference: SN74LV273AQDGSRQ1	QBS Package Reference: SN74LV541AQDGSRQ1	QBS Process Reference: LMV393QDRQ1
Test Group A - Accelerated Environment Stress Tests												
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	3/Pass	3/Pass	3/Pass	3/Pass	-
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	Note 1	1/77/0	1/77/0	1/77/0	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Autoclave	121C/15psig	96 Hours	-	1/77/0	1/77/0	1/77/0	-
ACU/HAST	A3	JEDEC JESD22-A102/JEDEC JESD22-A118	3	77	Unbiased HAST	130C/85%RH	96 Hours	3/231/0	-	-	-	-
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	1/77/0	1/77/0	1/77/0	-
TC-BP	A4	MIL-STD883 Method 2011	1	5	Post Temp Cycle Bond Pull	-	-	1/5/0	1/5/0	1/5/0	1/5/0	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temperature Storage Life	150C	1000 Hours	Note 1	1/45/0	1/45/0	1/45/0	-
Test Group B - Accelerated Lifetime Simulation Tests												
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test	125C	1000 Hours	Note 2	1/77/0	-	-	3/231/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate	125C	48 Hours	Note 3	-	-	-	3/2400/0
Test Group C - Package Assembly Integrity Tests												
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	-	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB Solderability	>95% Lead Coverage	-	Note 4	1/15/0	-	-	-
SD	C3	JEDEC J-STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	Note 4	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk>1.67	-	3/30/0	-	-	-	-
Test Group D - Die Fabrication Reliability Tests												

EM	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDD8	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
HCI	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
BTI	D4	-	-	-	Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group E - Electrical Verification Tests												
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0 Note 5	-	-	-	-

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles

#### **Ambient Operating Temperature by Automotive Grade Level:**

Grade 0 (or E): -40C to +150C

Grade 1 (or Q): -40C to +125C

Grade 2 (or T): -40C to +105C

Grade 3 (or I) : -40C to +85C

#### **E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):**

Room/Hot/Cold : HTOL, ED

Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room : AC/uHAST

Quality and Environmental data is available at TI's external Web site: <http://www.ti.com/>

TI Qualification ID: R-CHG-2302-026

Note 1: HAST and HSTL Package QBS is same package attributes and the manufacturing site is qualified with 3 lots.

Note 2: HTOL Process QBS is same silicon process technology family qualified with 3 lots.

Note 3: ELFR Process QBS is same wafer process technology qualified with 3 lots and generic data allowed per AEC Q100-008.

Note 4: SD Package QBS has same leadframe attributes and the manufacturing site is qualified with 1 lot.

Note 5: One lot is allowed per AEC-Q100: A1.5.1 Multiple Sites - When the specific product or process attribute to be qualified or requalified will affect more than one wafer fab site or assembly site, a minimum of one lot of testing per affected site is required.



# Qualification Results

## Automotive Qualification Summary

### (As per AEC and JEDEC Guidelines)

#### Q006 VSSOP at MLA

Approve Date 01-May-2024

#### Product Attributes

Attributes	QBS Package Reference: <u>SN74LV244AQDGSRQ1</u>	QBS Package Reference: <u>SN74LV273AQDGSRQ1</u>	QBS Package Reference: <u>SN74LV541AQDGSRQ1</u>
Automotive Grade Level	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125
Product Function	Logic	Logic	Logic
Wafer Fab Supplier	RFAB	RFAB	RFAB
Assembly Site	MLA	MLA	MLA
Package Group	VSSOP	VSSOP	VSSOP
Package Designator	DGS	DGS	DGS
Pin Count	20	20	20

Qual Device SN74LV244AQDGSRQ1 is qualified at MSL1 260C

Qual Device SN74LV273AQDGSRQ1 is qualified at MSL1 260C

Qual Device SN74LV541AQDGSRQ1 is qualified at MSL1 260C

#### Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>SN74LV244AQDGSRQ1</u>	Qual Device: <u>SN74LV273AQDGSRQ1</u>	Qual Device: <u>SN74LV541AQDGSRQ1</u>
Test Group A - Accelerated Environment Stress Tests										
PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	MSL1 260C	-	1/Pass	1/Pass	1/Pass
PC	A1.1	-	3	22	SAM Precon Pre	Review for delamination	-	1/22/0	1/22/0	1/22/0
PC	A1.2	-	3	22	SAM Precon Post	Review for delamination	-	1/22/0	1/22/0	1/22/0
HAST	A2.1	JEDEC JESD22-A110	3	77	Biased HAST	130C/85%RH	96 Hours	1/77/0	1/77/0	1/77/0
HAST	A2.1.2	-	3	1	Cross Section, post bHAST, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HAST	A2.1.3	-	3	3	Wire Bond Shear, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.1.4	-	3	3	Bond Pull over Stitch, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.1.5	-	3	3	Bond Pull over Ball, post bHAST, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2	JEDEC JESD22-A110	3	70	Biased HAST	130C/85%RH	192 Hours	1/77/0	1/77/0	1/77/0
HAST	A2.2.1	-	3	22	SAM Analysis, post bHAST 2X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
HAST	A2.2.2	-	3	1	Cross Section, post bHAST, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HAST	A2.2.3	-	3	3	Wire Bond Shear, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0

Type	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: <u>SN74LV244AQDGSRQ1</u>	Qual Device: <u>SN74LV273AQDGSRQ1</u>	Qual Device: <u>SN74LV541AQDGSRQ1</u>
HAST	A2.2.4	-	3	3	Bond Pull over Stitch, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
HAST	A2.2.5	-	3	3	Bond Pull over Ball, post bHAST, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	1/77/0	1/77/0
TC	A4.1.1	-	3	22	SAM Analysis, post TC 1X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
TC	A4.1.2	-	3	1	Cross Section, post TC, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
TC	A4.1.3	-	3	3	Wire Bond Shear, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1.4	-	3	3	Bond Pull over Stitch, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.1.5	-	3	3	Bond Pull over Ball, post TC, 1X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2	JEDEC JESD22-A104 and Appendix 3	3	70	Temperature Cycle	-65C/150C	1000 Cycles	1/77/0	1/77/0	1/77/0
TC	A4.2.1	-	3	22	SAM Analysis, post TC, 2X	Review for delamination	Completed	1/22/0	1/22/0	1/22/0
TC	A4.2.2	-	3	1	Cross Section, post TC, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
TC	A4.2.3	-	3	3	Wire Bond Shear, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2.4	-	3	3	Bond Pull over Stitch, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
TC	A4.2.5	-	3	3	Bond Pull over Ball, post TC, 2X	Post stress	-	1/3/0	1/3/0	1/3/0
HTSL	A6.1	JEDEC JESD22-A103	3	45	High Temperature Storage Life	150C	1000 Hours	1/45/0	1/45/0	1/45/0
HTSL	A6.1.1	-	3	1	Cross Section, post HTSL, 1X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
HTSL	A6.2	JEDEC JESD22-A103	3	44	High Temperature Storage Life	150C	2000 Hours	1/45/0	1/45/0	1/45/0
HTSL	A6.2.1	-	3	1	Cross Section, post HTSL, 2X	Post stress cross section	Completed	1/1/0	1/1/0	1/1/0
Test Group C - Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	1/30/0	1/30/0	1/30/0

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ZVEI ID: SEM-PA-07, SEM-PA-08, SEM-PA-11, SEM-PA-13, SEM-PA-18, SEM-PS-04, SEM-TF-01

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