LMK04714-Q1 Automotive Grade Ultra-Low-Noise JESD204B/C Dual-Loop Clock Jitter Cleaner

1 Features

- AEC-Q100 Grade 1: –40°C to 125°C
- Maximum clock output frequency: 3255 MHz
- Multi-mode: dual PLL, single PLL, and clock distribution
- 6-GHz external VCO or distribution input
- Ultra-low noise, at 2500 MHz:
  - 54-fs RMS jitter (12 kHz to 20 MHz)
  - 64-fs RMS jitter (100 Hz to 20 MHz)
  - –157.6-dBc/Hz noise floor
- Ultra-low noise, at 3200 MHz:
  - 61-fs RMS jitter (12 kHz to 20 MHz)
  - 67-fs RMS jitter (100 Hz to 100 MHz)
  - –156.5-dBc/Hz noise floor
- PLL2
  - PLL FOM of –230 dBc/Hz
  - PLL 1/f of –128 dBc/Hz
  - Phase detector rate up to 320 MHz
  - Two integrated VCOs: 2440 to 2600 MHz and 2945 to 3255 MHz
- Up to 14 differential device clocks
  - CML, LVPECL, LCPECL, HSDS, LVDS, and 2xLVCMOS programmable outputs
- Up to 1 buffered VCXO/XO output
  - LVPECL, LVDS, 2xLVCMOS programmable
- 1-1023 CLKOUT integer divider
- 1-8191 SYSREF integer divider
- 25-ps step analog delay for SYSREF clocks
- Digital delay and dynamic digital delay for device clocks and SYSREF
- Holdover mode with PLL1
- 0-delay with PLL1 or PLL2
- High Reliability
  - Controlled Baseline
  - One Assembly/Test Site
  - One Fabrication Site
  - Extended Product Life Cycle
  - Extended Product-Change Notification
  - Product Traceability

2 Applications

- Automotive Radar
- Data Converter Clocking
- LIDAR

3 Description

The LMK04714-Q1 is a high performance clock conditioner with JEDEC JESD204B/C support for space applications.

The 14 clock outputs from PLL2 can be configured to drive seven JESD204B/C converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. Not limited to JESD204B/C applications, each of the 14 outputs can be individually configured as high-performance outputs for traditional clocking systems.

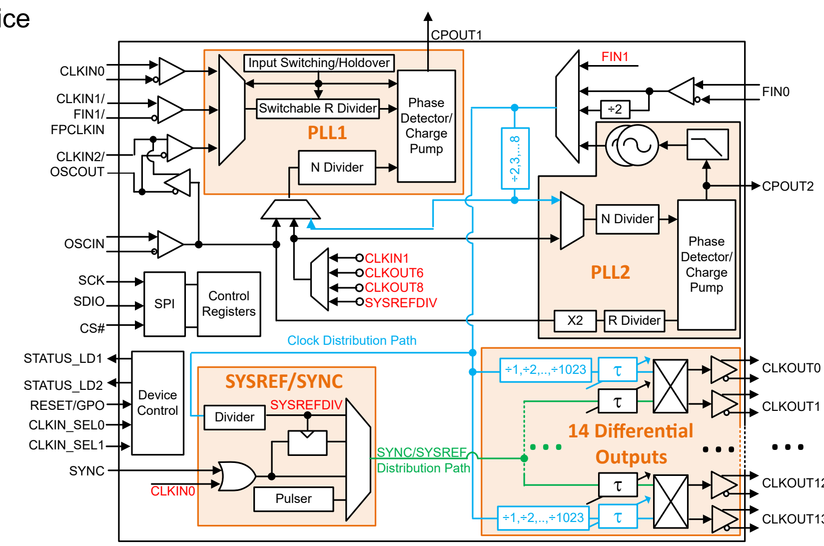
This device can be configured for operation in dual PLL, single PLL, or clock distribution modes with or without SYSREF generation or reclocking. PLL2 may operate with either internal or external VCO.

The high performance combined with features like the ability to trade off between power and performance, dual VCOs, dynamic digital delay, and holdover allows to provide flexible high performance clocking trees.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LMK04714-Q1	PAP (HTQFP, 64)	12 mm × 12 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 Pin Configuration and Functions

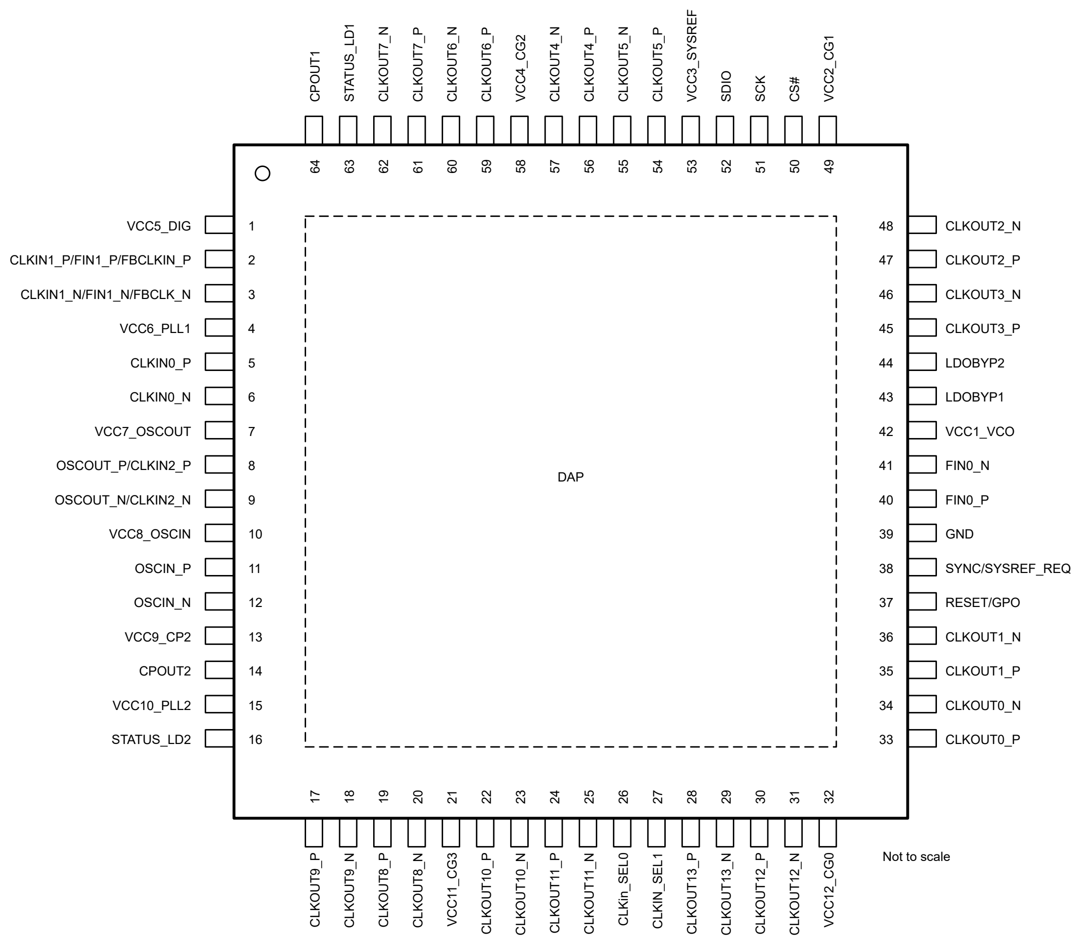


Figure 5-1. PAP Package 64-Pin HTQFP Top View

Table 5-1. Pin Functions

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
1	VCC5_DIG	–	PWR	Power supply for the digital circuitry.
2	CLKIN1_P/ FIN1_P/ FBCLKIN_P	I	ANLG	CLKIN1_P: Reference Clock input port 1 for PLL1. FIN1_P: External VCO input or clock distribution input. FBCLKIN_P: Feedback input for external clock feedback input (0–delay mode).

Table 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
3	CLKIN1_N	I	ANLG	Reference Clock input port 1 for PLL1.
	FIN1_N			External VCO input or clock distribution input.
	FBCLK_N			Feedback input for external clock feedback input (0–delay mode).
4	VCC6_PLL1	–	PWR	Power supply for PLL1, charge pump 1, holdover DAC
5	CLKIN0_P	I	ANLG	Reference Clock input port 0 for PLL1.
6	CLKIN0_N			
7	VCC7_OSCOUT	–	PWR	Power supply for OSCOUT pins.
8	OSCOUT_P	I/O	Programmable	Buffered output of OSCIN pins
	CLKIN2_P			Reference Clock input port 2 for PLL1.
9	OSCOUT_N	I/O	Programmable	Buffered output of OSCIN pins
	CLKIN2_N			Reference Clock input port 2 for PLL1.
10	VCC8_OSCIN	–	PWR	Power supply for OSCIN
11	OSCIN_P	I	ANLG	Feedback to PLL1 and reference input to PLL2. AC-coupled.
12	OSCIN_N			
13	VCC9_CP2	–	PWR	Power supply for PLL2 charge pump.
14	CPOUT2	O	ANLG	Charge pump 2 output.
15	VCC10_PLL2	–	PWR	Power supply for PLL2.
16	STATUS_LD2	I/O	Programmable	Programmable status pin.
17	CLKOUT9_P	O	Programmable	Clock output 9. For JESD204B/C systems suggest SYSREF Clock. [(1)] Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
18	CLKOUT9_N			
19	CLKOUT8_P	O	Programmable	Clock output 8. For JESD204B/C systems suggest Device Clock. [(1)] Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
20	CLKOUT8_N			
21	VCC11_CG3	–	PWR	Power supply for clock outputs 8, 9, 10, and 11.
22	CLKOUT10_P	O	Programmable	Clock output 10. For JESD204B/C systems suggest Device Clock. [(1)] Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
23	CLKOUT10_N			
24	CLKOUT11_P	O	Programmable	Clock output 11. For JESD204B/C systems suggest SYSREF Clock. [(1)] Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
25	CLKOUT11_N			
26	CLKin_SEL0	I/O	Programmable	Programmable status pin.
27	CLKIN_SEL1	I/O	Programmable	Programmable status pin.
28	CLKOUT13_P	O	Programmable	Clock output 13. For JESD204B/C systems suggest SYSREF Clock. [(1)] Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
29	CLKOUT13_N			
30	CLKOUT12_P	O	Programmable	Clock output 12. For JESD204B/C systems suggest Device Clock.[(1)] Programmable formats: CML, LVPECL, LCPECL, or LVDS.
31	CLKOUT12_N			
32	VCC12_CG0	–	PWR	Power supply for clock outputs 0, 1, 12, and 13.
33	CLKOUT0_P	O	Programmable	Clock output 0. For JESD204B/C systems suggest Device Clock.[(1)] Programmable formats: CML, LVPECL, LCPECL, or LVDS.
34	CLKOUT0_N			
35	CLKOUT1_P	O	Programmable	Clock output 1. For JESD204B/C systems suggest SYSREF Clock. Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
36	CLKOUT1_N			
37	RESET/GPO	I	CMOS	Device reset input or GPO
38	SYNC/ SYSREF_REQ	I	CMOS	Synchronization input or SYSREF_REQ for requesting continuous SYSREF.
39	GND	–	GND	This pin should be grounded.

Table 5-1. Pin Functions (continued)

PIN		I/O	TYPE	DESCRIPTION
NO.	NAME			
40	FIN0_P	I	ANLG	High-speed input for external VCO or clock distribution. Supports /2 for frequency greater than 3250 MHz.
41	FIN0_N			
42	VCC1_VCO	–	PWR	Power supply for VCO and clock distribution.
43	LDOBYP1	–	ANLG	LDO Bypass, bypassed to ground with 10-μF capacitor.
44	LDOBYP2	–	ANLG	LDO Bypass, bypassed to ground with a 0.1-μF capacitor.
45	CLKOUT3_P	O	Programmable	Clock output 3. For JESD204B/C systems suggest SYSREF Clock. (1) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
46	CLKOUT3_N			
47	CLKOUT2_P	O	Programmable	Clock output 2. For JESD204B/C systems suggest Device Clock. Programmable formats: CML, LVPECL, LCPECL, or LVDS.
48	CLKOUT2_N			
49	VCC2_CG1	–	PWR	Power supply for clock outputs 2 and 3.
50	CS#	I	CMOS	Chip Select
51	SCK	I	CMOS	SPI Clock
52	SDIO	I/O	CMOS	SPI Data
53	VCC3_SYSREF	–	PWR	Power supply for SYSREF divider and SYNC.
54	CLKOUT5_P	O	Programmable	Clock output 5. For JESD204B/C systems suggest SYSREF Clock. (1) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
55	CLKOUT5_N			
56	CLKOUT4_P	O	Programmable	Clock output 4. For JESD204B/C systems suggest Device Clock.(1) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
57	CLKOUT4_N			
58	VCC4_CG2	–	PWR	Power supply for clock outputs 4, 5, 6 and 7.
59	CLKOUT6_P	O	Programmable	Clock output 6. For JESD204B/C systems suggest Device Clock.(1) Programmable formats: CML, LVPECL, LCPECL, or LVDS.
60	CLKOUT6_N			
61	CLKOUT7_P	O	Programmable	Clock output 7. For JESD204B/C systems suggest SYSREF Clock. (1) Programmable formats: CML, LVPECL, LCPECL, LVDS, or 2xLVCMOS.
62	CLKOUT7_N			
63	STATUS_LD1	I/O	Programmable	Programmable status pin.
64	CPOUT1	O	ANLG	Charge pump 1 output.
DAP	DAP	–	GND	DIE ATTACH PAD, connect to GND.

(1) Actual best allocation of device clocks and SYSREF depends upon frequency planning to group common frequencies.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	PARAMETER	MIN	MAX	UNIT
V_{DD}, V_{DD_A}	Power supply voltage	–0.3	3.6	V
V_{IN}	Input voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Differential input current (CLKIN_P/N, OSCIN_P/N,FIN0_P/N,FIN1_P/N		5	mA
T_J	Junction Temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

	PARAMETER	CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over case temperature range (unless otherwise noted)

	PARAMETER	MIN	NOM	MAX	UNIT
V_{DD}	IO supply voltage	3.135	3.3	3.465	V
V_{DD_A}	Core supply voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	–40		125	°C

6.4 Thermal Information

	THERMAL METRIC[1]	PAP (HTQFP)	UNIT
		64 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	6.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

VDD, VDD_A = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 125°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Current Consumption							
I_{CC}	Power Down Supply Current	Device Powered Down			3.3	5	mA
	Supply Current[1]	PLL1 locked to external VCXO and PLL2 locked to internal VCO	4 CML 32 mA clocks in bypass 3 LVDS clock /12 4 SYSREF as LCPECL 3 SYSREF as LVDS		980		mA
			4 CML 32 mA clocks in bypass 3 LVDS clock /12 4 SYSREF as LCPECL (low state) 3 SYSREF as LVDS (low state)		850		mA
			4 CML 32 mA clocks in bypass 3 LVDS clock /12 7 SYSREF outputs powered down		700		mA
CLKIN Specifications							
f_{CLKINx}	LOS Circuitry	LOS_EN = 1		0.001		125	MHz
	PLL1	CLKinX-TYPE = 1 (MOS)	AC Coupled Input	0.001		250	MHz
		CLKinX-TYPE = 0 (Bipolar)	AC Coupled Input	0.001		750	MHz
	PLL2	CLKinX_TYPE = 0 (Bipolar)	AC Coupled Input	0.001		500	MHz
	0-delay	0-delay with external feedback (CLKIN1)	AC Coupled Input	0.001		750	MHz
	Distribution Mode	CLKIN1/FIN1 Pin only	AC Coupled Input	0.001		3250	MHz
$SLEW_{CLKIN}$	Input Slew Rate[2]			0.15	0.5		V/ns
$V_{CLKINx/FIN1}$	Single-ended clock input voltage	Input pin AC coupled; complementary pin AC coupled to GND		0.5		2.4	Vpp
V_{ID}CLKINx/ FIN1	Differential clock input voltage[3]	AC coupled		0.125		1.55	|V|
V_{SS}CLKINx/ FIN1				0.25		3.1	Vpp
|V_{CLKINx}-offset|	DC offset voltage between CLKINx_P /CLKINx_N. Each Pin AC Coupled	CLKIN0/1/2 (Bipolar)			0		|mV|
		CLKIN0/1 (MOS)			55		|mV|
		CLKIN2 (MOS)			20		|mV|
V_{CLKIN}VIH	High Input Voltage	V_{CLKIN} – V_{IH}	DC Coupled Input	2		Vcc	V
V_{CLKIN}VIL	Low Input Voltage	V_{CLKIN} – V_{IL}	DC Coupled Input	0		0.4	V
FIN0 Input Pin							
f_{FIN0}	External Input Frequency	AC Coupled Slew Rate > 150 V/us	FIN0_DIV2_EN = 1	1		3250	MHz
f_{FIN0}			FIN0_DIV2_EN = 2	1		6400	MHz
V_{ID}FIN0	Differential Input Voltage	AC Coupled		0.125		1.55	Vpp
V_{SS}FIN0				0.25		3.1	Vpp

VDD, VDD_A = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 125°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
PLL 1 Specifications							
f_{PD1}	Phase Detector Frequency					40	MHz
PN10kHz	PLL Normalized 1/f Noise(4)	PLL1_CP_GAIN = 350 µA			–117		dBc/Hz
		PLL1_CP_GAIN = 1550 µA			–118		
PN FOM	PLL Figure of Merit(5)	PLL1_CP_GAIN = 350 µA			–221.5		
		PLL1_CP_GAIN = 1550 µA			–223		
I_{CPOUT1}	Charge Pump Current(6)	V_{CPout} = V_{CC}/2	PLL1_CP_GAIN = 0		50		µA
			PLL1_CP_GAIN = 1		150		
			PLL1_CP_GAIN = 2		250		
			PLL1_CP_GAIN = 4		450		
			PLL1_CP_GAIN = 8		850		
I_{CPOUT1}%MIS	Charge Pump Sink / Source Mismatch	V_{CPout1} = V_{CC}/2, T_A = 25°C	V_{CPout1} = V_{CC}/2, T_A = 25°C		1	10	%
$I_{CPOUT1}V_{TUNE}$	Magnitude of Charge Pump Current Variation versus Charge Pump Voltage	0.5 V < V_{CPout1} < V_{CC} – 0.5 V, T_A = 25°C	0.5 V < V_{CPout1} < V_{CC} – 0.5 V, T_A = 25°C		1	10	%
I_{CPOUT1}%TEMP	Charge Pump Current vs. Temperature Varation				2	10	%
I_{CPOUT1}TRI	Charge Pump TRI_STATE Leakage Current					10	nA
OSCIN Input							
f_{OSCIN}	EN_PLL2_REF_2X = 0			0.001		500	MHz
	EN_PLL2_REF_2X = 1			0.001		320	
$SLEW_{OSCIN}$	Input Slew Rate			0.15	0.5		V/ns
V_{OSCIN}	Input voltage for OSCIN_P or OSCIN_N	AC coupled; single-ended; unused pin AC coupled to GND		0.2		2.4	Vpp
V_{ID}OSCIN	Differential voltage swing(3)	AC coupled		0.2		1.55	|V|
V_{SS}OSCIN				0.4		3.1	Vpp
V_{CLKINx}Offset	DC offset voltage between CLKINx_P/CLKINx_N. Each Pin AC Coupled				20		mV
PLL 2 Specifications							
f_{PD}	Phase Detector Frequency					320	MHz
PN10kHz	PLL Normalized 1/f Noise(4)	PLL2_CP_GAIN = 1600 µA			–123		dBc/Hz
		PLL2_CP_GAIN = 3200 µA			–128		
PN FOM	PLL Figure of Merit(5)	PLL2_CP_GAIN = 1600 µA			–226.5		
		PLL2_CP_GAIN = 3200 µA			–230		
I_{CPOUT}	Charge Pump Current Magnitude(6)	V_{CPOUT} = V_{CC}/2	PLL2_CP_GAIN = 2		1600		µA
			PLL2_CP_GAIN=3		3200		
I_{CPOUT1}%MIS	Charge Pump Sink / Source Mismatch	V_{CPOUT} = V_{CC}/2, T = 25°C	V_{CPOUT1} = Vcc/2, T = 25°C		1	10	%
$I_{CPout1}V_{TUNE}$	Magnitude of Charge Pump Current Variation versus Charge Pump Voltage	0.5 V < V_{CPOUT1} < V_{CC} – 0.5 V, T_A = 25°C	0.5 V < V_{CPOUT1} < V_{CC} – 0.5 V, T_A = 25°C		2	10	%
I_{CPOUT}%TEMP	Charge Pump Current versus Temperature Variation				3	10	%
I_{CPOUT1}TRI	Charge Pump TRI_STATE Leakage Current					10	nA

VDD, VDD_A = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 125°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Internal VCO Specifications							
f_{VCO}	VCO Frequency Range		VCO0	2440		2600	MHz
			VCO1	2945		3255	MHz
K_{VCO}	VCO Tuning Sensitivity		VCO0		13		MHz/V
			VCO1		26		MHz/V
$\|\Delta T_{CL}\|$	Allowable temperature Drift for Continous Lock[7]		VCO0			150	ºC
	Allowable temperature Drift for Continous Lock[7]		VCO1			180	ºC
L(f)VCO	Open Loop VCO Phase Noise	VCO0 at 2440 MHz	10 kHz		–88.4		dBc/Hz
			100 kHz		–117		
			800 kHz		–137.5		
			1 MHz		–139.7		
			10 MHz		–152.6		
		VCO0 at 2580 MHz	10 kHz		–85.7		
			100 kHz		–115.8		
			800 kHz		–137		
			1 MHz		–138.6		
			10 MHz		–151.8		
L(f)VCO	Open Loop VCO Phase Noise	VCO1 at 2945 MHz	10 kHz		–82.6		dBc/Hz
			100 kHz		–112.3		
			800 kHz		–134.9		
			1 MHz		–137.2		
			10 MHz		–151.1		
		VCO1 at 3250 MHz	10 kHz		–81		
			100 kHz		–110.4		
			800 kHz		–134.3		
			1 MHz		–135.6		
			10 MHz		–149.3		
Output Clock Skew and Timing							
$SKEW_{CLKOUTX}$	Output to Output Skew	Same Pair of Device clocks and same format			35		ps
		Even to Even or Odd to Odd, Same Format			15		
		Even clock to Odd Clock			35		
Additive Jitter in Distribution Mode from FIN Pin (note 6)							
$L(f)_{CLKOUT}$	Additive jitter, Distribution mode with no divide	245.76 MHz Output Frequency, 12 kHz to 20 MHz integration bandwidth	LVCMOS		50		fs
			LVDS		50		
			LVPECL		40		
			LCPECL		35		
			HSDS		40		
			CML		35		

VDD, VDD_A = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 125°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
LVCMOS Outputs							
f_{CLKOUT}	Frequency		5 pF Load			250	MHz
$L(f)_{CLKOUT}$	Noise Floor	245.76 MHz	20 MHz Offset		–160		dBc/Hz
V_{OH}	Output High Voltage	1 mA load		Vcc – 0.1			V
V_{OL}	Output Low Voltage	1 mA load				0.1	V
I_{OH}	Output High Current	FD = 1.65 V			–28		mA
I_{OL}	Output Low Current	Vd = 1.65 V			28		mA
ODC	Output Duty Cycle				50		%
LVDS Clock Outputs							
$L(f)_{CLKOUT}$	Noise Floor	245.76 MHz output	20 MHz Offset		–159.5		dBc/Hz
T_R/T_F	20% to 80% Rise/Fall Time, f_{OUT}≥ 1 GHz				175		ps
V_{OD}	Differential Output Voltage	DC Measurement, AC coupled to receiver input R_L = 100 Ω differential			350		mV
ΔV_{OD}	Change in V_{OD} for complimentary output states			–60		60	mV
V_{OS}	Output Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change on VOS for complimentary Output states					35	mV
I_{SHORT}	Short circuit Output Current			–24		24	mA
LCPECL Clock Outputs							
$L(f)_{CLKOUT}$	Noise Floor	245.76 MHz output	20 MHz Offset		–162.5		dBc/Hz
T_R/T_F	20% to 80% Rise/Fall Time	f_{OUT} ≥ 1 GHz			135		ps
V_{OH}	Output High Voltage	DC Measurement with 50 Ω to 0.5 V			1.4		V
V_{OL}	Output Low Voltage				0.6		V
V_{OD}	Differential Output Voltage	DC Measurement with 50 Ω to 0.5 V			870		mV
LVPECL Clock Outputs							
$L(f)_{CLKOUT}$	Noise Floor	245.76 MHz output, LVPECL 2.0 V	20 MHz Offset		–163		dBc/Hz
T_R/T_F	20% to 80% Rise/Fall Time	f_{OUT} ≥ 1 GHz			135		ps
V_{OH}	Output High Voltage	DC Measurement termination 50 Ω to V_{CC} - 2 V	LVPECL 1.6 V		V_{CC} – 1		V
			LVPECL 2.0 V		V_{CC} – 1.1		
V_{OL}	Output Low Voltage		LVPECL 1.6 V		V_{CC} – 1.8		V
			LVPECL 2.0 V		V_{CC} – 2		
V_{OD}	Differential Output Voltage	2.5 GHz, Em = 120 Ω to GND, R_L = AC coupled 100 Ω	LVPECL 1.6 V		0.7		V
			LVPECL 2.0 V		0.9		
HSDS Clock Outputs							
$L(f)_{CLKOUT}$	Noise Floor	245.76 MHz output	20 MHz Offset		–162		dBc/Hz
T_R/T_F	20% to 80% Rise/Fall Time	f_{OUT} ≥ 1 GHz			170		ps

VDD, VDD_A = 3.3 V ± 5 %, –40°C ≤ T_A ≤ 125°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	Output High Voltage	DC Measurement with 50 Ω to 0.5 V	HSDS 6 mA		V_{CC} – 0.9		V
			HSDS 8 mA		V_{CC} – 1.0		
V_{OL}	Output Low Voltage		HSDS 6 mA		V_{CC} – 1.5		V
			HSDS 8 mA		V_{CC} – 1.7		
V_{OD}	Output Voltage	DC Measurement with 50 Ω to 0.5 V	HSDS 6 mA		0.5		V
			HSDS 8 mA		0.75		
ΔV_{OD}	Change on VOS for complimentary Output states		HSDS 6 mA	–80		80	mV
			HSDS 8 mA	–115		115	
CML Outputs							
$L(f)_{CLKOUT}$	Noise Floor	20 MHz Offset			–163		dBc/Hz
T_R/T_F	20% to 80% Rise/Fall Time	f_{OUT} ≥ 1.5 GHz	CML 16 mA		140		ps
			CML 24 mA		140		
			CML 32 mA		140		
V_{OH}	Output High Voltage	50 Ω pullup to V_{CC}, DC Measurement			V_{CC} – 1		V
V_{OL}	Output Low Voltage	50 Ω pullup to V_{CC}, DC Measurement	CML 16 mA		V_{CC} – 0.8		V
			CML 24 mA		V_{CC} – 0.1		
			CML 32 mA		V_{CC} – 1.4		
V_{OD}	Output Voltage	50 Ω pullup to V_{CC}, DC Measurement	CML 16 mA		680		mV
			CML 24 mA		1000		
			CML 32 mA		1300		
		50 Ω pullup to V_{CC}, DC Measurement, R_L = AC coupled 100 Ω, 250 MHz	CML 16 mA		550		mV
			CML 24 mA		815		
			CML 32 mA		1070		
Digital Outputs (CLKin_SELX,STATUS_LDX, and RESET/GPO,SDIO)							
V_{OH}	Output High Voltage			V_{CC} – 0.4			V
V_{OL}	Output Low Voltage					0.4	V
Digital Inputs							
V_{IH}	High-level input voltage			1.2			V
V_{IL}	Low-level input voltage					0.5	V
I_{IH}	High-level input current	RESET/GPO,SYNC,SCK,SDIO, CS#				80	uA
		SYNC	V_{IH} = V_{CC}			25	
I_{IL}	Low-level input current	CLKINX_SEL,RESET/GPO,SYNC,SCK,SDIO, CS#		–5		5	uA
I_{IL}	Low-level input current	SYNC	V_{IL} = 0 V	–5		5	

(1) Use the TICS Pro tool to calculate Icc for a specific configuration
(2) Device will function with slew rate as low as 0.15 V/ns, however a slew rate of 0.5 V/ns or higher is recommended to get the best phase noise performance.
(3) See Differential Voltage Measurement Terminology for definition of VID and VOD voltages.
(4) The normalized PLL 1/f noise is a specification in modeling PLL in-band phase noise is that is close to the carrier and has a characteristic 10 dB/decade slope. PN10 kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10 kHz = LPLL_flicker(10 kHz) - 20 log(f_{OUT}/ 1 GHz), where LPLL_flicker(f) is the single side band phase noise of only the flicker noise's

contribution to total noise, L(f). To measure LPLL_flicker(f) it is important to be on the 10 dB/decade slope close to the carrier. A high compare frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). LPLL_flicker(f) can be masked by the reference oscillator performance if a low-power or noisy source is used. The total PLL in-band phase noise performance is the sum of LPLL_flicker(f) and LPLL_flat(f)

(5) The PLL figure of merit is a normalized metric used to quantify the flat portion of the in-band phase noise. It is calculated as PN_FOM = LPLL_flat(f) - 20 log(N) - 10 log(f_{PDX}). LPLL_flat(f) is the single side band phase noise measured at an offset frequency, f, in a 1 Hz bandwidth and f_{PDX} is the phase detector frequency of the synthesizer. LPLL_flat(f) contributes to the total noise, L(f). This metric is measured using a CLKIN input. If the OSCin input is used, the metric is about 2 dB worse.

(6) This parameter is programmable to more states than are shown in the electrical specifications

(7) Maximum Allowable Temperature Drift for Continuous Lock is how far the temperature can drift in either direction from the value it was at the time that the 0x168 register was last programmed with PLL2_FCAL_DIS = 0, and still have the part stay in lock. The action of programming the 0x168 register, even to the same value, activates a frequency calibration routine. This implies the part will work over the entire frequency range, but if the temperature drifts more than the maximum allowable drift for continuous lock, then it will be necessary to reload the appropriate register to ensure it stays in lock. This parameter is indirectly tested.

6.6 Timing Requirements

VDD, VDD_A = 3.3 V ± 5 %, –55°C ≤ T_A ≤ 125°C. Typical values are at VDD = VDD_A = 3.3 V, 25°C (unless otherwise noted)

	PARAMETER	MIN	NOM	MAX	UNIT
Timing Requirements					
td_S	Setup time for SDI edge to SCK rising edge	40			ns
td_H	Hold time for SDI edge to SCK rising edge	20			ns
t_{SCK}	Period of SCK	400			ns
t_{HIGH}	High width of SCK	120			ns
t_{LOW}	Low width of SCK	120			ns
t_{CS}	Setup time for CS# falling edge to SCK rising edge	40			ns
t_{CH}	Hold time for CS# rising edge from SCK rising edge	40			ns
t_{DV}	SCK falling edge to valid read back data			120	ns

6.7 Timing Diagram

Register programming information on the SDIO pin is clocked into a shift register on each rising edge of the SCK signal. On the rising edge of the CS# signal, the register is sent from the shift register to the register addressed. A slew rate of at least 30 V/µs is recommended for these signals. After programming is complete the CS# signal should be returned to a high state. If the SCK or SDIO lines are toggled while the VCO is in lock, as is sometimes the case when these lines are shared with other parts, the phase noise may be degraded during this programming.

4-wire mode read back has same timing as SDIO pin.

R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read.

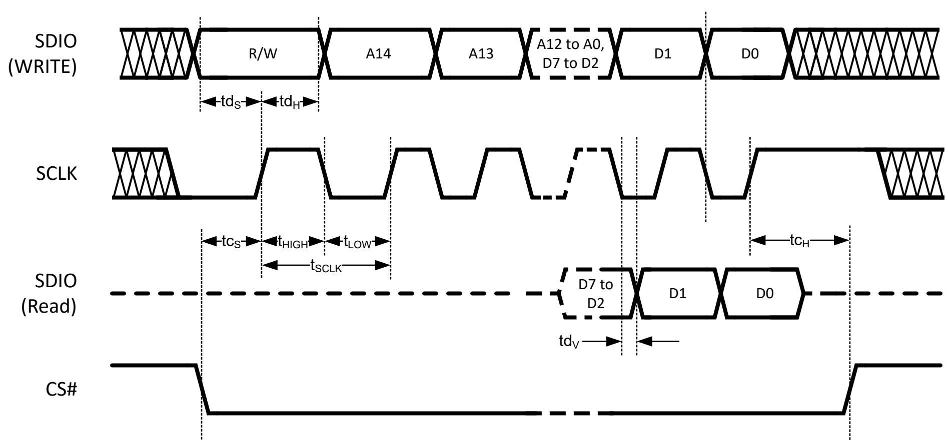
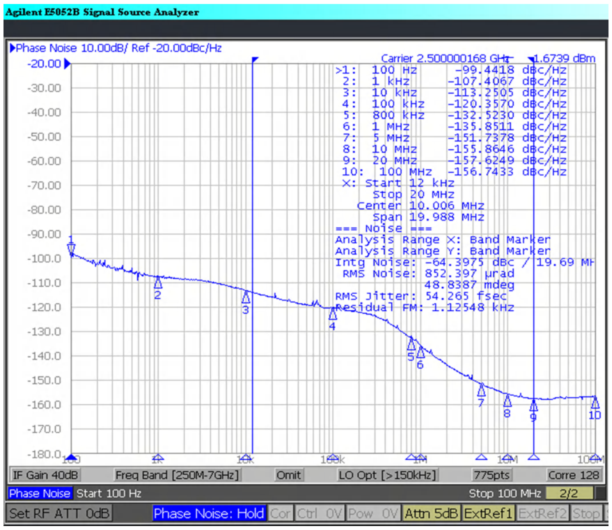


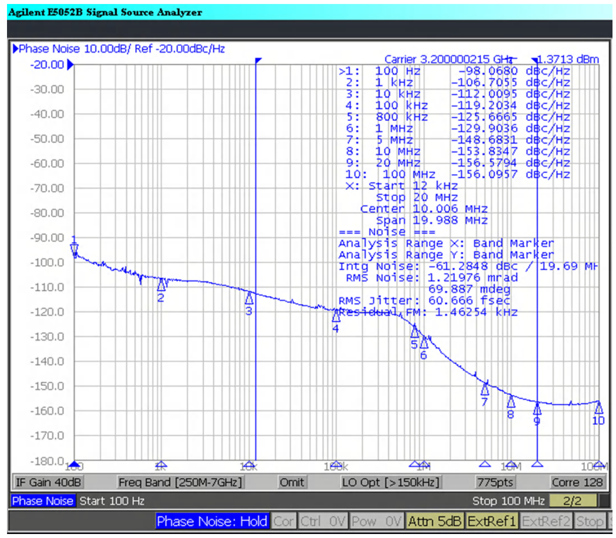
Figure 6-1. SPI Timing Diagram

6.8 Typical Characteristics



Jitter from 100 Hz to 100 MHz = 63.6 fs rms.
Output is CLKOUT4 as CML 32 mA with 68-nH to 20-Ω DC bias.
Other settings are CLKout4_5_IDL = 1 and CLKout4_5_BYP = 1.
PLL2 Loop Filter R2 = 470 Ω, C2 = 150 nF,
Charge Pump = 3200 µA.
Reference is R&S SMA100B Signal Generator with option SMAB - B711 through Prodyn BIB-100G Balun to OSCin.

Figure 6-2. PLL2 With VCO1 Performance at 2500 MHz With 312.5-MHz OSCin/Phase Detector Frequency

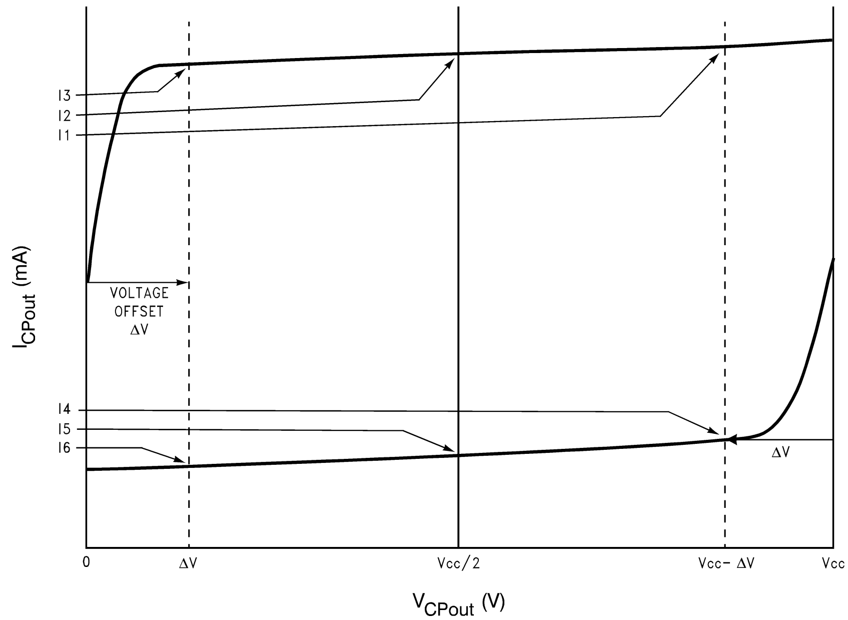


Jitter from 100 Hz to 100 MHz = 67 fs rms.
Output is CLKOUT4 as CML 32 mA with 68-nH to 20-Ω DC bias.
Other settings are CLKout4_5_IDL = 1 and CLKout4_5_BYP = 1.
PLL2 Loop Filter R2 = 470 Ω, C2 = 150 nF,
Charge Pump = 3200 µA.
Reference is R&S SMA100B Signal Generator with option SMAB - B711 through Prodyn BIB-100G Balun to OSCin.

Figure 6-3. PLL2 With VCO1 Performance at 3200 MHz With 320-MHz OSCin/Phase Detector Frequency

7 Parameter Measurement Information

7.1 Charge Pump Current Specification Definitions



I1 = Charge Pump Sink Current at $V_{CPout} = V_{CC} - \Delta V$
I2 = Charge Pump Sink Current at $V_{CPout} = V_{CC}/2$
I3 = Charge Pump Sink Current at $V_{CPout} = \Delta V$
I4 = Charge Pump Source Current at $V_{CPout} = V_{CC} - \Delta V$
I5 = Charge Pump Source Current at $V_{CPout} = V_{CC}/2$
I6 = Charge Pump Source Current at $V_{CPout} = \Delta V$
ΔV = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

7.1.1 Charge Pump Output Current Magnitude Variation vs Charge Pump Output Voltage

$$I_{CPout} \text{ Vs } V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

7.1.2 Charge Pump Sink Current vs Charge Pump Output Source Current Mismatch

$$I_{CPout} \text{ Sink Vs } I_{CPout} \text{ Source} = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

7.1.3 Charge Pump Output Current Magnitude Variation vs Ambient Temperature

$$I_{CPout} \text{ Vs } T_A = \frac{\left.|I_2|\right|_{T_A} - \left.|I_2|\right|_{T_A = 25°C}}{\left.|I_2|\right|_{T_A = 25°C}} \times 100\%$$

$$= \frac{\left.|I_5|\right|_{T_A} - \left.|I_5|\right|_{T_A = 25°C}}{\left.|I_5|\right|_{T_A = 25°C}} \times 100\%$$

7.2 Differential Voltage Measurement Terminology

The differential voltage of a differential signal can be described by two different definitions causing confusion when reading data sheets or communicating with other engineers. This section will address the measurement and description of a differential signal so that the reader will be able to understand and distinguish between the two different definitions when used.

The first definition used to describe a differential signal is the absolute value of the voltage potential between the inverting and noninverting signal. The symbol for this first measurement is typically V_{ID} or V_{OD} depending on if an input or output voltage is being described.

The second definition used to describe a differential signal is to measure the potential of the noninverting signal with respect to the inverting signal. The symbol for this second measurement is V_{SS} and is a calculated parameter. Nowhere in the IC does this signal exist with respect to ground, it only exists in reference to its differential pair. V_{SS} can be measured directly by oscilloscopes with floating references, otherwise this value can be calculated as twice the value of V_{OD} as described in the first description.

Figure 7-1 shows the two different definitions side-by-side for inputs and Figure 7-2 shows the two different definitions side-by-side for outputs. The V_{ID} and V_{OD} definitions show V_A and V_B DC levels that the noninverting and inverting signals toggle between with respect to ground. V_{SS} input and output definitions show that if the inverting signal is considered the voltage potential reference, the noninverting signal voltage potential is now increasing and decreasing above and below the noninverting reference. Thus the peak-to-peak voltage of the differential signal can be measured.

V_{ID} and V_{OD} are often defined as volts (V) and V_{SS} is often defined as volts peak-to-peak (V_{PP}).

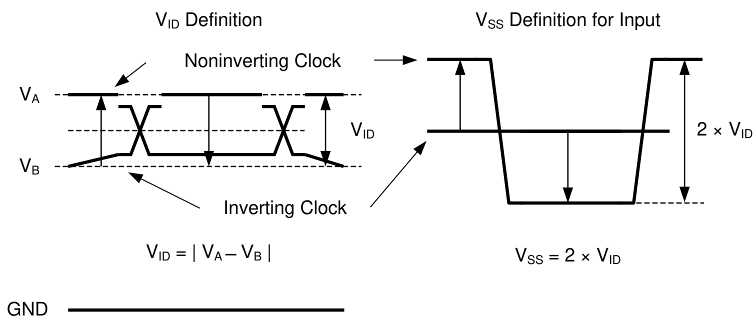


Figure 7-1. Two Different Definitions for Differential Input Signals

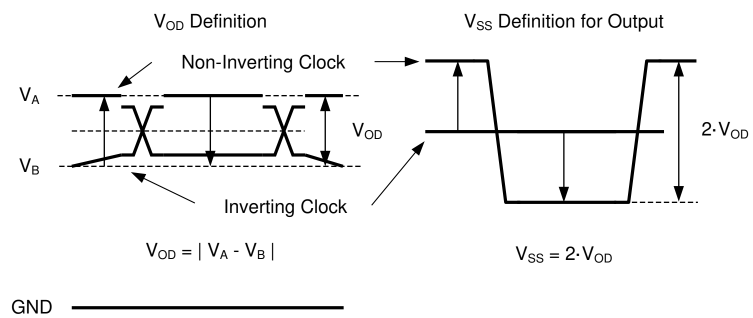


Figure 7-2. Two Different Definitions for Differential Output Signals

Refer to application note *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036) for more information.

8 Detailed Description

8.1 Overview

This device is very flexible to meet many application requirements. Use cases include dual loop, dual loop 0-delay nested, dual loop 0-delay cascaded, single loop, single loop 0-delay, and clock distribution.

The device may be used in JESD204B/C systems by providing a device clock and SYSREF to target devices, however traditional (non-JESD204B/C) systems are possible by programming pairs of outputs to share the clock divider or any mix of JESD204B/C and traditional outputs.

8.1.1 Differences from the LMK04832

The LMK04832 is a widely known device that is similar to this device. However, these devices are not the same and there are some differences.

Table 8-1. Differences Between the LMK04714-Q1 and LMK04832

Attribute	LMK04832	LMK04714-Q1
Automotive Qualification	No	AEC-Q100
Temperature	–40ºC to +85ºC	–40ºC to +125ºC
Package	9 × 9 mm	10 × 10 mm
Pin Rotation	n/a	Rotated 180° from LMK04832
6.4 GHz CLK/VCO Input Pin	No, Pins 8/9 are NC	Yes, Pins 40/41 are FIN0_P/FIN0_N
Pin After SYNC/SYSREFREQ Pin	NC (Pin 7)	GND (Pin 39)
Programming Speed	5 MHz	2.5 MHz

8.1.1.1 Jitter Cleaning

The dual loop PLL architecture provides the lowest jitter performance over a wide range of output frequencies and phase noise integration bandwidths. The first stage PLL (PLL1) is driven by an external reference clock and uses an external VCXO to provide a frequency accurate, low phase noise reference clock for the second stage frequency multiplication PLL (PLL2).

PLL1 typically uses a narrow loop bandwidth (typically 10 Hz to 200 Hz) to retain the frequency accuracy of the reference clock input signal while at the same time suppressing the higher offset frequency phase noise that the reference clock may have accumulated along its path or from other circuits. This cleaned reference clock provides the reference input to PLL2.

The low phase noise reference provided to PLL2 allows PLL2 to operate with a wide loop bandwidth (typically 50 kHz to 200 kHz). The loop bandwidth for PLL2 is chosen to take advantage of the superior high offset frequency phase noise profile of the internal VCO and the good low offset frequency phase noise of the reference VCXO.

Ultra-low jitter is achieved by allowing the phase noise of the external VCXO to dominate the final output phase noise at low offset frequencies and the phase noise of the internal VCO to dominate the final output phase noise at high offset frequencies. This results in best overall phase noise and jitter performance.

8.1.1.2 JEDEC JESD204B/C Support

This device clocks up to seven JESD204B/C targets using seven device clocks and seven SYSREF clocks and allows every clock output to be configured as a device clock or SYSREF clock.

8.1.2 Clock Inputs

Note

CLKIN1 can be used as a reference for dual loop, single loop, or clock distribution mode, providing flexibility configuring the device for different operation modes from one clock input.

8.1.2.1 Inputs for PLL1

CLKIN0, CLKIN1, and CLKIN2 are the three redundant inputs with their own PLL1 R dividers that can be used as a reference input to PLL1. The switching between these inputs can either be automatic or manual. For manual switching, CLKIN_SEL0 and CLKIN_SEL1 pins can be used for faster speed. These input pins are also shared for other functions.

- CLKIN1 is shared for use as an external 0-delay feedback (FBCLKIN), or for use with an external VCO (FIN).
- CLKIN2 is shared for use as OSCout. To use CLKIN2 as an input power down OSCout, see the *VCO_MUX, OSCout_MUX, OSCout_FMT* section.

8.1.2.2 Inputs for PLL2

In dual loop configurations, the PLL2 reference is from OSCin. However, in single PLL2 loop operation, it is also possible to use any of the three CLKIN inputs of PLL1 as a reference to PLL2.

8.1.2.3 Inputs When Using Clock Distribution Mode

For clock distribution mode, a reference signal may be applied to the FIN0 or FIN1 pins. CLKIN0 can be used to distribute a SYSREF signal through the device. In this use case, CLKIN0 is re-clocked by CLKIN1. The FIN0 pins are generally recommended over the FIN1 pins because they allow higher frequency, use a lower noise path, and cannot be used for other functions (like redundant input).

8.1.3 PLL1

PLL1 allows low offset jitter cleaning as well as the use of redundant inputs and frequency holdover.

8.1.3.1 Frequency Holdover

Frequency holdover keeps the clock outputs on frequency with minimum drift when the reference is lost until a valid reference clock signal is re-established. This can only be used if PLL1 is used.

8.1.3.2 External VCXO for PLL1

When PLL1 is used, an external VCXO is required. The close-in noise performance of this VCXO is critical for good jitter cleaning performance. The OSCout pin is powered on by default and gives a buffered copy of the PLL1 feedback and PLL2 reference input at OSCin. This reference input is typically a low noise VCXO or XO. This output can be used to clock external devices such as microcontrollers, FPGAs, CPLDs, and so forth, before the device is programmed.

- The OSCout buffer output type is programmable to LVDS, LVPECL, or LVCMOS.
- The VCXO buffered output can be synchronized to the VCO clock distribution outputs by using Cascaded 0-Delay Mode.

8.1.4 PLL2

8.1.4.1 Internal VCOs for PLL2

PLL2 has two internal VCOs. The output of the selected VCO is routed to the Clock Distribution Path. This same selection is also fed back to the PLL2 phase detector through a prescaler and N-divider.

8.1.4.2 External VCO Mode

An external VCO can be used with PLL2 with the input for the external VCO coming through FIN0 or FIN1, although FIN0 is generally preferred.

Note

The FIN0_P/FIN0_N input is generally recommended because it is lower noise, supports higher input frequency (up to 6 GHz if the div2 is used), and it leaves CLKIN1 available for redundant inputs.

FIN1_P/FIN1_N inputs are generally NOT recommended, for the reasons stated above, although they can be used.

8.1.5 Clock Distribution

There are a total of 14 PLL2 clock outputs driven from the internal or external VCO.

All clock outputs have programmable output types. They can be programmed to CML, LVPECL, LVDS, HSDS, or LCPECL. All odd clock outputs plus CLKOUT8 and CLKOUT10 may be programmed to LVCMOS.

In addition to these 14 clocks, there is also an additional OSCout output for a total of 15 differential output clocks. OSCout may be a buffered version of OSCIN, DCLKOUT6, DCLKOUT8, or SYSREF. Its output format is programmable to LVDS, LVPECL, or LVCMOS.

The following sections discuss specific features of the clock distribution channels that allow the user to control various aspects of the output clocks.

8.1.5.1 Clock Divider

There are seven clock dividers. In a traditional clocking system, each divider can drive two outputs. The divider range is 1 to 1023. Duty cycle correction may be enabled for the output. When the divider is used even clocks may not output CML.

In a JESD204B/C system, one clock output is a device clock driven from the clock divider and the other paired clock is from the SYSREF divider. For connectivity flexibility, either the even or odd clock output may be driven by the clock divider or be the SYSREF output.

8.1.5.2 High Performance Divider Bypass Mode

The even clock outputs (CLKOUT0/2/4/6/8/10/12) may bypass the clock divider to achieve the best possible noise floor and output swing. In this mode, the only usable output format is CML.

8.1.5.3 SYSREF Clock Divider

The SYSREF divider supports a divide range of 8 to 8191 (even and odd). There is no duty cycle correction for the SYSREF divider. The SYSREF output may be routed to all clock outputs.

8.1.5.4 Device Clock Delay

The device clocks support digital delay for phase adjustment of the clock outputs.

The digital delay allows outputs to be delayed from 8 to 1023 VCO cycles. The delay step can be as small as half the period of the clock distribution path. For example, a 3.2-GHz VCO frequency results in 156.25-ps steps.

The digital delay value takes effect on the clock output phase after a SYNC event.

8.1.5.5 Dynamic Digital Delay

The device clock dividers support a dynamic digital delay feature which allows the clock to be delayed by one full device clock cycle. With a single programming, an adjustment of up to 255 one cycle delays may occur. When making a multi-step adjustment, the adjustments are periodically applied to reduce impact to the clock.

Dynamic phase adjustments of half a clock distribution cycle are possible by half step.

The SYSREF digital delay value is reused for dynamic digital delay. To achieve a one cycle delay program the SYSREF digital delay value to one greater than half the SYSREF divide value.

8.1.5.6 SYSREF Delay: Global and Local

The SYSREF divider includes a digital delay block which allows a global phase shift with respect to the device clocks.

Each clock output pair includes a local SYSREF analog and digital delay for unique phase adjustment of each SYSREF clock.

The local analog delay allows for approximately 21-ps steps. Turning-on analog delay adds an additional 124 ps of delay in the clock path. The digital delay step can be as small as half the period of the clock distribution path. For example, a 3.2-GHz VCO frequency results in 156.25-ps steps.

The local digital delay and half step allows a SYSREF output to be delayed from 1.5 to 11 clock distribution path cycles.

8.1.5.7 Programmable Output Formats

All clock outputs can be programmed to an LVDS, HSDS, LVPECL, or LCPECL output type. Odd clock outputs in addition to CLKOUT8 and CLKOUT10 may also be programmed to LVCMOS. All odd clock outputs can also be programmed to CML. When in bypass mode the even clock output may only be CML.

The OSCout can be programmed to an LVDS, LVPECL, or LVCMOS output type.

Any HSDS output type can be programmed to 6-mA or 8-mA amplitude levels.

Any LVPECL output type can be programmed to 1600-mVpp or 2000-mVpp amplitude levels. The 2000-mVpp LVPECL output type is a Texas Instruments proprietary configuration that produces a 2000-mVpp differential swing for compatibility with many data converters and is also known as 2VPECL.

LCPECL allows for DC-coupling SYSREF to low voltage JESD204B/C targets.

8.1.5.8 Clock Output Synchronization

Using the SYNC input causes all active clock outputs to share a rising edge as programmed by fixed digital delay.

The SYNC event must occur for digital delay values to take effect.

8.1.6 0-Delay

Two types of 0-delay mode are supported.

1. Cascaded 0-delay
2. Nested 0-delay

Cascaded 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL2 input clock (OSCIN) to the phase of a clock output selected by the feedback mux. The 0-delay feedback uses internal feedback from the CLKOUT6, CLKOUT8, or SYSREF. The 0-delay feedback can also be from an external feedback through the FBCLKIN pins. The FB_MUX selects the feedback source. The OSCIN has a fixed deterministic phase relationship to the feedback clock, therefore OSCout will also have a fixed deterministic phase relationship to the feedback clock. In this mode, PLL1 input clock (CLKINx) also has a fixed deterministic phase relationship to PLL2 input clock (OSCIN); this results in a fixed deterministic phase relationship between all clocks from CLKINx to the clock outputs.

Nested 0-delay mode establishes a fixed deterministic phase relationship of the phase of the PLL1 input clock (CLKINx) to the phase of a clock output selected by the feedback mux. The 0-delay feedback uses internal feedback from the CLKOUT6, CLKOUT8, or SYSREF. The 0-delay feedback can also be from an external feedback through the FBCLKIN port. The FB_MUX selects the feedback source.

Without using 0-delay mode, there will be n possible fixed phase relationships from clock input to clock output depending on the clock output divide value.

Using an external 0-delay feedback reduces the number of available clock inputs by one.

8.1.7 Status Pins

The status pins can be monitored for feedback or in some cases used for input depending upon device programming. For example:

- The CLKin_SEL0 pin may indicate the LOS (loss-of-signal) for CLKIN0.
- The CLKin_SEL1 pin may be an input for selecting the active clock input.
- The Status_LD1 pin may indicate if the device is locked.
- The Status_LD2 pin may indicate if PLL2 is locked.

The status pins can be programmed to a variety of other outputs including PLL divider outputs, combined PLL lock detect signals, PLL1 Vtune railing, readback, and so forth. Refer to *Register Maps* for more information.

8.2 Functional Block Diagram

Figure 8-1 shows the high level block diagram.

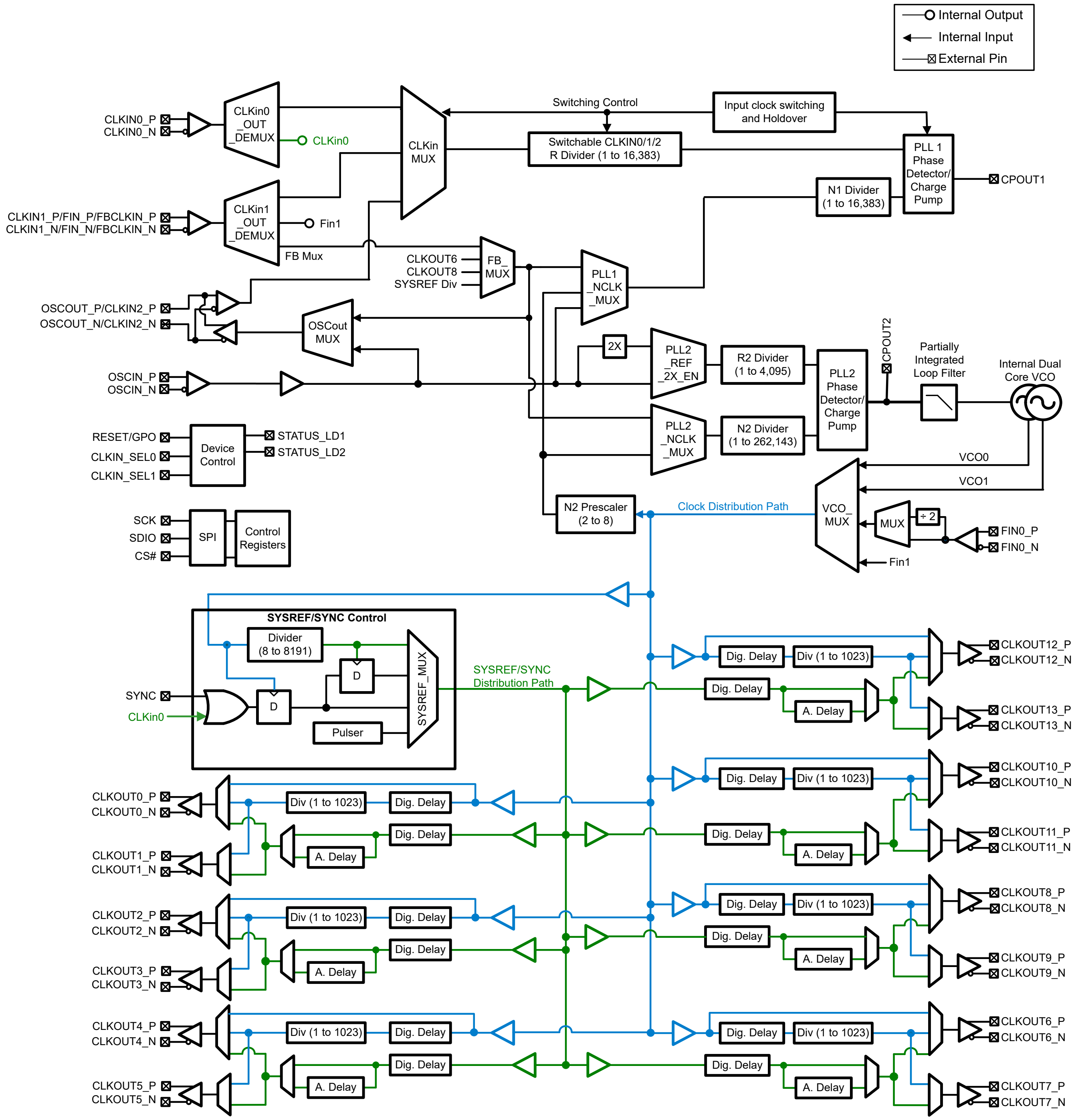


Figure 8-1. High Level Block Diagram

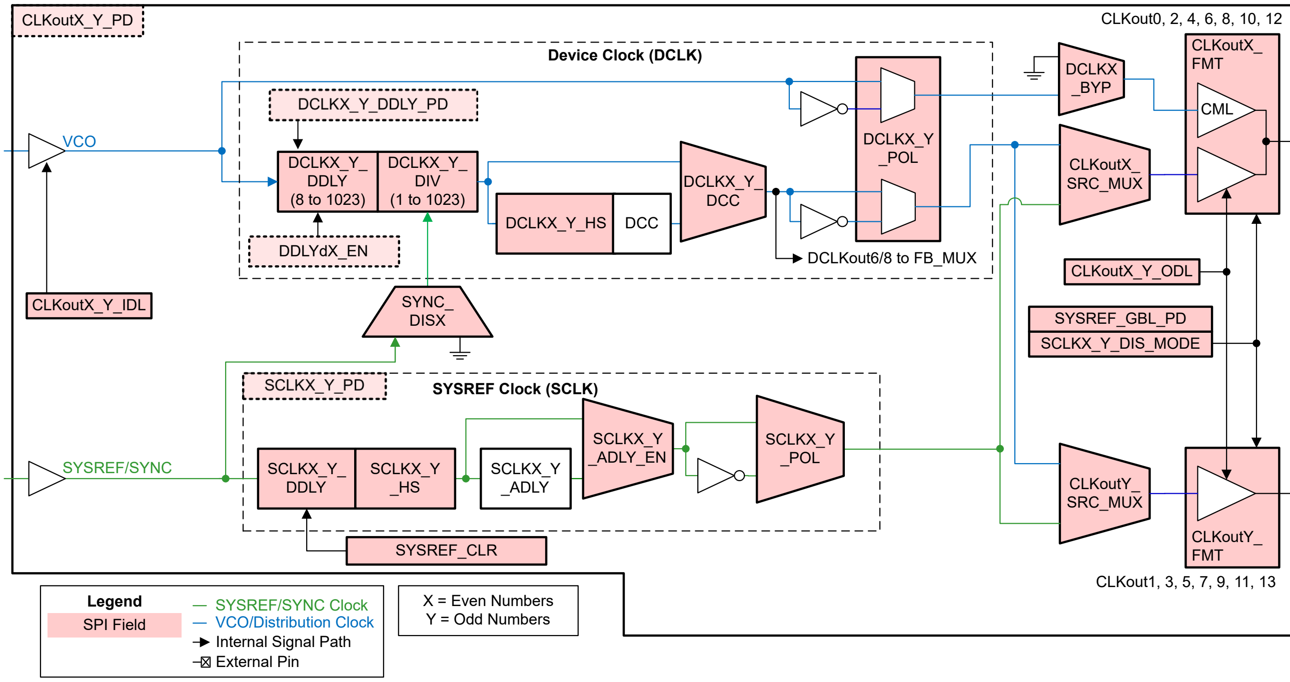


Figure 8-2. Device and SYSREF Clock Output Block

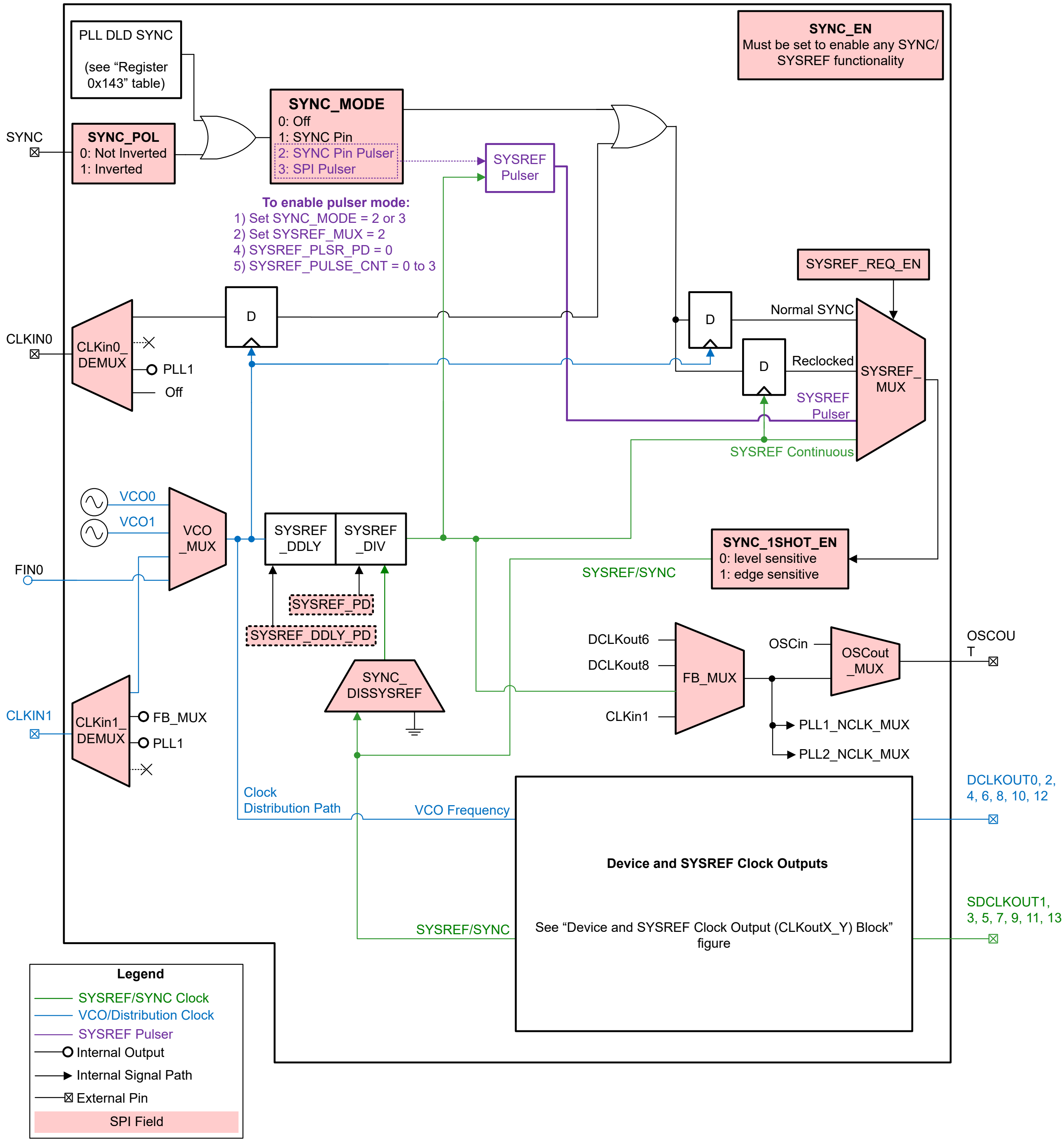


Figure 8-3. SYNC/SYSREF Clocking Paths

8.3 Feature Description

8.3.1 Synchronizing PLL R Dividers

In some cases, it is necessary to synchronize PLL R dividers to enable determinism of clocks outputs to inputs. This typically is required when the fraction Total PLL N divide / Total PLL R divide does not reduce to N / 1.

8.3.1.1 PLL1 R Divider Synchronization

It is possible to use the CLKIN0 or SYNC pin to synchronize the PLL1 R divider. To do this, the device is set up for synchronization, the PLL1 R divider is armed for synchronization, and then the rising sync edge arrives from either the SYNC pin or CLKIN0. After the PLL1 R divider is armed, PLL1 is unlocked until the synchronization edge arrives and allows the divider to operate and the PLL to lock. The procedure to synchronize PLL1 R is as follows:

1. Setup device for synchronizing PLL1 R:
   - PLL1R_SYNC_EN = 0x1
   - PLL1R_SYNC_SRC = 0x1 (SYNC pin) or 0x2 (CLKIN0)
   - CLKin0_DEMUX = 0x2 (PLL1)
   - CLKin1_DEMUX = 0x2 (PLL1)
   - CLKin0_TYPE = 0x1 (MOS) for DC-coupled or CLKin0_TYPE = 0x0 (Bipolar) for AC-coupled
2. Arm PLL1 R divider for synchronization
   - PLL1R_RST = 1, then 0.
   - PLL1 is unlocked.
3. Send rising edge on SYNC pin or CLKIN0.
   - PLL1 R divider is released from reset and PLL1 relocks.

It is necessary to meet a setup and hold time when CLKIN0 or SYNC pin goes high to ensure deterministic reset of the PLL1 R divider.

The SYNC_POL bit has no effect on SYNC polarity for PLL1 R synchronization.

8.3.1.2 PLL2 R Divider Synchronization

The SYNC pin must be used to synchronized the PLL2 R divider. When PLL2R_SYNC_EN = 1, as long as the SYNC pin is held high, the PLL2 R divider is held in reset. When the SYNC pin is returned low, the divider is allowed to continue dividing. While PLL2R_SYNC_EN = 1 and SYNC pin is high PLL2 is unlocked.

It is necessary to meet a setup and hold time when SYNC pin goes low to ensure deterministic reset of the PLL2 R divider.

The SYNC_POL bit has no effect on SYNC polarity for PLL2 R synchronization.

8.3.2 SYNC/SYSREF

The SYNC and SYSREF signals share the same SYNC/SYSREF Clock Distribution path. To properly use SYNC and/or SYSREF for JESD204B/C, it is important to understand the SYNC/SYSREF system. Figure 8-2 shows the detailed diagram of a clock output block with SYNC circuitry included. Figure 8-3 shows the interconnects and highlights some important registers used in controlling the device for SYNC/SYSREF purposes.

To reset or synchronize a divider, the following conditions must be met:

1. SYNC_EN must be set. This ensures proper operation of the SYNC circuitry.
2. SYSREF_MUX and SYNC_MODE must be set to a proper combination to provide a valid SYNC/SYSREF signal.
   - If SYSREF block is being used, the SYSREF_PD bit must be clear.
   - If the SYSREF Pulser is being used, the SYSREF_PLSR_PD bit must be clear.
   - For each CLKOUTx or CLKOUTy being used for SYSREF, the respective SCLKX_Y_PD bit must be cleared.
3. DCLKX_Y_DDLY_PD and SYSREF_DDLY_PD bits must be clear to power up the digital delay circuitry used during SYNC to cause deterministic phase between the device clock dividers and the global SYSREF divider.
4. The SYNC_DISX bit must be clear to allow SYNC/SYSREF signal to divider circuit. The SYSREF_MUX register selects the SYNC source which resets the SYSREF/CLKOUTx dividers, provided the corresponding SYNC_DISX bit is clear.
5. Other bits which impact the operation of SYNC such as SYNC_1SHOT_EN may be set as desired.
6. After these dividers are synchronized, the DCLKX_Y_DDLY_PD and SYSREF_DDLY_PD bits may be set to save current. Clearing them to power up may disrupt the output clock phase.

Table 8-2 shows the some possible combinations of SYSREF_MUX and SYNC_MODE.

Table 8-2. Some Possible SYNC Configurations

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
SYNC Disabled	0	0	CLKin0_DEMUX ≠ 0	No SYNC will occur.
Pin or SPI SYNC	1	0	CLKin0_DEMUX ≠ 0	Basic SYNC functionality, SYNC pin polarity is selected by SYNC_POL. To achieve SYNC through SPI, toggle the SYNC_POL bit.
Differential input SYNC	X	0 or 1	CLKin0_DEMUX = 0	Differential CLKin0 now operates as SYNC input.
JESD204B/C Pulser on pin transition.	2	2	SYSREF_PULSE_CNT sets pulse count	Produce SYSREF_PULSE_CNT programmed number of pulses on pin transition. SYNC_POL can be used to cause SYNC through SPI.
JESD204B/C Pulser on SPI programming.	3	2	SYSREF_PULSE_CNT sets pulse count	Programming SYSREF_PULSE_CNT register starts sending the number of pulses.
Re-clocked SYNC	1	1	SYSREF operational, SYSREF Divider as required for training frame size.	Allows precise SYNC for n-bit frame training patterns for non-JESD converters such as LM97600.
External SYSREF request	0	2	SYSREF_REQ_EN = 1 Pulser powered up	When SYNC pin is asserted, continuous SYSREF pulses occur. Turning on and off of the pulses is synchronized to prevent runt pulses from occurring on SYSREF.
Continuous SYSREF	X	3	SYSREF_PD = 0 SYSREF_DDLY_PD = 0 SYSREF_PLSR_PD = 1 (1)	Continuous SYSREF signal.

Table 8-2. Some Possible SYNC Configurations (continued)

NAME	SYNC_MODE	SYSREF_MUX	OTHER	DESCRIPTION
Re-clocked SYSREF distribution	0	0	SYSREF_DDLY_PD = 1 SYSREF_PLSR_PD = 1 SYSREF_PD = 1.	Fan-out of CLKin0 reclocked to the clock distribution path.

(1) SCLKX_Y_PD = 0 as required per SYSREF output. This applies to any SYNC or SYSREF output on SCLKX_Y when SCLKX_Y_MUX = 1 (SYSREF output)

Note

The SYNC/SYSREF signal is reclocked by the Clock Distribution Path, therefore an active clock must be present on the Clock Distribution Path (either from VCO or FIN0/FIN1 pins in distribution mode) for SYNC to take effect.

Note

Any device clock divider or the SYSREF divider which does not have the SYNC_DISX bit or SYNC_DISSYSREF bit set will reset while SYNC/SYSREF Distribution Path is high. This is especially important for the SYSREF divider which has the ability to reset itself if the SYNC_DISSYSREF = 0! **Be sure to set SYNC_DISX/SYNC_DISSYSREF bits as required.**

Note

While using Divide-by-2 or Divide-by-3 for DCLK_X_Y_DIV, SYNC procedure requires to first program Divide-by-4 and then back to Divide-by-2 or Divide-by-3 before doing SYNC.

8.3.3 JEDEC JESD204B/C

8.3.3.1 How to Enable SYSREF

Table 8-3 summarizes the bits required to make the SYSREF functionality operational.

Table 8-3. SYSREF Bits

REGISTER	FIELD	VALUE	DESCRIPTION
0x140	SYSREF_PD	0	Must be clear, power-up SYSREF circuitry including the SYSREF divider.
0x140	SYSREF_DDLY_PD	0	Must be clear to power-up digital delay circuitry. Must be powered up during initial SYNC to ensure deterministic timing to other clock dividers.
0x143	SYNC_EN	1	Must be set, enable SYNC.
0x143	SYSREF_CLR	1 → 0	Do not hold local SYSREF DDLY block in reset except at start. Anytime SYSREF_PD = 1, because of user programming or device RESET, it is necessary to set SYSREF_CLR for 15 VCO clock cycles to clear the local SYSREF digital delay. After the delay is cleared, SYSREF_CLR must be cleared to allow SYSREF to operate.

Enabling JESD204B/C operation involves synchronizing all the clock dividers with the SYSREF divider, then configuring the actual SYSREF functionality.

8.3.3.1.1 Setup of SYSREF Example

The following procedure is a programming example for a system which is to operate with a 3000-MHz VCO frequency. Use CLKOUT0 and CLKOUT2 to drive converters at 1500 MHz. Use CLKOUT4 to drive an FPGA at 150 MHz. Synchronize the converters and FPGA using a two SYSREF pulses at 10 MHz.

1. **Program registers 0x000 to 0x555 (refer to *Recommended Programming Sequence*). Key to prepare for SYSREF operations:**
    a. Prepare for manual SYNC: SYNC_POL = 0, SYNC_MODE = 1, SYSREF_MUX = 0

   b. Setup output dividers as per example: DCLK0_1_DIV and DCLK2_3_DIV = 2 for frequency of 1500 MHz. DCLK4_5_DIV = 20 for frequency of 150 MHz.
   c. Setup output dividers as per example: SYSREF_DIV = 300 for 10-MHz SYSREF.
   d. Setup SYSREF: SYSREF_PD = 0, SYSREF_DDLY_PD = 0, DCLK0_1_DDLY_PD = 0, DCLK2_3_DDLY_PD = 0, DCLK4_5_DDLY_PD = 0, SYNC_EN = 1, SYSREF_PLSR_PD = 0, SYSREF_PULSE_CNT = 1 (2 pulses). SCLK0_1_PD = 0, SCLK2_3_PD = 0, SCLK4_5_PD = 0.
   e. Clear Local SYSREF DDLY: SYSREF_CLR = 1.
2. **Establish deterministic phase relationships between SYSREF and Device Clock for JESD204B/C:**
   a. Set device clock and SYSREF divider digital delays: DCLK0_1_DDLY, DCLK2_3_DDLY, DCLK4_5_DDLY, and SYSREF_DDLY.
   b. Set device clock digital delay half steps: DCLK0_1_HS, DCLK2_3_HS, DCLK4_5_HS.
   c. Set SYSREF clock digital delay as required to achieve known phase relationships: SCLK0_1_DDLY, SCLK2_3_DDLY, and SCLK4_5_DDLY. If half step adjustments are required SCLK0_1_HS, SCLK2_3_HS, and SCLK4_5_HS.
   d. To allow SYNC to affect dividers: SYNC_DIS0 = 0, SYNC_DIS2 = 0, SYNC_DIS4 = 0, SYNC_DISSYSREF = 0.
   e. **Perform SYNC by toggling SYNC_POL = 1 then SYNC_POL = 0.**
3. Now that dividers are synchronized, **disable SYNC from resetting these dividers.** It is not desired for SYSREF to reset it's own divider or the dividers of the output clocks.
   a. Prevent SYNC (SYSREF) from affecting dividers: SYNC_DIS0 = 1, SYNC_DIS2 = 1, SYNC_DIS4 = 1, SYNC_DISSYSREF = 1.
4. **Release reset of local SYSREF digital delay.**
   a. SYSREF_CLR = 0. Note this bit needs to be set for only 15 clock distribution path clocks after SYSREF_PD = 0.
5. **Set SYSREF operation**.
   a. Allow pin SYNC event to start pulser: SYNC_MODE = 2.
   b. Select pulser as SYSREF signal: SYSREF_MUX = 2.
6. **Complete!** Assert the SYNC pin or toggle the SYNC_POL to send a series of 2 SYSREF pulses.

8.3.3.1.2 SYSREF_CLR

The local digital delay of the SCLKX_Y_DDLY is implemented as a shift buffer. To ensure no unwanted pulses occur at this SYSREF output at start-up, when using SYSREF, requires clearing the buffers by setting SYSREF_CLR = 1 for 15 VCO clock cycles. After a reset, this bit is set, so it must be cleared before SYSREF output is used.

If the SYSREF pulser is used. It is also required to set SYSREF_CLR = 1 for 15 VCO clock cycles after the SYSREF pulser is powered up.

8.3.3.2 SYSREF Modes

8.3.3.2.1 SYSREF Pulser

This mode allows for the output of 1, 2, 4, or 8 SYSREF pulses for every SYNC pin event or SPI programming. This implements the gapped periodic functionality of the JEDEC JESD204B/C specification.

When in SYSREF Pulser mode, the user can adjust the SYSREF_PULSE_CNT field in register 0x13E to program the pulser to send out a set number of pulses.

8.3.3.2.2 Continuous SYSREF

This mode allows for continuous output of the SYSREF clock.

Note

TI does not recommend continuous operation of the SYSREF clock due to crosstalk from the SYSREF clock to device clock. JESD204B/C is designed to operate with a single burst of pulses to initialize the system at start-up, after which it is theoretically not required to send another SYSREF because the system will continue to operate with deterministic phases.

8.3.3.2.3 SYSREF Request

This mode allows an external source to synchronously turn on or off a continuous stream of SYSREF pulses using the SYNC/SYSREF_REQ pin.

Setup the mode by programming SYSREF_REQ_EN = 1 and SYSREF_MUX = 2 (Pulser). The pulser does not need to be powered for this mode of operation.

When the SYSREF_REQ pin is asserted, the SYSREF_MUX is synchronously set to continuous mode, providing continuous pulses at the SYSREF frequency until the SYSREF_REQ pin is unasserted. When the SYSREF_REQ pin is unasserted, the final SYSREF pulse completes sending synchronously.

8.3.4 Digital Delay

Digital (coarse) delay allows a group of outputs to be delayed by 8 to 1023 clock distribution path cycles. The delay step can be as small as half the period of the clock distribution path cycle by using the DCLKX_Y_HS bit. There are two different ways to use the digital delay:

1. Fixed digital delay
2. Dynamic digital delay

In both delay modes, the regular clock divider is substituted with an alternative divide value.

8.3.4.1 Fixed Digital Delay

Use of Fixed Digital Delays

The fixed digital delay value takes effect on the clock outputs after a SYNC event. As such, the outputs will be LOW for a while during the SYNC event. Applications that cannot accept clock breakup when adjusting the digital delay during application run time can use dynamic digital delay to adjust phase.

Note

Fixed delays cannot be powered down or bypassed.

Note

Divide values less than 8 require special handling for fixed delays and will cause the output clocks to shift.

Note

For outputs with divide of 2 or 3, it is only with the internal VCO that SYNC and fixed delays are known to produce consistent phase.

Although there is some special behavior for divide values less than 8, Table 8-4 shows a known working way to get the desired delays. Note that the delay shift is only valid for DCLKOUTX_Y_DLY = 15. The general method is to set the fixed delay and then use dynamic delay to make the proper adjustments. Although not required, it simplifies calculations to set all fixed delays to 15, even for channels that do not require the special handling. The starting position is also adjusted by the divide value when the divide value is less than 8.

Use Equation 1 to calculate the total delay:

$$\text{ClockDelay} = \text{FixedDelay} + \text{FixedDelayCorrection} + \text{DynamicDelay} \tag{1}$$

Use Equation 2 to calculate the DynamicDelay (DDLYd_STEP_CNT):

$$\text{DynamicDelay} = (\text{ClockDelay} - \text{FixedDelay} - \text{FixedDelayCorrection}) \% \text{Divide} \quad (2)$$

Table 8-4. Method for Creating Fixed Delays for Divide Values less than 8 for DCLKOUTX_Y = 15

<table>
<tr><th>DIVIDE</th><th>DELAY SHIFT</th><th>SPECIAL HANDLING</th></tr>
<tr><td>2</td><td>+1</td><td rowspan="6">For each channel that requires special handling:
1. Set the fixed delay to 15.
2. Power up dynamic digital delay for channel
3. Power down dynamic digital delays for all other channels
4. Program the digital delay step value
5. Note that if the digital delay step value is zero, steps 2 through 4 can be skipped and the dynamic delay can be left powered down.</td></tr>
<tr><td>3</td><td>+1</td></tr>
<tr><td>4</td><td>0</td></tr>
<tr><td>5</td><td>+3</td></tr>
<tr><td>6</td><td>-1</td></tr>
<tr><td>7</td><td>0</td></tr>
<tr><td>≥ 8</td><td>0</td><td>None</td></tr>
</table>

Fixed Digital Delay Example

Consider the following example outlined in Table 8-5. This example uses the internal VCO at 2949.12 MHz. To set this up:

1. Program the divider values.
   - DCLK0_1_DIV = 8, _DCLK2_3_1_DIV = 8, DCLK4_5_1_DIV = 2, DCLK6_7_1_DIV = 2, _DCLK8_9_1_DIV = 4 _DCLK10_11_1_DIV = 6, _DCLK12_13_1_DIV = 5
2. Program the fixed delay settings.
   - DCLK0_1_DDLY = 8 (As 8 is the minimum fixed delay, this will be used as the reference point for a desired delay of zero.)
   - DCLK2_3_1_DDLY = 8 (one cycle delayed from CLKOUT0)
   - ,DCLK4_5_1_DDLY = 15, DCLK6_7_1_DDLY = 15, DCLK8_9_DDLY = 15, DCLK10_11_DDLY = 15, DCLK12_13_DDLY = 15 (Set all of these to 15 because the divide value is less than 8)
3. Issue a SYNC Pulse
   a. Write SYNC_DIS0 = 0, SYNC_DIS2 = 0, SYNC_DIS4 = 0, SYNC_DIS6 = 0, SYNC_DIS8 = 0, SYNC_DIS10 = 0
   b. Issue a sync pulse or toggle the SYNC_POL bit
4. Do the dynamic digital delays
   a. Power down all dynamic digital delays except for CLKOUT6 and CLKOUT 8
      - DCLK0_1_DDLY_PD = DCLK2_3_DDLY_PD = DCLK4_5_DDLY_PD = DCLK10_11_DDLY_PD = DCLK12_13_DDLY_PD = 1
      - CLKOUT4 and CLKOUT10 do not require digital delays because the calculated value that would be programmed is zero.
      - CLKOUT0 and CLKOUT2 do not require dynamic digital delays because their divide value 8 or larger.
      - DCLK6_7_DDLY_PD = 0
      - DCLK8_9_DDLY_PD = 0
   b. CLKOUT6:
      i. Write DDLYd6_EN = 1, DDLYd8_EN = 0
      ii. Write DDLY_STEP_CNT = 1 to activate dynamic digital delay
   c. CLKOUT8:
      i. Write DDLYd6_EN = 0, DDLYd8_EN = 1
      ii. Write DDLY_STEP_CNT = 3 to activate dynamic digital delay

Table 8-5. Fixed Digital Delay Example Setup

OUTPUT	FREQUENCY	DESIRED DELAY	DIVIDER AND FIXED DELAYS	DYNAMIC DELAYS
CLKOUT0	368.84 MHz	None (8)	DCLK0_1_DIV = 8 DCLK0_1_DDLY = 8	DCLK0_1_DDLY_PD = 1 No special handling required.
CLKOUT2	368.84 MHz	1 VCO Cycle (9)	DCLK2_3_DIV = 8 DCLK2_3_DDLY = 8 + 1 = 9	DCLK0_1_DDLY_PD = 1 No special handling required
CLKOUT4	1474.56 MHz	None (8)	DCLK4_5_DIV = 2 DCLK4_5_DDLY = 15	DCLK4_5_DDLY_PD = 1 No dynamic delays because (8 – 15 – 1) % 2 = 0
CLKOUT6	1474.56 MHz	1 VCO Cycle (9)	DCLK6_7_DIV = 2 DCLK6_7_DDLY = 15	DCLK6_7_DDLY_PD = 0 DDLYd6_EN = 1,0 DDLYd_STEP_CNT = (9 – 15 – 1) % 2 = 1
CLKOUT8	737.28 MHz	2 VCO Cycles (10)	DCLK8_9_DIV = 4 DCLK8_9_DDLY = 15	DCLK8_9_DDLY_PD = 0 DDLYd8_EN = 0,1 DDLYd_STEP_CNT=(10 – 15 – 0) % 4 = 3
CLKOUT10	491.52 MHz	None (8)	DCLK10_11_DIV = 6 DCLK10_11_DDLY = 15	DCLK10_11_DDLY_PD = 1 No dynamic delays because (8 –15 – (–1)) % 6 = 0
CLKOUT12	589.824 MHz	None (8)	DCLK12_13_DIV = 5 DCLK12_13_DDLY = 15	DCLK12_13_DDLY_PD=1 No dynamic delays because (8 – 15 – 3) % 5 = 0

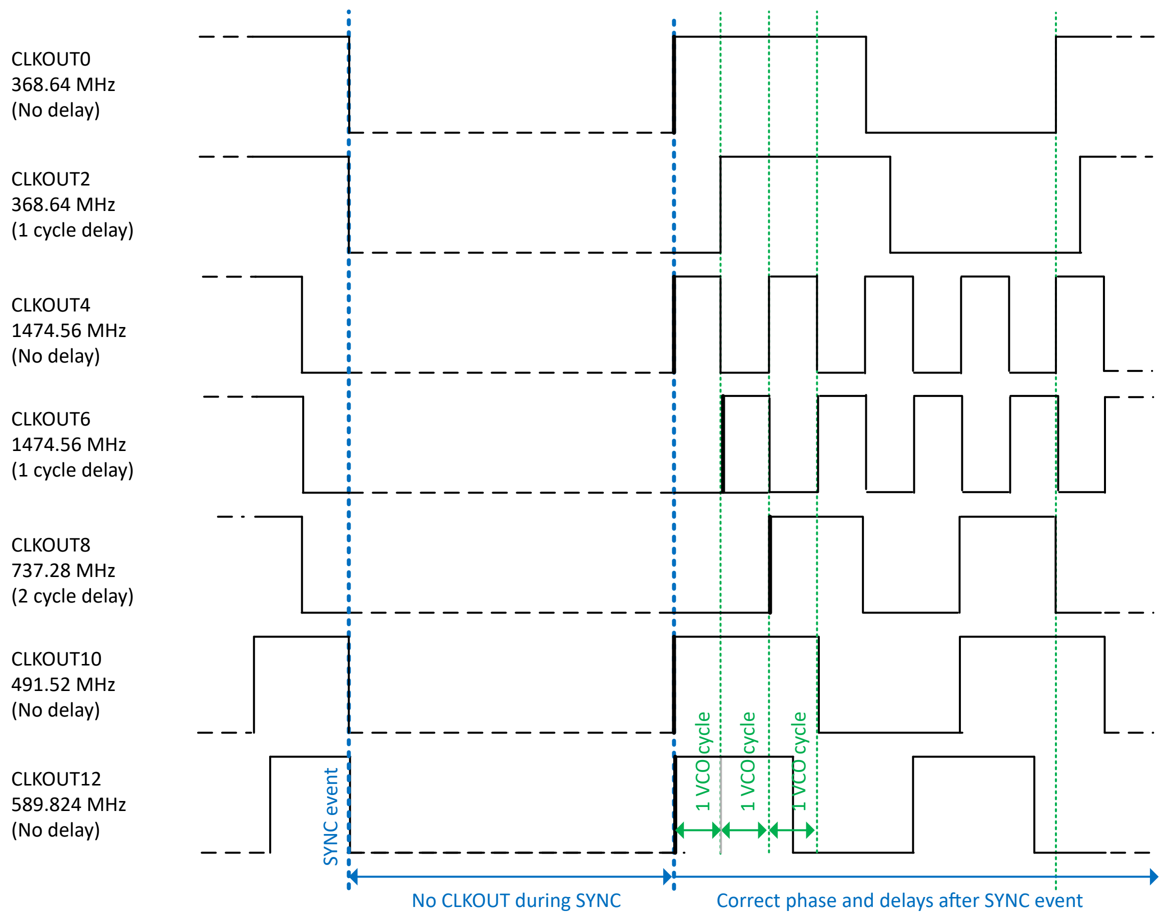


Figure 8-4. Fixed Digital Delay Example

8.3.4.2 Dynamic Digital Delay

Dynamic digital delay allows the phase of clocks to be changed with respect to each other with little impact to the clock signal.

For the device clock dividers this is accomplished by substituting the regular clock divider with an alternate divide value of one larger than the regular divider for one cycle. This substitution will occur a number of times equal to the value programmed into the DDLYd_STEP_CNT field for all outputs with DDLYdX_EN = 1.

For the SYSREF divider, an alternate divide value is substituted for the regular divide value. This substitution will occur a number of times equal to the value programmed into the DDLYd_STEP_CNT if DDLYd_SYSREF_EN = 1. To achieve one cycle delay as is done for the device clock dividers, set the SYSREF_DDLY value to one greater than SYSREF_DIV+SYSREF_DIV/2. For example, for a SYSREF divider of 100, to achieve 1 cycle delay, SYSREF_DDLY = 100 + 50 + 1 = 151.

While using the Dynamic Digital Delay feature, CLKin_OVERRIDE must be set to 0.

- By programming a larger alternate divider (delay) value, the phase of the adjusted outputs are delayed with respect to the other clocks.
- By programming a smaller alternate divider (delay) value, the phase of the adjusted outputs are advanced with respect to the other clocks.

8.3.4.3 Single and Multiple Dynamic Digital Delay Example

In this example, two separate adjustments are made to the device clocks. In the first adjustment, a single delay of one VCO cycle occurs between CLKOUT2 and CLKOUT0. In the second adjustment, two delays of one VCO cycle occur between CLKOUT2 and CLKOUT0. At this point in the example, CLKOUT2 is delayed three VCO cycles behind CLKOUT0.

Assuming the device already has the following initial configurations:

- VCO frequency: 2949.12 MHz
- CLKOUT0 = 368.64 MHz, DCLK0_1_DIV = 8
- CLKOUT2 = 368.64 MHz, DCLK2_3_DIV = 8

The following steps illustrate the example above:

1. Set DCLK2_3_DDLY = 4. First part of delay for CLKOUT2.
2. Set DCLK2_3_DDLY_PD = 0. Enable the digital delay for CLKOUT2.
3. Set DDLYd0_EN = 0 and DDLYd2_EN = 1. Enable dynamic digital delay for CLKOUT2 but not CLKOUT0.
4. Set DDLYd_STEP_CNT = 1. This begins the **first adjustment.**

Before step 4, CLKOUT2 clock edge is aligned with CLKOUT0.

After step 4, CLKOUT2 counts nine clock distribution path cycles to the next rising edge, one greater than the divider value, effectively delaying CLKOUT2 by one VCO cycle with respect to CLKOUT0. ***This is the first adjustment.***

5. Set DDLYd_STEP_CNT = 2. This begins the **second adjustment.**

Before step 5, CLKOUT2 clock edge was delayed one clock distribution path cycle from DCLKOUT0.

After step 5, CLKOUT2 counts nine clock distribution path cycles twice, each time one greater than the divide value, effectively delaying CLKOUT2 by two clock distribution path cycles with respect to CLKOUT0. ***This is the second adjustment.***

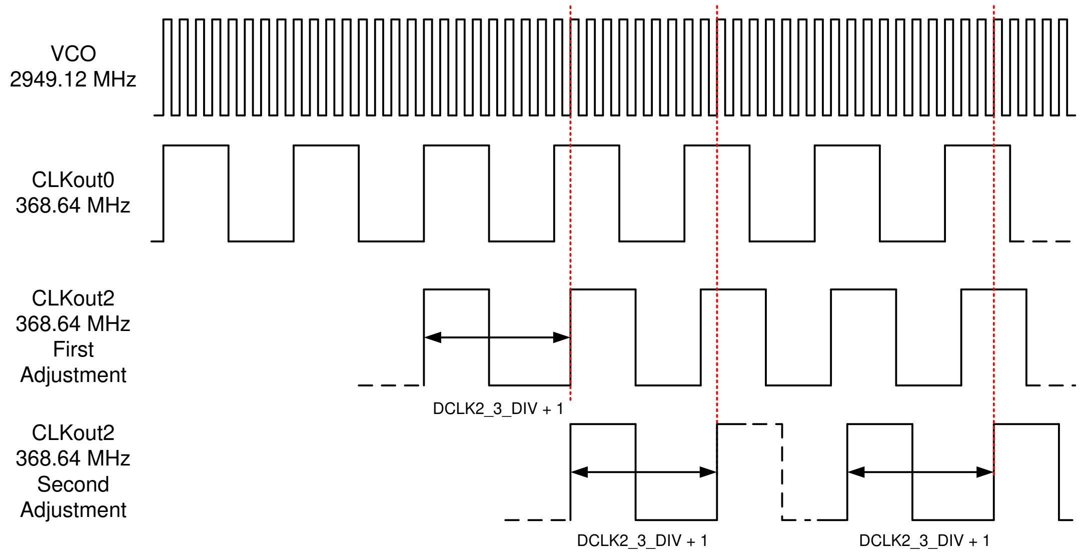


Figure 8-5. Single and Multiple Adjustment Dynamic Digital Delay Example

8.3.5 SYSREF to Device Clock Alignment

To ensure proper JESD204B/C operation, the timing relationship between the SYSREF and the Device clock must be adjusted for optimum setup and hold time as shown in Figure 8-6. The global SYSREF digital delay (SYSREF_DDLY), local SYSREF digital delay (SCLKX_Y_DDLY), local SYSREF half step (SCLKX_Y_HS), and local SYSREF analog delay (SCLKX_Y_ADLY, SCLK2_3_ADLY_EN) can be adjusted to provide the required setup and hold time between SYSREF and Device Clock. It is also possible to adjust the device clock digital delay (DCLKX_Y_DDLY) and half step (DCLK0_1_HS, DCLK0_1_DCC) to adjust phase with respect to SYSREF.

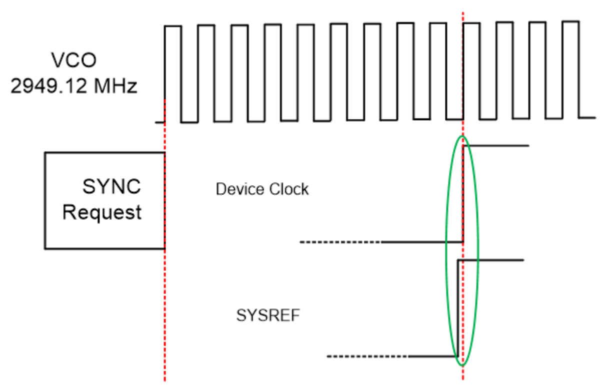


Figure 8-6. SYSREF to Device Clock Timing Alignment

The delay between clock and SYSREF is the difference between the delays for these paths.

$$\text{Clock to SYSREF Delay} = \text{TotalSysrefDelay} - \text{TotalClockDelay} \tag{3}$$

$$\text{TotalClockDelay} = \text{ClockFixedDelay} + \text{ClockFixedDelayCorrection} + \text{DynamicDelay} + \text{ClockHalfStep} \tag{4}$$

$$\text{TotalSysrefDelay} = 80\text{ ps} + \frac{1}{f_{VCO}} + \text{SysrefGlobalDelay} + \text{SysrefFixedDelay} + \text{SysrefHalfStep} + \text{SysrefAnalogDelay} \tag{5}$$

Table 8-6. Clock to SYSREF Delay Explanation and Example

VARIABLE/FIELD	COMMENTS	EXAMPLE (f_{VCO} = 2.5 GHz, DIVIDE = 6)
ClockFixed Delay (DCLKX_Y_DDLY)		ClockFixedDelay = 6000 ps (DCLK0_1_DDLY = 15)
ClockFixedDelayCorrection	Correction value when divide is less than 8. • Divide of 2 or 3: 1 • Divide of 5: –3 • Divide of 6: –1 • All other divides: 0	ClockFixedDelayCorrection = –400 ps (–1 VCO Cycle)
ClockDutyCycleCorrect (DCLKX_Y_DCC)	Adds one VCO cycle if enabled	ClockDutyCycleCorrect = 400 (DCLKX_Y_DCC = 1)
ClockDynamicDelay (dDLY_STEP_CNT)	ClockDynamicDelay is the cumulative effect of programming dDLY_STEP_CNT. It is zero if the dynamic delay is disabled for the channel	ClockDynamicDigitalDelay = 0 (DDLYd0_EN = 0)
ClockHalfStep (DCLKX_Y_HS)	This would be ½ of a VCO Cycle if enabled	ClockHalfStep = 200 (DCLKX_Y_DCC = 1)
SysrefGlobalDelay (SYSREF_DDLY)	SYSREF_DDLY≥8 for proper operation	SysRefGlobalDelay = 4800 ps (SYSREF_DDLY = 12)
SysrefFixedDelay (SCLKX_Y_DDLY)	This is the number of cycles represented by the delay	SysrefFixedDelay = 2 × 400 = 800 ps (SCLK0_1_DDLY = 1)
SysrefHalfStep (SCLKX_Y_HS)	The half step for the SYSREF is not exactly a half step, but rather about 60 ps less.	SysrefHalfStep = 200 – 60 = 140 ps (SCLK0_1_HS = 1)
SysrefAnalogDelay (SCLKX_Y_ADLY)	This is the stated value in ps for the analog delay	SysrefAnalogDelay = 230 ps (SCLK0_1_ADLY = 5)
TotalClockDelay = 6000 + (–400) + 400 – 200 + 0 = 5800 ps		
TotalSysrefDelay = 80 + 400 + 4800 + 800 – 140 + 230 = 6170 ps		
Clock to SYSREF Delay = 6170 – 5800 = 370 ps		

8.3.6 Input Clock Switching

Manual, pin select, and automatic are three different kinds clock input switching modes can be selected according to the combination of bits as illustrated in Figure 8-7.

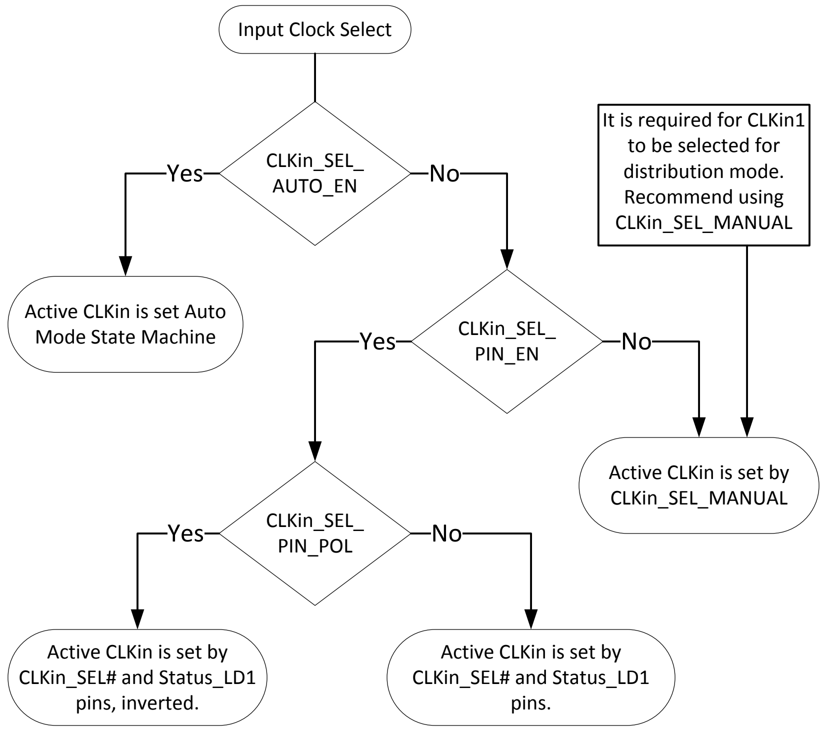


Figure 8-7. CLKINx Input Reference

The following sections provide information about how the active input clock is selected and what causes a switching event in the various clock input selection modes.

8.3.6.1 Input Clock Switching - Manual Mode

When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 0, the active CLKin is selected by CLKin_SEL_MANUAL. Programming a value of 0, 1, or 2 to CLKin_SEL_MANUAL causes CLKin0, CLKin1, or CLKin2, respectively, to be the selected active input clock. In this mode, the EN_CLKinX bits are overridden such that the CLKinX buffer operates even if CLKinX is disabled with EN_CLKinX = 0.

If holdover is entered in this mode by setting CLKin_SEL_MANUAL = 3, then the device will re-lock to the selected CLKin upon holdover exit.

8.3.6.2 Input Clock Switching - Pin Select Mode

When CLKin_SEL_AUTO_EN = 0 and CLKin_SEL_PIN_EN = 1, the active clock is selected by the CLKIN_SELx and STATUS_LD1 pins.

Configuring Pin Select Mode

The CLKin_SEL0_TYPE must be programmed to an input value for the CLKIN_SEL0 pin to function as an input for pin select mode.

The CLKin_SEL1_TYPE must be programmed to an input value for the CLKIN_SEL1 pin to function as an input for pin select mode.

The polarity of the clock input select pins can be inverted with the CLKin_SEL_PIN_POL bit.

Table 8-7 defines which input clock is active depending on the clock input select pins state. The CLKIN_SEL1, CLKIN_SEL0, and STATUS_LD1 pins must be set as input type. Any pin set to output will always report Low on the table below.

Table 8-7. Active Clock Input - Pin Select Mode, CLKin_SEL_INV = 0

CLKIN_SEL0 Pin	CLKIN_SEL1 Pin	STATUS_LD1 Pin	Active Clock
Low	Low	Low	CLKIN0

Table 8-7. Active Clock Input - Pin Select Mode, CLKin_SEL_INV = 0 (continued)

CLKIN_SEL0 Pin	CLKIN_SEL1 Pin	STATUS_LD1 Pin	Active Clock
Low	High	Low	CLKIN1
High	Low	High	CLKIN2
High	High	X	Holdover

The pin select mode overrides the EN_CLKinX bits such that the CLKINx buffer operates even if CLKINx is disabled with EN_CLKinX = 0. To switch as fast as possible, keep the clock input buffers enabled (EN_CLKinX = 1) that could be switched to.

8.3.6.3 Input Clock Switching - Automatic Mode

When CLKin_SEL_AUTO_EN = 1, LOS_EN = 1, and HOLDOVER_EXIT_MODE = 0 (Exit based on LOS), the active clock is selected in priority order with CLKin0 being the highest priority, CLKin1 second, and CLKin2 third.

For a clock input to be eligible to be switched to, it must be enabled using EN_CLKinX. The LOS_TIMEOUT should also be set to a frequency below the input frequency.

To ensure LOS is valid for AC-coupled inputs, the MOS mode must be set for the CLKin and no termination is allowed to be between the pins unless the pins are DC-blocked. For example, no 100-Ω termination across CLKin0 and CLKin0* pins on IC side of AC-coupling capacitors.

8.3.7 Digital Lock Detect (DLD)

Both PLL1 and PLL2 support digital lock detect. Digital lock detect compares the phase between the reference path (R) and the feedback path (N) of the PLL. When the time error, which is phase error, between the two signals is less than a specified window size (ε) a lock detect count increments. When the lock detect count reaches a user specified value, PLL1_DLD_CNT or PLL2_DLD_CNT, lock detect is asserted true. Once digital lock detect is true, a single phase comparison outside the specified window will cause digital lock detect to be asserted false. This is illustrated in Figure 8-8.

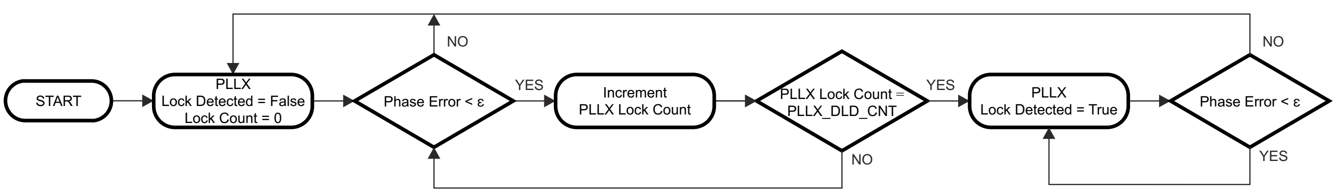


Figure 8-8. Digital Lock Detect Flowchart

This incremental lock detect count feature functions as a digital filter to ensure that lock detect is not asserted for only a brief time when the phases of R and N are within the specified tolerance for only a brief time during initial phase lock.

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect signal can be monitored on the Status_LD1 or Status_LD2 pin. The pin may be programmed to output the status of lock detect for PLL1, PLL2, or both PLL1 and PLL2.

8.3.7.1 Calculating Digital Lock Detect Frequency Accuracy

See *Digital Lock Detect Frequency Accuracy* for more detailed information on programming the registers to achieve a specified frequency accuracy in ppm with lock detect.

The digital lock detect feature can also be used with holdover to automatically exit holdover mode. See *Exiting Holdover* for more information.

8.3.8 Holdover

Holdover mode causes PLL2 to stay locked on frequency with minimal frequency drift when an input clock reference to PLL1 becomes invalid. While in holdover mode, the PLL1 charge pump is TRI-STATED and a fixed tuning voltage is set on CPout1 to operate PLL1 in open loop.

8.3.8.1 Enable Holdover

Program HOLDOVER_EN = 1 to enable holdover mode.

Holdover mode can be configured to set the CPout1 voltage upon holdover entry to a fixed user defined voltage (EN_MAN_DAC = 1) or a tracked voltage (EN_MAN_DAC = 0).

8.3.8.1.1 Fixed (Manual) CPout1 Holdover Mode

By programming MAN_DAC_EN = 1, then the MAN_DAC value will be set on the CPout1 pin during holdover.

The user can optionally enable CPout1 voltage tracking (TRACK_EN = 1), read back the tracked DAC value, then re-program MAN_DAC value to a user desired value based on information from previous DAC read backs. This allows the most user control over the holdover CPout1 voltage, but also requires more user intervention.

8.3.8.1.2 Tracked CPout1 Holdover Mode

By programming MAN_DAC_EN = 0 and TRACK_EN = 1, the tracked voltage of CPout1 is set on the CPout1 pin during holdover. When the DAC has acquired the current CPout1 voltage, the *DAC_Locked* signal is set, which may be observed on Status_LD1 or Status_LD2 pins by programming PLL1_LD_MUX or PLL2_LD_MUX, respectively.

Updates to the DAC value for the Tracked CPout1 sub-mode occurs at the rate of the PLL1 phase detector frequency divided by (DAC_CLK_MULT × DAC_CLK_CNTR).

The DAC update rate should be programmed for ≤ 100 kHz to ensure DAC holdover accuracy.

The ability to program slow DAC update rates, for example one DAC update per 4.08 seconds when using 1024-kHz PLL1 phase detector frequency with DAC_CLK_MULT = 16,384 and DAC_CLK_CNTR = 255, allows the device to *look-back* and set CPout1 at a previous *good* CPout1 tuning voltage values before the event which caused holdover to occur.

The current voltage of DAC value can be read back using RB_DAC_VALUE, see the *RB_DAC_VALUE* section.

8.3.8.2 During Holdover

PLL1 is run in open-loop mode.

- PLL1 charge pump is set to TRI-STATE.
- PLL1 DLD is unasserted.
- The HOLDOVER status is asserted
- During holdover, if PLL2 was locked prior to entry of holdover mode, PLL2 DLD continues to be asserted.
- CPout1 voltage is set to:
  - a voltage set in the MAN_DAC register (MAN_DAC_EN = 1).
  - a voltage determined to be the last valid CPout1 voltage (MAN_DAC_EN = 0).
- PLL1 attempts to lock with the active clock input.

The HOLDOVER status signal can be monitored on the Status_LD1 or Status_LD2 pin by programming the PLL1_DLD_MUX or PLL2_DLD_MUX register to *Holdover Status*.

8.3.8.3 Exiting Holdover

Holdover mode can be exited in one of two ways.

- Manually, by programming the device from the host.
- Automatically, when the LOS signal unasserts for a clock that provides a valid input to PLL1.

8.3.8.4 Holdover Frequency Accuracy and DAC Performance

When in holdover mode, PLL1 runs in open loop and the DAC sets the CPout1 voltage. If *fixed CPout1* mode is used, then the output of the DAC is dependent upon the MAN_DAC register. If *tracked CPout1* mode is used, then the output of the DAC is approximately the same voltage at the CPout1 pin before holdover mode was entered. When using Tracked mode and MAN_DAC_EN = 1, the DAC value during holdover is loaded with the programmed value in MAN_DAC and not the tracked value.

When in Tracked CPout1 mode, the DAC has a worst-case tracking error of ±2 LSBs once PLL1 tuning voltage is acquired. The step size is approximately 3.2 mV, therefore the VCXO frequency error during holdover mode caused by the DAC tracking accuracy is ±6.4 mV × Kv, where Kv is the tuning sensitivity of the VCXO in use. Therefore, the accuracy of the system when in holdover mode in ppm is:

$$\text{Holdover accuracy (ppm)} = \frac{\pm 6.4\ \text{mV} \times \text{Kv} \times 1\text{e}6}{\text{VCXO Frequency}} \tag{6}$$

As an example, consider a system with a 19.2-MHz clock input, a 153.6-MHz VCXO with a Kv of 17 kHz/V. The accuracy of the system in holdover in ppm is:

$$\pm 0.71\ \text{ppm} = \pm 6.4\ \text{mV} \times 17\ \text{kHz/V} \times 1\text{e}6\ /\ 153.6\ \text{MHz} \tag{7}$$

It is important to account for this frequency error when determining the allowable frequency error window to cause holdover mode to exit.

8.3.9 PLL2 Loop Filter

The loop filter acts as a low-pass filter that accumulates correction currents from the charge pump and converts those correction currents into a voltage. The loop filter determines the PLL loop bandwidth, which has a dramatic effect on the performance of the PLL since it directly impacts the phase noise, spur level, and switching speed of the device. The loop filter component values are dependent on the phase detector frequency, charge pump gain, and the gain of the VCO.

Loop filter design involves trade-offs. Choosing the optimal bandwidth is application dependent. Minimizing jitter may lead to higher spur levels and a longer lock time; therefore, determining the loop filter components varies by application, as well.

of how to use this tool to obtain an optimal loop filter design that aims to minimize jitter. On this example, the FPD

= 245.76 MHz, KPD = 3.2 mA, and the KVCO = 12.1 MHz/V (this values are also application dependent) which

resulted in an external loop filter of C1 = 220 pF, C2 = 68 nF, and R2 = 120 Ω.

PLL2 has an integrated loop filter of C1i = 60 pF, R3 = 2400 Ω, C3 = 50 pF, R4 = 200 Ω and C4 = 10 pF as shown in Figure 8-9. Loop filter components C1, C2, and R2 can be solved using the PLLatinumSim software

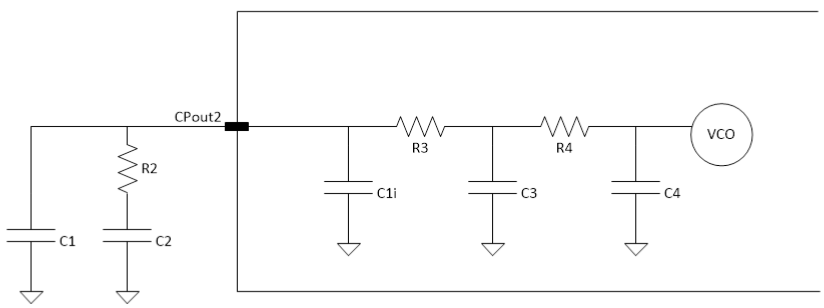


Figure 8-9. PLL2 On-Chip Loop Filter

8.4 Device Functional Modes

This device can be configured for many different use cases. The following simplified block diagrams help show the user the different use cases of the device.

8.4.1 DUAL PLL

8.4.1.1 Dual Loop

Figure 8-10 shows the typical use case of dual loop mode. In dual loop mode, the reference to PLL1 is from CLKin0, CLKin1, or CLKin2. An external VCXO is used to provide feedback for the first PLL and a reference to the second PLL. This first PLL cleans the jitter with the VCXO by using a narrow loop bandwidth. The VCXO may be buffered through the OSCout port. The VCXO is used as the reference to PLL2 and may be doubled using the frequency doubler. The internal VCO drives up to seven divide/delay blocks which drive up to 14 clock outputs.

Hitless switching and holdover functionality are optionally available when the input reference clock is lost. Holdover works by forcing a DAC voltage to the tuning voltage of the VCXO.

It is also possible to use an external VCO in place of PLL2's internal VCO. In this case one less CLKin is available as a reference as CLKin1 is used for external input.

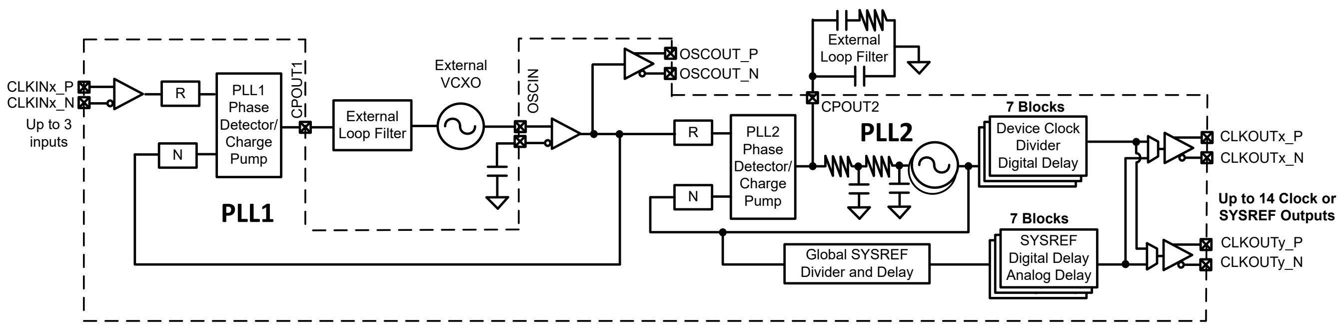


Figure 8-10. Simplified Functional Block Diagram for Dual Loop Mode

8.4.1.2 Dual Loop With Cascaded 0-Delay

Figure 8-11 shows the use case of cascaded 0-delay dual loop mode. This configuration differs from dual loop mode Figure 8-10 in that the feedback for PLL2 is driven by a clock output instead of the VCO output directly.

It is also possible to use an external VCO in place of the internal VCO of the PLL2, but one less CLKin is available as a reference and the external 0-delay feedback is not available.

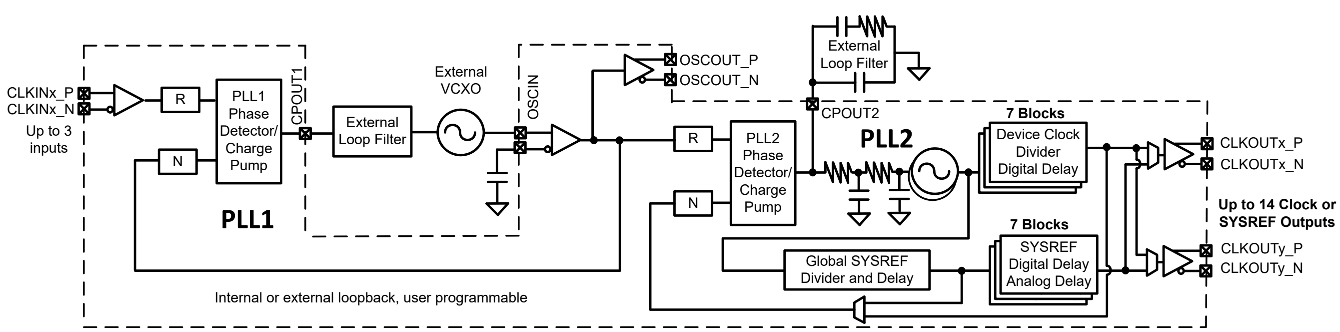


Figure 8-11. Simplified Functional Block Diagram for Cascaded 0-Delay Dual Loop Mode

8.4.1.3 Dual Loop With Nested 0-Delay

Figure 8-12 shows the use case of nested 0-delay dual loop mode. This configuration is similar to the dual PLL in Figure 8-10 except that the feedback to the first PLL is driven by a clock output. The PLL2 reference OSCIN is not deterministic to the CLKIN or feedback clock.

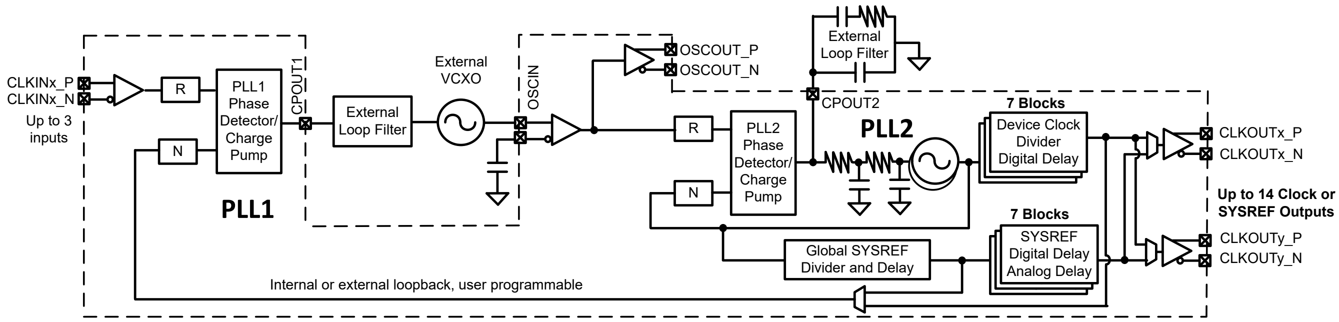


Figure 8-12. Simplified Functional Block Diagram for Nested 0-Delay Dual Loop Mode

8.4.2 Single PLL

8.4.2.1 PLL2 Single Loop

Figure 8-13 shows the use case of PLL2 single loop mode. When used with a high-frequency clean reference performance as good as dual loop mode may be achieved. Traditionally the OSCIN is used as a reference to PLL2, but it is also possible to use CLKINx as a reference to PLL2.

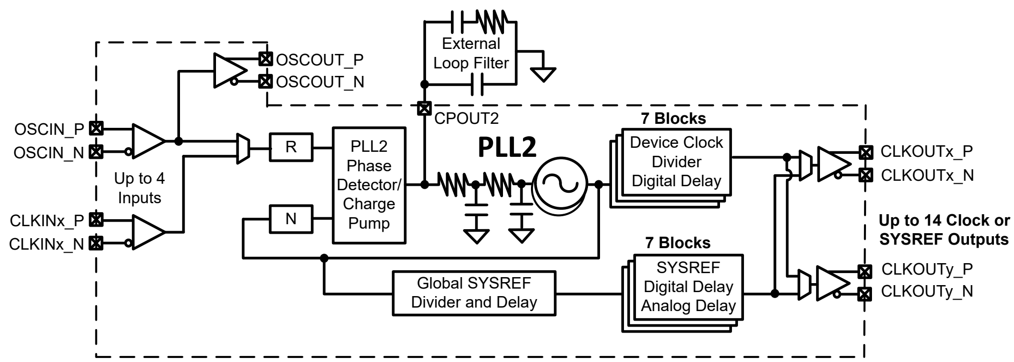


Figure 8-13. Simplified Functional Block Diagram for Single Loop Mode

8.4.2.1.1 PLL2 Single Loop With 0-Delay

Figure 8-14 illustrates the use case of 0-delay single loop mode. This configuration differs from single loop mode in that the feedback for PLL2 is driven by a clock output instead of the VCO output directly.

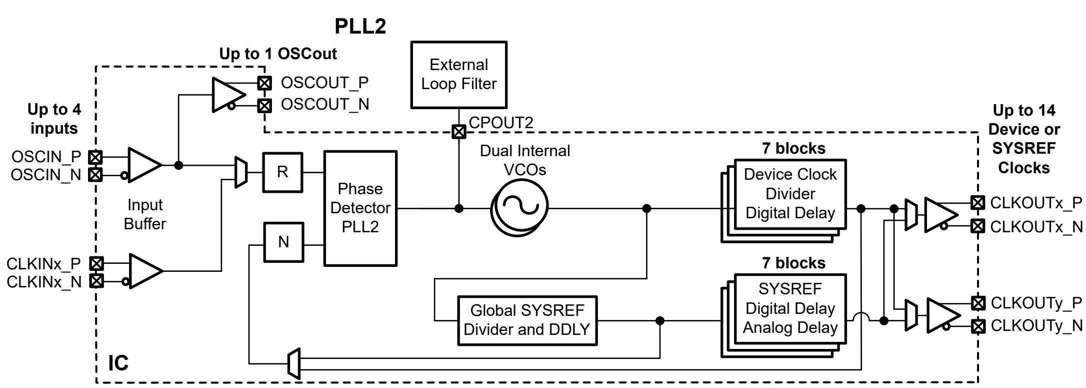


Figure 8-14. Simplified Functional Block Diagram for Single Loop Mode With 0-Delay

Figure 8-14 lists the required programming to set up PLL2 single loop with 0-delay mode.

Table 8-8. Single PLL with 0-Delay Mode Register Configuration

FIELD	REGISTER ADDRESS	FUNCTION	VALUE	SELECTED VALUE
PLL1_PD	0x140[7]	Powers down PLL1	1	Powered down
VCO_LDO_PD	0x140[6]	Powers down VCO_LDO	0	Powered up
VCO_PD	0x140[5]	Powers down VCO	0	Powered up
PLL2_PRE_PD	0x173[6]	Powers down PLL2 prescaler	0	Powered up
PLL2_PD	0x173[5]	Powers down PLL2	0	Powered up
OSCin_PD	0x140[4]	Powers down the OSCin port	0	Powered up
PLL2_NCLK_MUX	0x13F[5]	Selects the input to the PLL2 N divider	1	Feedback mux
PLL2_RCLK_MUX	0x13F[7]	Selects the source of PLL2's reference	0	OSCin
FB_MUX_EN	0x13F[0]	Enables the feedback mux	1	Enabled
VCO_MUX	0x138[6:5]	Selects the VCO 0, 1 or an external VCO	0 or 1	VCO0 or VCO1

8.4.2.2 PLL2 With an External VCO

The FIN0/FIN1 input pins can be used with an external VCO. The input may be single-ended or differential. At high frequency, the input impedance to FIN0/FIN1 is low. A resistive pad is recommended for matching.

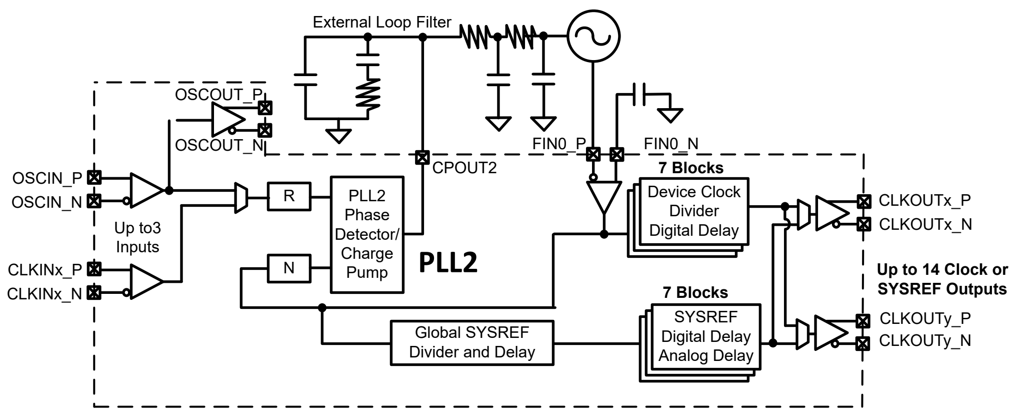


Figure 8-15. Simplified Functional Block Diagram for Single Loop Mode With External VCO

Table 8-9 list the required programming fields necessary to set up the device for PLL with an external VCO.

Table 8-9. Single PLL With External VCO Mode Register Configuration

FIELD	REGISTER ADDRESS	FUNCTION	VALUE	SELECTED VALUE
PLL1_NCLK_MUX	0x13F	Selects the input to the PLL1 N divider.	1	Feedback Mux
PLL2_NCLK_MUX	0x13F	Selects the input to the PLL2 N divider	0	PLL2 P
FB_MUX_EN	0x13F	Enables the Feedback Mux.	1	Enabled
FB_MUX	0x13F	Selects the output of the Feedback Mux.	0, 1, or 2	Select between DCLKout6, DCLKout8, SYSREF
OSCin_PD	0x140	Powers down the OSCin port.	0	Powered up
CLKin0_DEMUX	0x147	Selects where the output of CLKIN0 is directed.	2	PLL1
CLKin1_DEMUX	0x147	Selects where the output of CLKIN1 is directed.	0 or 2	FIN or PLL1
VCO_MUX	0x138	Selects the VCO 0, 1 or an external VCO	0 or 1	VCO 0 or VCO 1

8.4.3 Distribution Mode

Figure 8-16 shows the use case of distribution mode. As in all the other use cases, OSCIN to OSCOUT can be used as a buffer to OSCIN or from clock distribution path through CLKOUT6, CLKOUT8, or the SYSREF divider.

At high frequency, the input impedance to FIN0/FIN1 is low and a resistive pad is recommended for matching.

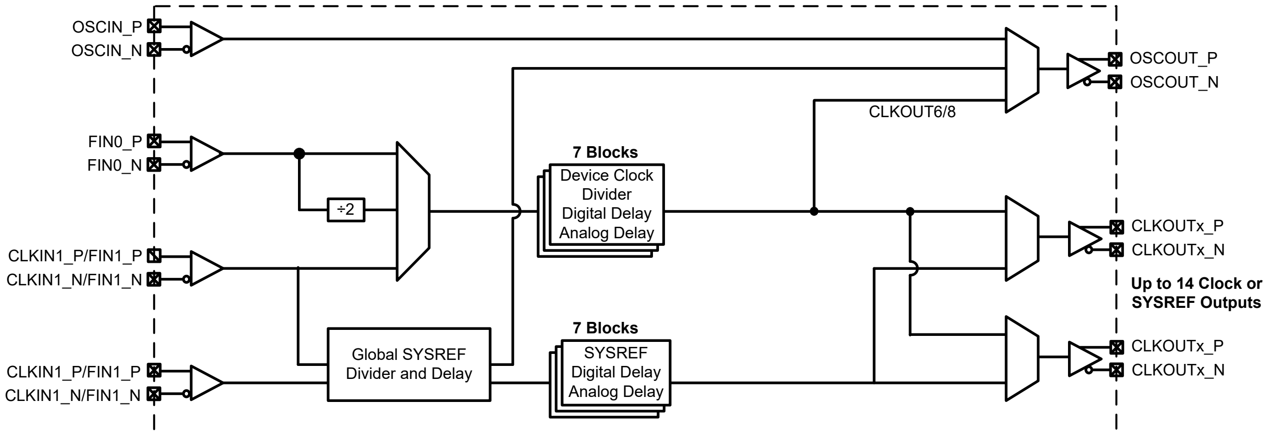


Figure 8-16. Simplified Functional Block Diagram for Distribution Mode

8.5 Programming

The device is programmed using 24-bit registers. Each register consists of a 1-bit command field (R/W), a 15-bit address field (A14 to A0) and a 8-bit data field (D7 to D0). The contents of each register is clocked in MSB first (R/W), and the LSB (D0) last. During programming, the CS* signal is held low. The serial data is clocked in on the rising edge of the SCK signal. After the LSB is clocked in, the CS* signal goes *high* to latch the contents into the shift register. TI recommends to program registers in numeric order (for example, 0x000 to 0x555 with exceptions noted in the *Recommended Programming Sequence*). Each register consists of one or more fields which control the device functionality. See the *Electrical Characteristics* table and Figure 6-1 for timing details.

8.5.1 Recommended Programming Sequence

Registers are generally programmed in numeric order with 0x000 being the first and 0x555 being the last register programmed. The recommended programming sequence from POR involves:

1. Program register 0x000 with RESET = 1.
2. Program defined registers from 0x000 to 0x165.
3. If PLL2 is used, program 0x173 with PLL2_PD and PLL2_PRE_PD clear to allow PLL2 to lock after PLL2_N is programmed.
4. Continue programming defined registers from 0x166 to 0x555.

Note

When using the internal VCO, PLL2_N registers 0x166, 0x167, and 0x168 must be programmed after other PLL2 dividers are programed to ensure proper VCO frequency calibration. This is also true for PLL2_N_CAL registers 0x163, 0x164, 0x165 when PLL2_NCLK_MUX = 1. So if any divider such as PLL2_R is altered to change the VCO frequency, the VCO calibration must be run again by programming PLL2_N.

Power up PLL2 by setting PLL2_PRE_PD = 0 and PLL2_PD = 0 in register 0x173 before programming PLL2_N.

8.6 Register Maps

8.6.1 Register Map for Device Programming

Table 8-10 provides the register map for device programming. Any register can be read from the same data address it is written to.

Table 8-10. Register Map

ADDRESS [14:0]	DATA[7:0]							
23:8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x000	RESET	0	0	SPI_3WIRE_DIS	0	0	0	0
0x002	0	0	0	0	0	0	0	POWERDOWN
0x003	ID_DEVICE_TYPE							
0x004	ID_PROD[7:0]							
0x005	ID_PROD[15:8]							
0x006	ID_MASKREV							
0x00C	ID_VNDR[15:8]							
0x00D	ID_VNDR[7:0]							
0x100	DCLK0_1_DIV[7:0]							
0x101	DCLK0_1_DDLY[7:0]							
0x102	CLKout0_1_PD	CLKout0_1_ODL	CLKout0_1_IDL	DCLK0_1_DDLY_PD	DCLK0_1_DDLY[9:8]		DCLK0_1_DIV[9:8]	
0x103	0	1	CLKout0_SRC_MUX	DCLK0_1_PD	DCLK0_1_BYP	DCLK0_1_DCC	DCLK0_1_POL	DCLK0_1_HS
0x104	0	0	CLKout1_SRC_MUX	SCLK0_1_PD	SCLK0_1_DIS_MODE		SCLK0_1_POL	SCLK0_1_HS
0x105	0	0	SCLK0_1_ADLY_EN	SCLK0_1_ADLY				
0x106	0	0	0	0	SCLK0_1_DDLY			
0x107	CLKout1_FMT				CLKout0_FMT			
0x108	DCLK2_3_DIV[7:0]							
0x109	DCLK2_3_DDLY[7:0]							
0x10A	CLKout2_3_PD	CLKout2_3_ODL	CLKout2_3_IDL	DCLK2_3_DDLY_PD	DCLK2_3_DDLY[9:8]		DCLK2_3_DIV[9:8]	
0x10B	0	1	CLKout2_SRC_MUX	DCLK2_3_PD	DCLK2_3_BYP	DCLK2_3_DCC	DCLK2_3_POL	DCLK2_3_HS
0x10C	0	0	CLKout3_SRC_MUX	SCLK2_3_PD	SCLK2_3_DIS_MODE		SCLK2_3_POL	SCLK2_3_HS
0x10D	0	0	SCLK2_3_ADLY_EN	SCLK2_3_ADLY				
0x10E	0	0	0	0	SCLK2_3_DDLY			
0x10F	CLKout3_FMT				CLKout2_FMT			
0x110	DCLK4_5_DIV[7:0]							
0x111	DCLK4_5_DDLY[7:0]							
0x112	CLKout4_5_PD	CLKout4_5_ODL	CLKout4_5_IDL	DCLK4_5_DDLY_PD	DCLK4_5_DDLY[9:8]		DCLK4_5_DIV[9:8]	
0x113	0	1	CLKout4_SRC_MUX	DCLK4_5_PD	DCLK4_5_BYP	DCLK4_5_DCC	DCLK4_5_POL	DCLK4_5_HS
0x114	0	0	CLKout5_SRC_MUX	SCLK4_5_PD	SCLK4_5_DIS_MODE		SCLK4_5_POL	SCLK4_5_HS
0x115	0	0	SCLK4_5_ADLY_EN	SCLK4_5_ADLY				
0x116	0	0	0	0	SCLK4_5_DDLY			
0x117	CLKout5_FMT				CLKout4_FMT			
0x118	DCLK6_7_DIV[7:0]							

Table 8-10. Register Map (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x119	DCLK6_7_DDLY[7:0]							
0x11A	CLKout6_7_PD	CLKout6_7_ODL	CLKout6_7_IDL	DCLK6_7_DDLY_PD	DCLK6_7_DDLY[9:8]		DCLK6_7_DIV[9:8]	
0x11B	0	1	CLKout6_SRC_MUX	DCLK6_7_PD	DCLK6_7_BYP	DCLK6_7_DCC	DCLK6_7_POL	DCLK6_7_HS
0x11C	0	0	CLKout7_SRC_MUX	SCLK6_7_PD	SCLK6_7_DIS_MODE		SCLK6_7_POL	SCLK6_7_HS
0x11D	0	0	SCLK6_7_ADLY_EN	SCLK6_7_ADLY				
0x11E	0	0	0	0	SCLK6_7_DDLY			
0x11F	CLKout7_FMT				CLKout6_FMT			
0x120	DCLK8_9_DIV[7:0]							
0x121	DCLK8_9_DDLY[7:0]							
0x122	CLKout8_9_PD	CLKout8_9_ODL	CLKout8_9_IDL	DCLK8_9_DDLY_PD	DCLK8_9_DDLY[9:8]		DCLK8_9_DIV[9:8]	
0x123	0	1	CLKout8_SRC_MUX	DCLK8_9_PD	DCLK8_9_BYP	DCLK8_9_DCC	DCLK8_9_POL	DCLK8_9_HS
0x124	0	0	CLKout9_SRC_MUX	SCLK8_9_PD	SCLK8_9_DIS_MODE		SCLK8_9_POL	SCLK8_9_HS
0x125	0	0	SCLK8_9_ADLY_EN	SCLK8_9_ADLY				
0x126	0	0	0	0	SCLK8_9_DDLY			
0x127	CLKout9_FMT				CLKout8_FMT			
0x128	DCLK10_11_DIV[7:0]							
0x129	DCLK10_11_DDLY[7:0]							
0x12A	CLKout10_11_PD	CLKout10_11_ODL	CLKout10_11_IDL	DCLK10_11_DDLY_PD	DCLK10_11_DDLY[9:8]		DCLK10_11_DIV[9:8]	
0x12B	0	1	CLKout10_SRC_MUX	DCLK10_11_PD	DCLK10_11_BYP	DCLK10_11_DCC	DCLK10_11_POL	DCLK10_11_HS
0x12C	0	0	CLKout11_SRC_MUX	SCLK10_11_PD	SCLK10_11_DIS_MODE		SCLK10_11_POL	SCLK10_11_HS
0x12D	0	0	SCLK10_11_ADLY_EN	SCLK10_11_ADLY				
0x12E	0	0	0	0	SCLK10_11_DDLY			
0x12F	CLKout11_FMT				CLKout10_FMT			
0x130	DCLK12_13_DIV[7:0]							
0x131	DCLK12_13_DDLY[7:0]							
0x132	CLKout12_13_PD	CLKout12_13_ODL	CLKout12_13_IDL	DCLK12_13_DDLY_PD	DCLK12_13_DDLY[9:8]		DCLK12_13_DIV[9:8]	
0x133	0	1	CLKout12_SRC_MUX	DCLK12_13_PD	DCLK12_13_BYP	DCLK12_13_DCC	DCLK12_13_POL	DCLK12_13_HS
0x134	0	0	CLKout13_SRC_MUX	SCLK12_13_PD	SCLK12_13_DIS_MODE		SCLK12_13_POL	SCLK12_13_HS
0x135	0	0	SCLK12_13_ADLY_EN	SCLK12_13_ADLY				
0x136	0	0	0	0	SCLK12_13_DDLY			
0x137	CLKout13_FMT				CLKout12_FMT			
0x138	0	VCO_MUX		OSCout_MUX	OSCout_FMT			
0x139	0	0	0	SYSREF_REQ_EN	SYNC_BYPASS	0	SYSREF_MUX	
0x13A	0	0	0	SYSREF_DIV[12:8]				
0x13B	SYSREF_DIV[7:0]							
0x13C	0	0	0	SYSREF_DDLY[12:8]				
0x13D	SYSREF_DDLY[7:0]							

Table 8-10. Register Map (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	7	6	5	4	3	2	1	0
0x13E	0	0	0	0	0	SYSREF_PULSE_CNT		
0x13F	PLL2_RCLK_MUX	0	PLL2_NCLK_MUX	PLL1_NCLK_MUX		FB_MUX		FB_MUX_EN
0x140	PLL1_PD	VCO_LDO_PD	VCO_PD	OSCin_PD	SYSREF_GBL_PD	SYSREF_PD	SYSREF_DDLY_PD	SYSREF_PLSR_PD
0x141	DDLYd_SYSREF_EN	DDLYd12_EN	DDLYd10_EN	DDLYd8_EN	DDLYd6_EN	DDLYd4_EN	DDLYd2_EN	DDLYd0_EN
0x142	DDLYd_STEP_CNT							
0x143	SYSREF_CLR	SYNC_1SHOT_EN	SYNC_POL	SYNC_EN	SYNC_PLL2_DLD	SYNC_PLL1_DLD	SYNC_MODE	
0x144	SYNC_DISSYSREF	SYNC_DIS12	SYNC_DIS10	SYNC_DIS8	SYNC_DIS6	SYNC_DIS4	SYNC_DIS2	SYNC_DIS0
0x146	CLKin_SEL_PIN_EN	CLKin_SEL_PIN_POL	CLKin2_EN	CLKin1_EN	CLKin0_EN	CLKin2_TYPE	CLKin1_TYPE	CLKin0_TYPE
0x147	CLKin_SEL_AUTO_REVERT_EN	CLKin_SEL_AUTO_EN	CLKin_SEL_MANUAL		CLKin1_DEMUX		CLKin0_DEMUX	
0x148	0	0	CLKin_SEL0_MUX			CLKin_SEL0_TYPE		
0x149	0	SDIO_RDBK_TYPE	CLKin_SEL1_MUX			CLKin_SEL1_TYPE		
0x14A	0	0	RESET_MUX			RESET_TYPE		
0x14B	LOS_TIMEOUT		LOS_EN	TRACK_EN	HOLDOVER_FORCE	MAN_DAC_EN	MAN_DAC[9:8]	
0x14C	MAN_DAC[7:0]							
0x14D	0	0	DAC_TRIP_LOW					
0x14E	DAC_CLK_MULT		DAC_TRIP_HIGH					
0x14F	DAC_CLK_CNTR							
0x150	0	CLKin_OVERRIDE	HOLDOVER_EXIT_MODE	HOLDOVER_PLL1_DET	LOS_EXTERNAL_INPUT	HOLDOVER_VTUNE_DET	CLKin_SWITCH_CP_TRI	HOLDOVER_EN
0x151	0	0	HOLDOVER_DLD_CNT[13:8]					
0x152	HOLDOVER_DLD_CNT[7:0]							
0x153	0	0	CLKin0_R[13:8]					
0x154	CLKin0_R[7:0]							
0x155	0	0	CLKin1_R[13:8]					
0x156	CLKin1_R[7:0]							
0x157	0	0	CLKin2_R[13:8]					
0x158	CLKin2_R[7:0]							
0x159	0	0	PLL1_N[13:8]					
0x15A	PLL1_N[7:0]							
0x15B	PLL1_WND_SIZE		PLL1_CP_TRI	PLL1_CP_POL	PLL1_CP_GAIN			
0x15C	0	0	PLL1_DLD_CNT[13:8]					
0x15D	PLL1_DLD_CNT[7:0]							
0x15E	0	0	0	HOLDOVER_EXIT_NADJ				
0x15F	PLL1_LD_MUX					PLL1_LD_TYPE		
0x160	0	0	0	0	PLL2_R			
0x161	PLL2_R							
0x162	PLL2_P			0	OSCin_FREQ		0	PLL2_REF_2X_EN
0x163	0	0	0	0	0	0	PLL2_N_CAL[17:16]	
0x164	PLL2_N_CAL[15:8]							
0x165	PLL2_N_CAL[7:0]							

Table 8-10. Register Map (continued)

ADDRESS [14:0]	DATA[7:0]							
23:8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0x166	0	0	0	0	0	PLL2_FCAL_DIS	PLL2_N[17:16]	
0x167	PLL2_N[15:8]							
0x168	PLL2_N[7:0]							
0x169	0	PLL2_WND_SIZE		PLL2_CP_GAIN		PLL2_CP_POL	PLL2_CP_TRI	PLL2_DLD_EN
0x16A	0	0	PLL2_DLD_CNT[13:8]					
0x16B	PLL2_DLD_CNT[7:0]							
0x170	1	0	1	1	1	0	1	0
0x177	0	0	PLL1R_RST	0	0	0	0	0
0x182	0	0	0	0	0	0	CLR_PLL1_LD_LOST	CLR_PLL2_LD_LOST
0x183	0	0	0	0	RB_PLL1_DLD_LOST	RB_PLL1_DLD	RB_PLL2_DLD_LOST	RB_PLL2_DLD
0x184	RB_DAC_VALUE[9:8]		RB_CLKin2_SEL	RB_CLKin1_SEL	RB_CLKin0_SEL	RB_CLKin2_LOS	RB_CLKin1_LOS	RB_CLKin0_LOS
0x185	RB_DAC_VALUE[7:0]							
0x188	0	X	RB_HOLDOVER	X	RB_DAC_RAIL	RB_DAC_HIGH	RB_DAC_LOW	RB_DAC_LOCKED
0x555	SPI_LOCK							

8.6.2 Device Register Descriptions

The following section details the fields of each register, the Power-On-Reset Defaults, and specific descriptions of each bit.

In some cases similar fields are located in multiple registers. In this case specific outputs may be designated as X or Y. In these cases, the X represents even numbers from 0 to 12 and the Y represents odd numbers from 1 to 13. In the case where X and Y are both used in a bit name, then Y = X + 1.

Table 8-11. Device Register Descriptions Summary

Address Range	Functionality	Description
0x00 to 0x00D	System Functions	Read only information such as product and vendor ID, etc
0x100 to 0x137	Device Clock and SYSREF clock Output Controls	For each of the seven clock output pairs, a group of registers control each individual output's behavior. CLKout0_1: 0x100 to 0x107 CLKout2_3: 0x108 to 0x10F CLKout4_5: 0x110 to 0x117 CLKout6_7: 0x118 to 0x11F CLKout8_9: 0x120 to 0x127 CLKout10_11: 0x128 to 0x12F CLKout12_13: 0x130 to 0x137
0x138 and 0x145	SYSREF, SYNC, and Device Config	Settings for SYSREF and SYNC configurations such as SYSREF divide value, delay, pulse count, etc. Sets VCO and OSCout muxes output signal and OSCout's output format. Powerdown registers for device components (except CLKoutX_Y)
0x146 to 0x149	CLKin Control Control	Controls different behaviors for CLKinX such as selecting input clock source, enabling CLKinX, etc.
0x14A	RESET_MUX, RESET_TYPE	Controls the RESET_MUX and RESET_TYPE
0x14B to 0x152	Holdover	Controls different behaviors when enabling holdover
0x153 to 0x15F and 0x177	PLL1 Configuration	Controls different behaviors for PLL1 such as setting and syncing the R and N dividers, calibrating PLL1, etc.
0x160 to 0x173	PLL2 Configuration	Controls different behaviors for PLL2 such as setting and syncing the R and N dividers, calibrating PLL2, etc.
0x174 to 0x555 (except 0x177)	Misc Registers	Readback access for different registers and SPI Lock

8.6.2.1 System Functions

8.6.2.1.1 RESET, SPI_3WIRE_DIS

This register contains the RESET function and the ability to turn off 3-wire SPI mode. To use a 4-wire SPI mode, selecting SPI Read back in one of the output MUX settings. For example CLKin0_SEL_MUX or RESET_MUX. It is possible to have 3-wire and 4-wire readback at the same time.

Table 8-12. Register 0x000

BIT	NAME	POR DEFAULT	DESCRIPTION
7	RESET	0	0: Normal operation 1: Reset (automatically cleared)
6:5	NA	0	Reserved
4	SPI_3WIRE_DIS	0	Disable 3-wire SPI mode. 0: 3 Wire Mode enabled 1: 3 Wire Mode disabled
3:0	NA	NA	Reserved

8.6.2.1.2 POWERDOWN

This register contains the POWERDOWN function.

Table 8-13. Register 0x002

BIT	NAME	POR DEFAULT	DESCRIPTION
7:1	NA	0	Reserved
0	POWERDOWN	0	0: Normal operation 1: Power down device.

8.6.2.1.3 ID_DEVICE_TYPE

This register contains the product device type. This is read only register.

Table 8-14. Register 0x003

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_DEVICE_TYPE	6	PLL product device type.

8.6.2.1.4 ID_PROD

These registers contain the product identifier. This is a read only register.

Table 8-15. ID_PROD Field Registers

MSB	LSB
0x005[7:0] / ID_PROD[15:8]	0x004[7:0] / ID_PROD[7:0]

Table 8-16. Registers 0x004 and 0x005

REGISTER	BIT	FIELD NAME	POR DEFAULT	DESCRIPTION
0x005	7:0	ID_PROD[15:8]	209 (0xD1)	MSB of the product identifier.
0x004	7:0	ID_PROD[7:0]	99 (0x63)	LSB of the product identifier.

8.6.2.1.5 ID_MASKREV

This register contains the IC version identifier. This is a read only register.

Table 8-17. Register 0x006

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	ID_MASKREV	112 (0x70)	IC version identifier

8.6.2.1.6 ID_VNDR

These registers contain the vendor identifier. This is a read only register.

Table 8-18. ID_VNDR Field Registers

MSB	LSB
0x00C[7:0] / ID_VNDR[15:8]	0x00D[7:0] / ID_VNDR[7:0]

Table 8-19. Registers 0x00C, 0x00D

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION
0x00C	7:0	ID_VNDR[15:8]	81 (0x51)	MSB of the vendor identifier.
0x00D	7:0	ID_VNDR[7:0]	4 (0x04)	LSB of the vendor identifier.

8.6.2.2 (0x100 to 0x137) Device Clock and SYSREF Clock Output Controls

Table 8-20 lists all CLKoutX_Y groups and their respective registers with a brief description.

Table 8-20. Field Registers by Clock Output Group

Register Name	CLKout0 and CLKout1	CLKout2 and CLKout3	CLKout4 and CLKout5	CLKout6 and CLKout7	CLKout8 and CLKout9	CLKout10 and CLKout11	CLKout12 and CLKout13	Description
DCLKX_Y_DIV	0x102[1:0] and 0x100[7:0]	0x10A[1:0] and 0x108[7:0]	0x112[1:0] and 0x110[7:0]	0x11A[1:0] and 0x118[7:0]	0x122[1:0] and 0x120[7:0]	0x12A[1:0] and 0x128[7:0]	0x132[1:0] and 0x130[7:0]	Divides VCO frequency to obtain desired output frequency
DCLKX_Y_DDLY	0x102[2:3] and 0x101[7:0]	0x10A[2:3] and 0x109[7:0]	0x112[2:3] and 0x111[1:0]	0x11A[2:3] and 0x119[7:0]	0x122[2:3] and 0x121[7:0]	0x12A[2:3] and 0x129[7:0]	0x132[2:3] and 0x131[7:0]	Delays the output clock by a number of VCO cycles
CLKoutX_Y_PD	0x102[7]	0x10A[7]	0x112[7]	0x11A[7]	0x122[7]	0x12A[7]	0x132[7]	Powers down CLKout group
CLKoutX_Y_ODL	0x102[6]	0x10A[6]	0x112[6]	0x11A[6]	0x122[6]	0x12A[6]	0x132[6]	Sets output drive levels
CLKoutX_Y_IDL	0x102[5]	0x10A[5]	0x112[5]	0x11A[5]	0x122[5]	0x12A[5]	0x132[5]	Sets input drive levels
DCLKX_Y_DDLY_PD	0x102[4]	0x10A[4]	0x112[4]	0x11A[4]	0x122[4]	0x12A[4]	0x132[4]	Powers down digital delay
CLKoutX_SRC_MUX and CLKoutY_SRC_MUX	CLKout0: 0x103[5] and CLKout1: 0x104[5]	CLKout2: 0x10B[5] and CLKout3: 0x10C[5]	CLKout4: 0x113[5] and CLKout5: 0x114[5]	CLKout6: 0x11B[5] and CLKout7: 0x11C[5]	CLKout8: 0x123[5] and CLKout9: 0x124[5]	CLKout10: 0x12B[5] and CLKout11: 0x12C[5]	CLKout12: 0x133[5] and CLKout13: 0x134[5]	Selectes source
DCLKX_Y_PD	0x103[4]	0x10B[4]	0x113[4]	0x11B[4]	0x123[4]	0x12B[4]	0x133[4]	Powers down clock source
DCLKX_Y_BYP	0x103[3]	0x10B[3]	0x113[3]	0x11B[3]	0x123[3]	0x12B[3]	0x133[3]	Enables high perfomrnace bypass path
DCLKX_Y_DCC	0x103[2]	0x10B[2]	0x113[2]	0x11B[2]	0x123[2]	0x12B[2]	0x133[2]	Duty cycle correction for divider
DCLKX_Y_POL	0x103[1]	0x10B[1]	0x113[1]	0x11B[1]	0x123[1]	0x12B[1]	0x133[1]	Inverts polarity of device clock
DCLKX_Y_HS	0x103[0]	0x10B[0]	0x113[0]	0x11B[0]	0x123[0]	0x12B[0]	0x133[0]	Sets device clock half step
SCLKX_Y_PD	0x104[4]	0x10C[4]	0x114[4]	0x11C[4]	0x124[4]	0x12C[4]	0x134[4]	Powers down SYSREF
SCKX_Y_DIS_MODE	0x104[3:2]	0x10C[3:2]	0x114[3:2]	0x11C[3:2]	0x124[3:2]	0x12C[3:2]	0x134[3:2]	Sets disable mode when controlled by SYSREF
SCLKX_Y_POL	0x104[1]	0x10C[1]	0x114[1]	0x11C[1]	0x124[1]	0x12C[1]	0x134[1]	Inverts polarity of SYSREF clock
SCLKX_Y_HS	0x104[0]	0x10C[0]	0x114[0]	0x11C[0]	0x124[0]	0x12C[0]	0x134[0]	Sets SYSREF clock half step
SCLKX_Y_ADLY_EN	0x105[5]	0x10D[5]	0x115[5]	0x11D[5]	0x125[5]	0x12D[5]	0x135[5]	Enables analog delay

Table 8-20. Field Registers by Clock Output Group (continued)

Register Name	CLKout0 and CLKout1	CLKout2 and CLKout3	CLKout4 and CLKout5	CLKout6 and CLKout7	CLKout8 and CLKout9	CLKout10 and CLKout11	CLKout12 and CLKout13	Description
SCLKX_Y_ADLY	0x105[4:0]	0x10D[4:0]	0x115[4:0]	0x11D[4:0]	0x125[4:0]	0x12D[4:0]	0x135[4:0]	Sets analog delay for SYSREF clock
SCLKX_Y_DDLY	0x106[3:0]	0x10E[3:0]	0x116[3:0]	0x11E[3:0]	0x126[3:0]	0x12E[3:0]	0x136[3:0]	Sets digital delay for SYSREF clock
CLKoutX_FMT and CLKoutY_FMT	CLKout0: 0x107[3:0] and CLKout1: 0x107[7:4]	CLKout2: 0x10F[3:0] and CLKout3: 0x10F[7:4]	CLKout4: 0x117[3:0] and CLKout5: 0x117[7:4]	CLKout6: 0x11F[3:0] and CLKout7: 0x11F[7:4]	CLKout8: 0x127[3:0] and CLKout9: 0x127[7:4]	CLKout10: 0x12F[3:0] and CLKout11: 0x12F[7:4]	CLKout12: 0x137[3:0] and CLKout13: 0x137[7:4]	Sets clock formats

8.6.2.2.1 DCLKX_Y_DIV

The device clock divider can drive up to two outputs, an even (X) and an odd (Y) clock output. Divide is a 10 bit number and split across two registers.

Table 8-21. DCLKX_Y_DIV Field Registers

MSB	LSB
0x0102[1:0] = DCLK0_1_DIV[9:8]	0x100[7:0] = DCLK0_1_DIV[7:0]
0x010A[1:0] = DCLK2_3_DIV[9:8]	0x108[7:0] = DCLK2_3_DIV[7:0]
0x0112[1:0] = DCLK4_5_DIV[9:8]	0x110[7:0] = DCLK4_5_DIV[7:0]
0x011A[1:0] = DCLK6_7_DIV[9:8]	0x118[7:0] = DCLK6_7_DIV[7:0]
0x0122[1:0] = DCLK8_9_DIV[9:8]	0x120[7:0] = DCLK8_9_DIV[7:0]
0x012A[1:0] = DCLK10_11_DIV[9:8]	0x128[7:0] = DCLK10_11_DIV[7:0]
0x0132[1:0] = DCLK12_13_DIV[9:8]	0x130[7:0] = DCLK12_13_DIV[7:0]

Table 8-22. Registers 0x100, 0x108, 0x110, 0x118, 0x120, 0x128, and 0x130 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="3">0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132</td><td rowspan="3">1:0</td><td rowspan="3">DCLKX_Y_DIV[9:8]</td><td rowspan="8">X_Y = 0_1 → 2
X_Y = 2_3 → 4
X_Y = 4_5 → 8
X_Y = 6_7 → 8
X_Y = 8_9 → 8
X_Y = 10_11 → 8
X_Y = 12_13 → 2</td><td colspan="2">DCLKX_Y_DIV sets the divide value for the clock output, the divide may be even or odd. Both even or odd divides output a 50% duty cycle clock if duty cycle correction (DCC) is enabled.</td></tr>
<tr><td>Field Value</td><td>Divider Value</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td rowspan="5">0x100, 0x108, 0x110, 0x118, 0x120, 0x128, and 0x130</td><td rowspan="5">7:0</td><td rowspan="5">DCLKX_Y_DIV[7:0]</td><td>1 (0x01)</td><td>1 (1)</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>1022 (0x3FE)</td><td>1022</td></tr>
<tr><td>1023 (0x3FF)</td><td>1023</td></tr>
</table>

(1) Duty cycle correction must also be enabled, DCLKX_Y_DCC = 1.

8.6.2.2.2 DCLKX_Y_DDLY

This register controls the digital delay for the device clock outputs.

Table 8-23. DCLKX_Y_DDLY Field Registers

MSB	LSB
0x0102[2:3] = DCLK0_1_DDLY[9:8]	0x101[7:0] = DCLK0_1_DDLY[7:0]
0x010A[2:3] = DCLK2_3_DDLY[9:8]	0x109[7:0] = DCLK2_3_DDLY[7:0]
0x0112[2:3] = DCLK4_5_DDLY[9:8]	0x111[7:0] = DCLK4_5_DDLY[7:0]
0x011A[2:3] = DCLK6_7_DDLY[9:8]	0x119[7:0] = DCLK6_7_DDLY[7:0]
0x0122[2:3] = DCLK8_9_DDLY[9:8]	0x121[7:0] = DCLK8_9_DDLY[7:0]
0x012A[2:3] = DCLK10_11_DDLY[9:8]	0x129[7:0] = DCLK10_11_DDLY[7:0]
0x0132[2:3] = DCLK12_13_DDLY[9:8]	0x131[7:0] = DCLK12_13_DDLY[7:0]

Table 8-24. Registers 0x101, 0x109, 0x111, 0x119, 0x121, 0x129, 0x131 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="5">0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132</td><td rowspan="5">2:3</td><td rowspan="5">DCLKX_Y_DDLY[9:8]</td><td rowspan="11">10 (0x0A)</td><td colspan="2">Static digital delay which takes effect after a SYNC.</td></tr>
<tr><td>Field Value</td><td>Delay Values</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>Reserved</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td rowspan="6">0x101, 0x109, 0x111, 0x119, 0x121, 0x129, 0x131</td><td rowspan="6">7:0</td><td rowspan="6">DCLKX_Y_DDLY[7:0]</td><td>7 (0x07)</td><td>Reserved</td></tr>
<tr><td>8 (0x08)</td><td>8</td></tr>
<tr><td>9 (0x09)</td><td>9</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>1022 (0x3FE)</td><td>1022</td></tr>
<tr><td>1023 (0x3FF)</td><td>1023</td></tr>
</table>

Depending on the DCLK divide value, there may be an adjustment in phase delay required. Table 8-25 illustrate the impact of different divide values on the final digital delay.

Table 8-25. Digital Delay Adjustment based on Divide Values

DIVIDE VALUE	DIGITAL DELAY ADJUSTMENT
2, 3	–2[(1)]
4, 7 to 1023	0
5	+2
6	+1

(1) Before SYNC, program divider to Divide-by-4, then back to Divide-by-2 or Divide-by-3 to ensure '-2' delay relationship.

For example, Table 8-26 shows a system with clock outputs having divide values /2,/4,/5 and /6 to share a common edge.

Table 8-26. Digital Delay Adjustment Illustration

DIVIDE VALUE	PROGRAMMED DDLY	ACTUAL DDLY
2	13	11
4	11	11
5	8	11
6	10	11

8.6.2.2.3 CLKoutX_Y_PD, CLKoutX_Y_ODL, CLKoutX_Y_IDL, DCLKX_Y_DDLY_PD, DCLKX_Y_DDLY[9:8], DCLKX_Y_DIV[9:8]

Table 8-27. Registers 0x102, 0x10A, 0x112, 0x11A, 0x122, 0x12A, 0x132

BIT	NAME	POR DEFAULT	DESCRIPTION
7	CLKoutX_Y_PD	1	Power down the clock group defined by X and Y. 0: Enabled 1: Power down entire clock group including both CLKoutX and CLKoutY.
6	CLKoutX_Y_ODL	0	Sets output drive level for clocks. This has no impact for the even clock output in bypass mode. 0: Normal operation 1: Higher current consumption and lower noise floor.
5	CLKoutX_Y_IDL	0	Sets input drive level for clocks. 0: Normal operation 1: Higher current consumption and lower noise floor.
4	DCLKX_Y_DDLY_PD	0	Powerdown the device clock digital delay circuitry. 0: Enabled 1: Power down static digital delay for device clock divider.
3:2	DCLKX_Y_DDLY[9:8]	0	MSB of static digital delay, see *DCLKX_Y_DDLY*.
1:0	DCLKX_Y_DIV[9:8]	0	MSB of device clock divide value, see Table 8-22.

8.6.2.2.4 CLKoutX_SRC_MUX, DCLKX_Y_PD, DCLKX_Y_BYP, DCLKX_Y_DCC, DCLKX_Y_POL, DCLKX_Y_HS

These registers control the analog delay properties for the device clocks.

Table 8-28. Registers 0x103, 0x10B, 0x113, 0x11B, 0x123, 0x12B, 0x133

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	NA	1	Reserved
5	CLKoutX_SRC_MUX	0	Select CLKoutX clock source. Source must also be powered up. 0: Device Clock 1: SYSREF
4	DCLKX_Y_PD	0	Power down the clock group defined by X and Y. 0: Enabled 1: Power down enter clock group X_Y.
3	DCLKX_Y_BYP	0	Enable high performance bypass path for even clock outputs. 0: CLKoutX not in high performance bypass mode. CML is not valid for CLKoutX_FMT. 1: CLKoutX in high performance bypass mode. Only CML clock format is valid.
2	DCLKX_Y_DCC	0	Duty cycle correction for device clock divider. Required for half step. 0: No duty cycle correction. 1: Duty cycle correction enabled.
1	DCLKX_Y_POL	0	Invert polarity of device clock output. This also applies to CLKoutX in high performance bypass mode. Polarity invert is a method to get a half-step phase adjustment in high performance bypass mode or /1 divide value. 0: Normal polarity 1: Invert polarity
0	DCLKX_Y_HS	0	Sets the device clock half step value. Must be set to zero (0) for a divide of 1. No effect if DCLKX_Y_DCC = 0. 0: No phase adjustment 1: Adjust device clock phase –0.5 clock distribution path cycles.

8.6.2.2.5 CLKoutY_SRC_MUX, SCLKX_Y_PD, SCLKX_Y_DIS_MODE, SCLKX_Y_POL, SCLKX_Y_HS

These registers set the half step for the device clock, the SYSREF output MUX, the SYSREF clock digital delay, and half step.

Table 8-29. Registers 0x104, 0x10C, 0x114, 0x11C, 0x124, 0x12C, 0x134

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>5</td><td>CLKoutY_SRC_MUX</td><td>0</td><td colspan="2">Select CLKoutX clock source. Source must also be powered up.
0: Device Clock
1: SYSREF</td></tr>
<tr><td>4</td><td>SCLKX_Y_PD</td><td>1</td><td colspan="2">Power down the SYSREF clock output circuitry.
0: SYSREF enabled
1: Power down SYSREF path for clock pair.</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">SCLKX_Y_DIS_MODE</td><td rowspan="6">0</td><td colspan="2">Set disable mode for clock outputs controlled by SYSREF. Some cases will assert when SYSREF_GBL_PD = 1.</td></tr>
<tr><td>Field Value</td><td>Disable Mode</td></tr>
<tr><td>0 (0x00)</td><td>Active in normal operation</td></tr>
<tr><td>1 (0x01)</td><td>If SYSREF_GBL_PD = 1, the output is a logic low, otherwise it is active.</td></tr>
<tr><td>2 (0x02)</td><td>If SYSREF_GBL_PD = 1, the output is a nominal Vcm voltage for odd clock channels[1] and low for even clocks. Otherwise outputs are active.</td></tr>
<tr><td>3 (0x03)</td><td>Output is a nominal Vcm voltage[1]</td></tr>
</table>

Table 8-29. Registers 0x104, 0x10C, 0x114, 0x11C, 0x124, 0x12C, 0x134 (continued)

BIT	NAME	POR DEFAULT	DESCRIPTION
1	SCLKX_Y_POL	0	Sets the polarity of clock on SCLKX_Y when SYSREF clock output is selected with CLKoutX_MUX or CLKoutY_MUX. 0: Normal 1: Inverted
0	SCLKX_Y_HS	0	Sets the local SYSREF clock half step value. 0: No phase adjustment 1: Adjust device SYSREF phase -0.5 clock distribution path cycles.

(1) If LVPECL mode is used with emitter resistors to ground, the output Vcm will be approximately 0 V, each pin will be approximately 0 V. If CML mode is used with pullups to V_{CC}, the output V_{CM} will be approximately V_{CC} V, each pin will be approximately V_{CC} V.

8.6.2.2.6 SCLKX_Y_ADLY_EN, SCLKX_Y_ADLY

These registers set the analog delay parameters for the SYSREF outputs.

Table 8-30. Registers 0x105, 0x10D, 0x115, 0x11D, 0x125, 0x12D, 0x135

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5	SCLKX_Y_ADLY_EN	0	Enables analog delay for the SYSREF output. 0: Disabled 1: Enabled	
4:0	SCLKX_Y_ADLY	0	SYSREF analog delay in approximately 21 ps steps. Selecting analog delay adds an additional 125 ps in propagation delay. Range is 125 ps to 608 ps.	
			Field Value	**Delay Value**
			0 (0x0)	125 ps
			1 (0x1)	146 ps (+21 ps from 0x00)
			2 (0x2)	167 ps (+42 ps from 0x00)
			3 (0x3)	188 ps (+63 ps from 0x00)
			...	...
			14 (0xE)	587 ps (+462 ps from 0x00)
			15 (0xF)	608 ps (+483 ps from 0x00)

8.6.2.2.7 SCLKX_Y_DDLY

Table 8-31. Registers 0x106, 0x10E, 0x116, 0x11E, 0x126, 0x12E, 0x136

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:4	NA	0	Reserved	
3:0	SCLKX_Y_DDLY	0	Sets the number of VCO cycles to delay SDCLKout by	
			Field Value	**Delay Cycles**
			0 (0x00)	Bypass
			1 (0x01)	2
			2 (0x02)	3
			...	...
			10 (0x0A)	11
			11 to 15 (0x0B to 0x0F)	Reserved

8.6.2.2.8 CLKoutY_FMT, CLKoutX_FMT

The difference in the tables is that some of the clock outputs have inverted CMOS polarity settings.

Table 8-32. Registers 0x107 (CLKout0_1), 0x11F (CLKout6_7), 0x12F (CLKout10_11)

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="18">7:4</td><td rowspan="18">CLKoutY_FMT</td><td rowspan="18">0</td><td colspan="3">Set CLKoutY clock format</td></tr>
<tr><td>Field Value</td><td colspan="2">Output Format</td></tr>
<tr><td>0 (0x00)</td><td colspan="2">Powerdown</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">LVDS</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">HSDS 6 mA</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">HSDS 8 mA</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">LVPECL 1600 mV</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">LVPECL 2000 mV</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">LCPECL</td></tr>
<tr><td>7 (0x07)</td><td colspan="2">CML 16 mA</td></tr>
<tr><td>8 (0x08)</td><td colspan="2">CML 24 mA</td></tr>
<tr><td>9 (0x09)</td><td colspan="2">CML 32 mA</td></tr>
<tr><td>10 (0x0A)</td><td colspan="2">CMOS (Off/Inv)</td></tr>
<tr><td>11 (0x0B)</td><td colspan="2">CMOS (Norm/Off)</td></tr>
<tr><td>12 (0x0C)</td><td colspan="2">CMOS (Inv/Inv)</td></tr>
<tr><td>13 (0x0D)</td><td colspan="2">CMOS (Inv/Norm)</td></tr>
<tr><td>14 (0x0E)</td><td colspan="2">CMOS (Norm/Inv)</td></tr>
<tr><td>15 (0x0F)</td><td colspan="2">CMOS (Norm/Norm)</td></tr>
<tr><td rowspan="18">3:0</td><td rowspan="18">CLKoutX_FMT</td><td rowspan="18">0</td><td colspan="3">Set CLKoutX clock format</td></tr>
<tr><td>Field Value</td><td>Output Format DCLKX_BYP = 0</td><td>Output Format DCLKX_BYP = 1</td></tr>
<tr><td>0 (0x00)</td><td>Powerdown</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>LVDS</td><td>Reserved</td></tr>
<tr><td>2 (0x02)</td><td>HSDS 6 mA</td><td>Reserved</td></tr>
<tr><td>3 (0x03)</td><td>HSDS 8 mA</td><td>Reserved</td></tr>
<tr><td>4 (0x04)</td><td>LVPECL 1600 mV</td><td>Reserved</td></tr>
<tr><td>5 (0x05)</td><td>LVPECL 2000 mV</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>LCPECL</td><td>Reserved</td></tr>
<tr><td>7 (0x07)</td><td>Reserved</td><td>CML 16 mA</td></tr>
<tr><td>8 (0x08)</td><td>Reserved</td><td>CML 24 mA</td></tr>
<tr><td>9 (0x09)</td><td>Reserved</td><td>CML 32 mA</td></tr>
<tr><td>10 (0x0A)</td><td>CMOS (Off/Inv)(1)</td><td>Reserved</td></tr>
<tr><td>11 (0x0B)</td><td>CMOS (Norm/Off)(1)</td><td>Reserved</td></tr>
<tr><td>12 (0x0C)</td><td>CMOS (Inv/Inv)(1)</td><td>Reserved</td></tr>
<tr><td>13 (0x0D)</td><td>CMOS (Inv/Norm)(1)</td><td>Reserved</td></tr>
<tr><td>14 (0x0E)</td><td>CMOS (Norm/Inv)(1)</td><td>Reserved</td></tr>
<tr><td>15 (0x0F)</td><td>CMOS (Norm/Norm)(1)</td><td>Reserved</td></tr>
</table>

(1) Only valid for CLKout10.

Table 8-33. Registers 0x10F (CLKout2_3), 0x117 (CLKout4_5), 0x127 (CLKout8_9), 0x137 (CLKout12_13)

BIT	NAME	POR DEFAULT	DESCRIPTION		
7:4	CLKoutY_FMT	0	Set CLKoutY clock format		
			Field Value	**Output Format**	
			0 (0x00)	Powerdown	
			1 (0x01)	LVDS	
			2 (0x02)	HSDS 6 mA	
			3 (0x03)	HSDS 8 mA	
			4 (0x04)	LVPECL 1600 mV	
			5 (0x05)	LVPECL 2000 mV	
			6 (0x06)	LCPECL	
			7 (0x07)	CML 16 mA	
			8 (0x08)	CML 24 mA	
			9 (0x09)	CML 32 mA	
			10 (0x0A)	CMOS (Off/Norm)	
			11 (0x0B)	CMOS (Inv/Off)	
			12 (0x0C)	CMOS (Norm/Norm)	
			13 (0x0D)	CMOS (Norm/Inv)	
			14 (0x0E)	CMOS (Inv/Norm)	
			15 (0x0F)	CMOS (Inv/Inv)	
3:0	CLKoutX_FMT	0	Set CLKoutX clock format		
			Field Value	**Output Format DCLKX_BYP = 0**	**Output Format DCLKX_BYP = 1**
			0 (0x00)	Powerdown	Reserved
			1 (0x01)	LVDS	Reserved
			2 (0x02)	HSDS 6 mA	Reserved
			3 (0x03)	HSDS 8 mA	Reserved
			4 (0x04)	LVPECL 1600 mV	Reserved
			5 (0x05)	LVPECL 2000 mV	Reserved
			6 (0x06)	LCPECL	Reserved
			7 (0x07)	Reserved	CML 16 mA
			8 (0x08)	Reserved	CML 24 mA
			9 (0x09)	Reserved	CML 32 mA
			10 (0x0A)	CMOS (Off/Norm)[(1)]	Reserved
			11 (0x0B)	CMOS (Inv/Off)[(1)]	Reserved
			12 (0x0C)	CMOS (Norm/Norm)[(1)]	Reserved
			13 (0x0D)	CMOS (Norm/Inv)[(1)]	Reserved
			14 (0x0E)	CMOS (Inv/Norm)[(1)]	Reserved
			15 (0x0F)	CMOS (Inv/Inv)[(1)]	Reserved

(1) Only valid for CLKout8.

8.6.2.3 SYSREF, SYNC, and Device Config

8.6.2.3.1 VCO_MUX, OSCout_MUX, OSCout_FMT

Table 8-34. Register 0x138

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	NA	0	Reserved	
6:5	VCO_MUX	2	Selects clock distribution path source from VCO0, VCO1, or CLKIN (external VCO)	
			Field Value	**VCO Selected**
			0 (0x00)	VCO 0
			1 (0x01)	VCO 1
			2 (0x02)	FIN1 / CLKIN1 (external VCO)
			3 (0x03)	FIN0
4	OSCout_MUX	0	Select the source for OSCout: 0: Buffered OSCIN 1: Feedback Mux	
3:0	OSCout_FMT	4	Selects the output format of OSCout. When powered down, these pins may be used as CLKIN2.	
			Field Value	**OSCOUT Format**
			0 (0x00)	Power down (CLKIN2)
			1 (0x01)	LVDS
			2 (0x02)	Reserved
			3 (0x03)	Reserved
			4 (0x04)	LVPECL 1600 mVpp
			5 (0x05)	LVPECL 2000 mVpp
			6 (0x06)	LVCMOS (Norm / Inv)
			7 (0x07)	LVCMOS (Inv / Norm)
			8 (0x08)	LVCMOS (Norm / Norm)
			9 (0x09)	LVCMOS (Inv / Inv)
			10 (0x0A)	LVCMOS (Off / Norm)
			11 (0x0B)	LVCMOS (Off / Inv)
			12 (0x0C)	LVCMOS (Norm / Off)
			13 (0x0D)	LVCMOS (Inv / Off)
			14 (0x0E)	LVCMOS (Off / Off)

8.6.2.3.2 SYSREF_REQ_EN, SYNC_BYPASS, SYSREF_MUX

This register sets the source for the SYSREF outputs. Refer to Figure 8-3 and *SYNC/SYSREF*.

Table 8-35. Register 0x139

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>5</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>4</td><td>SYSREF_REQ_EN</td><td>0</td><td colspan="2">Enables the SYNC/SYSREF_REQ pin to force the SYSREF_MUX = 3 for continuous pulses. When using this feature enable pulser and set SYSREF_MUX = 2 (Pulser).</td></tr>
<tr><td>3</td><td>SYNC_BYPASS</td><td>0</td><td colspan="2">Bypass SYNC polarity invert and other circuitry.
0: Normal
1: SYNC signal is bypassed</td></tr>
<tr><td>2</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">SYSREF_MUX</td><td rowspan="6">0</td><td colspan="2">Selects the SYSREF source.</td></tr>
<tr><td>Field Value</td><td>SYSREF Source</td></tr>
<tr><td>0 (0x00)</td><td>Normal SYNC</td></tr>
<tr><td>1 (0x01)</td><td>Re-clocked</td></tr>
<tr><td>2 (0x02)</td><td>SYSREF Pulser</td></tr>
<tr><td>3 (0x03)</td><td>SYSREF Continuous</td></tr>
</table>

8.6.2.3.3 SYSREF_DIV

These registers set the value of the SYSREF output divider.

Table 8-36. SYSREF_DIV[12:0]

MSB	LSB
0x13A[4:0] = SYSREF_DIV[12:8]	0x13B[7:0] = SYSREF_DIV[7:0]

Table 8-37. Registers 0x13A and 0x13B

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x13A</td><td>7:5</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x13A</td><td rowspan="4">4:0</td><td rowspan="4">SYSREF_DIV[12:8]</td><td rowspan="4">12</td><td colspan="2">Divide value for the SYSREF outputs.</td></tr>
<tr><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 to 7 (0x00 to 0x07)</td><td>Reserved</td></tr>
<tr><td>8 (0x08)</td><td>8</td></tr>
<tr><td rowspan="4">0x13B</td><td rowspan="4">7:0</td><td rowspan="4">SYSREF_DIV[7:0]</td><td rowspan="4">0</td><td>9 (0x09)</td><td>9</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>8190 (0x1FFE)</td><td>8190</td></tr>
<tr><td>8191 (0X1FFF)</td><td>8191</td></tr>
</table>

8.6.2.3.4 SYSREF_DDLY

These registers set the delay of the SYSREF digital delay value.

Table 8-38. SYSREF Digital Delay Register Configuration, SYSREF_DDLY[12:0]

MSB	LSB
0x13C[4:0] / SYSREF_DDLY[12:8]	0x13D[7:0] / SYSREF_DDLY[7:0]

Table 8-39. Registers 0X13C and 0X13D

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION
0x13C	7:5	NA	0	Reserved

Table 8-39. Registers 0X13C and 0X13D (continued)

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x13C	4:0	SYSREF_DDLY[12:8]	0	Sets the value of the SYSREF digital delay.	
				Field Value	**Delay Value**
				0x00 to 0x07	Reserved
				8 (0x08)	8
0x13D	7:0	SYSREF_DDLY[7:0]	8	9 (0x09)	9
				...	...
				8190 (0x1FFE)	8190
				8191 (0X1FFF)	8191

8.6.2.3.5 SYSREF_PULSE_CNT

This register sets the number of SYSREF pulses if SYSREF is not in continuous mode. See *SYSREF_REQ_EN, SYNC_BYPASS, SYSREF_MUX* for further description of SYSREF's outputs.

Programming the register causes the specified number of pulses to be output if "SYSREF Pulses" is selected by SYSREF_MUX and SYSREF functionality is powered up.

Table 8-40. Register 0x13E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:2	NA	0	Reserved	
1:0	SYSREF_PULSE_CNT	3	Sets the number of SYSREF pulses generated when not in continuous mode. See *SYSREF_REQ_EN, SYNC_BYPASS, SYSREF_MUX* for more information on SYSREF modes.	
			Field Value	**Number of Pulses**
			0 (0x00)	1 pulse
			1 (0x01)	2 pulses
			2 (0x02)	4 pulses
			3 (0x03)	8 pulses

8.6.2.3.6 PLL2_RCLK_MUX, PLL2_NCLK_MUX, PLL1_NCLK_MUX, FB_MUX, FB_MUX_EN

This register controls the feedback feature.

Table 8-41. Register 0x13F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	PLL2_RCLK_MUX	0	Selects the source for PLL2 reference. 0: OSCIN 1: Currently selected CLKIN.	
6	NA	0	Reserved	
5	PLL2_NCLK_MUX	0	Selects the input to the PLL2 N Divider 0: PLL2 Prescaler 1: Feedback Mux	
4:3	PLL1_NCLK_MUX	0	Selects the input to the PLL1 N Divider. 0: OSCIN 1: Feedback Mux 2: PLL2 Prescaler	
2:1	FB_MUX	0	When in 0-delay mode, the feedback mux selects the clock output to be fed back into the PLL1 N Divider.	
			Field Value	**Source**
			0 (0x00)	CLKOUT6
			1 (0x01)	CLKOUT8
			2 (0x02)	SYSREF Divider
			3 (0x03)	External

Table 8-41. Register 0x13F (continued)

BIT	NAME	POR DEFAULT	DESCRIPTION
0	FB_MUX_EN	0	When using 0-delay, FB_MUX_EN must be set to 1 power up the feedback mux. 0: Feedback mux powered down 1: Feedback mux enabled

8.6.2.3.7 PLL1_PD, VCO_LDO_PD, VCO_PD, OSCin_PD, SYSREF_GBL_PD, SYSREF_PD, SYSREF_DDLY_PD, SYSREF_PLSR_PD

This register contains power-down controls for OSCIN and SYSREF functions.

Table 8-42. Register 0x140

BIT	NAME	POR DEFAULT	DESCRIPTION
7	PLL1_PD	1	Power down PLL1 0: Normal operation 1: Power down
6	VCO_LDO_PD	1	Power down VCO_LDO 0: Normal operation 1: Power down
5	VCO_PD	1	Power down VCO 0: Normal operation 1: Power down
4	OSCin_PD	0	Power down the OSCIN port. 0: Normal operation 1: Power down
3	SYSREF_GBL_PD	0	Power down individual SYSREF outputs depending on the setting of SCLKX_Y_DIS_MODE for each SYSREF output. SYSREF_GBL_PD allows many SYSREF outputs to be controlled through a single bit. 0: Normal operation 1: Activate Power down Mode
2	SYSREF_PD	0	Power down the SYSREF circuitry and divider. If powered down, SYSREF output mode cannot be used. SYNC cannot be provided either. 0: SYSREF can be used as programmed by individual SYSREF output registers. 1: Power down
1	SYSREF_DDLY_PD	0	Power down the SYSREF digital delay circuitry. 0: Normal operation, SYSREF digital delay may be used. Must be powered up during SYNC for deterministic phase relationship with other clocks. 1: Power down
0	SYSREF_PLSR_PD	0	Power down the SYSREF pulse generator. 0: Normal operation 1: Power down

8.6.2.3.8 DDLYdSYSREF_EN, DDLYdX_EN

This register enables dynamic digital delay for enabled device clocks and SYSREF when DDLYd_STEP_CNT is programmed.

Table 8-43. Register 0x141

BIT	NAME	POR DEFAULT	DESCRIPTION	
7	DDLYd _SYSREF_EN	0	Enables dynamic digital delay on SYSREF outputs	0: Disabled 1: Enabled
6	DDLYd12_EN	0	Enables dynamic digital delay on DCLKout12	
5	DDLYd10_EN	0	Enables dynamic digital delay on DCLKout10	
4	DDLYd8_EN	0	Enables dynamic digital delay on DCLKout8	
3	DDLYd6_EN	0	Enables dynamic digital delay on DCLKout6	
2	DDLYd4_EN	0	Enables dynamic digital delay on DCLKout4	
1	DDLYd2_EN	0	Enables dynamic digital delay on DCLKout2	
0	DDLYd0_EN	0	Enables dynamic digital delay on DCLKout0	

8.6.2.3.9 DDLYd_STEP_CNT

This register sets the number of dynamic digital delay adjustments that will occur. Upon programming, the dynamic digital delay adjustment begins for each clock output with dynamic digital delay enabled. Dynamic digital delay can only be started by SPI.

Other registers must be set: SYNC_MODE = 3

Table 8-44. Register 0x142

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:0	DDLYd_STEP_CNT	0	Sets the number of dynamic digital delay adjustments that will occur.	
			Field Value	**Dynamic Digital Delay Adjustments**
			0 (0x00)	No Adjust
			1 (0x01)	1 step
			2 (0x02)	2 steps
			3 (0x03)	3 steps
			...	...
			254 (0xFE)	254 steps
			255 (0xFF)	255 steps

8.6.2.3.10 SYSREF_CLR, SYNC_1SHOT_EN, SYNC_POL, SYNC_EN, SYNC_PLL2_DLD, SYNC_PLL1_DLD, SYNC_MODE

This register sets general SYNC parameters such as polarization, and mode. Refer to Figure 8-3 for block diagram. Refer to Table 8-2 for using SYNC_MODE for specific SYNC use cases.

Table 8-45. Register 0x143

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>SYSREF_CLR</td><td>0</td><td colspan="2">Except during SYSREF Setup Procedure (see SYNC/SYSREF), this bit should always be programmed to 0. While this bit is set, extra current is used.</td></tr>
<tr><td>6</td><td>SYNC_1SHOT_EN</td><td>0</td><td colspan="2">SYNC one shot enables edge sensitive SYNC.
0: SYNC is level sensitive and outputs will be held in SYNC as long as SYNC is asserted.
1: SYNC is edge sensitive, outputs will be SYNCed on rising edge of SYNC. This results in the clock being held in SYNC for a minimum amount of time.</td></tr>
<tr><td>5</td><td>SYNC_POL</td><td>0</td><td colspan="2">Sets the polarity of the SYNC pin.
0: Not Inverted
1: Inverted</td></tr>
<tr><td>4</td><td>SYNC_EN</td><td>0</td><td colspan="2">Enables the SYNC functionality.
0: Disabled
1: Enabled</td></tr>
<tr><td>3</td><td>SYNC_PLL2_DLD</td><td>0</td><td colspan="2">0: Off
1: Assert SYNC until PLL2 DLD = 1</td></tr>
<tr><td>2</td><td>SYNC_PLL1_DLD</td><td>0</td><td colspan="2">0: Off
1: Assert SYNC until PLL1 DLD = 1</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">SYNC_MODE</td><td rowspan="6">1</td><td colspan="2">Sets the method of generating a SYNC event.</td></tr>
<tr><td>Field Value</td><td>SYNC Generation</td></tr>
<tr><td>0 (0x00)</td><td>Prevent SYNC Pin, SYNC_PLL1_DLD flag, or SYNC_PLL2_DLD flag from generating a SYNC event.</td></tr>
<tr><td>1 (0x01)</td><td>SYNC event generated from SYNC pin or if enabled the SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.</td></tr>
<tr><td>2 (0x02)</td><td>For use with pulser - SYNC/ SYSREF pulses are generated by pulser block via SYNC Pin or if enabled SYNC_PLL1_DLD flag or SYNC_PLL2_DLD flag.</td></tr>
<tr><td>3 (0x03)</td><td>For use with pulser - SYNC/SYSREF pulses are generated by pulser block when programming register 0x13E (SYSREF_PULSE_CNT) is written to (see SYSREF_PULSE_CNT).</td></tr>
</table>

8.6.2.3.11 SYNC_DISSYSREF, SYNC_DISX

SYNC_DISX will prevent a clock output from being synchronized or interrupted by a SYNC event or when outputting SYSREF.

Table 8-46. Register 0x144

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>SYNC_DISSYSREF</td><td>0</td><td>Prevent the SYSREF clocks from becoming synchronized during a SYNC event. If SYNC_DISSYSREF is enabled, the device will continue to operate normally during a SYNC event.</td></tr>
<tr><td>6</td><td>SYNC_DIS12</td><td>0</td><td rowspan="7">Prevent the device clock output from becoming synchronized during a SYNC event or SYSREF clock. If SYNC_DIS bit for a particular output is enabled, then the device will continue to operate normally during a SYNC event or SYSREF clock.</td></tr>
<tr><td>5</td><td>SYNC_DIS10</td><td>0</td></tr>
<tr><td>4</td><td>SYNC_DIS8</td><td>0</td></tr>
<tr><td>3</td><td>SYNC_DIS6</td><td>0</td></tr>
<tr><td>2</td><td>SYNC_DIS4</td><td>0</td></tr>
<tr><td>1</td><td>SYNC_DIS2</td><td>0</td></tr>
<tr><td>0</td><td>SYNC_DIS0</td><td>0</td></tr>
</table>

8.6.2.3.12 PLL1R_SYNC_EN, PLL1R_SYNC_SRC, PLL2R_SYNC_EN, FIN0_DIV2_EN, FIN0_INPUT_TYPE

These bits are used when synchronizing PLL1 and PLL2 R dividers.

Table 8-47. Register 0x145

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>6</td><td>PLL1R_SYNC_EN</td><td>0</td><td colspan="2">Enable synchronization for PLL1 R divider
0: Not enabled
1: Enabled</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">PLL1R_SYNC_SRC</td><td rowspan="6">0</td><td colspan="2">Select the source for PLL1 R divider synchronization</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>SYNC Pin</td></tr>
<tr><td>2 (0x02)</td><td>CLKIN0</td></tr>
<tr><td>3 (0x03)</td><td>Reserved</td></tr>
<tr><td>3</td><td>PLL2R_SYNC_EN</td><td>0</td><td colspan="2">Enable synchronization for PLL2 R divider. Synchronization for PLL2 R always comes from the SYNC pin.
0: Not enabled
1: Enabled</td></tr>
<tr><td>2</td><td>FIN0_DIV2_EN</td><td>0</td><td colspan="2">Sets the input path to use or bypass the divide-by-2.
0: Bypassed (÷1)
1: Divided (÷2)</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">FIN0_INPUT_TYPE</td><td rowspan="6">0</td><td colspan="2">Program input type to hardware interface used.</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>Differential Input</td></tr>
<tr><td>1 (0x01)</td><td>Single Ended Input (FIN0_P)</td></tr>
<tr><td>2 (0x02)</td><td>Single Ended Input (FIN0_N)</td></tr>
<tr><td>3 (0x03)</td><td>Reserved</td></tr>
</table>

8.6.2.4 (0x146 - 0x149) CLKIN Control

8.6.2.4.1 CLKin_SEL_PIN_EN, CLKin_SEL_PIN_POL, CLKin2_EN, CLKin1_EN, CLKin0_EN, CLKin2_TYPE, CLKin1_TYPE, CLKin0_TYPE

This register has CLKin enable and type controls. See *Input Clock Switching* for more info on how clock input selection works.

Table 8-48. Register 0x146

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>CLKin_SEL_PIN_EN</td><td>0</td><td colspan="2">Enables pin control according to Input Clock Switching.</td></tr>
<tr><td>6</td><td>CLKin_SEL_PIN_POL</td><td>0</td><td colspan="2">Inverts the CLKin polarity for use in pin select mode.
0: Active High
1: Active Low</td></tr>
<tr><td>5</td><td>CLKin2_EN</td><td>0</td><td colspan="2">Enable CLKin2 to be used during auto-switching.
0: Not enabled for auto mode
1: Enabled for auto clock switching mode</td></tr>
<tr><td>4</td><td>CLKin1_EN</td><td>1</td><td colspan="2">Enable CLKin1 to be used during auto-switching.
0: Not enabled for auto mode
1: Enabled for auto clock switching mode</td></tr>
<tr><td>3</td><td>CLKin0_EN</td><td>1</td><td colspan="2">Enable CLKin0 to be used during auto-switching.
0: Not enabled for auto mode
1: Enabled for auto clock switching mode</td></tr>
<tr><td>2</td><td>CLKin2_TYPE</td><td>0</td><td rowspan="3">0: Bipolar
1: MOS</td><td rowspan="3">There are two buffer types for CLKin0, 1, and 2: bipolar and CMOS. Bipolar is recommended for differential inputs like LVDS or LVPECL. CMOS is recommended for DC-coupled single ended inputs.
When using bipolar, CLKINx_P and CLKINx_N must be AC-coupled.
When using CMOS, CLKINx_P and CLKINx_N may be AC or DC-coupled if the input signal is differential. If the input signal is single-ended the used input may be either AC or DC-coupled and the unused input must AC grounded.</td></tr>
<tr><td>1</td><td>CLKin1_TYPE</td><td>0</td></tr>
<tr><td>0</td><td>CLKin0_TYPE</td><td>0</td></tr>
</table>

8.6.2.4.2 CLKin_SEL_AUTO_REVERT_EN, CLKin_SEL_AUTO_EN, CLKin_SEL_MANUAL, CLKin1_DEMUX, CLKin0_DEMUX

Table 8-49. Register 0x147

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>CLKin_SEL_
AUTO_REVERT_EN</td><td>0</td><td colspan="2">If the active clock is detected on a higher priority clock while the device is in auto clock switching mode, the clock input is immediately switched. Highest priority input is lowest numbered active clock input.</td></tr>
<tr><td>6</td><td>CLKin_SEL_AUTO_EN</td><td>0</td><td colspan="2">Enables pin control according to Figure 8-7.</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">CLKin_SEL_MANUAL</td><td rowspan="6">1</td><td colspan="2">Selects the clock input when in manual mode according to Figure 8-7.</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>CLKIN0</td></tr>
<tr><td>1 (0x01)</td><td>CLKIN1</td></tr>
<tr><td>2 (0x02)</td><td>CLKIN2</td></tr>
<tr><td>3 (0x03)</td><td>Holdover</td></tr>
</table>

Table 8-49. Register 0x147 (continued)

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">CLKin1_DEMUX</td><td rowspan="6">0</td><td colspan="2">Selects where the output of the CLKin1 buffer is directed.</td></tr>
<tr><td>Field Value</td><td>CLKin1 Destination</td></tr>
<tr><td>0 (0x00)</td><td>FIN</td></tr>
<tr><td>1 (0x01)</td><td>Feedback Mux (0-delay mode)</td></tr>
<tr><td>2 (0x02)</td><td>PLL1</td></tr>
<tr><td>3 (0x03)</td><td>Off</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">CLKin0_DEMUX</td><td rowspan="6">3</td><td colspan="2">Selects where the output of the CLKin0 buffer is directed.</td></tr>
<tr><td>Field Value</td><td>CLKin0 Destination</td></tr>
<tr><td>0 (0x00)</td><td>SYSREF Mux</td></tr>
<tr><td>1 (0x01)</td><td>Reserved</td></tr>
<tr><td>2 (0x02)</td><td>PLL1</td></tr>
<tr><td>3 (0x03)</td><td>Off</td></tr>
</table>

8.6.2.4.3 CLKin_SEL0_MUX, CLKin_SEL0_TYPE

This register has CLKin_SEL0 controls.

Table 8-50. Register 0x148

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="10">5:3</td><td rowspan="10">CLKin_SEL0_MUX</td><td rowspan="10">0</td><td colspan="3">This set the output value of the CLKin_SEL0 pin. This register only applies if CLKin_SEL0_TYPE is set to an output mode</td></tr>
<tr><td>Field Value</td><td colspan="2">Output Format</td></tr>
<tr><td>0 (0x00)</td><td colspan="2">Logic Low</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">CLKin0 LOS</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">CLKin0 Selected</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">DAC Locked</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">DAC Low</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">DAC High</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">SPI Readback</td></tr>
<tr><td>7 (0x07)</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">CLKin_SEL0_TYPE</td><td rowspan="9">2</td><td colspan="3">This sets the IO type of the CLKin_SEL0 pin.</td></tr>
<tr><td>Field Value</td><td>Configuration</td><td>Function</td></tr>
<tr><td>0 (0x00)</td><td>Input</td><td rowspan="3">Input mode, see Input Clock Switching - Pin Select Mode for description of input mode.</td></tr>
<tr><td>1 (0x01)</td><td>Input with pullup resistor</td></tr>
<tr><td>2 (0x02)</td><td>Input with pulldown resistor</td></tr>
<tr><td>3 (0x03)</td><td>Output (push-pull)</td><td rowspan="4">Output modes; the CLKin_SEL0_MUX register for description of outputs.</td></tr>
<tr><td>4 (0x04)</td><td>Output inverted (push-pull)</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Output (open-drain)</td></tr>
</table>

8.6.2.4.4 SDIO_RDBK_TYPE, CLKin_SEL1_MUX, CLKin_SEL1_TYPE

This register has CLKin_SEL1 controls and register readback SDIO pin type.

Table 8-51. Register 0x149

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7</td><td>NA</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td>6</td><td>SDIO_RDBK_TYPE</td><td>1</td><td colspan="3">Sets the SDIO pin to open drain when during SPI readback in 3 wire mode.
0: Output, push-pull
1: Output, open drain.</td></tr>
<tr><td rowspan="10">5:3</td><td rowspan="10">CLKin_SEL1_MUX</td><td rowspan="10">0</td><td colspan="3">This set the output value of the CLKin_SEL1 pin. This register only applies if CLKin_SEL1_TYPE is set to an output mode.</td></tr>
<tr><td>Field Value</td><td colspan="2">Output Format</td></tr>
<tr><td>0 (0x00)</td><td colspan="2">Logic Low</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">CLKin1 LOS</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">CLKin1 Selected</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">DAC Locked</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">DAC Low</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">DAC High</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">SPI Readback</td></tr>
<tr><td>7 (0x07)</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">CLKin_SEL1_TYPE</td><td rowspan="9">2</td><td colspan="2">This sets the IO type of the CLKin_SEL1 pin.</td><td></td></tr>
<tr><td>Field Value</td><td>Configuration</td><td>Function</td></tr>
<tr><td>0 (0x00)</td><td>Input</td><td rowspan="3">Input mode, see Input Clock Switching - Pin Select Mode for description of input mode.</td></tr>
<tr><td>1 (0x01)</td><td>Input with pullup resistor</td></tr>
<tr><td>2 (0x02)</td><td>Input with pulldown resistor</td></tr>
<tr><td>3 (0x03)</td><td>Output (push-pull)</td><td rowspan="4">Output modes; see the CLKin_SEL1_MUX register for description of outputs.</td></tr>
<tr><td>4 (0x04)</td><td>Output inverted (push-pull)</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Output (open-drain)</td></tr>
</table>

8.6.2.5 RESET_MUX, RESET_TYPE

This register contains control of the RESET pin.

Table 8-52. Register 0x14A

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>7:6</td><td>NA</td><td>0</td><td colspan="3">Reserved</td></tr>
<tr><td rowspan="9">5:3</td><td rowspan="9">RESET_MUX</td><td rowspan="9">0</td><td colspan="3">This sets the output value of the RESET pin. This register only applies if RESET_TYPE is set to an output mode.</td></tr>
<tr><th>Field Value</th><th colspan="2">Output Format</th></tr>
<tr><td>0 (0x00)</td><td colspan="2">Logic Low</td></tr>
<tr><td>1 (0x01)</td><td colspan="2">Reserved</td></tr>
<tr><td>2 (0x02)</td><td colspan="2">CLKin2 Selected</td></tr>
<tr><td>3 (0x03)</td><td colspan="2">DAC Locked</td></tr>
<tr><td>4 (0x04)</td><td colspan="2">DAC Low</td></tr>
<tr><td>5 (0x05)</td><td colspan="2">DAC High</td></tr>
<tr><td>6 (0x06)</td><td colspan="2">SPI Readback</td></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">RESET_TYPE</td><td rowspan="9">2</td><td colspan="3">This sets the IO type of the RESET pin.</td></tr>
<tr><th>Field Value</th><th>Configuration</th><th>Function</th></tr>
<tr><td>0 (0x00)</td><td>Input</td><td rowspan="3">Reset Mode
Reset pin high = Reset</td></tr>
<tr><td>1 (0x01)</td><td>Input with pullup resistor</td></tr>
<tr><td>2 (0x02)</td><td>Input with pulldown resistor</td></tr>
<tr><td>3 (0x03)</td><td>Output (push-pull)</td><td rowspan="4">Output modes; see the RESET_MUX register for description of outputs.</td></tr>
<tr><td>4 (0x04)</td><td>Output inverted (push-pull)</td></tr>
<tr><td>5 (0x05)</td><td>Reserved</td></tr>
<tr><td>6 (0x06)</td><td>Output (open-drain)</td></tr>
</table>

8.6.2.6 (0x14B - 0x152) Holdover

8.6.2.6.1 LOS_TIMEOUT, LOS_EN, TRACK_EN, HOLDOVER_FORCE, MAN_DAC_EN, MAN_DAC[9:8]

This register contains the holdover functions.

Table 8-53. Register 0x14B

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">LOS_TIMEOUT</td><td rowspan="6">0</td><td colspan="2">This controls the amount of time in which no activity on a CLKin forces a clock switch event.</td></tr>
<tr><td>Field Value</td><td>Timeout</td></tr>
<tr><td>0 (0x00)</td><td>5 MHz typical</td></tr>
<tr><td>1 (0x01)</td><td>25 MHz typical</td></tr>
<tr><td>2 (0x02)</td><td>100 MHz typical</td></tr>
<tr><td>3 (0x03)</td><td>200 MHz typical</td></tr>
<tr><td>5</td><td>LOS_EN</td><td>0</td><td colspan="2">Enables the LOS (Loss-of-Signal) timeout control. Valid for MOS clock inputs.
0: Disabled
1: Enabled</td></tr>
<tr><td>4</td><td>TRACK_EN</td><td>0</td><td colspan="2">Enable the DAC to track the PLL1 tuning voltage, optionally for use in holdover mode. After device reset, tracking starts at DAC code = 512.
Tracking can be used to monitor PLL1 voltage in any mode.
0: Disabled
1: Enabled, will only track when PLL1 is locked.</td></tr>
<tr><td>3</td><td>HOLDOVER
_FORCE</td><td>0</td><td colspan="2">This bit forces holdover mode. When holdover mode is forced, if MAN_DAC_EN = 1, then the DAC will set the programmed MAN_DAC value. Otherwise, the tracked DAC value will set the DAC voltage.
0: Disabled
1: Enabled.</td></tr>
<tr><td>2</td><td>MAN_DAC_EN</td><td>1</td><td colspan="2">This bit enables the manual DAC mode.
0: Automatic
1: Manual</td></tr>
<tr><td>1:0</td><td>MAN_DAC[9:8]</td><td>2</td><td colspan="2">See MAN_DAC for more information on the MAN_DAC settings.</td></tr>
</table>

8.6.2.6.2 MAN_DAC

These registers set the value of the DAC in holdover mode when used manually.

Table 8-54. MAN_DAC[9:0]

MSB	LSB
0x14B[1:0]	0x14C[7:0]

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x14B	7:2			See *LOS_TIMEOUT, LOS_EN, TRACK_EN, HOLDOVER_FORCE, MAN_DAC_EN, MAN_DAC[9:8]* for information on these bits.	
0x14B	1:0	MAN_DAC[9:8]	2	Sets the value of the manual DAC when in manual DAC mode.	
				Field Value	**DAC Value**
				0 (0x00)	0
				1 (0x01)	1
0x14C	7:0	MAN_DAC[7:0]	0	2 (0x02)	2
				...	...
				1022 (0x3FE)	1022
				1023 (0x3FF)	1023

8.6.2.6.3 DAC_TRIP_LOW

This register contains the high value at which holdover mode is entered.

Table 8-55. Register 0x14D

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:6	NA	0	Reserved	
5:0	DAC_TRIP_LOW	0	Voltage from GND at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.	
			Field Value	**DAC Trip Value**
			0 (0x00)	1 x Vcc / 64
			1 (0x01)	2 x Vcc / 64
			2 (0x02)	3 x Vcc / 64
			3 (0x03)	4 x Vcc / 64
			...	...
			61 (0x17)	62 x Vcc / 64
			62 (0x18)	63 x Vcc / 64
			63 (0x19)	64 x Vcc / 64

8.6.2.6.4 DAC_CLK_MULT, DAC_TRIP_HIGH

This register contains the multiplier for the DAC clock counter and the low value at which holdover mode is entered.

Table 8-56. Register 0x14E

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">DAC_CLK_MULT</td><td rowspan="6">0</td><td colspan="2">This is the multiplier for the DAC_CLK_CNTR which sets the rate at which the DAC value is tracked.</td></tr>
<tr><td>Field Value</td><td>DAC Multiplier Value</td></tr>
<tr><td>0 (0x00)</td><td>4</td></tr>
<tr><td>1 (0x01)</td><td>64</td></tr>
<tr><td>2 (0x02)</td><td>1024</td></tr>
<tr><td>3 (0x03)</td><td>16384</td></tr>
<tr><td rowspan="10">5:0</td><td rowspan="10">DAC_TRIP_HIGH</td><td rowspan="10">0</td><td colspan="2">Voltage from Vcc at which holdover is entered if HOLDOVER_VTUNE_DET is enabled.</td></tr>
<tr><td>Field Value</td><td>DAC Trip Value</td></tr>
<tr><td>0 (0x00)</td><td>1 x Vcc / 64</td></tr>
<tr><td>1 (0x01)</td><td>2 x Vcc / 64</td></tr>
<tr><td>2 (0x02)</td><td>3 x Vcc / 64</td></tr>
<tr><td>3 (0x03)</td><td>4 x Vcc / 64</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>61 (0x17)</td><td>62 x Vcc / 64</td></tr>
<tr><td>62 (0x18)</td><td>63 x Vcc / 64</td></tr>
<tr><td>63 (0x19)</td><td>64 x Vcc / 64</td></tr>
</table>

8.6.2.6.5 DAC_CLK_CNTR

This register contains the value of the DAC when in tracked mode.

Table 8-57. Register 0x14F

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="10">7:0</td><td rowspan="10">DAC_CLK_CNTR</td><td rowspan="10">127</td><td colspan="2">This with DAC_CLK_MULT set the rate at which the DAC is updated. The update rate is = DAC_CLK_MULT * DAC_CLK_CNTR / PLL1 PDF</td></tr>
<tr><td>Field Value</td><td>DAC Value</td></tr>
<tr><td>0 (0x00)</td><td>0</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>253 (0xFD)</td><td>253</td></tr>
<tr><td>254 (0xFE)</td><td>254</td></tr>
<tr><td>255 (0xFF)</td><td>255</td></tr>
</table>

8.6.2.6.6 CLKin_OVERRIDE, HOLDOVER_EXIT_MODE, HOLDOVER_PLL1_DET, LOS_EXTERNAL_INPUT, HOLDOVER_VTUNE_DET, CLKin_SWITCH_CP_TRI, HOLDOVER_EN

This register has controls for enabling clock in switch events.

Table 8-58. Register 0x150

BIT	NAME	POR DEFAULT	DESCRIPTION
7	NA	0	Reserved
6	CLKin _OVERRIDE	0	When manual clock select is enabled, then CLKin_SEL_MANUAL = 0/1/2 selects a manual clock input. CLKin_OVERRIDE = 1 will force that clock input. CLKin_OVERRIDE = 1 is used with clock distribution mode for best performance. 0: Normal, no override. 1: Force select of only CLKin0/1/2 as specified by CLKin_SEL_MANUAL in manual mode. Dynamic digital delay will not operate.
5	HOLDOVER_ EXIT_MODE	0	0: Exit based on LOS status. If clock is active by LOS, then begin exit. 1: Exit based on PLL1 DLD. When the PLL1 phase detector confirming valid clock.
4	HOLDOVER _PLL1_DET	0	This enables the HOLDOVER when PLL1 lock detect signal transitions from high to low. 0: PLL1 DLD does not cause a clock switch event 1: PLL1 DLD causes a clock switch event
3	LOS_EXTERNAL_INPUT	0	Use external signals for LOS status instead of internal LOS circuitry. CLKin_SEL0 pin is used for CLKin0 LOS, CLKin_SEL1 pin is used for CLKin1 LOS, and Status_LD1 is used for CLKin2 LOS. For any of these pins to be valid, the corresponding _TYPE register must be programmed as an input. 0: Disabled 1: Enabled
2	HOLDOVER_ VTUNE_DET	0	Enables the DAC Vtune rail detector. When the DAC achieves a specified Vtune, if this bit is enabled, the current clock input is considered invalid and an input clock switch event is generated. 0: Disabled 1: Enabled
1	CLKin_SWITCH_CP_TRI	0	Enable clock switching with tri-stated charge pump. 0: Not enabled. 1: PLL1 charge pump tri-states during clock switching.
0	HOLDOVER_EN	0	Sets whether holdover mode is active or not. 0: Disabled 1: Enabled

8.6.2.6.7 HOLDOVER_DLD_CNT

Table 8-59. HOLDOVER_DLD_CNT[13:0]

MSB	LSB
0x151[5:0] / HOLDOVER_DLD_CNT[13:8]	0x152[7:0] / HOLDOVER_DLD_CNT[7:0]

This register has the number of valid clocks of PLL1 PDF before holdover is exited.

Table 8-60. Registers 0x151 and 0x152

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x151</td><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x151</td><td rowspan="4">5:0</td><td rowspan="4">HOLDOVER _DLD_CNT[13:8]</td><td rowspan="4">2</td><td colspan="2">The number of valid clocks of PLL1 PDF before holdover mode is exited.</td></tr>
<tr><td>Field Value</td><td>Count Value</td></tr>
<tr><td>0 (0x00)</td><td>0</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="4">0x152</td><td rowspan="4">7:0</td><td rowspan="4">HOLDOVER _DLD_CNT[7:0]</td><td rowspan="4">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16382 (0x3FFE)</td><td>16382</td></tr>
<tr><td>16383 (0x3FFF)</td><td>16383</td></tr>
</table>

8.6.2.7 (0x153 - 0x15F) PLL1 Configuration

8.6.2.7.1 CLKin0_R

Table 8-61. CLKin0_R[13:0]

MSB	LSB
0x153[5:0] / CLKin0_R[13:8]	0x154[7:0] / CLKin0_R[7:0]

These registers contain the value of the CLKin0 divider.

Table 8-62. Registers 0x153 and 0x154

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x153	7:6	NA	0	Reserved	
0x153	5:0	CLKin0_R[13:8]	0	The value of PLL1 N counter when CLKin0 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
0x154	7:0	CLKin0_R[7:0]	120	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

8.6.2.7.2 CLKin1_R

Table 8-63. CLKin1_R[13:0]

MSB	LSB
0x155[5:0] / CLKin1_R[13:8]	0x156[7:0] / CLKin1_R[7:0]

These registers contain the value of the CLKin1 R divider.

Table 8-64. Registers 0x155 and 0x156

REGISTER	BIT	NAME	POR DEFAULT	DESCRIPTION	
0x155	7:6	NA	0	Reserved	
0x155	5:0	CLKin1_R[13:8]	0	The value of PLL1 R counter when CLKin1 is selected.	
				Field Value	**Divide Value**
				0 (0x00)	Reserved
				1 (0x01)	1
0x156	7:0	CLKin1_R[7:0]	150	2 (0x02)	2
				...	...
				16382 (0x3FFE)	16382
				16383 (0x3FFF)	16383

8.6.2.7.3 CLKin2_R

Table 8-65. CLKin2_R[13:0]

MSB	LSB
0x157[5:0] / CLKin2_R[13:8]	0x158[7:0] / CLKin2_R[7:0]

Table 8-66. Registers 0x157 and 0x158

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x157</td><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x157</td><td rowspan="4">5:0</td><td rowspan="4">CLKin2_R[13:8]</td><td rowspan="4">0</td><td colspan="2">The value of PLL1 R counter when CLKin2 is selected.</td></tr>
<tr><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="4">0x158</td><td rowspan="4">7:0</td><td rowspan="4">CLKin2_R[7:0]</td><td rowspan="4">150</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16382 (0x3FFE)</td><td>16382</td></tr>
<tr><td>16383 (0x3FFF)</td><td>16383</td></tr>
</table>

8.6.2.7.4 PLL1_N

Table 8-67. PLL1_N[13:0]

MSB	LSB
0x159[5:0] / PLL1_N[13:8]	0x15A[7:0] / PLL1_N[7:0]

These registers contain the N divider value for PLL1.

Table 8-68. Registers 0x159 and 0x15A

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x159</td><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x159</td><td rowspan="4">5:0</td><td rowspan="4">PLL1_N[13:8]</td><td rowspan="4">0</td><td colspan="2">The value of PLL1 N counter.</td></tr>
<tr><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="3">0x15A</td><td rowspan="3">7:0</td><td rowspan="3">PLL1_N[7:0]</td><td rowspan="3">120</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>4,095 (0xFFF)</td><td>4,095</td></tr>
</table>

8.6.2.7.5 PLL1_WND_SIZE, PLL1_CP_TRI, PLL1_CP_POL, PLL1_CP_GAIN

This register controls the PLL1 phase detector.

Table 8-69. Register 0x15B

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">PLL1_WND_SIZE</td><td rowspan="6">3</td><td colspan="2">PLL1_WND_SIZE sets the window size used for digital lock detect for PLL1. If the phase error between the reference and feedback of PLL1 is less than specified time, then the PLL1 lock counter increments.</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>4 ns</td></tr>
<tr><td>1 (0x01)</td><td>9 ns</td></tr>
<tr><td>2 (0x02)</td><td>19 ns</td></tr>
<tr><td>3 (0x03)</td><td>43 ns</td></tr>
<tr><td>5</td><td>PLL1_CP_TRI</td><td>0</td><td colspan="2">This bit allows for the PLL1 charge pump output pin, CPout1, to be placed into TRI-STATE.
0: PLL1 CPout1 is active
1: PLL1 CPout1 is at TRI-STATE</td></tr>
<tr><td>4</td><td>PLL1_CP_POL</td><td>1</td><td colspan="2">PLL1_CP_POL sets the charge pump polarity for PLL1. Many VCXOs use positive slope.
A positive slope VCXO increases output frequency with increasing voltage. A negative slope VCXO decreases output frequency with increasing voltage.
0: Negative Slope VCO/VCXO
1: Positive Slope VCO/VCXO</td></tr>
<tr><td rowspan="10">3:0</td><td rowspan="10">PLL1_CP_GAIN</td><td rowspan="10">4</td><td colspan="2">This bit programs the PLL1 charge pump output current level.</td></tr>
<tr><td>Field Value</td><td>Gain</td></tr>
<tr><td>0 (0x00)</td><td>50 µA</td></tr>
<tr><td>1 (0x01)</td><td>150 µA</td></tr>
<tr><td>2 (0x02)</td><td>250 µA</td></tr>
<tr><td>3 (0x03)</td><td>350 µA</td></tr>
<tr><td>4 (0x04)</td><td>450 µA</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>14 (0x0E)</td><td>1450 µA</td></tr>
<tr><td>15 (0x0F)</td><td>1550 µA</td></tr>
</table>

8.6.2.7.6 PLL1_DLD_CNT

Table 8-70. PLL1_DLD_CNT[13:0]

MSB	LSB
0x15C[5:0] / PLL1_DLD_CNT[13:8]	0x15D[7:0] / PLL1_DLD_CNT[7:0]

This register contains the value of the PLL1 DLD counter.

Table 8-71. Registers 0x15C and 0x15D

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x15C</td><td>7:6</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x15C</td><td rowspan="4">5:0</td><td rowspan="4">PLL1_DLD _CNT[13:8]</td><td rowspan="4">32</td><td colspan="2">The reference and feedback of PLL1 must be within the window of phase error as specified by PLL1_WND_SIZE for this many phase detector cycles before PLL1 digital lock detect is asserted.</td></tr>
<tr><td>Field Value</td><td>Delay Value</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="5">0x15D</td><td rowspan="5">7:0</td><td rowspan="5">PLL1_DLD _CNT[7:0]</td><td rowspan="5">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16,382 (0x3FFE)</td><td>16,382</td></tr>
<tr><td>16,383 (0x3FFF)</td><td>16,383</td></tr>
</table>

8.6.2.7.7 HOLDOVER_EXIT_NADJ

Table 8-72. Register 0x15E

BIT	NAME	POR DEFAULT	DESCRIPTION
7:5	NA	0	Reserved
4:0	HOLDOVER_EXIT_NADJ	30	When holdover exists, PLL1 R counter and PLL1 N counter are reset. HOLDOVER_EXIT_NADJ is a 2s complement number which provides a relative timing offset between PLL1 R and PLL1 N divider.

8.6.2.7.8 PLL1_LD_MUX, PLL1_LD_TYPE

This register configures the PLL1 LD pin.

Table 8-73. Register 0x15F

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	PLL1_LD_MUX	1	This sets the output value of the Status_LD1 pin.	
			Field Value	**MUX Value**
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
			8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N /2
			12 (0x0C)	PLL1_N / 4
			13 (0x0D)	PLL2_N / 2
			14 (0x0E)	PLL2_N / 4
			15 (0x0F)	PLL1_R / 2
			16 (0x10)	PLL1_R / 4
			17 (0x11)	PLL2_R[(1)] / 2
			18 (0x12)	PLL2_R / 4[(1)]
2:0	PLL1_LD_TYPE	6	Sets the IO type of the Status_LD1 pin.	
			Field Value	**TYPE**
			0 (0x00)	Input for External CLKin2 LOS
			1 (0x01)	Input for External CLKin2 LOS (pullup)
			2 (0x02)	Input for External CLKin2 LOS (pulldown)
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open-drain)

(1) Only valid when PLL2_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

8.6.2.8 (0x160 - 0x16E) PLL2 Configuration

8.6.2.8.1 PLL2_R

Table 8-74. PLL2_R[11:0]

MSB	LSB
0x160[3:0] / PLL2_R[11:8]	0x161[7:0] / PLL2_R[7:0]

This register contains the value of the PLL2 R divider.

Table 8-75. Registers 0x160 and 0x161

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x160</td><td>7:4</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x160</td><td rowspan="4">3:0</td><td rowspan="4">PLL2_R[11:8]</td><td rowspan="4">0</td><td colspan="2">Valid values for the PLL2 R divider.</td></tr>
<tr><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="5">0x161</td><td rowspan="5">7:0</td><td rowspan="5">PLL2_R[7:0]</td><td rowspan="5">2</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>4,094 (0xFFE)</td><td>4,094</td></tr>
<tr><td>4,095 (0xFFF)</td><td>4,095</td></tr>
</table>

8.6.2.8.2 PLL2_P, OSCin_FREQ, PLL2_REF_2X_EN

This register sets other PLL2 functions.

Table 8-76. Register 0x162

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="10">7:5</td><td rowspan="10">PLL2_P</td><td rowspan="10">2</td><td colspan="2">The PLL2 N Prescaler divides the output of the VCO as selected by Mode_MUX1 and is connected to the PLL2 N divider.</td></tr>
<tr><td>Field Value</td><td>Value</td></tr>
<tr><td>0 (0x00)</td><td>8</td></tr>
<tr><td>1 (0x01)</td><td>2</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>4 (0x04)</td><td>4</td></tr>
<tr><td>5 (0x05)</td><td>5</td></tr>
<tr><td>6 (0x06)</td><td>6</td></tr>
<tr><td>7 (0x07)</td><td>7</td></tr>
<tr><td rowspan="8">4:2</td><td rowspan="8">OSCin_FREQ</td><td rowspan="8">3</td><td colspan="2">The frequency of the PLL2 reference input to the PLL2 Phase Detector (OSCIN_P/OSCIN_N pins) must be programmed to support proper operation of the frequency calibration routine which locks the internal VCO to the target frequency.</td></tr>
<tr><td>Field Value</td><td>OSCIN Frequency</td></tr>
<tr><td>0 (0x00)</td><td>0 to 63 MHz</td></tr>
<tr><td>1 (0x01)</td><td>>63 MHz to 127 MHz</td></tr>
<tr><td>2 (0x02)</td><td>>127 MHz to 255 MHz</td></tr>
<tr><td>3 (0x03)</td><td>Reserved</td></tr>
<tr><td>4 (0x04)</td><td>>255 MHz to 500 MHz</td></tr>
<tr><td>5 (0x05) to 7(0x07)</td><td>Reserved</td></tr>
<tr><td>1</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>0</td><td>PLL2_REF_2X_EN</td><td>1</td><td colspan="2">Enabling the PLL2 reference frequency doubler allows for higher phase detector frequencies on PLL2 than would normally be allowed with the given VCXO frequency.
Higher phase detector frequencies reduces the PLL2 N values which makes the design of wider loop bandwidth filters possible.
0: Doubler Disabled
1: Doubler Enabled</td></tr>
</table>

8.6.2.8.3 PLL2_N_CAL

PLL2_N_CAL[17:0]

PLL2 never uses 0-delay during frequency calibration. These registers contain the value of the PLL2 N divider used with PLL2 pre-scaler during calibration for cascaded 0-delay mode. Once calibration is complete, PLL2 will use the PLL2_N value. Cascaded 0-delay mode occurs when PLL2_NCLK_MUX = 1.

Table 8-77. PLL2_N_CAL[17:0]

MSB	—	LSB
0x163[1:0] / PLL2_N_CAL[17:16]	0x164[7:0] / PLL2_N_CAL[15:8]	0x165[7:0] / PLL2_N_CAL[7:0]

Table 8-78. Registers 0x163, 0x164, and 0x165

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x163</td><td>7:2</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="2">0x163</td><td rowspan="2">1:0</td><td rowspan="2">PLL2_N _CAL[17:16]</td><td rowspan="2">0</td><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td rowspan="2">0x164</td><td rowspan="2">7:0</td><td rowspan="2">PLL2_N_CAL[15:8]</td><td rowspan="2">0</td><td>1 (0x01)</td><td>1</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td rowspan="2">0x165</td><td rowspan="2">7:0</td><td rowspan="2">PLL2_N_CAL[7:0]</td><td rowspan="2">12</td><td>...</td><td>...</td></tr>
<tr><td>262,143 (0x3FFFF)</td><td>262,143</td></tr>
</table>

8.6.2.8.4 PLL2_N

This register disables frequency calibration and sets the PLL2 N divider value. Programming register 0x168 starts a VCO calibration routine if PLL2_FCAL_DIS = 0.

Table 8-79. PLL2_N[17:0]

MSB	—	LSB
0x166[1:0] / PLL2_N[17:16]	0x167[7:0] / PLL2_N[15:8]	0x168[7:0] / PLL2_N[7:0]

Table 8-80. Registers 0x166, 0x167, and 0x168

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x166</td><td>7:3</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td>0x166</td><td>2</td><td>PLL2_FCAL_DIS</td><td>0</td><td colspan="2">Setting this to 1 disables PLL2 frequency calibration on programming of register 0x168</td></tr>
<tr><td rowspan="2">0x166</td><td rowspan="2">1:0</td><td rowspan="2">PLL2_N[17:16]</td><td rowspan="2">0</td><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td rowspan="2">0x167</td><td rowspan="2">7:0</td><td rowspan="2">PLL2_N[15:8]</td><td rowspan="2">0</td><td>1 (0x01)</td><td>1</td></tr>
<tr><td>2 (0x02)</td><td>2</td></tr>
<tr><td rowspan="2">0x168</td><td rowspan="2">7:0</td><td rowspan="2">PLL2_N[7:0]</td><td rowspan="2">12</td><td>...</td><td>...</td></tr>
<tr><td>262,143 (0x3FFFF)</td><td>262,143</td></tr>
</table>

8.6.2.8.5 PLL2_WND_SIZE, PLL2_CP_GAIN, PLL2_CP_POL, PLL2_CP_TRI

This register controls the PLL2 phase detector.

Table 8-81. Register 0x169

<table>
<tr><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>7</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="6">6:5</td><td rowspan="6">PLL2_WND_SIZE</td><td rowspan="6">2</td><td colspan="2">PLL2_WND_SIZE sets the window size used for digital lock detect for PLL2. If the phase error between the reference and feedback of PLL2 is less than specified time, then the PLL2 lock counter increments.</td></tr>
<tr><td>Field Value</td><td>Maximum Phase Detector Frequency / Window Size</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>320 MHz / 1 ns</td></tr>
<tr><td>2 (0x02)</td><td>240 MHz / 1.8 ns</td></tr>
<tr><td>3 (0x03)</td><td>160 MHz / 2.6 ns</td></tr>
<tr><td rowspan="6">4:3</td><td rowspan="6">PLL2_CP_GAIN</td><td rowspan="6">3</td><td colspan="2">This bit programs the PLL2 charge pump output current level. The table below also shows the impact of the PLL2 TRISTATE bit in conjunction with PLL2_CP_GAIN.</td></tr>
<tr><td>Field Value</td><td>Definition</td></tr>
<tr><td>0 (0x00)</td><td>Reserved</td></tr>
<tr><td>1 (0x01)</td><td>Reserved</td></tr>
<tr><td>2 (0x02)</td><td>1600 µA</td></tr>
<tr><td>3 (0x03)</td><td>3200 µA</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">PLL2_CP_POL</td><td rowspan="4">0</td><td colspan="2">PLL2_CP_POL sets the charge pump polarity for PLL2. The internal VCO requires the negative charge pump polarity to be selected. Many VCOs use positive slope.
A positive slope VCO increases output frequency with increasing voltage. A negative slope VCO decreases output frequency with increasing voltage.</td></tr>
<tr><td>Field Value</td><td>Description</td></tr>
<tr><td>0</td><td>Negative Slope VCO/VCXO</td></tr>
<tr><td>1</td><td>Positive Slope VCO/VCXO</td></tr>
<tr><td>1</td><td>PLL2_CP_TRI</td><td>0</td><td colspan="2">PLL2_CP_TRI TRI-STATEs the output of the PLL2 charge pump.
0: Disabled
1: TRI-STATE</td></tr>
<tr><td>0</td><td>PLL2_DLD_EN</td><td>0</td><td colspan="2">PLL2 DLD circuitry is enabled when the PLL2 DLD is used to provide an output to a lock detect status pin. PLL2_DLD_EN allows enabling the PLL2 DLD circuitry without needing to provide PLL2 DLD to a status pin. This enables PLL2 DLD status to be read back using SPI while allowing the Status pins to be used for other purposes.
0: PLL2 DLD circuitry is on only of PLL2 DLD or PLL1 + PLL2 DLD signal is output from a Status_LD_MUX.
1: PLL2 DLD circuitry is forced on.</td></tr>
</table>

8.6.2.8.6 PLL2_DLD_CNT

Table 8-82. PLL2_DLD_CNT[13:0]

MSB	LSB
0x16A[5:0] / PLL2_DLD_CNT[13:8]	0x16B[7:0] / PLL2_DLD_CNT[7:0]

This register has the value of the PLL2 DLD counter.

Table 8-83. Registers 0x16A and 0x16B

<table>
<tr><th>REGISTER</th><th>BIT</th><th>NAME</th><th>POR DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td>0x16A</td><td>7</td><td>NA</td><td>0</td><td colspan="2">Reserved</td></tr>
<tr><td rowspan="4">0x16A</td><td rowspan="4">5:0</td><td rowspan="4">PLL2_DLD _CNT[13:8]</td><td rowspan="4">32</td><td colspan="2">The reference and feedback of PLL2 must be within the window of phase error as specified by PLL2_WND_SIZE for PLL2_DLD_CNT cycles before PLL2 digital lock detect is asserted.</td></tr>
<tr><td>Field Value</td><td>Divide Value</td></tr>
<tr><td>0 (0x00)</td><td>Not Valid</td></tr>
<tr><td>1 (0x01)</td><td>1</td></tr>
<tr><td rowspan="5">0x16B</td><td rowspan="5">7:0</td><td rowspan="5">PLL2_DLD_CNT</td><td rowspan="5">0</td><td>2 (0x02)</td><td>2</td></tr>
<tr><td>3 (0x03)</td><td>3</td></tr>
<tr><td>...</td><td>...</td></tr>
<tr><td>16,382 (0x3FFE)</td><td>16,382</td></tr>
<tr><td>16,383 (0x3FFF)</td><td>16,383</td></tr>
</table>

8.6.2.8.7 PLL2_LD_MUX, PLL2_LD_TYPE

This register sets the output value of the Status_LD2 pin.

Table 8-84. Register 0x16E

BIT	NAME	POR DEFAULT	DESCRIPTION	
7:3	PLL2_LD_MUX	0	This sets the output value of the Status_LD2 pin.	
			Field Value	**MUX Value**
			0 (0x00)	Logic Low
			1 (0x01)	PLL1 DLD
			2 (0x02)	PLL2 DLD
			3 (0x03)	PLL1 & PLL2 DLD
			4 (0x04)	Holdover Status
			5 (0x05)	DAC Locked
			6 (0x06)	Reserved
			7 (0x07)	SPI Readback
			8 (0x08)	DAC Rail
			9 (0x09)	DAC Low
			10 (0x0A)	DAC High
			11 (0x0B)	PLL1_N / 2
			12 (0x0C)	PLL1_N / 4
			13 (0x0D)	PLL2_N / 2
			14 (0x0E)	PLL2_N / 4
			15 (0x0F)	PLL1_R / 2
			16 (0x10)	PLL1_R / 4
			17 (0x11)	PLL2_R / 2[(1)]
			18 (0x12)	PLL2_R / 4[(1)]
2:0	PLL2_LD_TYPE	6	Sets the IO type of the Status_LD2 pin.	
			Field Value	**TYPE**
			0 (0x00)	Reserved
			1 (0x01)	Reserved
			2 (0x02)	Reserved
			3 (0x03)	Output (push-pull)
			4 (0x04)	Output inverted (push-pull)
			5 (0x05)	Reserved
			6 (0x06)	Output (open drain)

(1) Only valid when PLL1_LD_MUX is not set to 2 (PLL2_DLD) or 3 (PLL1 & PLL2 DLD).

8.6.2.9 (0x16F - 0x555) Misc Registers

8.6.2.9.1 PLL2_PRE_PD, PLL2_PD, FIN0_PD

Table 8-85. Register 0x173

BIT	NAME	POR DEFAULT	DESCRIPTION
7	N/A	0	Reserved
6	PLL2_PRE_PD	1	Powerdown PLL2 prescaler 0: Normal Operation 1: Powerdown
5	PLL2_PD	1	Powerdown PLL2 0: Normal Operation 1: Powerdown
4	FIN0_PD	1	Powerdown FIN0 0: Normal Operation 1: Powerdown
3:0	N/A	0	Reserved

8.6.2.9.2 PLL1R_RST

Refer to *PLL1 R Divider Synchronization* for more information on synchronizing PLL1 R divider.

Table 8-86. Register 0x177

BIT	NAME	POR DEFAULT	DESCRIPTION
7:6	NA	0	Reserved
5	PLL1R_RST	0	When set, PLL1 R divider will be held in reset. PLL1 will never lock with PLL1R_RST = 1. This bit is used in when synchronizing the PLL1 R divider. 0: PLL1 R divider normal operation. 1: PLL1 R divider held in reset.
4:0	NA	0	Reserved

8.6.2.9.3 CLR_PLL1_LD_LOST, CLR_PLL2_LD_LOST

Table 8-87. Register 0x182

BIT	NAME	POR DEFAULT	DESCRIPTION
7:2	NA	0	Reserved
1	CLR_PLL1_LD_LOST	0	To reset RB_PLL1_LD_LOST, write CLR_PLL1_LD_LOST with 1 and then 0. 0: RB_PLL1_LD_LOST will be set on next falling PLL1 DLD edge. 1: RB_PLL1_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL1_LD_LOST to become set again.
0	CLR_PLL2_LD_LOST	0	To reset RB_PLL2_LD_LOST, write CLR_PLL2_LD_LOST with 1 and then 0. 0: RB_PLL2_LD_LOST will be set on next falling PLL2 DLD edge. 1: RB_PLL2_LD_LOST is held clear (0). User must clear this bit to allow RB_PLL2_LD_LOST to become set again.

8.6.2.9.4 RB_PLL1_LD_LOST, RB_PLL1_LD, RB_PLL2_LD_LOST, RB_PLL2_LD

For PLL2 DLD read back to be valid, either PLL2 DLD or PLL1 + PLL2 DLD signal must be output from the status pins, or PLL2_DLD_EN bit must be set = 1.

Table 8-88. Register 0x183

BIT	NAME	POR DEFAULT	DESCRIPTION
7:4	N/A	0	Reserved
3	RB_PLL1_LD_LOST	0	This is set when PLL1 DLD edge falls. Does not set if cleared while PLL1 DLD is low.
2	RB_PLL1_LD	0	Read back 0: PLL1 DLD is low. Read back 1: PLL1 DLD is high.
1	RB_PLL2_LD_LOST	0	This is set when PLL2 DLD edge falls. Does not set if cleared while PLL2 DLD is low.

Table 8-88. Register 0x183 (continued)

BIT	NAME	POR DEFAULT	DESCRIPTION
0	RB_PLL2_LD	0	PLL1_LD_MUX or PLL2_LD_MUX must select setting 2 (PLL2 DLD) for valid reading of this bit. Read back 0: PLL2 DLD is low. Read back 1: PLL2 DLD is high.

8.6.2.9.5 RB_DAC_VALUE (MSB), RB_CLKinX_SEL, RB_CLKinX_LOS

This register provides read back access to CLKinX selection indicator and CLKinX LOS indicator. The 2 MSBs are shared with the RB_DAC_VALUE. See the *RB_DAC_VALUE* section for more information.

Table 8-89. Register 0x184

BIT	NAME	POR DEFAULT	DESCRIPTION
7:6	RB_DAC_VALUE[9:8]		See the *RB_DAC_VALUE* section.
5	RB_CLKin2_SEL		Read back 0: CLKin2 is not selected for input to PLL1. Read back 1: CLKin2 is selected for input to PLL1.
4	RB_CLKin1_SEL		Read back 0: CLKin1 is not selected for input to PLL1. Read back 1: CLKin1 is selected for input to PLL1.
3	RB_CLKin0_SEL		Read back 0: CLKin0 is not selected for input to PLL1. Read back 1: CLKin0 is selected for input to PLL1.
2	N/A		
1	RB_CLKin1_LOS		Read back 1: CLKin1 LOS is active. Read back 0: CLKin1 LOS is not active.
0	RB_CLKin0_LOS		Read back 1: CLKin0 LOS is active. Read back 0: CLKin0 LOS is not active.

8.6.2.9.6 RB_DAC_VALUE

Contains the value of the DAC for user readback.

Table 8-90. RB_DAC_VALUE[9:0]

MSB	LSB
0x184 [7:6] / RB_DAC_VALUE[9:8]	0x185 [7:0] / RB_DAC_VALUE[7:0]

Table 8-91. Registers 0x184 and 0x185

REGISTER	BIT	NAME	POR DEFAULT	
0x184	7:6	RB_DAC_ VALUE[9:8]	2	DAC value is 512 on power on reset, if PLL1 locks upon power-up the DAC value will change.
0x185	7:0	RB_DAC_ VALUE[7:0]	0	

8.6.2.9.7 RB_HOLDOVER

Table 8-92. Register 0x188

BIT	NAME	POR DEFAULT	DESCRIPTION
7:5	N/A		Reserved
4	RB_HOLDOVER		Read back 0: Not in HOLDOVER. Read back 1: In HOLDOVER.
3:0	N/A		Reserved

8.6.2.9.8 SPI_LOCK

Prevents SPI registers from being written to, except for 0x555.

This register cannot be read back.

Table 8-93. Register 0x555

BIT	NAME	POR DEFAULT	DESCRIPTION
7:0	SPI_LOCK	0	0: Registers unlocked. 1 to 255: Registers locked.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

Texas Instruments provides the TICSPRO software to assist with device setup, frequency divider calculations, and general device programming as well as the PLLatinum™ simulation software for loop filter design and phase noise/jitter simulation on ti.com.

9.1.1 Treatment of Unused Pins

Not all pins are needed for every application. In general, power down the unused feature in software. The unused pin may be left floating or grounded through a 1-kΩ resistor.

Table 9-1. Treatment of Unused Pins

PINS	TREATMENT IF UNUSED
CLKOUTx_P/CLKOUTx_N	1 kΩ to GND or float pin
RESET/GPO	1 kΩ to GND or float pin
SYNC/SYSREF_REQ	1 kΩ to GND or float pin
FIN0_P/FIN0_N	1 kΩ to GND or float pin
STATUS_LD1,STATUS_LD2	1 kΩ to GND or float pin
CPOUT1,CPOUT2	1 kΩ to GND or float pin
OSCOUT_P/CLKIN2_P	1 kΩ to GND or float pin
OSCOUT_N/CLKIN2_N	1 kΩ to GND or float pin

9.1.2 Frequency Planning and Spur Minimization

Frequency planning refers to strategically assigning frequencies to outputs for the purposes of spur minimization. Spurs vary as a function of output frequency, output format, and output assignments. Spurs can be directly coupling from one output to the next or be caused by a mixing product. For instance, if one output is at 3 GHz and another output is at 750 MHz, one can see a 750 MHz-spur coupling through the 3-GHz output. In some situations, it is also possible to have a spur that occurs at the greatest common divisor of the two frequencies (250 MHz in this case). In either case, the choice of which outputs the 3-GHz and 750-MHz frequencies are assigned to can have an impact on spurs.

Table 9-2. Factors Impacting Spurs

Factor	General Guidelines and Tips
Output Frequency	To a point, higher frequencies tend to couple stronger to other outputs, but bypassing impacts this.
Output Format	Stronger signals and single-ended signals tend to couple stronger to other outputs. LVDS tends to couple less than LVPECL as well. For LVCMOS, consider using both sides of the output with one side inverted to the other (Norm/Inv) to minimize crosstalk.
Frequency Assignment to Output (Frequency Planning)	Outputs that are physically closer and that share the same power supply tend to have stronger crosstalk. Outputs are grouped by supply in the following manner: Clock Group 0: (CLK0,CLK1,CLK12,CLK13), Clock Group 1: (CLK2, CLK3), Clock Group 2 (CLK4, CLK5, CLK6, CLK7), Clock Group 3 (CLK8, CLK9, CLK10, CLK11). Use frequency planning to minimize spur levels to the most critical outputs.

Frequency planning involves trial and error, but there is some strategy in planning. Try to ensure that the same frequencies are placed on outputs that have the strongest crosstalk and that different frequencies are placed on outputs that have weaker crosstalk

Table 9-3. Crosstalk Matrix

	CLK0,CLK1	CLK2,CLK3	CLK4,CLK5	CLK6,CLK7	CLK8,CLK9	CLK10,CLK11	CLK12,CLK13
CLK0, CLK1	n/a	M	L	L	L	M	**H**
CLK2, CLK3	M	n/a	M	L	L	M	M
CLK4, CLK5	L	M	n/a	**H**	L	M	M
CLK6, CLK7	L	L	**H**	n/a	L	M	M
CLK8, CLK9	L	L	L	L	n/a	**H**	M
CLK10, CLK11	M	M	M	M	**H**	n/a	**H**
CLK12, CLK13	**H**	M	M	M	M	**H**	n/a

L = Low Crosstalk, **M** = Medium Crosstalk, **H** = High Crosstalk

9.1.3 Digital Lock Detect Frequency Accuracy

The digital lock detect circuit is used to determine PLL1 locked, PLL2 locked, and holdover exit events. A window size and lock count register are programmed to set a ppm frequency accuracy of reference to feedback signals of the PLL for each event to occur. When a PLL digital lock event occurs, the digital lock detect of the PLL is asserted true. When the holdover exit event occurs, the device will exit holdover mode when HOLDOVER_EXIT_MODE = 1 (Exit based on DLD).

Table 9-4. Digital Lock Detect Related Fields

EVENT	PLL	WINDOW SIZE	LOCK COUNT
PLL1 Locked	PLL1	PLL1_WND_SIZE	PLL1_DLD_CNT
PLL2 Locked	PLL2	PLL2_WND_SIZE	PLL2_DLD_CNT
Holdover exit	PLL1	PLL1_WND_SIZE	HOLDOVER_DLD_CNT

For a digital lock detect event to occur, there must be a *lock count* number of phase detector cycles of PLLX during which the time and phase error of the PLLX_R reference and PLLX_N feedback signal edges are within the user programmable *window size*. There must be at least one *lock count* phase detector event before a lock event occurs, therefore a minimum digital lock event time can be calculated as *lock count* / f_{PDX} where X = 1 for PLL1 or 2 for PLL2.

By using Equation 8, values for a *lock count* and *window size* can be chosen to set the frequency accuracy required by the system in ppm before the digital lock detect event occurs:

$$ppm = \frac{1e6 \times PLLX\_WND\_SIZE \times f_{PDX}}{PLLX\_DLD\_CNT} \quad (8)$$

The effect of the *lock count* value is that it shortens the effective lock window size by dividing the *window size* by *lock count*.

If at any time the PLLX_R reference and PLLX_N feedback signals are outside the time window set by *window size*, then the *lock count* value is reset to 0.

9.1.3.1 Minimum Lock Time Calculation Example

To calculate the minimum PLL2 *digital* lock time given a PLL2 phase detector frequency of 40 MHz and PLL2_DLD_CNT = 10,000. Then, the minimum lock time of PLL2 will be 10,000 / 40 MHz = 250 µs.

9.1.4 Driving CLKIN AND OSCIN Inputs

9.1.4.1 Driving CLKIN and OSCIN PINS With a Differential Source

CLKin and OSCin pins can be driven by differential signals. TI recommends setting the input mode to bipolar (CLKinX_BUF_TYPE = 0) when using differential reference clocks. The device internally biases the input pins so the differential interface should be AC-coupled. The recommended circuits for driving the CLKin pins with either LVDS or LVPECL are shown in Figure 9-1 and Figure 9-2.

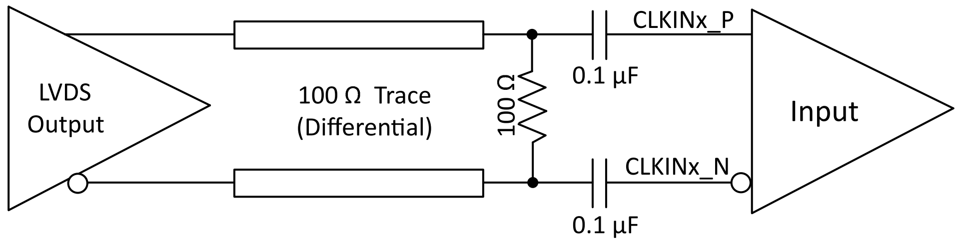


Figure 9-1. CLKINx_P/CLKINx_N or OSCIN Termination for an LVDS Reference Clock Source

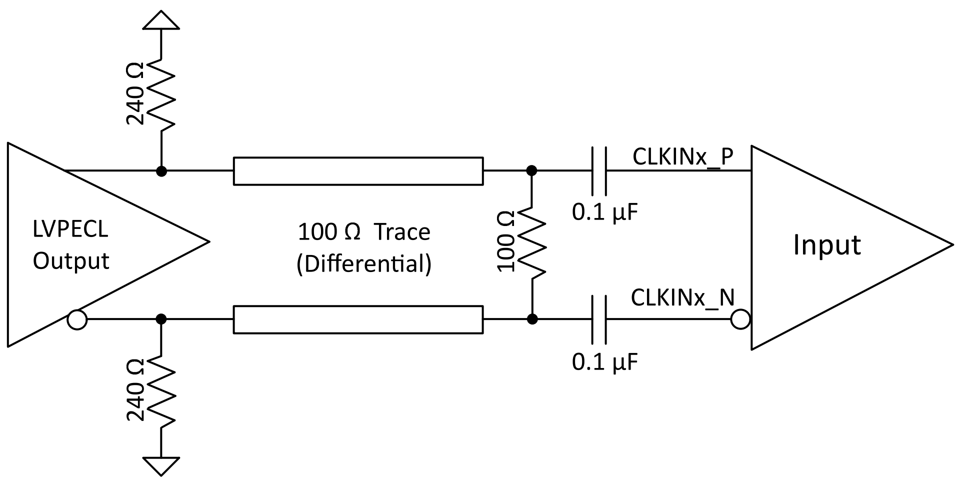


Figure 9-2. CLKINx_P/CLKINx_N or OSCIN Termination for an LVPECL Reference Clock Source

Finally, a reference clock source that produces a differential sine wave output can drive the CLKIN pins using the following circuit. Note: the signal level must conform to the requirements for the CLKIN pins listed in the *Electrical Characteristics* table.

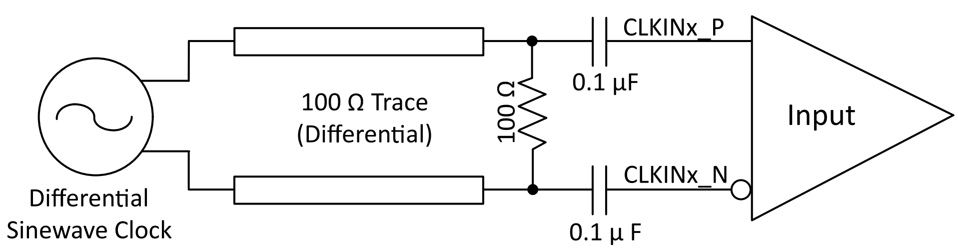


Figure 9-3. CLKINx_P/CLKINx_N or OSCIN Termination for a Differential Sinewave Reference Clock Source

9.1.4.2 Driving CLKIN Pins With a Single-Ended Source

The CLKIN and OSCIN pins can be driven using a single-ended reference clock source, for example, either a sine wave source or an LVCMOS/LVTTL source. CLKIN supports both AC coupling or DC coupling. OSCin must use AC coupling. In the case of the sine wave source that is expecting a 50-Ω load, TI recommends using AC coupling as shown in Figure 9-4 with a 50-Ω termination.

Note

The signal level must conform to the requirements for the CLKin or OSCin pins listed in the *Electrical Characteristics* table.

To support LOS functionality, CLKinX_BUF_TYPE must be set to MOS mode (CLKinX_BUF_TYPE = 1) when AC-coupled. When AC coupling, if the 100-Ω termination is placed on the IC side of the blocking capacitors, then the LOS functionality will not be valid.

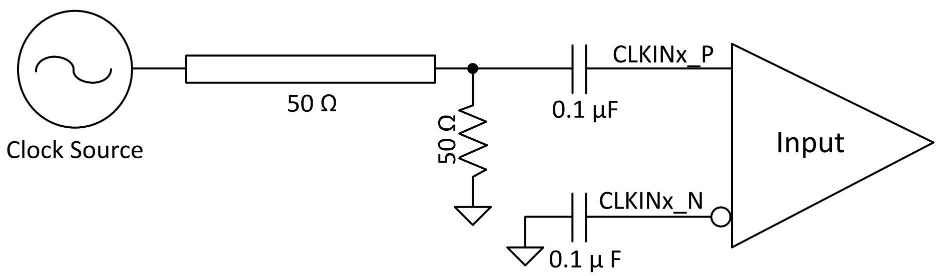


Figure 9-4. CLKINx_P/CLKINx_N Single-Ended Termination

If the CLKin pins are being driven with a single-ended LVCMOS/LVTTL source, either DC coupling or AC coupling may be used. If DC coupling is used, the CLKinX_BUF_TYPE should be set to MOS buffer mode (CLKinX_BUF_TYPE = 1) and the voltage swing of the source must meet the specifications for DC-coupled, MOS-mode clock inputs given in the *Electrical Characteristics* table. If AC coupling is used, the CLKinX_BUF_TYPE should be set to the bipolar buffer mode (CLKinX_BUF_TYPE = 0). The voltage swing at the input pins must meet the specifications for AC-coupled, bipolar mode clock inputs given in the *Electrical Characteristics* table. In this case, some attenuation of the clock input level may be required. A simple resistive divider circuit before the AC-coupling capacitor is sufficient.

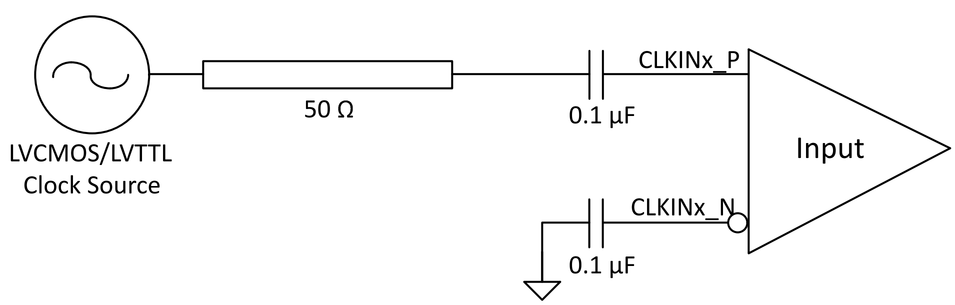


Figure 9-5. DC-Coupled LVCMOS/LVTTL Reference Clock

9.1.5 OSCin Doubler for Best Phase Noise Performance

PLL2 OSCin input path includes an on-chip Frequency Doubler. To have the best phase noise performance, TI recommends to maximize the PLL2 phase detector frequency. For example, using 122.88-MHz VCXO, PLL2 phase detector frequency can be increased to 245.76 MHz by setting PLL2_REF_2X_EN. Doubler path is a high performance path for OSCin clock. For configuration where doubler cannot be used, TI recommends to use Doubler and PLL2_RDIV = 2. To have deterministic phase relationship between input clock and output clocks, 0-delay modes should be used (nested 0-delay mode for dual loop configuration instead of cascaded 0-delay mode).

9.1.6 Termination and Use of Clock Output Drivers

When terminating clock drivers keep in mind these guidelines for optimum phase noise and jitter performance:

- Transmission line theory should be followed for good impedance matching to prevent reflections.
- Clock drivers should be presented with the proper loads. For example:
  - LVDS drivers are current drivers and require a closed current loop.

  - LVPECL drivers are open emitters and require a DC path to ground.
- Receivers should be presented with a signal biased to their specified DC bias level (common mode voltage) for proper operation. Some receivers have self-biasing inputs that automatically bias to the proper voltage level. In this case, the signal should normally be AC coupled.

It is possible to drive a non-LVPECL or non-LVDS receiver with an LVDS or LVPECL driver as long as the above guidelines are followed. Check the data sheet of the receiver or input being driven to determine the best termination and coupling method to be sure that the receiver is biased at its optimum DC voltage (common mode voltage). For example, when driving the OSCIN_P/OSCIN_N input, it should be AC coupled because the input is internally biased to the optimal DC bias level.

9.1.6.1 Termination for DC Coupled Differential Operation

For DC coupled operation of an LVDS driver, terminate with 100 Ω as close as possible to the LVDS receiver as shown in Figure 9-6.

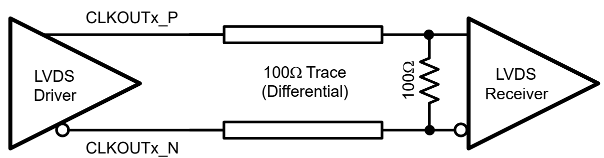


Figure 9-6. Differential LVDS Operation, DC Coupling, No Biasing of the Receiver

For DC coupled operation of an LVPECL driver, terminate with 50 Ω to V_{CC} - 2 V as shown in Figure 9-7. Alternatively terminate with a Thevenin equivalent circuit (120 Ω resistor connected to V_{CC} and an 82 Ω resistor connected to ground with the driver connected to the junction of the 120 Ω and 82 Ω resistors) as shown in Figure 9-8 for V_{CC} = 3.3 V.

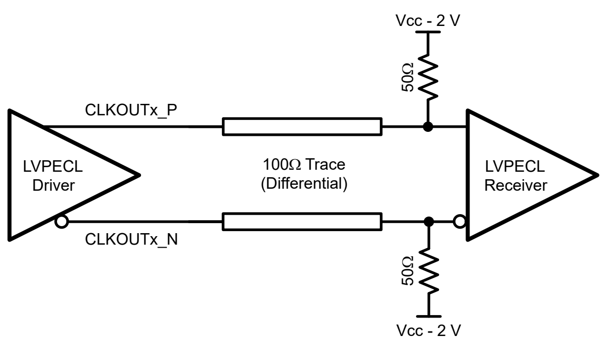


Figure 9-7. Differential LVPECL Operation, DC Coupling

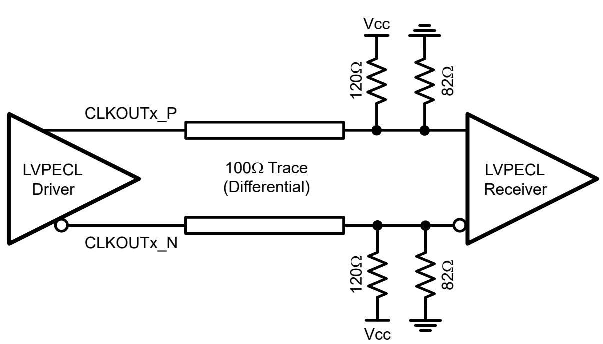


Figure 9-8. Differential LVPECL Operation, DC Coupling, Thevenin Equivalent

9.1.6.2 Termination for AC Coupled Differential Operation

AC coupling allows for shifting the DC bias level (common mode voltage) when driving different receiver standards. Since AC coupling prevents the driver from providing a DC bias voltage at the receiver it is important to ensure the receiver is biased to its ideal DC level.

When driving non-biased LVDS receivers with an LVDS driver, the signal may be AC coupled by adding DC blocking capacitors, however the proper DC bias point needs to be established at the receiver. One way to do this is with the termination circuitry in Figure 9-9.

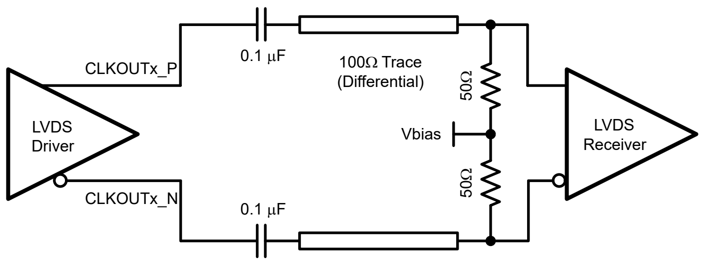


Figure 9-9. Differential LVDS Operation, AC Coupling, External Biasing at the Receiver

Some LVDS receivers may have internal biasing on the inputs. In this case, the circuit shown in Figure 9-9 is modified by replacing the 50 Ω terminations to Vbias with a single 100 Ω resistor across the input pins of the receiver, as shown in Figure 9-10. When using AC coupling with LVDS outputs, there may be a startup delay observed in the clock output due to capacitor charging. The previous figures employ a 0.1 µF capacitor. This value may need to be adjusted to meet the startup requirements for a particular application.

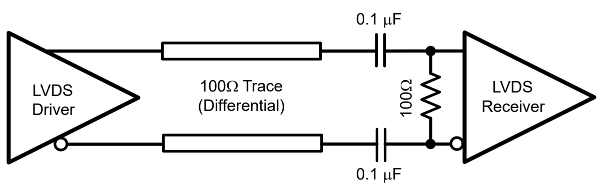


Figure 9-10. LVDS Termination for a Self-Biased Receiver

LVPECL drivers require a DC path to ground. When AC coupling an LVPECL signal use 120 Ω emitter resistors close to the LVPECL driver to provide a DC path to ground as shown in Figure 9-11. For proper receiver operation, the signal should be biased to the DC bias level (common mode voltage) specified by the receiver. The typical DC bias voltage for LVPECL receivers is 2 V. A Thevenin equivalent circuit (82 Ω resistor connected to V_{CC} and a 120 Ω resistor connected to ground with the driver connected to the junction of the 82 Ω and 120 Ω resistors) is a valid termination as shown in Figure 9-11 for V_{CC} = 3.3 V. Note this Thevenin circuit is different from the DC coupled example in Figure 9-8.

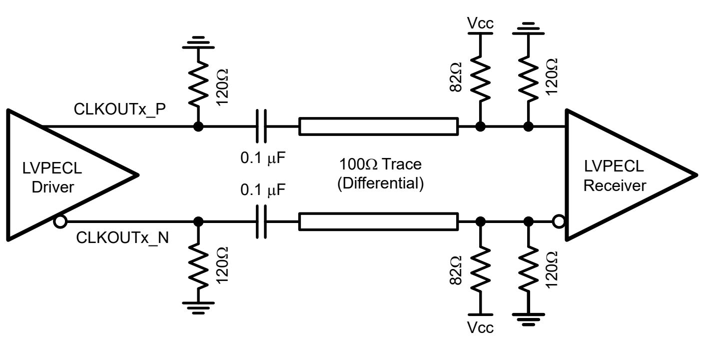


Figure 9-11. Differential LVPECL Operation, AC Coupling, Thevenin Equivalent, External Biasing at the Receiver

9.1.6.3 Termination for Single-Ended Operation

A balun can be used with either LVDS or LVPECL drivers to convert the balanced, differential signal into an unbalanced, single-ended signal.

It is possible to use an LVPECL driver as one or two separate 800 mVpp signals. When using only one LVPECL driver of a CLKOUTx_P/CLKOUTx_N pair, be sure to properly terminated the unused driver. When DC coupling one of the LMK04808C clock LVPECL drivers, the termination should be 50 Ω to V_{CC} - 2 V as shown in Figure 9-12. The Thevenin equivalent circuit is also a valid termination as shown in Figure 9-13 for Vcc = 3.3 V.

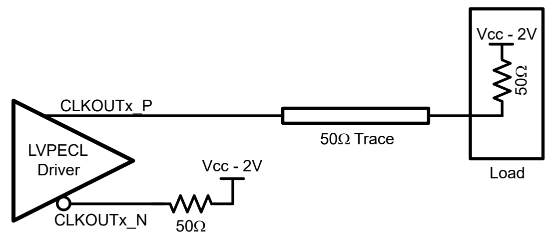


Figure 9-12. Single-Ended LVPECL Operation, DC Coupling

Figure 9-13. Single-Ended LVPECL Operation, DC Coupling, Thevenin Equivalent

When AC coupling an LVPECL driver use a 120 Ω emitter resistor to provide a DC path to ground and ensure a 50 Ω termination with the proper DC bias level for the receiver. The typical DC bias voltage for LVPECL receivers is 2 V. If the companion driver is not used it should be terminated with either a proper AC or DC termination. This latter example of AC coupling a single-ended LVPECL signal can be used to measure single-ended LVPECL performance using a spectrum analyzer or phase noise analyzer. When using most RF test equipment no DC bias point (0 VDC) is required for safe and proper operation. The internal 50 Ω termination of the test equipment correctly terminates the LVPECL driver being measured as shown in Figure 9-14.

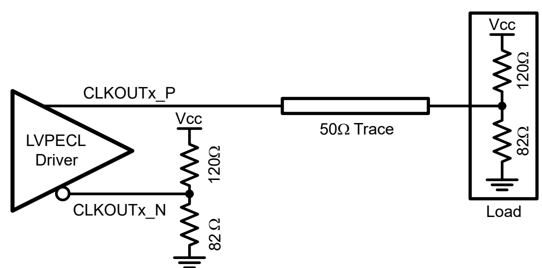


Figure 9-14. Single-Ended LVPECL Operation, AC Coupling

9.2 Typical Application

This design example highlights the available tools used to design loop filters and create a programming map.

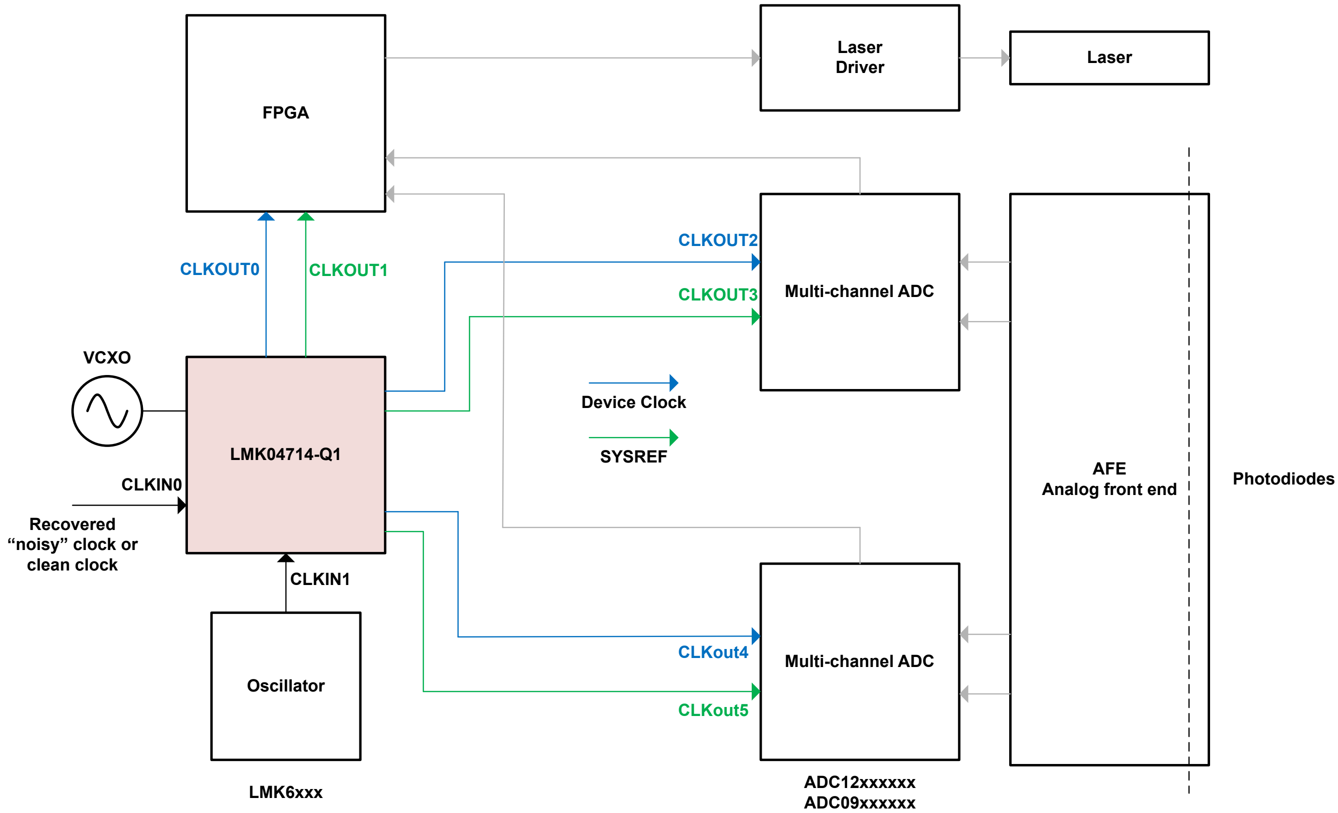


Figure 9-15. Typical LIDAR Automotive Application

9.2.1 Design Requirements

Clocks outputs:

- 1x 122.88 MHz LVCMOS
- 1x 122.88 MHz HSDS
- 1x 245.76 MHz LVPECL
- 1x 983.04 MHz LVDS
- 1x 2949.12 MHz CML

For best performance, the highest possible phase detector frequency is used at PLL2. As such, a 122.88-MHz VCXO is used. Assume that the 2949.12-MHz CML clock is the most performance critical one.

9.2.2 Detailed Design Procedure

TI has the TICSPRO and PLLatinum™ simulation tools that can be used to determine register values and design the loop filter. CML and LVPECL output formats have the best noise floor, but consume more current, therefore it is best to use these formats when noise floor matters. As for frequency planning, CLKOUT4 has the most critical output, and this output has a strong interaction with the CLKOUT6. To avoid a strong interaction, the CLKOUT6 was not used in this example and a spur was added to the CLKOUT4. The 122.88-MHz HSDS clock could potentially generate a lot of spurs and mixing products, so this HSDS clock was placed on the CLKOUT8 that has the weakest interaction with the other channels.

9.2.2.1 Device Selection

Enter the required frequencies into the tools. In this design, VCO0 and VCO1 both meet the design requirements. VCO0 offers a relatively improved VCO performance over VCO1. In this case, choose VCO0 for improved RMS jitter in the 12-kHz to 20-MHz integration range.

9.2.2.2 Device Configuration and Simulation

The tools automatically configure the simulation to meet the input and output frequency requirements given, and make assumptions about other parameters to give some default simulations. However, the user may chose to make adjustments for more accurate simulations to their application. For example:

- Entering the VCO Gain of the external VCXO or possible external VCO used device.
- Adjust the charge pump current to help with loop filter component selection. Lower charge pump currents result in smaller components but may increase impacts of leakage and at the lowest values reduce PLL phase noise performance.
- Clock Architect allows loading a custom phase noise plot for reference or VCXO block. Typically, a custom phase noise plot is entered for CLKin to match the reference phase noise to device; a phase noise plot for the VCXO can additionally be provided to match the performance of VCXO used. For improved accuracy in simulation and optimum loop filter design, be sure to load these custom noise profiles for use in application.
- The PLLatinum™ Simulation tool can also be used to design and simulate a loop filter.

9.2.2.3 Device Setup

Frequency Planning

- Even clock outputs have the simplest output path and lowest noise floor, so they were chosen.
- CLKOUT4 is used so therefore CLKOUT6 & CLKOUT7 should either not be used or at least be assigned the same frequency as CLKOUT4.
- CLKOUT8 is used, so therefore CLKOUT10 & CLKOUT11 should either not be used or at least be assigned the same frequency as CLKOUT8.

Output Formats

- CML and LVPECL are chosen for the 983.04 and 2949.12 MHz clocks for the lower noise floor
- CMOS is chosen for the 122.88 MHz clock for lower current consumption

Programming

- Using the clock design tools configuration the TICS Pro software is manually updated with this information to meet the required application.

- For best performance the input and output drive level bits may be set. Best noise floor performance is achieved with CLKout2_3_IDL = 1 and CLKout2_3_ODL = 1.
- The CLKoutX_Y_ODL bit has no impact on even clock outputs in high performance bypass mode.

9.3 System Examples

9.3.1 System Level Diagram

Figure 9-16 and Figure 9-17 show the external circuitry for clocking and for power supply.

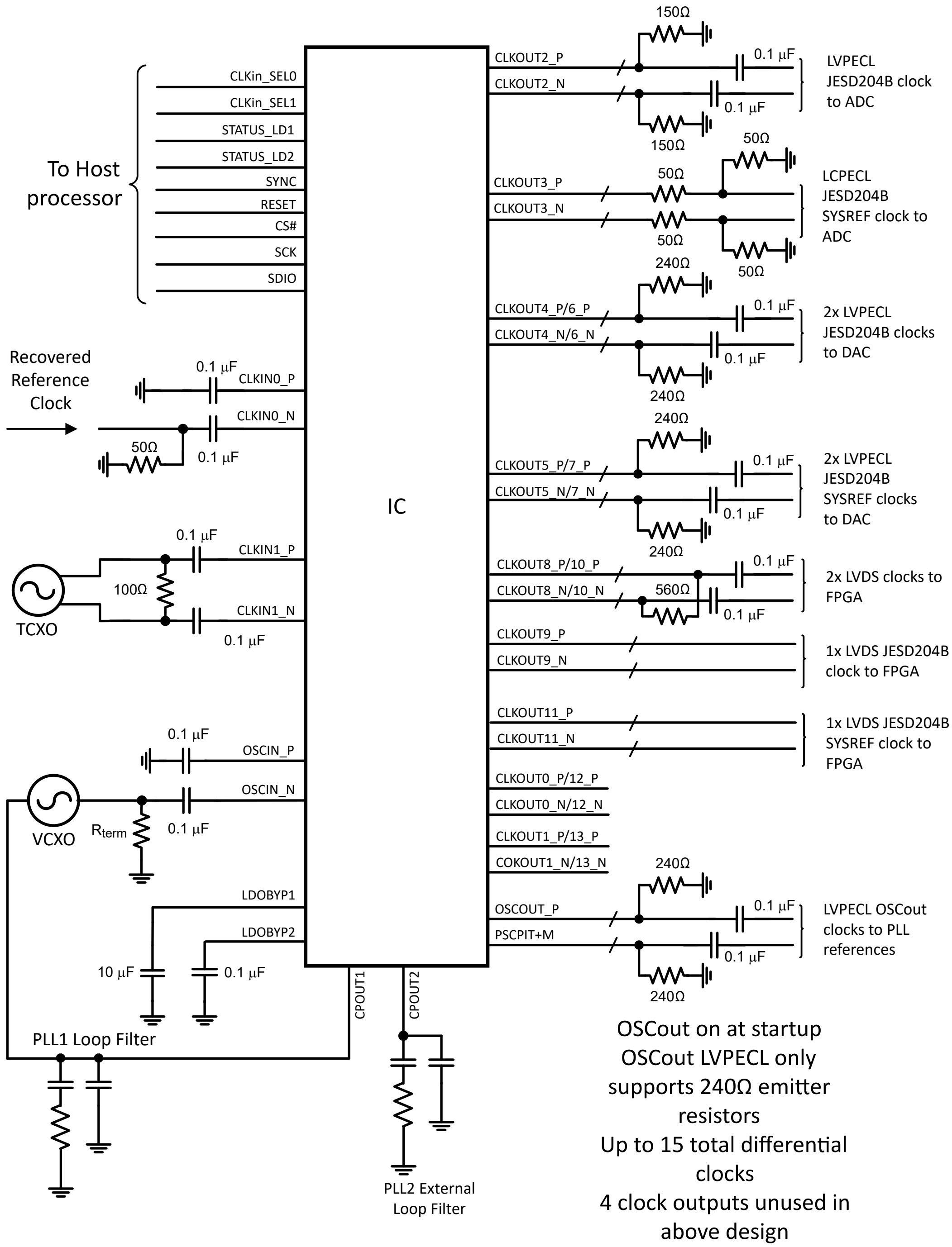


Figure 9-16. Example Application - System Schematic Except for Power

Figure 9-16 shows the primary reference clock input is at CLKin0/0*. A secondary reference clock is driving CLKin1/1*. Both clocks are depicted as AC-coupled drivers. The VCXO attached to the OSCin/OSCin* port is configured as an AC-coupled single-ended driver. Any of the input ports (CLKin0/0*, CLKin1/1*, CLKin2/2*, OSCin/OSCin*) may be configured as either differential or single-ended.

The loop filter for PLL1 is configured as a 2nd-order passive filter, while the loop filter for PLL2 is configured as a 4th order passive filter (using internal 3rd and 4th order components). Typically it is not necessary to increase the filter beyond 2nd order for PLL1. PLL2 allows software programmability of the 3rd and 4th order components.PLLatinum Sim can be used to compute the loop filter values for optimal phase noise.

All the LVPECL clock outputs are AC-coupled with 0.1 µF capacitors. Some LVPECL outputs are depicted with 240-Ω emitter resistors, and some are depicted with 150-Ω emitter resistors. LVPECL clock outputs can use emitter resistors between 120 Ω and 240 Ω. OSCout LVPECL format only supports 240-Ω emitter resistors is depicted with 240-Ω emitter resistors. The LCPECL SYSREF output is DC-coupled, with termination values matching the conditions specified for LCPECL in the electrical characteristics The JESD204B and JESD204C LVDS outputs are DC-coupled. Unused outputs are left floating.

PCB design will influence crosstalk performance. Tightly coupled clock traces will have less crosstalk than loosely coupled clock traces. Proximity to other clock traces will influence crosstalk.

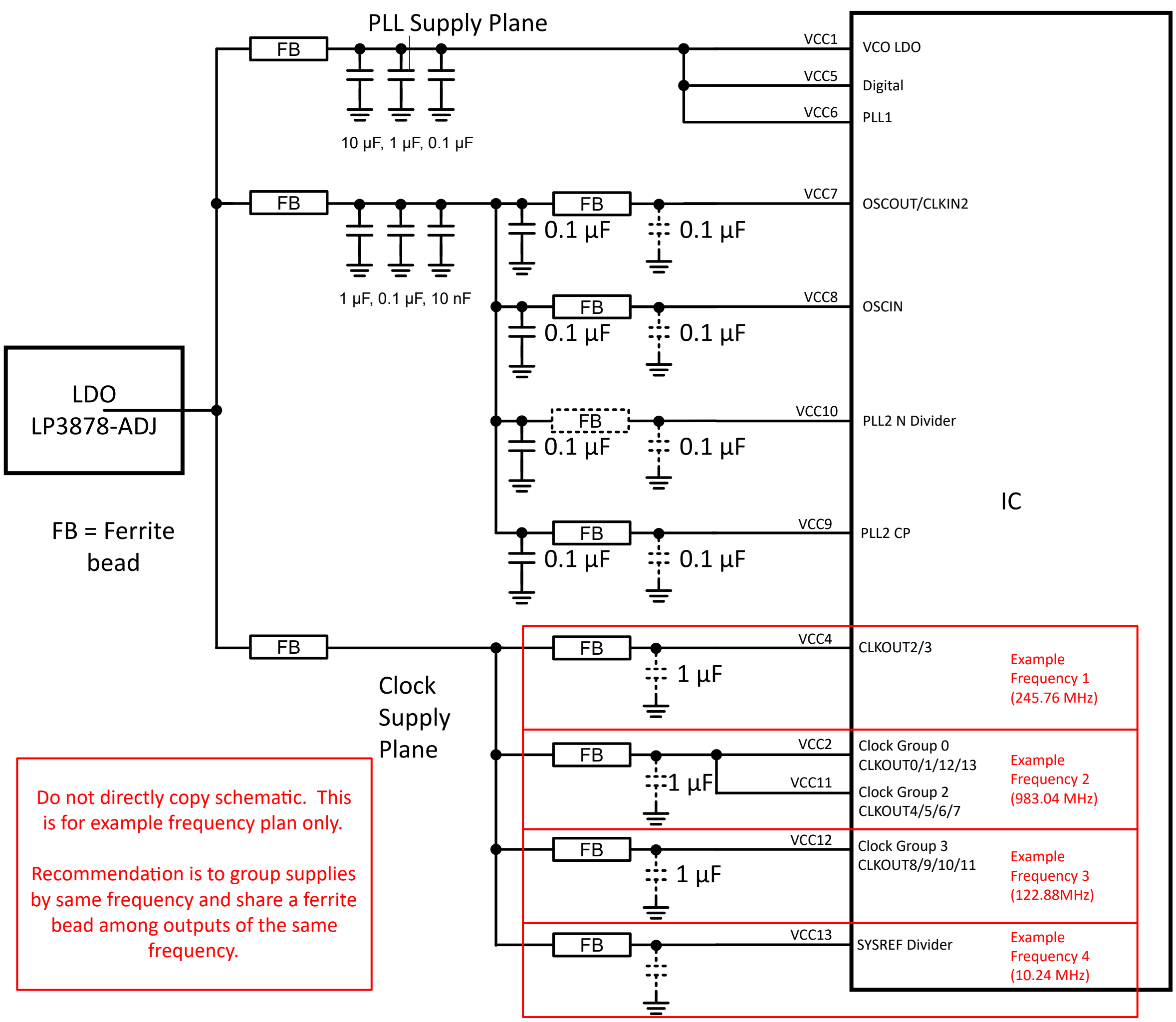


Figure 9-17. Example Application - Power System Schematic

Figure 9-17 shows an example decoupling and bypassing scheme, which could apply to the configuration shown in Figure 9-16. Components drawn in dotted lines are optional. Two power planes are used in these example designs, one for the clock outputs and one for the PLL circuits. It is possible to reduce the number of decoupling components by tying together clock output Vcc pins for CLKouts that share the same frequency or otherwise can tolerate potential crosstalk between outputs with different frequencies. In the two examples, VCC2 and VCC11 can be tied together since no outputs are utilized from Clock Group 0. PCB design will influence impedance to the supply. Vias and traces will increase the impedance to the power supply. Ensure good direct return current paths.

9.4 Power Supply Recommendations

9.5 Layout

9.5.1 Thermal Management

Power consumption can be high enough to require attention from thermal management. For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C. That is, as an estimate, T_A (ambient temperature) plus device power consumption times $R_{\theta JA}$ should not exceed 125°C.

9.5.2 Layout Guidelines

In general, the following general guidelines are useful to keep in mind.

- GND pins on the outer perimeter of the package may be routed on the package back to the DAP
- Ensure the DAP on device is well-grounded with many vias.
- Use a low loss dielectric material, such as Rogers 4350B, for optimal output power.
- For power supply bypassing, isolate each clock group.

In addition to this, there are special considerations for the routing of the outputs. The outputs are divided in to several output groups.

- Clock Group 0: CLKOUT0, CLKOUT1, CLKOUT12, CLKOUT13
- Clock Group 1: CLKOUT2, CLKOUT3
- Clock Group 2: CLKOUT4, CLKOUT5, CLKOUT6, CLKOUT7
- Clock Group 3: CLKOUT8, CLKOUT9, CLKOUT10, CLKOUT11

It is optimal to isolate the power supply pins for these clock group pins with a ferrite bead to crosstalk between the outputs, especially if the output groups have different frequencies. If there is flexibility in planning which frequencies go to which outputs, crosstalk can be minimized by putting different frequencies in different output groups (as opposed to putting them in the same output group).

9.5.3 Layout Example

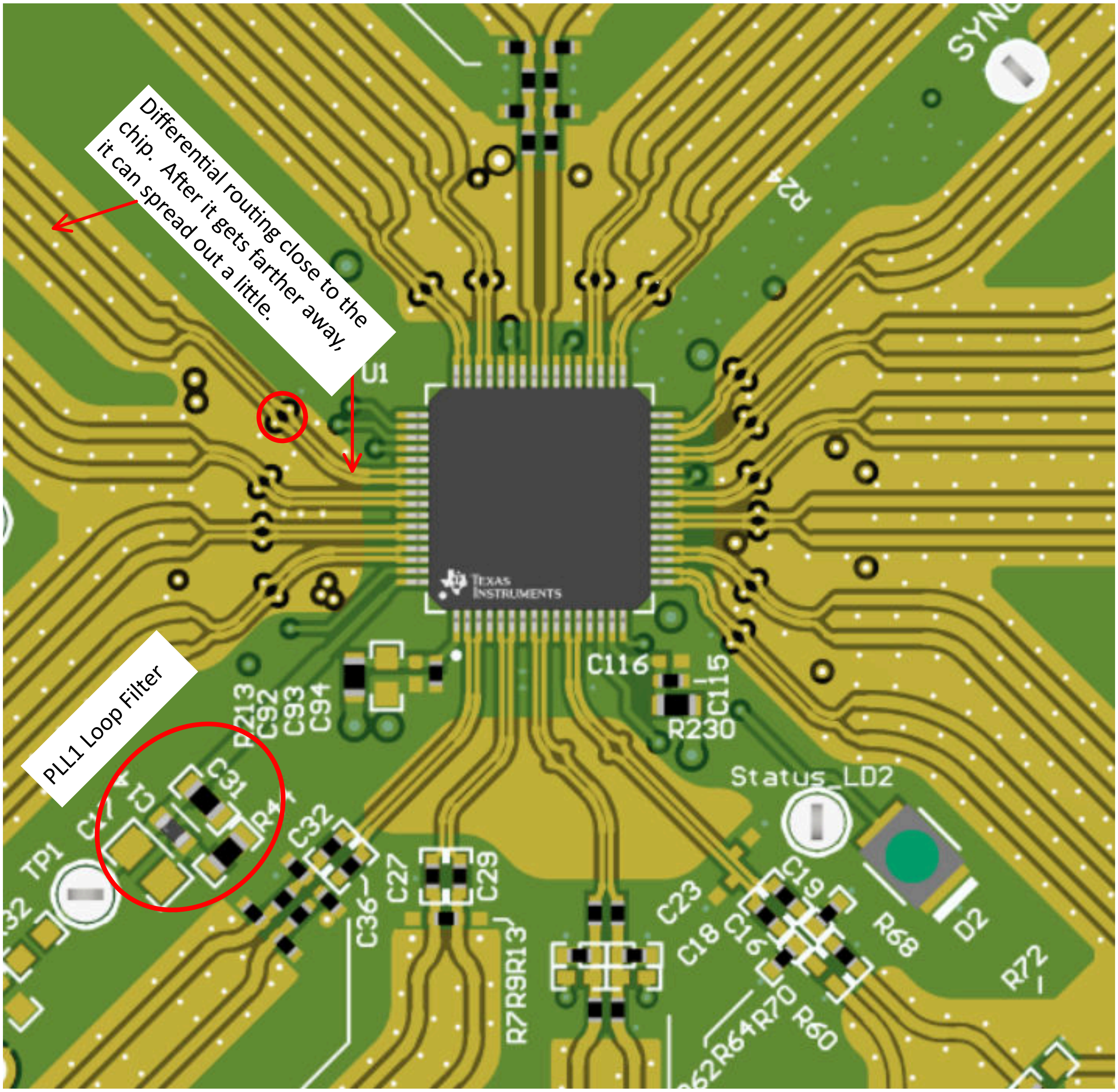


Figure 9-18. Top Layer

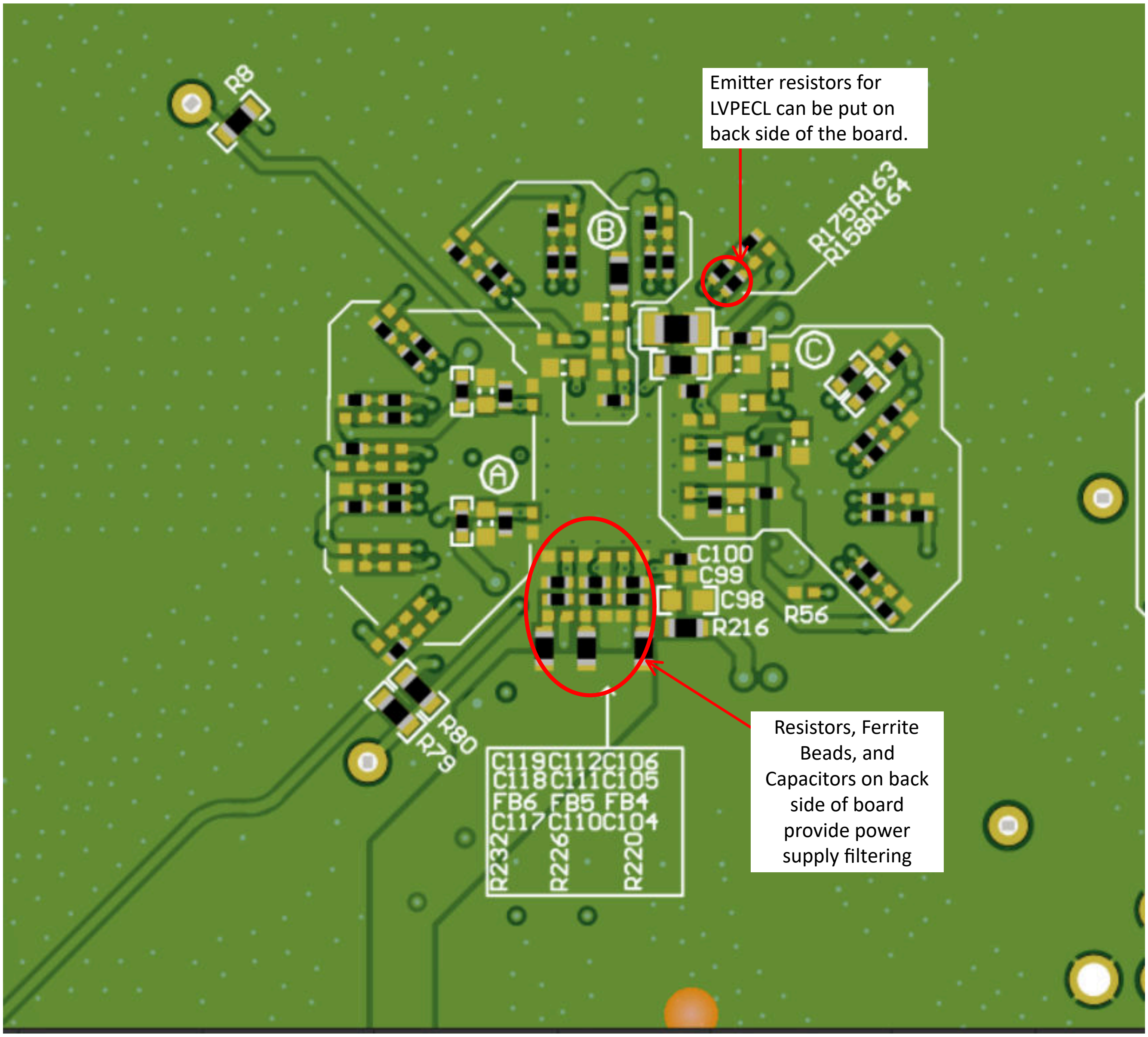


Figure 9-19. Bottom Layer

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

10.1.1.1 Clock Tree Architect

Part selection, loop filter design, simulation.

To run the online Clock Tree Architect tool, go to Clock Tree Architect.

10.1.1.2 PLLatinum Simulation

Supports loop filter design and simulation. All simulation is for a single loop, to perform dual loop simulations, the result of the first PLL simulation must be loaded as a reference to the second PLL simulation.

To download the PLLatinum™ simulation tool, go to www.ti.com/tool/PLLATINUMSIM-SW

10.1.1.3 TICS Pro

EVM programming software. Can also be used to generate register map for programming and calculate current consumption estimate.

For TICS Pro, go to www.ti.com/tool/TICSPRO-SW

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation, see the following:

- *AN-912 Common Data Transmission Parameters and their Definitions* (SNLA036)

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

PLLatinum™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

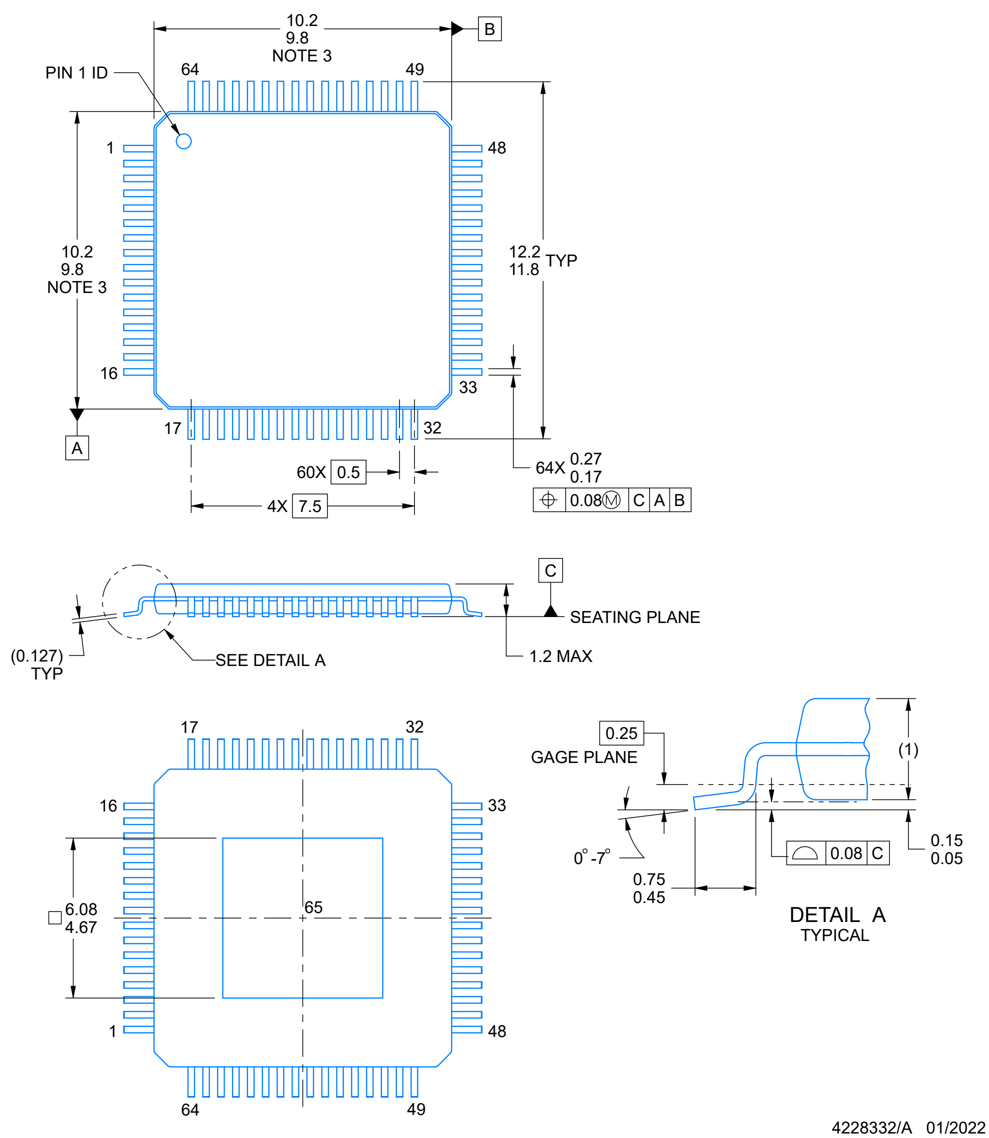
The following pages include mechanical, packaging, and orderable information. This data is subject to change without notice and revision of this document.

PACKAGE OUTLINE

PAP0064E

PowerPAD™ TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.

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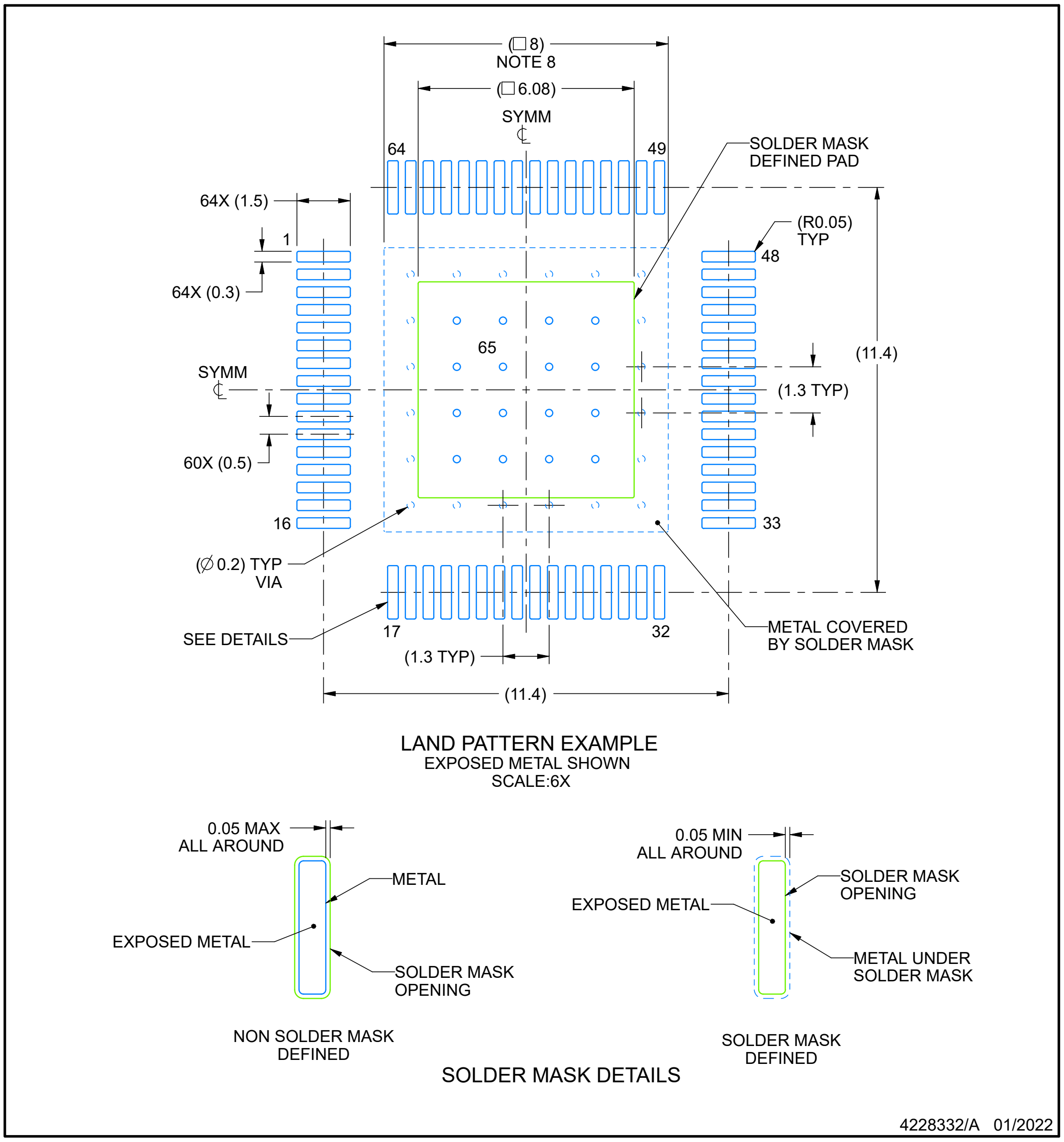
EXAMPLE BOARD LAYOUT

PAP0064E **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

TEXAS INSTRUMENTS
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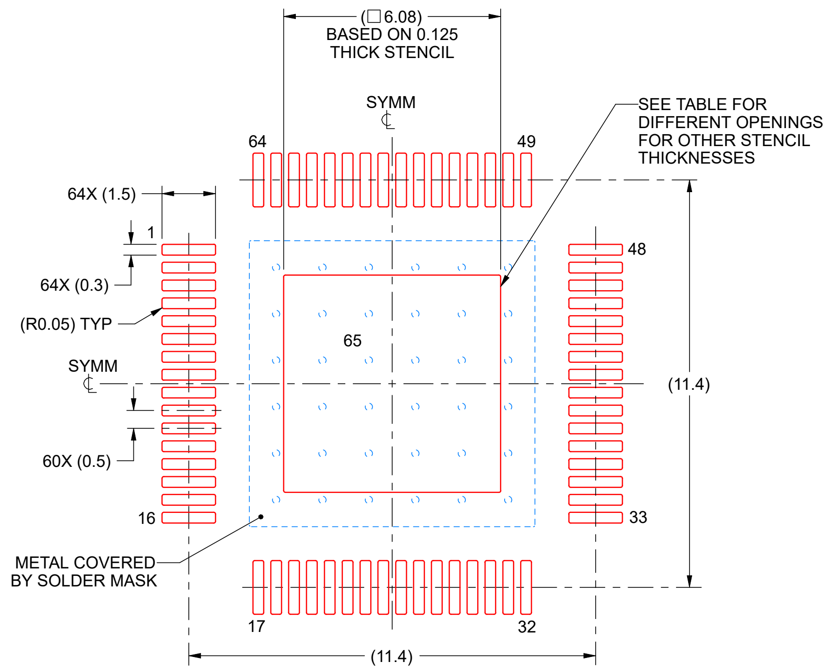
EXAMPLE STENCIL DESIGN

PAP0064E **PowerPAD™ TQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.80 X 6.80
0.125	6.08 X 6.08 (SHOWN)
0.15	5.55 X 5.55
0.175	5.14 X 5.14

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK04714QPAPRQ1	ACTIVE	HTQFP	PAP	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LMK04714 QPAPQ1	Samples
LMK04714QPAPTQ1	ACTIVE	HTQFP	PAP	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	LMK04714 QPAPQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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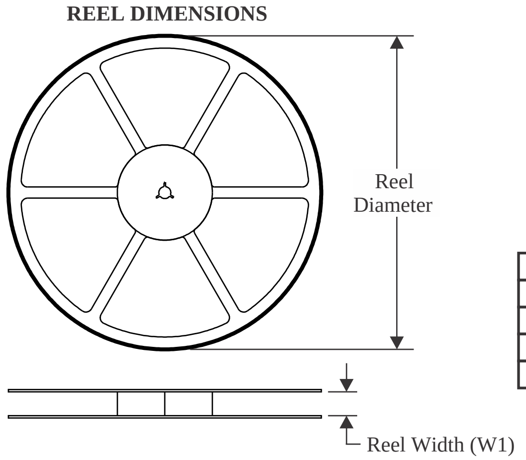
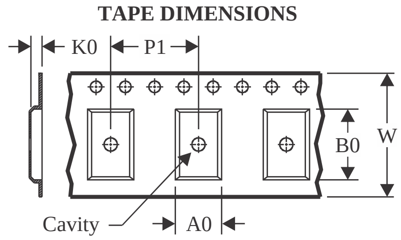
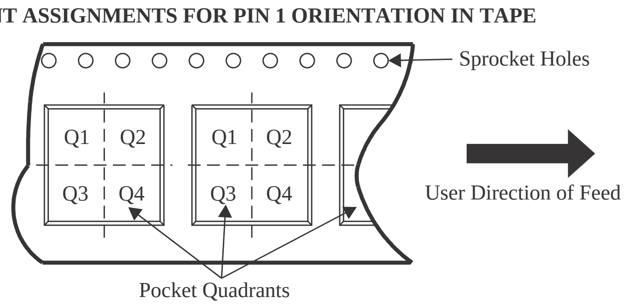
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





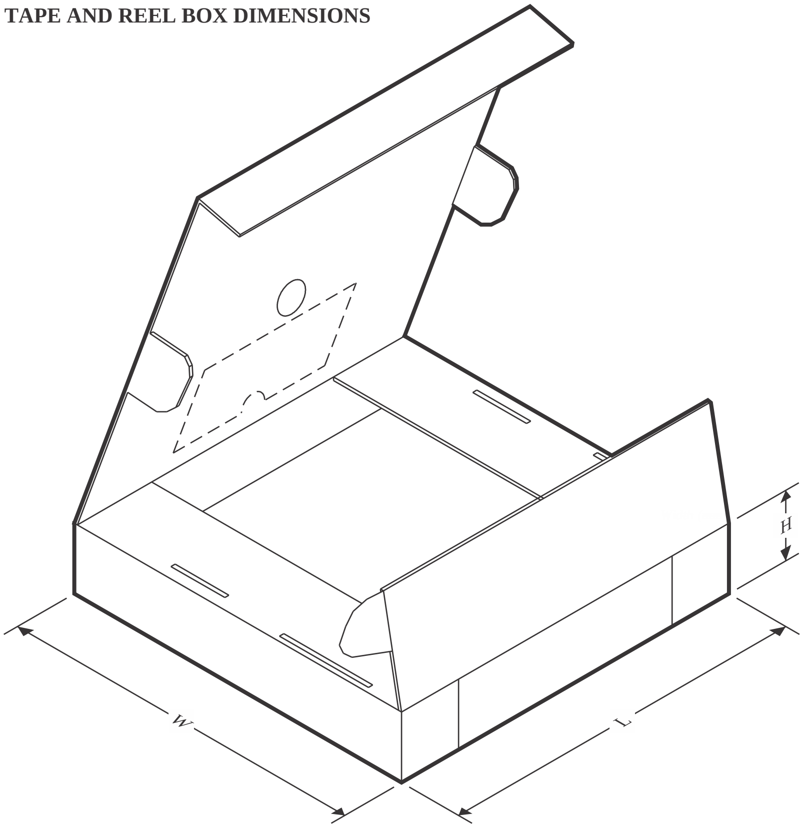
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

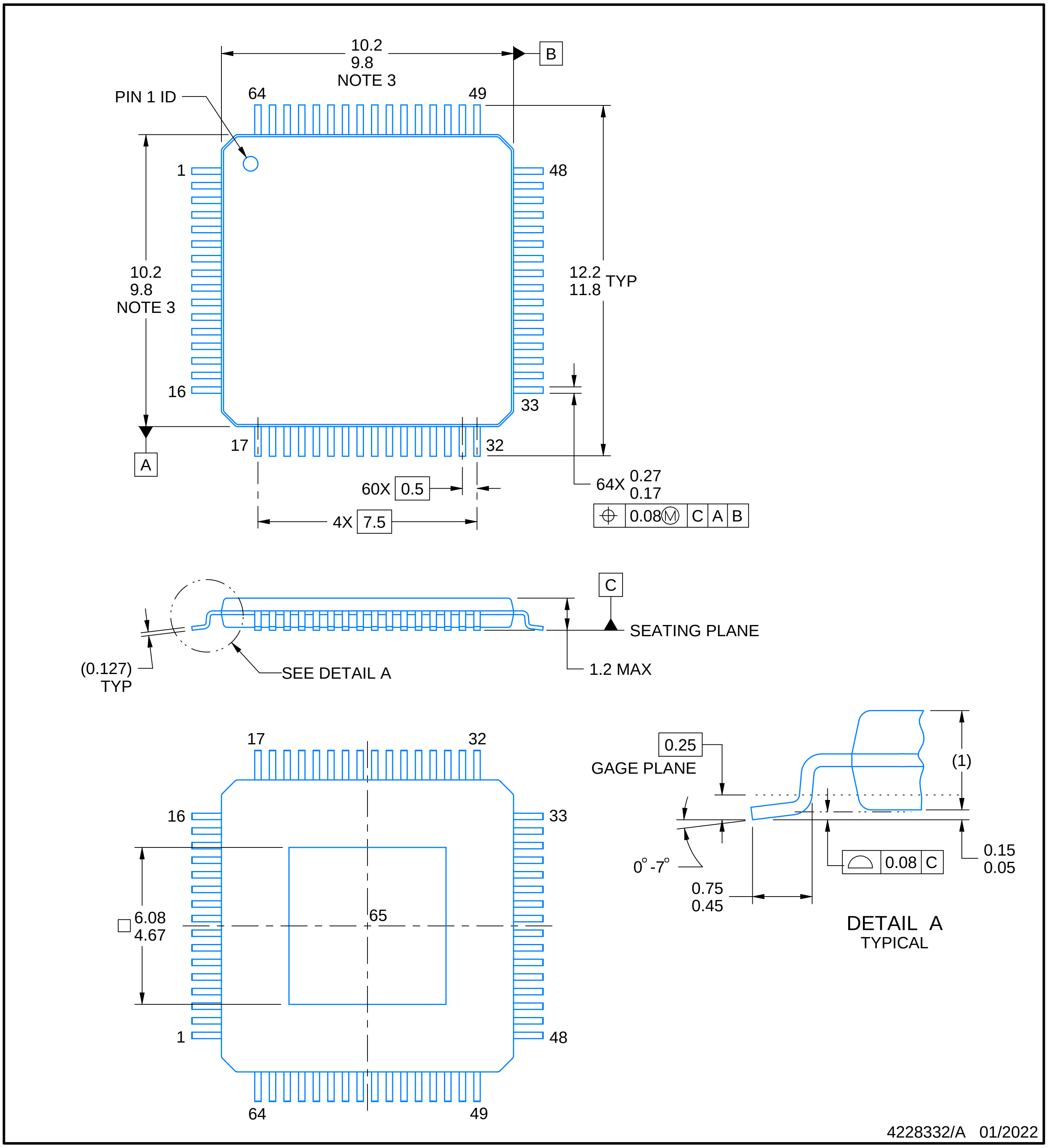
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK04714QPAPRQ1	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
LMK04714QPAPTQ1	HTQFP	PAP	64	250	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK04714QPAPRQ1	HTQFP	PAP	64	1000	367.0	367.0	55.0
LMK04714QPAPTQ1	HTQFP	PAP	64	250	367.0	367.0	55.0



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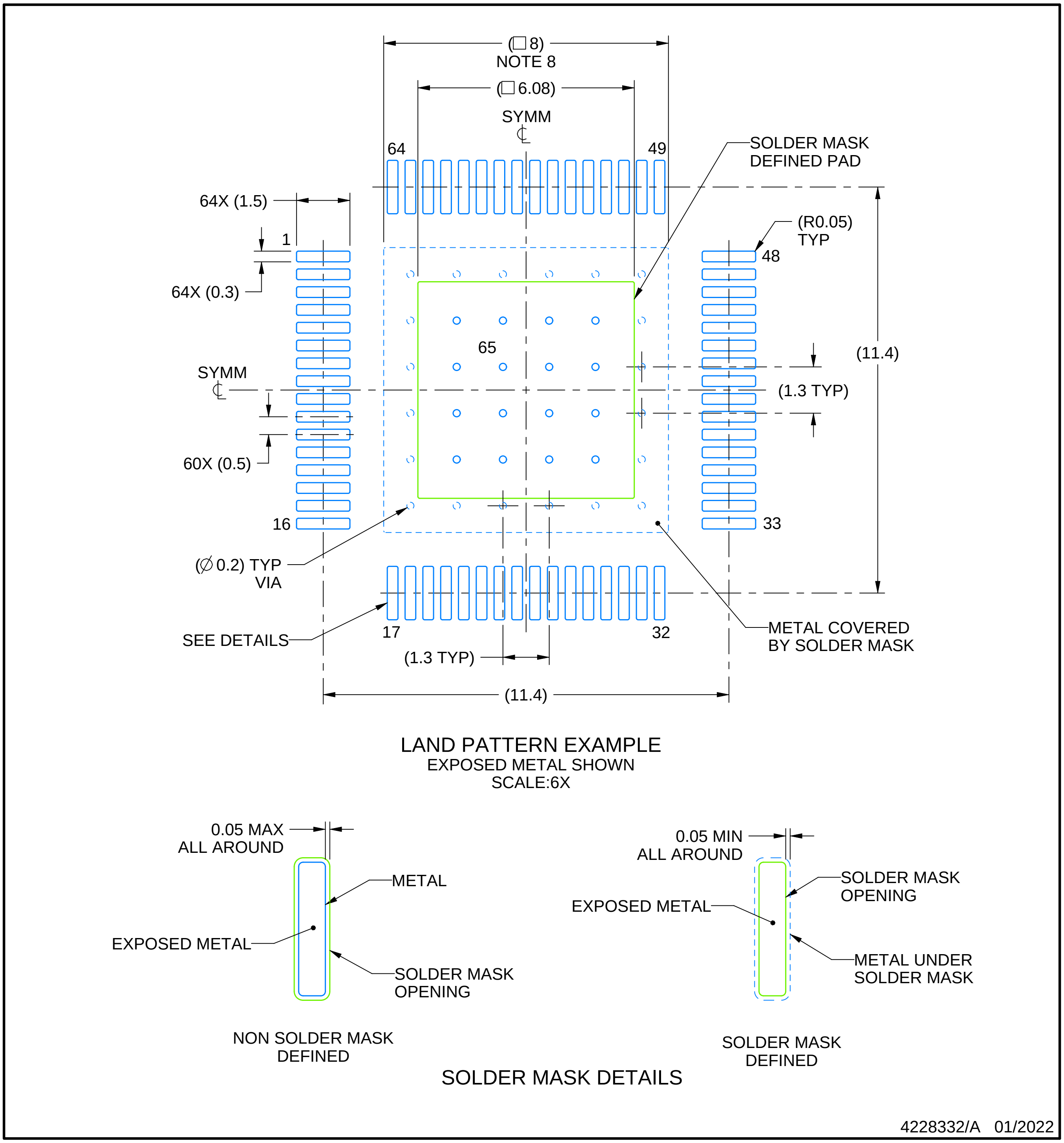

NOTES: (continued)

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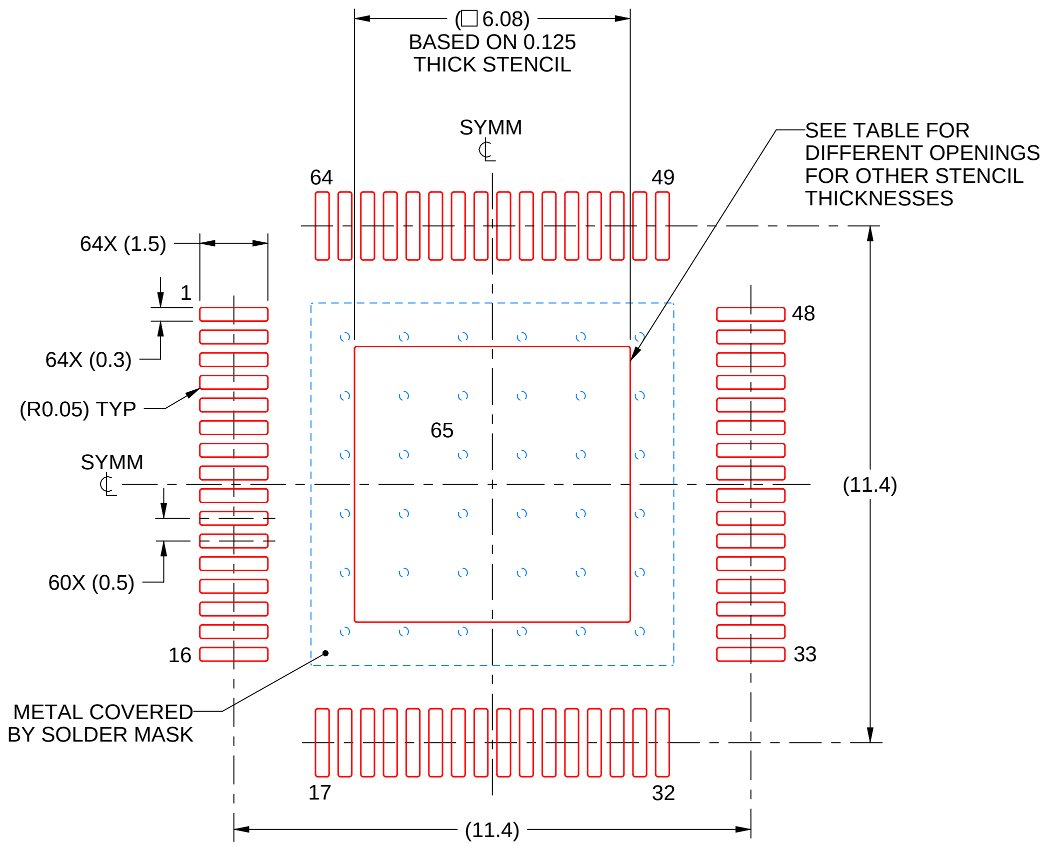

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	6.80 X 6.80
0.125	6.08 X 6.08 (SHOWN)
0.15	5.55 X 5.55
0.175	5.14 X 5.14

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