Si5510/08 Data Short

Low-Phase-Noise, Jitter-Attenuating Clock for 5G/eCPRI

The Si5510/08 are low-noise, high-performance wireless jitter attenuator clocks with any-frequency outputs for eCPRI (ethernet-based Common Public Radio Interface) applications. The Si5510/08 are based on Skyworks' fifth-generation DSPLL™ technology, which combines frequency synthesis and jitter attenuation in a highly integrated digital solution with a cost-effective oscillator without the need for any external loop filter components.

A fixed frequency oscillator (XO or XTAL) provides a phase noise reference and frequency stability for Free-Run and Holdover modes. A VCXO option is available for applications demanding the highest level of phase noise performance.

The RFPLL generates high performance low phase noise CPRI clocks for wireless remote radio heads (RRH). Each of the 18 clock outputs are configurable in any combination of high-performance JESD204B/C DCLK and SYSREF clock pairs, or other system clocks through the integer Q dividers. The RFPLL is a fully featured phase-locked-loop with adjustable DCO capability.

In addition to the RFPLL, the Si5510 integrates two low-noise MultiSynth™ fractional dividers. Any of the 18 clock outputs can be derived from either of the two MultiSynths.

Applications:

- LTE-A and 5G Remote Radio Units (RRU) or Active Antenna Units (AAU)
- JESD204B/C clock generation
- Remote Access Networks (RAN), picocells, small cells
- Remote Radio Heads (RRH), wireless repeaters, mobile fronthaul and backhaul

KEY POINTS

- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Ultra high-performance clock generation for LTE-A and 5G RRUs
- Integer output frequencies up to 3.2 GHz
- Fractional output frequencies up to 650 MHz
- JESD204B/C clock generation (DCLK/SYSREF) with synchronization across multiple devices
- Programmable delay at each output
- Ultra-low jitter: 47 fs RMS typical
- Low-Power Mode
- Phase Noise:
  - Noise floor –164 dBc/Hz at 491.52 MHz
  - –145 dBc/Hz at 800 kHz offset for a 491.52 MHz carrier frequency
- Spurs < –95 dBc at 122.88 MHz
- Supports DCO adjustable at 1 ppt resolution
- Full suite of status monitors

1. Feature List

- RFPLL
  - Supports JESD204B/C Subclass 0, 1, and 2 Clocking
  - Ultra-low Phase Noise (example at 491.52 MHz carrier):
    - –164 dBc/Hz noise floor
    - –145 dBc/Hz at 800 kHz offset
  - Ultra-low jitter performance:
    - <50 fs typ XO (12 kHz–20 MHz at 491.52 MHz)
    - <45 fs typ VCXO (12 kHz–20 MHz at 491.52 MHz)
  - Selectable jitter attenuation bandwidth: 10 Hz to 4 kHz
  - Automatic Free-Run, Holdover, and Locked modes
  - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- 18 Programmable Clock Outputs:
  - JESD204B/C DCLK or SYSREF. Up to nine DCLK/SYSREF pairs
  - Integer Q dividers: PP2S/1PPS to 3.2 GHz
  - JESD204B/C SYSREF pulser mode
  - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output-to-Output Static Delay: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, ac-coupled LVPECL, LVCMOS, slew rate limited (SRL) LVCMOS, HCSL, CML
- Utilizes fifth-generation DSPLL™ and MultiSynth technologies
- Zero Delay Mode
- 4/6 clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic holdover mode
- Core voltage: 3.3 V, 1.8 V
- Output driver supply voltages (VDDO): 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^2C or SPI (3 or 4-wire)
- ClockBuilder Pro™ (CBPro™) software tool simplifies device configuration
- Package: 72-Lead QFN, 10 x 10 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications given on this page are for reference only. Please refer to for device performance.

2. Package Outline

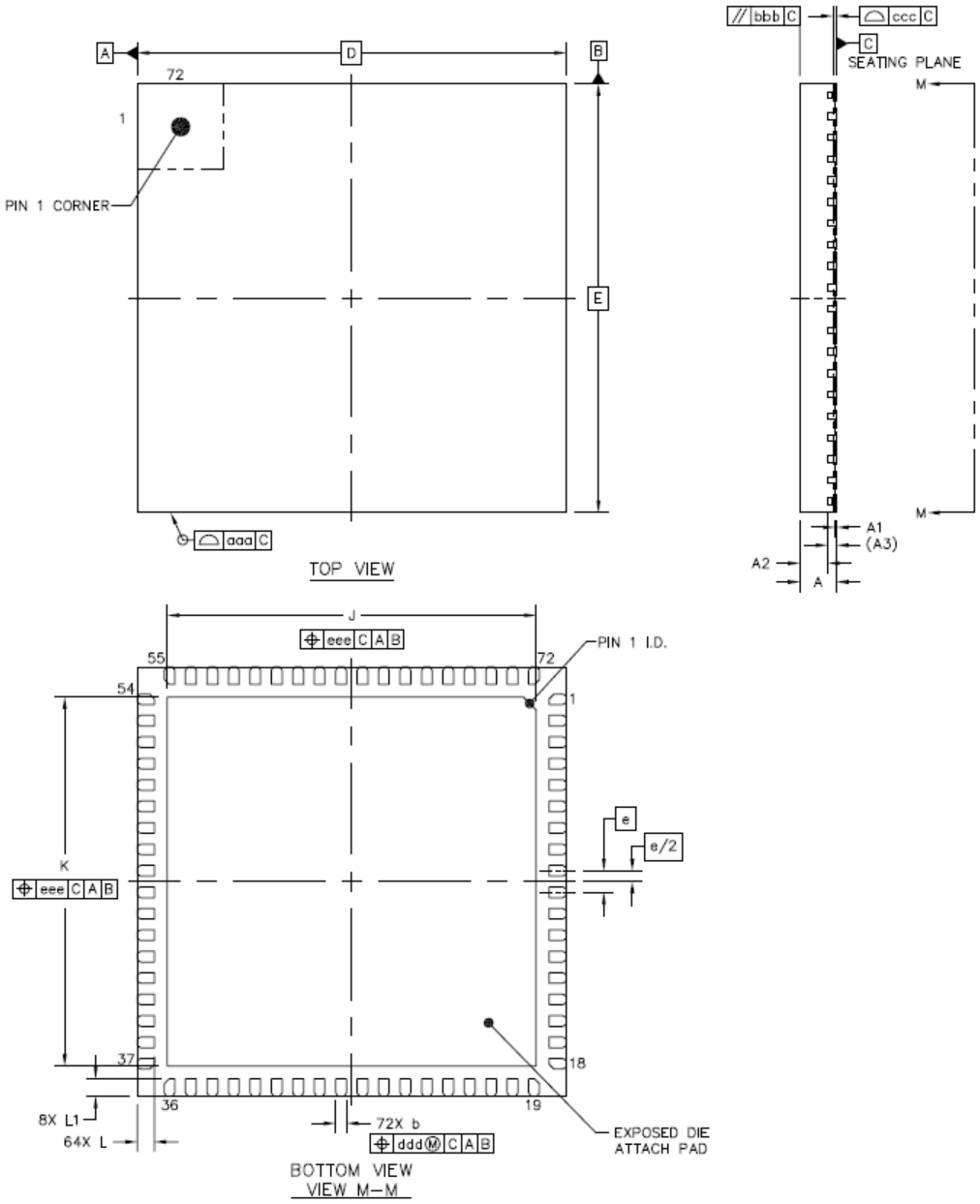

Figure 2.1. 72-QFN Package Diagram

Table 2.1. Package Dimensions

	Symbol	Min	Typ	Max
Total Thickness	A	0.8	0.85	0.9
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	–	0.65	–
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.2	0.25	0.3

		Symbol	Min	Typ	Max
Body Size	X	D		10 BSC	
	Y	E		10 BSC	
Lead Pitch		e		0.5 BSC	
EP Size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	
Weight		N/A	—	0.35g	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.

3. PCB Land Pattern

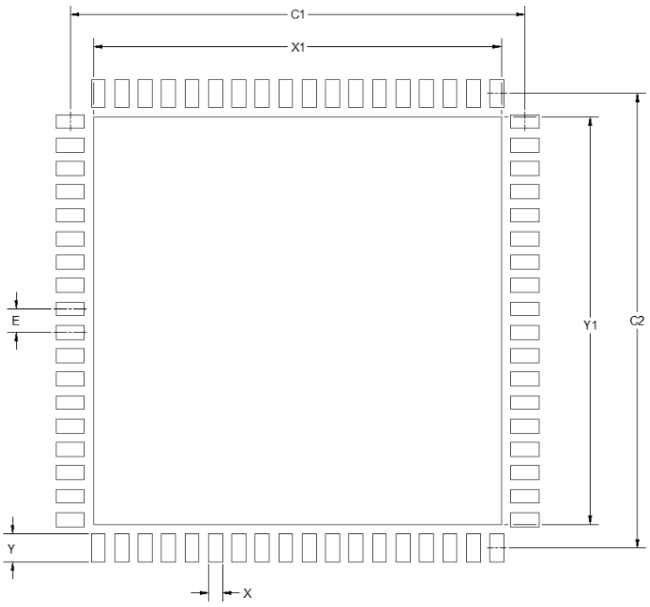

Figure 3.1. PCB Land Pattern

Table 3.1. PCB Land Pattern Dimensions

Dimension	mm
C1	9.70
C2	9.70
E	0.50
X	0.30
Y	0.60
X1	8.70
Y1	8.70

Note:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.*

SKYWORKS®

ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

skyworksinc.com/CBPro

Portfolio
skyworksinc.com

SW/HW
skyworksinc.com/CBPro

Quality
skyworksinc.com/quality

Support & Resources
skyworksinc.com/support

Skyworks Solutions, Inc. | Nasdaq: SWKS | sales@skyworksinc.com | www.skyworksinc.com
USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540