Si5403/02/01 Data Short

NetSync™ Network Synchronizer Clock for 5G/SyncE/IEEE 1588 applications

The Si540x family of NetSync™ Network Synchronizer clocks utilizes Skyworks' market-leading, fifth-generation DSPLL® and MultiSyth™ technologies. The Si540x device family consists of the Si5403, which has four PLLs, two MultiSyth any-frequency dividers, and 18 outputs. The Si5402 has four PLLs and two MultiSyths with 14 outputs, and the Si5401 completes the device family with three PLLs, one MultiSyth, and 10 outputs.

This feature-rich family of devices does not require external loop filters and has internal voltage supply regulation that reduce susceptibility to supply noise. Additional features include low transient hitless switching, low-power mode, and a full suite of status monitors.

NetSync clocks offer Synchronous Ethernet (SyncE)-compliant wander filtering and software adjustment of output frequency and phase for IEEE 1588 applications while offering ultra-low jitter output clocks, which eliminates the need for a follow-on jitter attenuator device.

For IEEE 1588 Precision Time Protocol (PTP) applications, the Si540x devices are available with Skyworks' AccuTime™ software to provide a full IEEE 1588-2008 compliant solution including operation in full timing support (FTS), partial timing support (PTS), and assisted partial timing support (APTS). Alternatively, the IEEE 1588-ready hardware features of the Si540x can be coupled with existing or third-party software to provide a complete solution.

This unique combination of features offers savings in system costs, PCB real estate, and power consumption, which makes them an ideal choice for today's complex equipment.

Applications:

- Core, metro and edge switches and routers
- 5G BBUs
- 5G O-RAN
  - Central unit (O-CU)
  - Distributed unit (O-DU)
  - Front-haul gateway switches (FHGWS)
- IEEE 1588 grandmasters, boundary clocks and slaves
- SmartNICs

KEY POINTS

- Ultra high-performance network synchronizer for wireline applications
- SyncE, SONET, and SDH
- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Optional AccuTime™ IEEE 1588 software
- Integer output frequencies up to 1.2288 GHz
- Fractional output frequencies up to 650 MHz
- Programmable delay at each output
- Ultra-low jitter 51 fs RMS typ
- Low-Power Mode
- Supports IEEE1588 with DCO adjustable at 1ppt resolution
- Locks to 1PPS and PP2S
- Full suite of status monitors
- Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), G.8262 (EEC Options 1 and 2), G.8262.1 (eEEC), and G.8273.1 (T-GM)
- AccuTime™ IEEE 1588 Software
  - Field tested proven with compliance reports available
  - Demonstration Platform Support
  - O-RAN compatible
  - IEEE 1588 servo loop and protocol stack software runs on host processor

1. Feature List

- REFPLL
  - Provides low-noise outputs using an external crystal or crystal oscillator
  - Provides output stability and holdover from external TCXO or OCXO
  - Excellent jitter performance:
    - 52 fs typ (12 kHz–20 MHz at 312.5 MHz)
  - Selectable jitter attenuation bandwidth: 10 Hz to 4 kHz
- DSPLL A, DSPLL B
  - Independent network synchronization DSPLLs
  - Supports ITU-T G.8273.2 (T-TSC, T-BC) and ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A)
  - Programmable loop bandwidth: 1 mHz to 4 kHz
  - Automatic Free-Run, Holdover, and Locked modes
  - Input monitoring
  - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- PPSPLL
  - Dedicated PLL for 1PPS and PP2S inputs
  - Targeted at IEEE1588 grandmaster and APTS applications
  - Can modulate DSPLL A to support frequency lock to a higher frequency clock and simultaneous phase lock to a 1PPS/PP2S
  - Adaptive architecture allows rapid locking
  - Programmable loop bandwidth 1 mHz to 25 mHz
  - Programmable phase slope limiting (PSL) and phase pull-in rate (PPI)
- 18 Programmable Clock Outputs:
  - Integer Q dividers: PP2S/1PPS to 1.2288 GHz
  - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output Delay Adjustment: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, AC coupled LVPECL, LVCMOS, slew rate limited (SRL) LVCMOS, HCSL, CML
- Zero Delay Mode for all PLLs
- Three differential or five single-ended clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 1PPS, PP2S, 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic holdover mode
- Low-Power Mode
- Core voltage: 3.3 V, 1.8 V
- Output supply pins: 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^2C or SPI (3 or 4-wire)
- In-circuit programmable with non-volatile memory
- ClockBuilder Pro™ software tool simplifies device configuration
- Package: 72-Lead QFN, 10x10 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications given on this page are for reference only. Refer to for device performance.

2. Package Outline

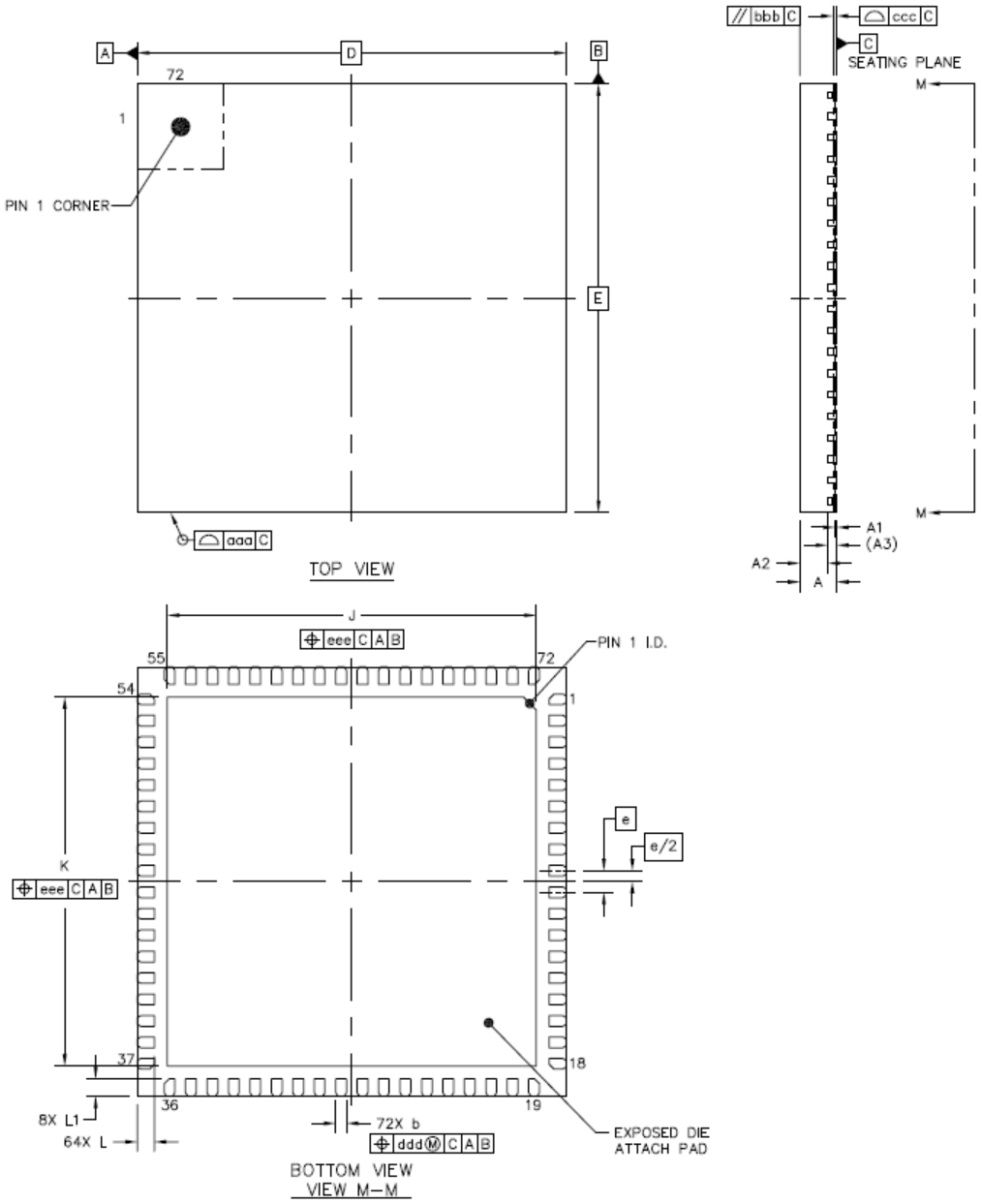

Figure 2.1. 72-QFN Package Diagram

Table 2.1. Package Dimensions

	Symbol	Min	Typ	Max
Total Thickness	A	0.8	0.85	0.9
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	–	0.65	–
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.2	0.25	0.3

		Symbol	Min	Typ	Max
Body Size	X	D		10 BSC	
	Y	E		10 BSC	
Lead Pitch		e		0.5 BSC	
EP Size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	
Weight		N/A	—	0.35g	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.

3. PCB Land Pattern

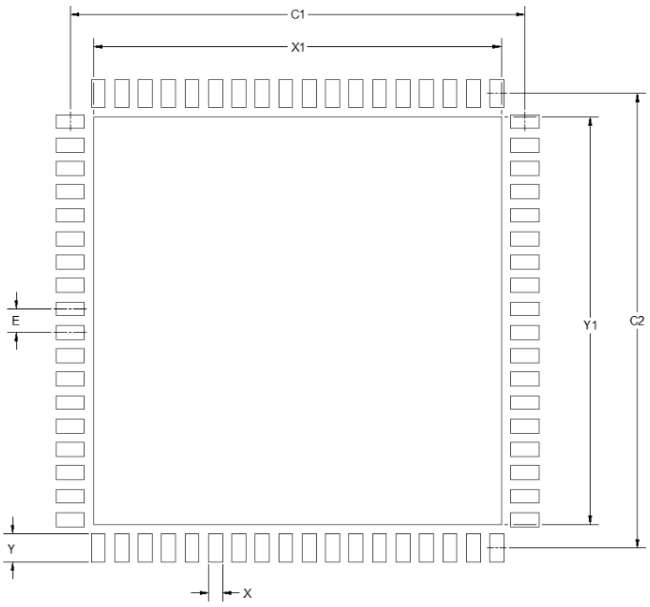

Figure 3.1. PCB Land Pattern

Table 3.1. PCB Land Pattern Dimensions

Dimension	mm
C1	9.70
C2	9.70
E	0.50
X	0.30
Y	0.60
X1	8.70
Y1	8.70

Note:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.*

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