

# 3.3 V/5 V, 50 MHz to 200 MHz PECL Clock Synthesizer

# **NB4N507A**

# Description

The NB4N507A is a precision clock synthesizer which generates a very low jitter differential PECL output clock. It produces a clock output based on an integer multiple of an input reference frequency.

The NB4N507A accepts a standard fundamental mode crystal, using Phase–Locked–Loop (PLL) techniques, will produce output clocks up to 200 MHz. In addition, the PLL circuitry will produce a 50% duty cycle square–wave clock output (see Figure 7).

The NB4N507A can be programmed to generate a selection of input reference frequency multiples. An exact 155.52 MHz output clock can be generated from a 19.44 MHz crystal and the x8 multiplier selection. The NB4N507A is intended for low output jitter clock generation.

The PECL outputs are 15 mA open collector and must be DC loaded and AC terminated. See Figures 4 and 6.

### **Features**

- Input Crystal Frequency of 10 27 MHz
- Enable Usage of Common Low-Cost Crystal
- Differential PECL Output Clock Frequencies up to 200 MHz
- Duty Cycle of 48%/52%
- Operating Range: V<sub>CC</sub> = 3.0 V to 5.5 V
- Ideal for SONET Applications and Oscillator Manufacturers
- Available in Die Form
- Packaged in 16-Pin Narrow SOIC
- Pb-Free Packages are Available\*

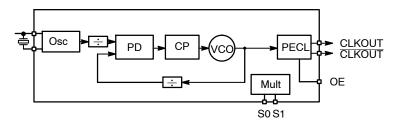
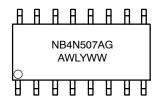


Figure 1. Simplified Logic Block Diagram



SOIC-16 D SUFFIX CASE 751B-05

### **MARKING DIAGRAM**



A = Assembly Location
WL = Wafer Lot

Y = Year
WW = Work Week
G = Pb-Free Package

# **ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

<sup>\*</sup>For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

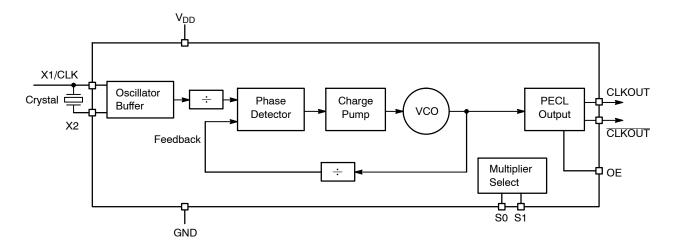


Figure 2. NB4N507A Logic Diagram

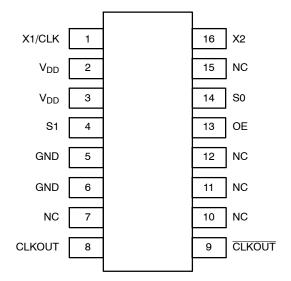


Figure 3. 16-Pin SOIC (Top View)

**Table 1. CLOCK MULTIPLIER SELECT TABLE** 

S1	S0	Multiplier
L	L	9.72X*
L	М	10X
L	Н	12X
M	L	6.25X
M	М	8X
M	Н	5X
Н	L	NA
Н	М	3X
Н	Н	4X

<sup>\*</sup>Example Crystal = 16 MHz, f<sub>CLKOUT</sub> = 155.52 MHz

**Table 2. OE, OUTPUT ENABLE FUNCTION** 

OE	Function
0	Disable
1	Enable

L = GND

 $H = V_{DD}$  M = OPEN

**Table 3. PIN DESCRIPTION** 

Pin # SOIC-16	Name	I/O	Description
1	X1/CLK	Crystal Input	Crystal or Clock Input
2,3	$V_{DD}$	Power Supply	Positive Supply Voltage (3.0 V to 5.5 V)
4	S1	Tri-Level Input	Multiplier Select Pin; When Left Open, Defaults to V <sub>DD</sub> ÷ 2
5,6	GND	Power Supply	Negative Supply Voltage
7,10,11,12, 15	NC	No Connect	Pin 10 does not require an external resistor. The NB4N507A will function with or without a resistor on Pin 10.
8	CLKOUT	PECL Output*	Non-inverted differential PECL clock output.
9	CLKOUT	PECL Output*	Inverted differential PECL clock output.
13	OE	(LV)CMOS/(LV)TTL Input	Output Enable for the CLKOUT/CLKOUT Outputs. Outputs are enabled when HIGH or when left open; OE pin has internal pullup resistor. Disables both outputs when LOW. CLKOUT goes LOW, CLKOUT goes HIGH.
14	S0	Tri-Level Input	Multiplier Select Pin; When Left Open, Defaults to V <sub>DD</sub> ÷ 2
16	X2	Crystal Input	Crystal Input

<sup>\*</sup>The PECL Outputs are 15 mA open collector and must be DC loaded and AC terminated. See Figures 4, 5 and 6.

**Table 4. ATTRIBUTES** 

Chara	Value	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 1 kV > 150 V > 1 kV
Moisture Sensitivity, Indefinite	Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	1145 Devices	
Meets or exceeds JEDEC Spec	c EIA/JESD78 IC Latchup Test	

<sup>1.</sup> For additional information, see Application Note AND8003/D.

# **Table 5. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		6	V
VI	Input Voltage			GND $-0.5 \le V_{I} \le V_{DD} + 0.5$	V
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-16	100 60	°C/W
θJC	Thermal Resistance (Junction-to-Case)	(Note 2)	SOIC-16	33 to 36	°C/W
T <sub>sol</sub>	Wave Solder Pb Pb-Free	< 3 sec @ 248°C < 3 sec @ 260°C		265 265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 6. DC CHARACTERISTICS ( $V_{DD} = 3.0 \text{ V to } 5.5 \text{ V}$ , GND = 0 V,  $T_A = -40 ^{\circ}\text{C}$  to  $+85 ^{\circ}\text{C}$  (Note 3))

Symbol	Characteristic		Min	Тур	Max	Unit
I <sub>DD</sub>	Power Supply Current (does not include output load resistor current)	$V_{DD} = 5 V$ $V_{DD} = 3.3 V$	15 10	27 23	35 30	mA mA
V <sub>OH</sub>	Output HIGH Voltage (Notes 5 & 6)	$V_{DD} = 5 V$ $V_{DD} = 3.3 V$	3.95 2.57	4.05 2.67	4.15 2.77	V
V <sub>OL</sub>	Output LOW Voltage (Notes 5 & 6)	$V_{DD} = 5 V$ $V_{DD} = 3.3 V$	3.12 1.90	3.20 2.00	3.30 2.10	V
V <sub>IH</sub>	Input HIGH Voltage (Note 4)	S0, S1, X1/CLK OE	V <sub>DD</sub> – 0.5 2.0		V <sub>DD</sub>	V
V <sub>IL</sub>	Input LOW Voltage,(Note 4)	S0, S1, X1/CLK OE	0		0.5 0.8	V
C <sub>x</sub>	Internal Crystal Capacitance, X1 & X2			0		pF
C <sub>in</sub>	Input Capacitance, S0, S1, OE			5.0		pF

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 3. PECL output parameters vary 1:1 with  $V_{DD}$ .
- 4. S0 and S1 default to  $V_{DD} \div 2$  when left open.

Table 7. AC CHARACTERISTICS ( $V_{DD}$  = 3.0 V to 5.5 V, GND = 0 V,  $T_A$  =  $-40^{\circ}$ C to  $+85^{\circ}$ C (Note 5))

Symbol	Characteristic	Min	Тур	Max	Unit
f <sub>Xtal</sub>	Crystal Input Frequency (Note 7)	10		27	MHz
f <sub>CLK</sub>	Input Clock Frequency (Note 8)	5		52	MHz
f <sub>OUT</sub>	Output Frequency Range	50		200	MHz
V <sub>out pk-pk</sub>	Output Amplitude	550	680		mV
DC	Clock Output Duty Cycle (Note 8)	48		52	%
PLL <sub>BW</sub>	PLL Bandwidth (Note 8)	10			kHz
t <sub>jitter (pd)</sub>	Period Jitter (RMS, 1σ, 10,000 Cycles)			10	ps
t <sub>jitter (pd)</sub>	Period Jitter (Peak-to-Peak, 10,000 Cycles)			±20	ps
tr/tf	Output Rise and Fall Times (Note 8)	50	270	500	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

- 5. PECL outputs loaded with external resistors for proper operation (see Figures 4, 5 and 6).
- 6. V<sub>OH</sub> and V<sub>OL</sub> can be set by the external resistors, which can be modified.
   7. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. The value of these capacitors is given by the following equation, where CL is the specified crystal load capacitance: Crystal caps (pF) = (CL-5) x 2. So, for a crystal with 16 pF load capacitance, use two 22 pF caps, including board trace capacitance (see Figure 7).
- 8. Guaranteed by design and characterization.

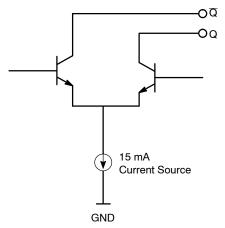


Figure 4. Output Structure

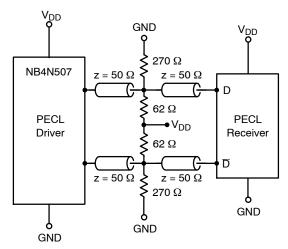


Figure 5. Evaluation Test Load for the NB4N507A

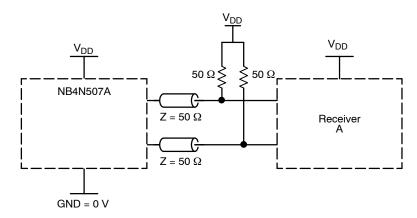


Figure 6. Alternate Termination for Output Driver and Device Evaluation

# APPLICATIONS INFORMATION

High Frequency Differential PECL Oscillators: The NB4N507A, along with a low frequency fundamental mode crystal, can build a high frequency differential PECL output oscillator. For example, a 10 MHz crystal connected to the NB4N507A with the 12X output selected (S1 = 0, S0 = 1) produces a 120 MHz PECL output clock.

# **Crystal Oscillator Input Interface**

The NB4N507A features an integrated crystal oscillator to minimize system implementation costs. The oscillator circuit is a parallel resonant circuit and thus, for optimum performance, a parallel resonant crystal should be used.

As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the NB4N507A as possible to avoid any board level parasitics. Surface mount crystals are recommended, but not required.

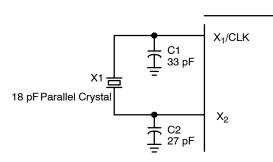


Figure 7. Crystal Input Interface

# **High Frequency VCXO:** The bandwidth of the PLL is guaranteed to be greater than 10 kHz. This means that the PLL will track any modulation on the input with a frequency of less than 10 kHz. By using this property, a low frequency VCXO can be built. The output can then be multiplied by the NB4N507A, thereby producing a high frequency VCXO.

**High Frequency TCXO:** Extending the previous application, an inexpensive, low frequency TCXO can be built and the output frequency can be multiplied using the NB4N507A. Since the output of the chip is phase–locked to the input, the NB4N507A has no temperature dependence, and the temperature coefficient of the combined system is the same as that of the low frequency TCXO.

# **Decoupling and External Components**

The NB4N507A requires a 0.01  $\mu$ F decoupling capacitor to be connected between  $V_{DD}$  and GND on pins 2 and 5. It must be connected close to the NB4N507A. Other  $V_{DD}$  and GND connections should be connected to those pins, or to the  $V_{DD}$  and GND planes on the board. Another four resistors are needed for the PECL outputs as shown in Figure 4. Suggested values of these resistors are shown, but they can be varied to change the differential pair output swing, and the DC level.

# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NB4N507ADG	SOIC-16 (Pb-Free)	48 Units / Rail
NB4N507ADR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# Resource Reference of Application Notes

AN1405/D - ECL Clock Distribution Techniques

AN1406/D - Designing with PECL (ECL at +5.0 V)

AN1503/D - ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D - Metastability and the ECLinPS Family

AN1568/D - Interfacing Between LVDS and ECL

AN1672/D - The ECL Translator Guide

AND8001/D - Odd Number Counters Design

AND8001/D - Odd Number Counters Design
AND8002/D - Marking and Date Codes

AND8090/D - AC Characteristics of ECL Devices

# **Resource Reference of Application Notes**

AND8020/D - Termination of ECL Logic Devices

AND8066/D - Interfacing with ECLinPS

AND8090/D - AC Characteristics of ECL Devices

ECLinPS is a trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.



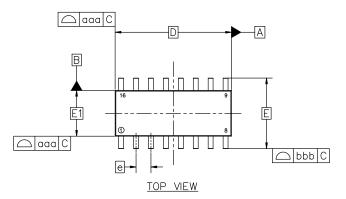


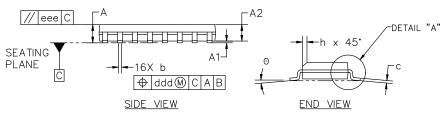
# SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

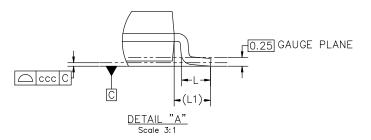
# **DATE 29 MAY 2024**

### NOTES:

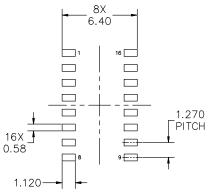
- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- 2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
- 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
- DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE 6 DIMENSION AT MAXIMUM MATERIAL CONDITION.







MILLIMETERS						
DIM	MIN	NOM	MAX			
А	1.35	1.55	1.75			
A1	0.00	0.05	0.10			
A2	1.35	1.50	1.65			
b	0.35	0.42	0.49			
С	0.19	0.22	0.25			
D		9.90 BSC				
E		6.00 BSC				
E1	3.90 BSC					
е		1.27 BSC				
h	0.25		0.50			
L	0.40	0.83	1.25			
L1		1.05 REF				
Θ	0.		7°			
TOLERAN	CE OF FC	RM AND	POSITION			
aaa	0.10					
bbb	0.20					
ccc		0.10				
ddd		0.25				
eee		0.10				



# RECOMMENDED MOUNTING FOOTPRINT

\*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE onsemi SOLDERING
AND MOUNTING TECHNIQUES REFERENCE
MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from Printed versions are uncontrolled except when stamped "CONTROLLED"	
DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1	.27P	PAGE 1 OF 2

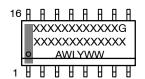
onsemi and ONSemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



# SOIC-16 9.90x3.90x1.50 1.27P CASE 751B ISSUE L

**DATE 29 MAY 2024** 

# GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code

A = Assembly Location

WL = Wafer Lot
 Y = Year
 WW = Work Week
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

077/15/		077/15.0		071/15 0		T	
STYLE 1: PIN 1.	COLLECTOR	STYLE 2:	CATHODE	STYLE 3: PIN 1.		TYLE 4: PIN 1.	COLLECTOR DVF #1
PIN 1. 2.		PIN 1. 2.		PIN 1. 2.	COLLECTOR, DYE #1 BASE, #1	2.	
2. 3.	EMITTER	2. 3.	NO CONNECTION				
				3.		3.	
4.	NO CONNECTION	4.		4.		4.	
5.	EMITTER	5.		5.		5.	
6.	BASE	6.		6.		6.	
7.		7.			EMITTER, #2		COLLECTOR, #4
8.		8.		8.			COLLECTOR, #4
9.		9.			COLLECTOR, #3		BASE, #4
10.			ANODE		BASE, #3		EMITTER, #4
	NO CONNECTION	11.			EMITTER, #3		BASE, #3
	EMITTER		CATHODE		COLLECTOR, #3		EMITTER, #3
	BASE		CATHODE		COLLECTOR, #4		BASE, #2
	COLLECTOR	14.			BASE, #4		EMITTER, #2
15.			ANODE		EMITTER, #4		BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1
STYLE 5:		STYLE 6:		STYLE 7:			
STYLE 5: PIN 1.	DRAIN, DYE #1	STYLE 6: PIN 1.	CATHODE	STYLE 7: PIN 1.	SOURCE N-CH		
	DRAIN, DYE #1 DRAIN, #1			PIN 1.	SOURCE N-CH COMMON DRAIN (OUTPUT)		
PIN 1.	,	PIN 1.	CATHODE	PIN 1.	COMMON DRAIN (OUTPUT)		
PIN 1. 2.	DRAIN, #1	PIN 1. 2.	CATHODE CATHODE	PIN 1. 2.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3.	DRAIN, #1 DRAIN, #2	PIN 1. 2. 3.	CATHODE CATHODE	PIN 1. 2. 3.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4.	DRAIN, #1 DRAIN, #2 DRAIN, #2	PIN 1. 2. 3. 4.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4	PIN 1. 2. 3. 4. 5.	CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3	PIN 1. 2. 3. 4. 5. 6.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE	PIN 1. 2. 3. 4. 5. 6.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4	PIN 1. 2. 3. 4. 5. 6. 7.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 SOURCE, #4	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE ANODE ANODE ANODE ANODE ANODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GOMMON DRAIN (OUTPUT) GATE N-CH		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 DRAIN, #4 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2 SOURCE, #2 SOURCE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) CATE N-CH COMMON DRAIN (OUTPUT)		
PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	DRAIN, #1 DRAIN, #2 DRAIN, #2 DRAIN, #3 DRAIN, #3 DRAIN, #4 GATE, #4 SOURCE, #4 GATE, #3 SOURCE, #3 GATE, #2	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12. 13.	CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE CATHODE ANODE	PIN 1. 2. 3. 4. 5. 6. 7. 8. 9. 10. 11. 12.	COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) SOURCE P-CH SOURCE P-CH COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) COMMON DRAIN (OUTPUT) GATE N-CH COMMON DRAIN (OUTPUT)		

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Reposit Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC-16 9.90X3.90X1.50 1	.27P	PAGE 2 OF 2

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, ONSEMI., and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries. onsemi owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of onsemi's product/patent coverage may be accessed at <a href="www.onsemi.com/site/pdf/Patent-Marking.pdf">www.onsemi.com/site/pdf/Patent-Marking.pdf</a>. onsemi reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and onsemi makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems. or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

# ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

 $\textbf{Technical Library:} \ \underline{www.onsemi.com/design/resources/technical-documentation}$ 

onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at

www.onsemi.com/support/sales