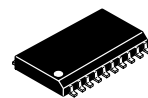


# Inverting Octal 3-STATE Buffer

## MM74HC240



SOIC-20 WB  
CASE 751D-05



TSSOP-20 WB  
CASE 948E

### General Description

The MM74HC240 3-STATE buffer utilizes advanced silicon-gate CMOS technology. It possesses high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. It has a fanout of 15 LS-TTL equivalent inputs.

The MM74HC240 is an inverting buffer and has two active LOW enables ( $1\bar{G}$  and  $2\bar{G}$ ). Each enable independently controls 4 buffers.

All inputs are protected from damage due to static discharge by diodes to  $V_{CC}$  and ground.

### Features

- Typical Propagation Delay: 12 ns
- 3-STATE Outputs for Connection to System Buses
- Wide Power Supply Range: 2-6 V
- Low Quiescent Supply Current: 160  $\mu$ A (74 Series)
- Output Current: 6 mA
- These are Pb-Free Devices

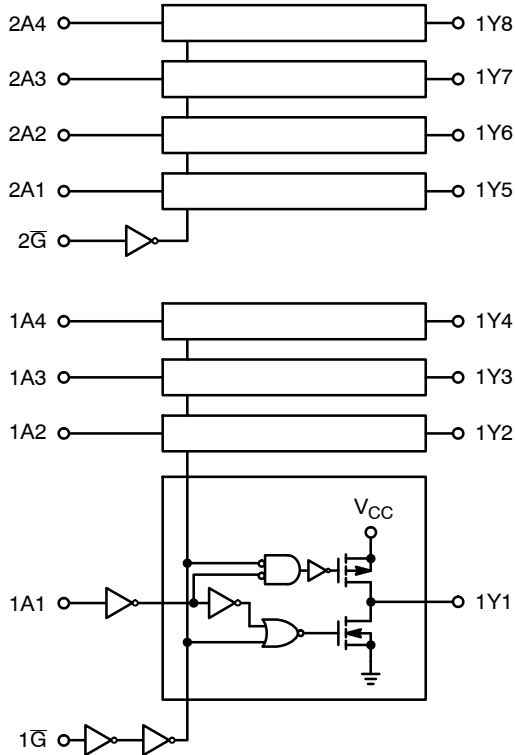
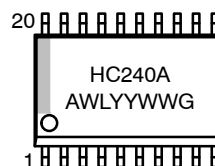
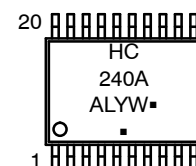


Figure 1. Logic Diagram

### MARKING DIAGRAMS



(SOIC-20 WB)

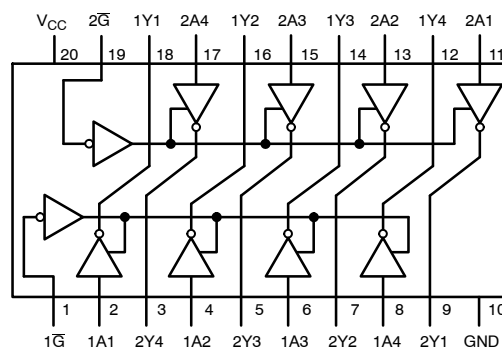


(TSSOP-20 WB)

- HC240A = Specific Device Code
- A = Assembly Location
- L/WL = Wafer Lot
- Y/YY = Year
- W/WW = Work Week
- or G = Pb-Free Package

(Note: Microdot may be in either location)

### CONNECTION DIAGRAM



(Top View)

### TRUTH TABLE

$1\bar{G}$	1A	1Y	$2\bar{G}$	2A	2Y
L	L	H	L	L	H
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = HIGH Level  
L = LOW Level  
Z = HIGH Impedance

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

# MM74HC240

## MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply Voltage	-0.5 to +7.0	V
V <sub>IN</sub>	DC Input Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
V <sub>OUT</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub> , I <sub>OK</sub>	Clamp Diode Current	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±35	mA
I <sub>CC</sub>	DC VCC or GND Current, per Pin	±70	mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
P <sub>D</sub>	Power Dissipation (Note 2) S. O. Package Only	600 500	mW
T <sub>L</sub>	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.
2. Power Dissipation temperature derating – plastic “N” package: 12 mW/°C from 65°C to 85°C.

## RECOMMENDED OPERATING CONDITIONS (Note 1)

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	Supply Voltage	2	6	V
V <sub>IN</sub> , V <sub>OUT</sub>	DC Input or Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature Range	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Times V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	-	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS (Note 3)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		-40°C ≤ T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit	
				Typ	Guaranteed Limits						
V <sub>IH</sub>	Minimum HIGH Level Input Voltage		2.0	-	1.5	1.5	1.5		V		
			4.5	-	3.15	3.15	3.15				
			6.0	-	4.2	4.2	4.2				
V <sub>IL</sub>	Maximum LOW Level Input Voltage		2.0	-	0.5	0.5	0.5		V		
			4.5	-	1.35	1.35	1.35				
			6.0	-	1.8	1.8	1.8				
V <sub>OH</sub>	Minimum HIGH Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	2.0	1.9	1.9	1.9		V		
			4.5	4.5	4.4	4.4	4.4				
			6.0	6.0	5.9	5.9	5.9				
		V <sub>IL</sub>	Maximum LOW Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 6.0 mA  I <sub>OUT</sub>   ≤ 7.8 mA	4.5	4.2	3.98	3.84	3.7		V
					6.0	5.7	5.48	5.34	5.2		
					6.0	5.7	5.48	5.34	5.2		
V <sub>OL</sub>	Maximum LOW Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>OUT</sub>   ≤ 20 μA	2.0	0	0.1	0.1	0.1		V		
			4.5	0	0.1	0.1	0.1				
			6.0	0	0.1	0.1	0.1				
		I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	4.5	0.2	0.26	0.33	0.4		V
					6.0	0.2	0.26	0.33	0.4		
					6.0	-	±0.1	±1.0	±1.0		
			6.0	-	±0.1	±1.0	±1.0		μA		

# MM74HC240

## DC ELECTRICAL CHARACTERISTICS (Note 3) (continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		-40°C ≤ T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Typ	Guaranteed Limits					
I <sub>OZ</sub>	Maximum 3-STATE Output Leakage Current	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = V <sub>CC</sub> or GND G = V <sub>IH</sub> , G = V <sub>IL</sub>	6.0	-	±0.5	±5	±10			μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA	6.0	-	8.0	80	160			μA

3. For a power supply of 5 V ±10% the worst case output voltages (V<sub>OH</sub>, and V<sub>OL</sub>) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V<sub>IH</sub> and V<sub>IL</sub> occur at V<sub>CC</sub> = 5.5 V and 4.5 V respectively. (The V<sub>IH</sub> value at 5.5 V is 3.85 V.) The worst case leakage current (I<sub>IN</sub>, I<sub>CC</sub>, and I<sub>OZ</sub>) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay	C <sub>L</sub> = 45 pF	12	18	ns
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Enable Delay to Active Output	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 45 pF	14	28	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Disable Delay from Active Output	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 5 pF	13	25	ns

## AC ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 2.0 V to 6.0 V, C<sub>L</sub> = 50 pF, t<sub>r</sub> = t<sub>f</sub> = 6 ns (unless otherwise specified))

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		-40°C ≤ T <sub>A</sub> ≤ 85°C		-55°C ≤ T <sub>A</sub> ≤ 125°C		Unit
				Typ	Guaranteed Limits					
t <sub>PHL</sub> , t <sub>PLH</sub>	Maximum Propagation Delay	C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	2.0	55	100	126	149	ns		
			4.5	12	20	25	30	ns		
			6.0	11	17	21	25	ns		
t <sub>PZH</sub> , t <sub>PZL</sub>	Maximum Output Enable Time	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF C <sub>L</sub> = 150 pF	2.0	75	150	189	224	ns		
			4.5	15	30	38	45	ns		
			6.0	13	26	32	38	ns		
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Maximum Output Disable Time	R <sub>L</sub> = 1 kΩ C <sub>L</sub> = 50 pF	2.0	75	150	189	224	ns		
			4.5	15	30	38	45	ns		
			6.0	13	26	32	38	ns		
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Rise and Fall Time		2.0	-	60	75	90	ns		
			4.5	-	12	15	18	ns		
			6.0	-	10	13	15	ns		
C <sub>PD</sub>	Power Dissipation Capacitance (Note 4)	(per buffer) G = V <sub>IH</sub> G = V <sub>IL</sub>	-	12	-	-	-	pF		
C <sub>IN</sub>	Maximum Input Capacitance		-	5	10	10	10	pF		
C <sub>OUT</sub>	Maximum Output Capacitance		-	10	20	20	20	pF		

4. C<sub>PD</sub> determines the no load power consumption, P<sub>D</sub> = C<sub>PD</sub> · V<sub>CC</sub><sup>2</sup> · f + I<sub>CC</sub> · V<sub>CC</sub>, and the no load dynamic current consumption, I<sub>S</sub> = C<sub>PD</sub> · V<sub>CC</sub> · f + I<sub>CC</sub>.

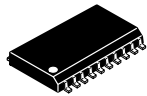
# MM74HC240

## ORDERING INFORMATION

Device	Package	Shipping†
MM74HC240WM	SOIC-20 WB (Pb-Free)	38 Units / Tube
MM74HC240WMX	SOIC-20 WB (Pb-Free)	1000 Units / Tape & Reel
MM74HC240MTCX	TSSOP-20 WB (Pb-Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-20 WB  
CASE 751D-05  
ISSUE H

DATE 22 APR 2015



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

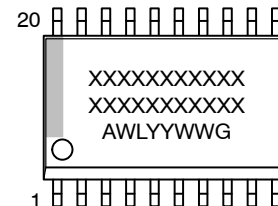
RECOMMENDED  
SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC  
MARKING DIAGRAM\*



- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

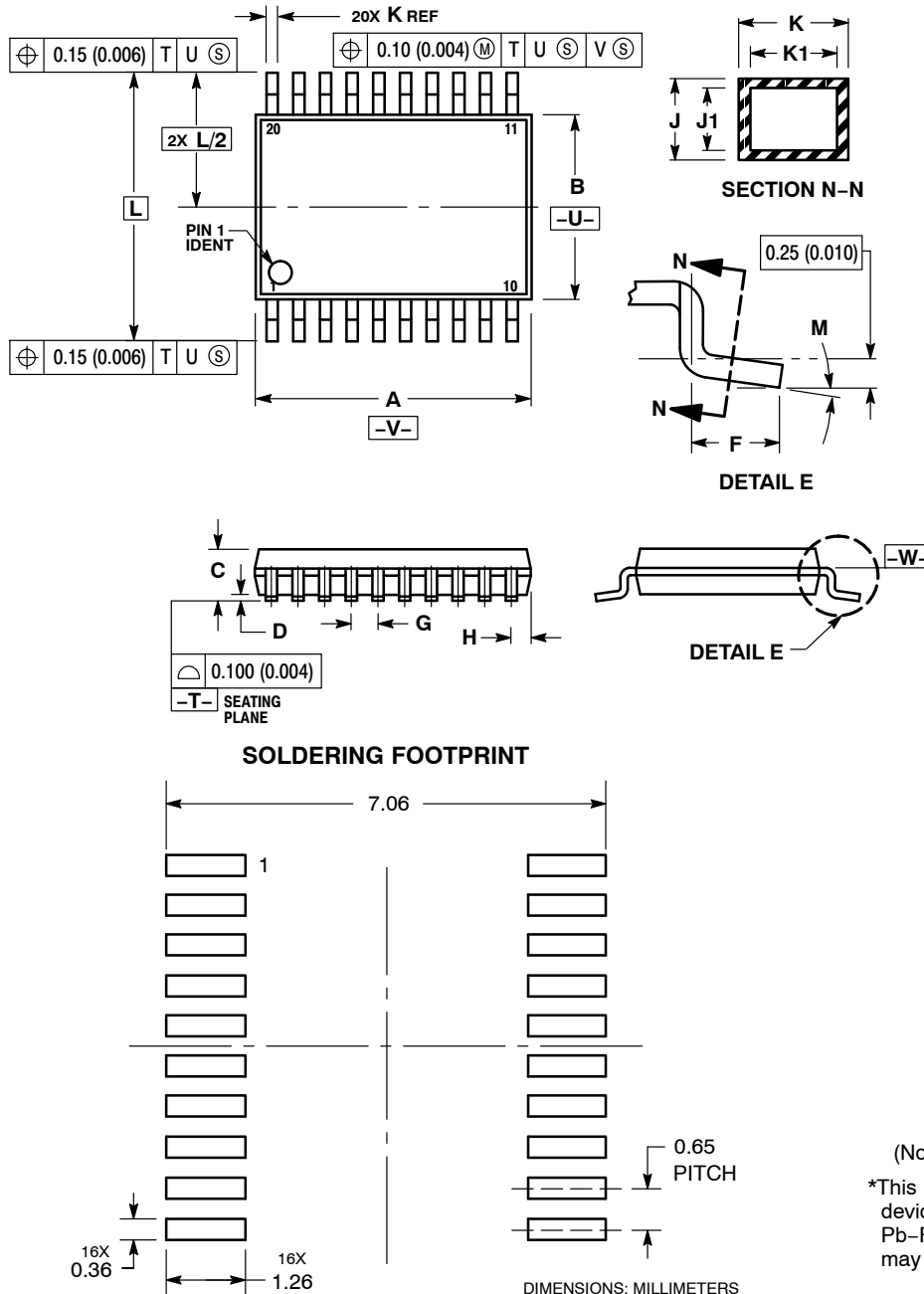
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TSSOP-20 WB  
CASE 948E  
ISSUE D

DATE 17 FEB 2016

SCALE 2:1

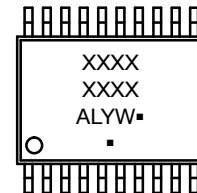


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**GENERIC MARKING DIAGRAM\***



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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