

MC74LCX16244

Low-Voltage CMOS 16-Bit Buffer

With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16244 is a high performance, non-inverting 16-bit buffer operating from a 2.3 to 3.6 V supply. The device is nibble controlled. Each nibble has separate Output Enable inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX16244 inputs to be safely driven from 5.0 V devices. The MC74LCX16244 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

The 4.5 ns maximum propagation delays support high performance applications. Current drive capability is 24 mA at the outputs. The Output Enable (\overline{OEn}) inputs, when HIGH, disable the outputs by placing them in a HIGH Z condition.

The MC74LCX16244 contains sixteen non-inverting buffers with 3-state 5.0 V-tolerant outputs. The device is nibble controlled with each nibble functioning identically, but independently. The control pins may be tied together to obtain full 16-bit operation. The 3-state outputs are controlled by an Output Enable (\overline{OEn}) input for each nibble. When \overline{OEn} is LOW, the outputs are on. When \overline{OEn} is HIGH, the outputs are in the high impedance state.

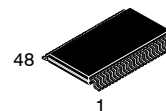
Features

- Designed for 2.3 V to 3.6 V V_{CC} Operation
- 4.5 ns Maximum t_{pd}
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 μ A)
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine Model >200 V
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



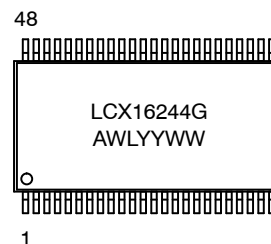
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TSSOP-48
DT SUFFIX
CASE 1201

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

MC74LCX16244

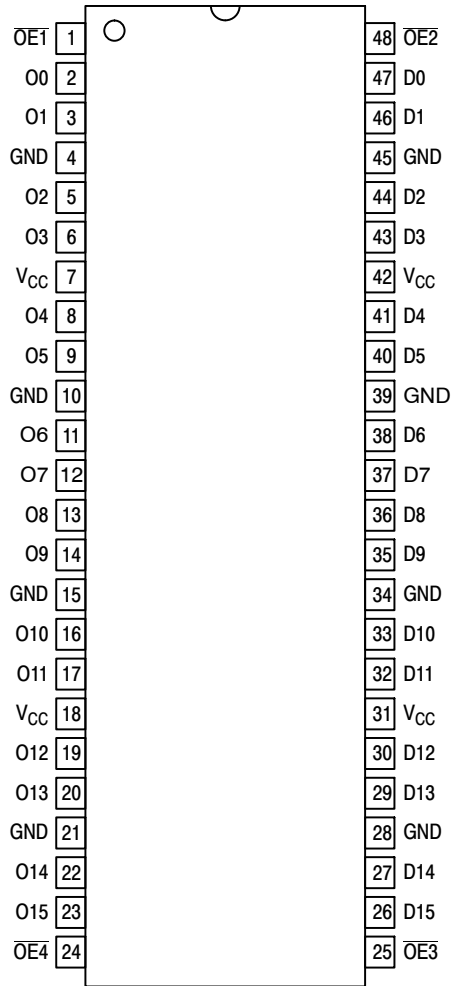


Figure 1. Pinout: 48-Lead (Top View)

Table 1. PIN NAMES

Pins	Function
$\overline{OE}n$	Output Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

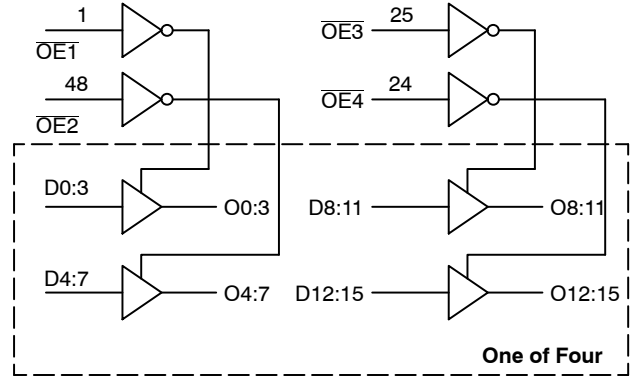


Figure 2. Logic Diagram

TRUTH TABLE

$\overline{OE}1$	D0:3	O0:3	$\overline{OE}2$	D4:7	O4:7	$\overline{OE}3$	D8:11	O8:11	$\overline{OE}4$	D12:15	O12:15
L	L	L	L	L	L	L	L	L	L	L	L
L	H	H	L	H	H	L	H	H	L	H	H
H	X	Z	H	X	Z	H	X	Z	H	X	Z

H = High Voltage Level

L = Low Voltage Level

Z = High Impedance State

X = High or Low Voltage Level and Transitions Are Acceptable; for I_{CC} reasons, DO NOT FLOAT Inputs.

MC74LCX16244

ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX16244DTG	TSSOP-48 (Pb-Free)	39 Units / Rail
M74LCX16244DTR2G	TSSOP-48 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V_{CC}	DC Supply Voltage	-0.5 to +7.0		V
V_I	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
V_O	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State (Note 1)	V
I_{IK}	DC Input Diode Current	-50	$V_I < GND$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
I_O	DC Output Source/Sink Current	± 50		mA
I_{CC}	DC Supply Current Per Supply Pin	± 100		mA
I_{GND}	DC Ground Current Per Ground Pin	± 100		mA
T_{STG}	Storage Temperature Range	-65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage Operating Data Retention Only	2.0	2.5, 3.3	3.6	V
		1.5	2.5, 3.3	3.6	
V_I	Input Voltage	0		5.5	V
V_O	Output Voltage (HIGH or LOW State) (3-State)	0		V_{CC}	V
		0		5.5	
I_{OH}	HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			-24	mA
				-12	
				-8	
I_{OL}	LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			+24	mA
				+12	
				+8	
T_A	Operating Free-Air Temperature	-40		+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, V_{IN} from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$	0		10	ns/V

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DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units
			Min	Max	
V_{IH}	HIGH Level Input Voltage (Note 2)	$2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	1.7		V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	2.0		
V_{IL}	LOW Level Input Voltage (Note 2)	$2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$		0.7	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$		0.8	
V_{OH}	HIGH Level Output Voltage	$2.3\text{ V} \leq V_{CC} \leq 3.6\text{ V}; I_{OL} = 100\ \mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.3\text{ V}; I_{OH} = -8\text{ mA}$	1.8		
		$V_{CC} = 2.7\text{ V}; I_{OH} = -12\text{ mA}$	2.2		
		$V_{CC} = 3.0\text{ V}; I_{OH} = -18\text{ mA}$	2.4		
		$V_{CC} = 3.0\text{ V}; I_{OH} = -24\text{ mA}$	2.2		
V_{OL}	LOW Level Output Voltage	$2.3\text{ V} \leq V_{CC} \leq 3.6\text{ V}; I_{OL} = 100\ \mu\text{A}$		0.2	V
		$V_{CC} = 2.3\text{ V}; I_{OL} = 8\text{ mA}$		0.6	
		$V_{CC} = 2.7\text{ V}; I_{OL} = 12\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 16\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 24\text{ mA}$		0.55	
I_{OZ}	3-State Output Current	$V_{CC} = 3.6\text{ V}, V_{IN} = V_{IH}\text{ or } V_{IL}, V_{OUT} = 0\text{ to } 5.5\text{ V}$		± 5	μA
I_{OFF}	Power Off Leakage Current	$V_{CC} = 0, V_{IN} = 5.5\text{ V or } V_{OUT} = 5.5\text{ V}$		10	μA
I_{IN}	Input Leakage Current	$V_{CC} = 3.6\text{ V}, V_{IN} = 5.5\text{ V or GND}$		± 5	μA
I_{CC}	Quiescent Supply Current	$V_{CC} = 3.6\text{ V}, V_{IN} = 5.5\text{ V or GND}$		10	μA
ΔI_{CC}	Increase in I_{CC} per Input	$2.3 \leq V_{CC} \leq 3.6\text{ V}; V_{IH} = V_{CC} - 0.6\text{ V}$		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS ($t_R = t_F = 2.5\text{ ns}; R_L = 500\ \Omega$)

Symbol	Parameter	Waveform	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						Units
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $C_L = 50\text{ pF}$		$V_{CC} = 2.7\text{ V}$ $C_L = 50\text{ pF}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ $C_L = 30\text{ pF}$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Input to Output	1	1.5 1.5	4.5 4.5	1.5 1.5	5.2 5.2	1.5 1.5	5.4 5.4	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	1.5 1.5	5.5 5.5	1.5 1.5	6.3 6.3	1.5 1.5	7.2 7.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	1.5 1.5	5.4 5.4	1.5 1.5	5.7 5.7	1.5 1.5	6.5 6.5	ns
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

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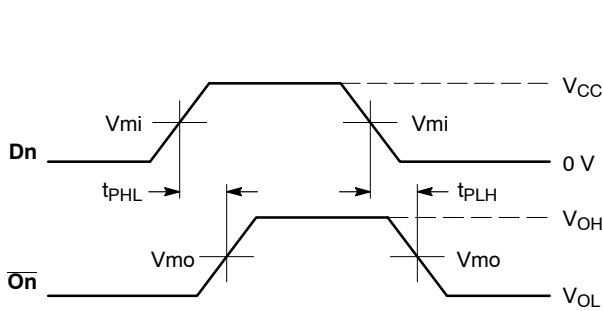
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = +25°C			Units
			Min	Typ	Max	
V _{OLP}	Dynamic LOW Peak Voltage (Note 4)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		0.8 0.6		V
V _{OLV}	Dynamic LOW Valley Voltage (Note 4)	V _{CC} = 3.3 V, C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V V _{CC} = 2.5 V, C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V		-0.8 -0.6		V

4. Number of outputs defined as “n”. Measured with “n-1” outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

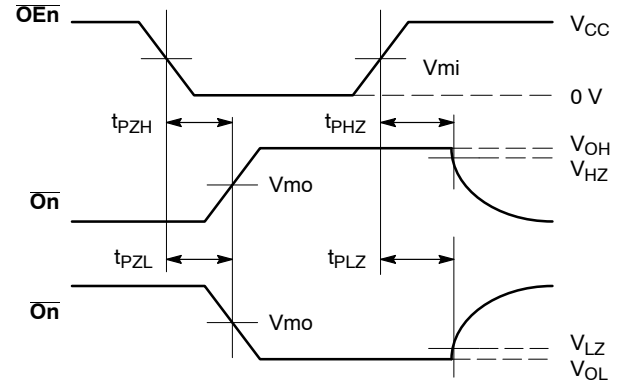
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	10 MHz, V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	20	pF



WAVEFORM 1 – PROPAGATION DELAYS

t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES

t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns

Figure 3. AC Waveforms

Table 2. AC WAVEFORMS

Symbol	V _{CC}		
	3.3 V ± 0.3 V	2.7 V	2.5 V ± 0.2 V
V _{mi}	1.5 V	1.5 V	V _{CC} / 2
V _{mo}	1.5 V	1.5 V	V _{CC} / 2
V _{HZ}	V _{OL} + 0.3 V	V _{OL} + 0.3 V	V _{OL} + 0.15 V
V _{LZ}	V _{OH} - 0.3 V	V _{OH} - 0.3 V	V _{OH} - 0.15 V

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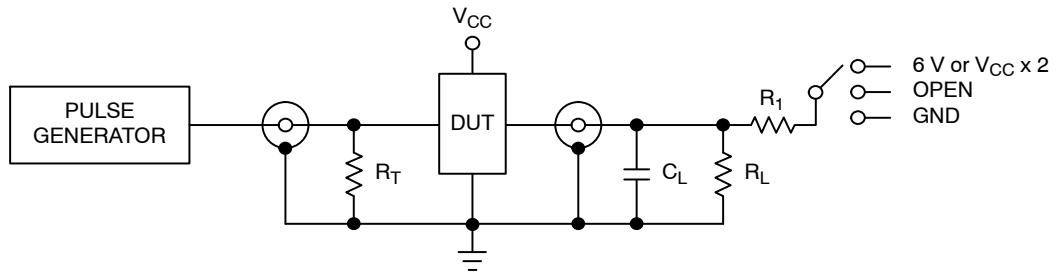


Figure 4. Test Circuit

Table 3. TEST CIRCUIT

Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	6 V at $V_{CC} = 3.3 \pm 0.3$ V 6 V at $V_{CC} = 2.5 \pm 0.2$ V
Open Collector/Drain t_{PLH} and t_{PHL}	6 V
t_{PZH} , t_{PHZ}	GND

$C_L = 50$ pF at $V_{CC} = 3.3 \pm 0.3$ V or equivalent (includes jig and probe capacitance)

$C_L = 30$ pF at $V_{CC} = 2.5 \pm 0.2$ V or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 500 \Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

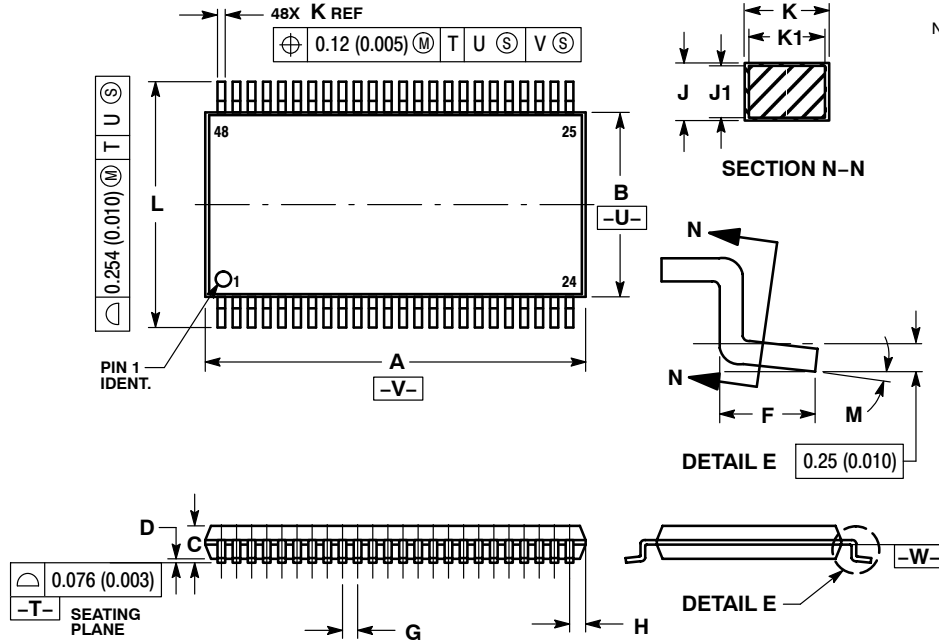
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1
SCALE 1:1

TSSOP-48
CASE 1201-01
ISSUE B

DATE 06 JUL 2010

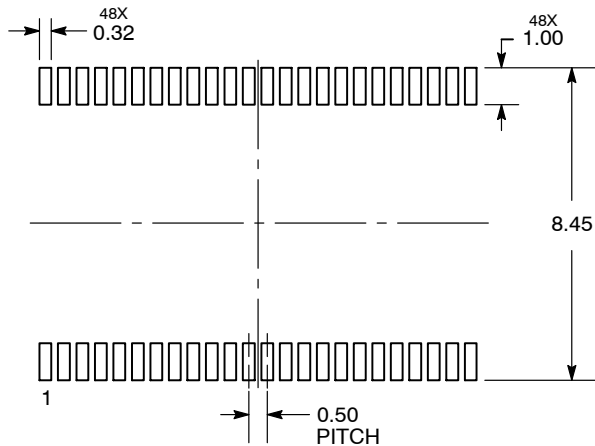


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0°	8°	0°	8°

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- XXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- YY = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

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