TAS2780 Digital Input Mono Class-D Audio Amplifier With Speaker IV Sense

1 Features

Key Features
- 24-V Supply for Class-D Output Stage
- Y-Bridge Multi-Level Supply Architecture
- Spread Spectrum Control
- Ultrasonic Output Support up to 40 kHz

Output Power:
- 25 W, 1% THD+N (4 Ω, 18 V)
- 30 W Maximum Output Power, 10 % THD+N

Efficiency (1% THDN) and Power Consumption
- 83% at 1W, 4 Ω, PVDD = 12 V, VBAT1S = 3.8 V
- 83% at 1W, 8 Ω, PVDD = 18 V, VBAT1S = 5 V
- 85% at 1W, 4 Ω, PVDD = 18 V, VBAT1S = 5 V
- 89% at 15W, 4 Ω, PVDD = 18 V, VBAT1S = 5 V
- 93% at 15W , 8 Ω, PVDD = 18 V, VBAT1S = 5 V
- <0.5 µA in Hardware Shutdown Mode

Power Supplies and Management:
- PVDD: 3 V to 24 V
- VBAT1S: 2.7 V to 5.5 V
- AVDD: 1.8 V
- IOVDD: 1.8 V/ 3.3 V

Interfaces and Control:
- SDOUT for Echo Cancellation
- I^2S/TDM: 8 Channels of 32 bits up to 96 KSPS
- I^2C: Selectable Addresses with Fast Mode+
- Inter-Chip Communication Bus
- 44.1 kHz to 96 kHz Sample Rates

Integrated Speaker Management, Protection and EMI:
- Real-time IV-Sense for Speaker Protection
- Short and Open Load Protection
- Thermal and Over Current Protection
- Brownout Protection with Power Limiter
- Over Power and Low Battery Protection
- PVDD and VBAT1S Supply Tracking Limiters
- Thermal Foldback
- Post Filter Feedback
- Output Slew Rate Control

2 Applications

- Laptop and Desktop Computers
- Smart Speakers
- Tablets and Handhelds
- Wireless Speakers

3 Description

The TAS2780 is a mono, digital input Class-D audio amplifier optimized for efficiently driving high peak power into loudspeakers. The Class-D amplifier is capable of delivering 25 W of continuous power into a 4 Ω load with less than 1% THD+N at a supply voltage of 18 V. The broad voltage input range and the high output power makes this amplifier versatile enough to work with battery or line powered systems.

The TAS2780 can be used as a conventional amp or with host-based speaker protection algorithms. The integrated speaker voltage and current sense provides for real time feedback of loudspeaker conditions to the protection algorithms through a return I^2S path.

Y-Bridge power architecture improves amplifier efficiency by internally selecting the supplies for optimal headroom. Brownout prevention scheme with multiple thresholds allows reducing the gain in signal path when the supply drops.

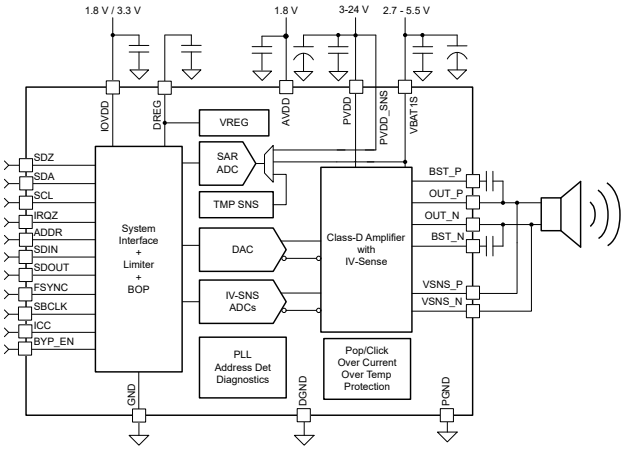
Up to eight TAS2780 devices can share a common bus via I^2S/TDM and I^2C/SPI interfaces.

The TAS2780 is available in a 30 pin HR-QFN package for a compact PCB footprint.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS2780	HR QFN	4 mm x 3.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2022) to Revision B (March 2023)	Page
• Updated PVDD to 24 V with -20° C temp condition footnote in *Absolute Maximum Ratings* and *Recommended Operating Conditions.*	4
• Clarifications to edge rate register description	72
• PFFB ffeature recommendation for ferrite bead filters	81
• Startup configuration script added to fix power-up pop issue	84

Changes from Revision * (February 2022) to Revision A (June 2022)	Page
• Change device status from "Advanced Information" to "Production Data."	1

5 Pin Configuration and Functions

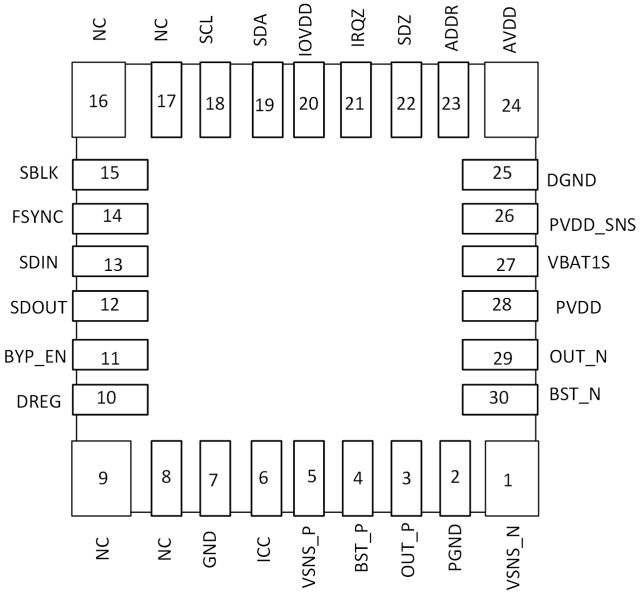


Figure 5-1. 30-Pin HR-QFN Package - Bottom View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
ADDR	23	I	Address detect pin. Resistor value at this pin selects the I^{2}C address. See Section 8.3.1.
AVDD	24	P	Analog power input. Connect to 1.8-V supply and decouple to GND with a capacitor.
BST_N	30	P	Class-D negative bootstrap. Connect a capacitor between BST_N and OUT_N.
BST_P	4	P	Class-D positive bootstrap. Connect a capacitor between BST_P and OUT_P.
BYP_EN	11	O	Low voltage signaling pin with open drain output. It can be used to enable/disable an external DC-DC converter.
DGND	25	P	Device substrate ground. Connect to PCB ground plane. Avoid any common routing inductance between this pin and GND pin.
DREG	10	P	Digital core voltage regulator output. Bypass to GND with a capacitor. Do not connect to external load.
FSYNC	14	I	Frame Synchronization Clock.
GND	7	P	Analog ground. Connect to PCB ground plane.
ICC	6	IO	Inter-chip communication pin.
IOVDD	20	P	Digital IO power supply. Connect to an 1.8-V or a 3.3-V supply and decouple with a capacitor to GND.
IRQZ	21	O	Open drain, active low, interrupt pin. Pull up to IOVDD with resistor if optional internal pull up is not used.
NC	8, 9, 16, 17		Not Connected.
OUT_N	29	O	Class-D negative output.
OUT_P	3	O	Class-D positive output.
PGND	2	P	Class-D ground. Connect to PCB ground plane.
PVDD	28	P	Class-D power supply input. Decouple with a capacitor.
PVDD_SNS	26	I	PVDD remote sense pin.
SBCLK	15	I	Serial Bit Clock.
SCL	18	I	I^{2}C Clock Pin. Pull up to IOVDD with a resistor.
SDA	19	IO	I^{2}C Data Pin. Pull up to IOVDD with a resistor.

Table 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SDIN	13	I	Serial Data Input.
SDOUT	12	IO	Serial Data Output.
SDZ	22	I	Active low hardware shutdown.
VBAT1S	27	P	Single-cell battery supply input. Decouple with a capacitor.
VSNS_N	1	I	Voltage Sense negative input. Connect to Class-D negative output or after an LC filter.
VSNS_P	5	I	Voltage Sense positive input. Connect to Class-D positive output or after an LC filter.

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Supply Voltage	AVDD	-0.3	2	V
	IOVDD	-0.3	5	V
	PVDD	-0.3	26	V
	VBAT1S	-0.3	6	V
	PVDD - VBAT1S	-0.3	22	V
Internal Supply Voltage	DREG	-0.3	1.5	V
IO Voltage(1)	Digital IOs referenced to IOVDD supply	-0.3	5	V
Operating free-air temperature, T_A ; Device is functional and reliable, some performance characteristics may be degraded.	PVDD is 23 V or below	-40	85	°C
	PVDD higher than 23 V	-20	85	°C
Performance free-air temperature, T_P ; All performance characteristics are met.		-20	70	°C
Operating junction temperature, T_J	PVDD is 23 V or below	-40	150	°C
	PVDD higher than 23 V	-20	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) All digital inputs and IOs are failsafe.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
AVDD	Supply voltage	1.65	1.8	1.95	V
IOVDD	Supply voltage	3	3.3	3.6	V
		1.65	1.8	1.95	

			MIN	TYP	MAX	UNIT
PVDD	Supply voltage (functional)(1)	Min operating free-air and Min operating junction temperature of -20°C	3		24	V
		Min operating free-air and Min operating junction temperature of -40°C	3		23	
	Supply voltage (performance)	Min operating free-air and Min operating junction temperature of -20°C	4.5		24	
		Min operating free-air and Min operating junction temperature of -40°C	4.5		23	
VBAT1S	Supply voltage (functional)(1)		2.7		5.5	V
	Supply voltage (performance)		3.4		5.5	
R_{SPK}	Speaker impedance		3.2			Ω
L_{SPK}	Speaker inductance		5			µH

(1) Device will remain functional but performance will degrade.

6.4 Thermal Information

THERMAL METRIC(1)		HR_QFN 30 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25 °C, PVDD = 18 V, VBAT1S = 3.8 V, AVDD = 1.8V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1(2), measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT and OUTPUT						
V_{IH}	High-level digital input logic voltage threshold	All digital pins	0.7×IOVDD			V
V_{IL}	Low-level digital input logic voltage threshold	All digital pins			0.3 × IOVDD	V
V_{OH}	High-level digital output voltage	All digital pins except SDA, SCL, IRQZ, BYP_EN; I_{OH} = 100 µA.	IOVDD–0.2V			V
V_{OL}	Low-level digital output voltage	All digital pins except SDA, SCL,IRQZ, BY_EN; I_{OL} = –100 µA.			0.2	V
$V_{OL(I2C)}$	Low-level digital output voltage	SDA and SCL; I_{OL} = -1 mA.			0.2 x IOVDD	V
$V_{OL(IRQZ)}$	Low-level digital output voltage for IRQZ and BY_EN open drain outputs	IRQZ, BY_EN; I_{OL} = -1 mA.			0.2	V
I_{IH}	Input logic-high leakage for digital inputs	All digital pins; Input = Supply Rail.	–1		1	µA
I_{IL}	Input logic-low leakage for digital inputs	All digital pins; Input = GND.	–1		1	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pull down resistance for IO pins when asserted on			18		kΩ
R_{OS}	OUT to VSNS resistors	Load disconnected		10		kΩ
IO	Output Current Strength	Measured at 0.4 V below supply and 0.4 V above GND.		8		mA

T_A = 25 °C, PVDD = 18 V, VBAT1S = 3.8 V, AVDD = 1.8V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1(2), measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AMPLIFIER PERFORMANCE						
P_{OUT}	Peak Output Power	THD+N = 10 %, VBAT1S = 5 V, PWR_MODE0(1), PWR_MODE1(2)		30		W
	Maximum Continuous Output Power	THD+N = 1 %, VBAT1S= 5 V, PWR_MODE0, PWR_MODE1		25		
	System Efficiency	P_{OUT} = 1 W, VBAT1S= 5 V, PWR_MODE1		85		%
		P_{OUT} = 1 W, VBAT1S= 5 V, PWR_MODE0		79		
		P_{OUT} = 3 W, VBAT1S= 5 V, PWR_MODE0 and PWR_MODE1		85		
		P_{OUT} = 8 W, VBAT1S = 5 V, PWR_MODE0 and PWR_MODE1		88		
THD+N	Total Harmonic Distortion and Noise	P_{OUT} = 1 W		-84		dB
		P_{OUT} = 1 W, f_{in} = 6.667 kHz		-84		
IMD	Inter-Modulation Distortion	ITU-R, 19 kHz / 20 kHz, 1: 1: 12.5 W		-83		dB
V_N	Idle Channel Noise	A-Weighted, 20 Hz - 20 kHz, PWR_MODE0		40		µV
		A-Weighted, 20 Hz - 20 kHz, PWR_MODE2 (3)		34		
		A-Weighted, 20 Hz - 20k Hz, PWR_MODE1		32		
	Idle Channel Noise with Ultrasonic Chirp (100 us duty cycle, 25 ms period)	A-Weighted, 20 Hz - 20 kHz, VBAT1S = 5 V, PWR_MODE3 (4), 1 V_{Peak}, Register 0x73 set to E0h		34		
F_{PWM}	Class-D PWM Switching Frequency	Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0		384		kHz
		Fixed Frequency Mode, CLASSD_SYNC=0		384		
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 44.1, 88.2 kHz		352.8		
		Fixed Frequency Mode, CLASSD_SYNC=1, f_s = 48, 96 kHz		384		
V_{OS}	Output Offset Voltage	Idle Mode	-1.3	±0.33	1.3	mV
DNR	Dynamic Range	A-Weighted, -60 dBFS		110		dB
		A-Weighted, -60 dBFS, PWR_MODE2		109		
		A-Weighted, -60 dBFS, PWR_MODE0		109		
SNR	Signal to Noise Ratio	A-Weighted, Referenced to 1 % THD+N Output Level		110		dB
		A-Weighted, Referenced to 1 % THD+N Output Level, PWR_MODE2		110		
		A-Weighted, Referenced to 1 % THD+N Output Level, PWR_MODE0		109		
K_{CP}	Click and Pop Performance	Idle mode, Into and out of Shutdown, A-weighted		0.8		mV
	Full Scale Output Voltage	f_s ≤ 48 kHz		21		dBV
	Minimum Programmable Gain	f_s ≤ 48 kHz		11		dBV
	Maximum Programmable Gain	f_s ≤ 48 kHz		21		
	Programmable Output Level Step Size			0.5		dB
	Mute attenuation	Device in Software Shutdown or Muted in Normal Operation		108		dB
	Chip to Chip Group Delay		-1		1	µs
	PVDD Power Supply Rejection Ratio	PVDD = 18 V + 200 mV_{pp}, f_{ripple} = 217 Hz		118		dB
		PVDD = 18 V + 200 mV_{pp}, f_{ripple} = 1 kHz		110		
		PVDD = 18 V + 200 mV_{pp}, f_{ripple} = 20 kHz		95		
	VBAT1S Power Supply Rejection Ratio	VBAT1S = 3.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		114		dB
		VBAT1S = 3.8 V + 200 mV_{pp}, f_{ripple} = 1 kHz		110		
		VBAT1S = 3.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		90		
	AVDD Power Supply Rejection Ratio	AVDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 217 Hz		105		dB
		AVDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 1 kHz		104		
		AVDD = 1.8 V + 200 mV_{pp}, f_{ripple} = 20 kHz		87		

T_A = 25 °C, PVDD = 18 V, VBAT1S = 3.8 V, AVDD = 1.8V, IOVDD =1.8 V, R_L = 4Ω + 15µH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1(2), measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power Supply Inter-modulation	PVDD, 217 Hz, 100-mVpp, Input f=1kHz @ 400 mW		-120		dB
		VBAT1S,217 Hz, 100-mVpp, Input f=1kHz @ 400 mW		-120		
		AVDD, 217 Hz, 100-mVpp, Input f = 1 kHz @ 400 mW		-80		
		IOVDD 217 Hz, 100-mVpp, Input f = 1 kHz @ 400 mW		-120		
	Turn ON Time from Release of SW Shutdown	No Volume Ramping		1.12		ms
		Volume Ramping		6.7		
	Turn OFF Time from Assertion of SW Shutdown to Amp Hi-Z	No Volume Ramping		0.56		ms
		Volume Ramping		6		
	Out of HW Shutdown to First I^2C command		1			ms
DIAGNOSTIC GENERATOR						
THD+N	Total Harmonic Distortion and Noise	Pout = 1 W		-82		dB
f_{err}	Frequency Error	Using internal oscillator: DG_CLK = 0		2		%
DIE TEMPERATURE SENSOR						
	Resolution			8		bits
	Minimum Temperature Measurement Range			-40		°C
	Maximum Temperature Measurement Range			150		°C
	Die Temperature Resolution			1		°C
	Die Temperature Accuracy		-5		5	°C
VOLTAGE MONITOR						
	Resolution			12		bits
	PVDD Measurement Range	Minimum Level		2		V
		Maximum Level		23		
	PVDD Resolution			22.5		mV
	PVDD Accuracy	2 V ≤ PVDDV ≤ 23 V		±60		mV
	VBAT1S Measurement Range	Minimum Level		2		V
		Maximum Level		6		
	VBAT1S Resolution			20		mV
	VBAT1S Accuracy	2.3 V ≤ VBAT1S ≤ 6 V		±20		mV
TDM SERIAL AUDIO PORT						
	Minimum PCM Sample Rates and FSYNC Input Frequency			44.1		kHz
	Maximum PCM Sample Rates and FSYNC Input Frequency			96		
	Minimum SBCLK Input Frequency	I^2S/TDM Operation		0.7056		MHz
	Maximum SBCLK Input Frequency	I^2S/TDM Operation		24.576		
	SBCLK Maximum Input Jitter	RMS Jitter below 40 kHz that can be tolerated without performance degradation			0.5	ns
		RMS Jitter above 40 kHz that can be tolerated without performance degradation			1	
	Minimum SBCLK Cycles per FSYNC in I^2S and TDM Modes	Other Values: 24, 32, 48, 64, 96, 125, 128, 192, 250, 256, 384, 500		16		Cycles
	Maximum SBCLK Cycles per FSYNC in I^2S and TDM Modes	Other Values: 24, 32, 48, 64, 96, 125, 128, 192, 250, 256, 384, 500		512		

T_A = 25 °C, PVDD = 18 V, VBAT1S = 3.8 V, AVDD = 1.8V, IOVDD =1.8 V, R_L = 4Ω + 15μH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1(2), measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PCM PLAYBACK CHARACTERISTICS f_s ≤ 48 kHz						
f_s	Minimum Sample Rate			44.1		kHz
	Maximum Sample Rate			48		
	Frequency for Passband Ripple			0.454		f_s
	Passband Ripple	20 Hz to LPF cutoff frequency	-0.15		0.15	dB
	Stop Band Attenuation	≥ 0.55 f_s		60		dB
		≥ 1 f_s		65		
	Group Delay (Including Noise Gate)	DC to 0.454 f_s, DC blocker disabled		19		1/f_s
PCM PLAYBACK CHARACTERISTICS f_s > 48 kHz						
fs	Minimum Sample Rates			88.2		kHz
	Maximum Sample Rate			96		
	Frequency for Passband Ripple	f_s = 96 kHz		0.437		f_s
	Passband 3db Frequency	f_s = 96 kHz		0.459		f_s
	Passband Ripple	DC to LPF cutoff frequency	-0.5		0.5	dB
	Stop Band Attenuation	≥ 0.56 f_s		60		dB
		≥ 1 f_s		65		
	Group Delay (Including Noise Gate)	DC to 0.375 f_s for 96 kHz, DC blocker disabled		35		1/f_s
SPEAKER CURRENT SENSE						
	Resolution			16		bits
DNR	Dynamic Range	Un-weighted, relative to 0 dBFS.		70		dB
THD+N	Total Harmonic Distortion and Noise	Pout = 15 W		-64		dB
	Full Scale Input Current	Measured at -6 dBFS. Re-scaled at 0 dBFS.		5		A
	Differential Mode Gain		0.98		1.02	
	Frequency Response	20 Hz - 20 kHz	-0.1		0.1	dB
	Group Delay			5		1/f_s
SPEAKER VOLTAGE SENSE						
	Resolution			16		bits
DNR	Dynamic Range	Un-Weighted, Relative 0 dBFS		75		dB
THD+N	Total Harmonic Distortion and Noise	Pout = 15 W		-71		dB
	Full Scale Input Voltage			16		V_{PK}
	Differential Mode Gain		0.98		1.02	
	Frequency Response	20 Hz - 20 kHz	-0.1		0.1	dB
	Group Delay			5		1/f_s
SPEAKER VOLTAGE/CURRENT SENSE RATIO						
	Gain Linearity	Pout ≥ 40 mW to 0.1% THD+N, using a 40 Hz -40 dBFS pilot tone, PWR_MODE0 and PWR_MODE1	-1		1	%
	Gain error over temperature	-20°C to 70°C, Pout = 1 W		±0.6		%
	Phase Error between V and I			300		ns
PROTECTION CIRCUITRY						
	Brownout Prevention Latency to First Attack	BOP_SRC=1		19		μs
	Thermal Shutdown Temperature			142		°C
	Thermal Shutdown Retry	OTE_RETRY=1		1.5		s

T_A = 25 °C, PVDD = 18 V, VBAT1S = 3.8 V, AVDD = 1.8V, IOVDD =1.8 V, R_L = 4Ω + 15μH, f_{in} = 1 kHz, f_s = 48 kHz, Gain = 21 dBV, SDZ = 1, NG_EN=0, EN_LLSR=0, PWR_MODE1(2), measured filter free as in Section 7 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output Over Current Limit on PVDD	Output to Output, Output to GND or Output to PVDD Short	5.5	6.6		A
	Output Over Current Limit on VBAT1S	Output to Output, Output to GND or Output to VBAT1S Short	2	2.6		A
	VBAT1S Undervoltage Lockout Threshold	UVLO is asserted		2		V
		UVLO is de-asserted		2.16		
	AVDD Undervoltage Lockout Threshold	UVLO is asserted		1.45		V
		UVLO is de-asserted		1.51		
	IOVDD Undervoltage Lockout Threshold	UVLO is asserted		1.13		V
		UVLO is de-asserted		1.25		
	VBAT1S Internal LDO Undervoltage Lockout Threshold	UVLO is asserted	4			V
TYPICAL CURRENT CONSUMPTION						
	Hardware Shutdown	SDZ = 0, PVDD		0.05		μA
		SDZ = 0, VBAT1S		0.01		
		SDZ = 0, AVDD		0.14		
		SDZ = 0, IOVDD		0.005		
	Software Shutdown	All Clocks Stopped, PVDD		0.05		μA
		All Clocks Stopped, VBAT1S		0.5		
		All Clocks Stopped, AVDD		10.2		
		All Clocks Stopped, IOVDD		0.55		
	Noise Gate Mode	f_s = 48 kHz, PVDD		0.012		mA
		f_s = 48 kHz, VBAT1S		0.13		
		f_s = 48 kHz, AVDD		3		
		f_s = 48 kHz, IOVDD		0.01		
	Idle Mode - PWR_MODE1	f_s = 48 kHz, PVDD		0.04		mA
		f_s = 48 kHz, VBAT1S		2.2		
		f_s = 48 kHz, AVDD, IV Sense = Enabled		9.2		
		f_s = 48 kHz, AVDD, IV Sense = Disabled		6.8		
		f_s = 48 kHz, IOVDD		0.02		
	Idle Mode - PWR_MODE2	f_s = 48 kHz, PVDD		3		mA
		f_s = 48 kHz, AVDD, IV Sense = Enabled		9.2		
		f_s = 48 kHz, AVDD, IV Sense = Disabled		6.8		
		f_s = 48 kHz, IOVDD		0.02		
	Idle Mode - PWR_MODE0	f_s = 48 kHz, PVDD		2.28		mA
		f_s = 48 kHz, VBAT1S		2.1		
		f_s = 48 kHz, AVDD, IV Sense = Enabled		9.2		
		f_s = 48 kHz, AVDD, IV Sense = Disabled		6.8		
		f_s = 48 kHz, IOVDD		0.02		

(1) **PWR_MODE0**: CDS_MODE=10, VBAT1S_MODE=0
(2) **PWR_MODE1**: CDS_MODE=00, VBAT1S_MODE=0
(3) **PWR_MODE2**: CDS_MODE=11, VBAT1S_MODE=1
(4) **PWR_MODE3**: CDS_MODE=01, VBAT1S_MODE=0

6.6 I²C Timing Requirements

T_A = 25 °C, AVDD = IOVDD = 1.8 V (unless otherwise noted)

		MIN	MAX	UNIT
Standard-Mode				
f_{SCL}	SCL clock frequency	0	100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4		µs
t_{LOW}	LOW period of the SCL clock	4.7		µs
t_{HIGH}	HIGH period of the SCL clock	4		µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7		µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices		3.45	µs
$t_{SU;DAT}$	Data set-up time	250		ns
t_r	SDA and SCL rise time		1000	ns
t_f	SDA and SCL fall time		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4		µs
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
C_b	Capacitive load for each bus line		400	pF
Fast-Mode				
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6		µs
t_{LOW}	LOW period of the SCL clock	1.3		µs
t_{HIGH}	HIGH period of the SCL clock	0.6		µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6		µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0	0.9	µs
$t_{SU;DAT}$	Data set-up time	100		ns
t_r	SDA and SCL rise time	20 + 0.1 × C_b[pF]	300	ns
t_f	SDA and SCL fall time	20 + 0.1 × C_b[pF]	300	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.6		µs
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
C_b	Capacitive load for each bus line (10pF to 400pF)		400	pF
Fast-Mode Plus				
f_{SCL}	SCL clock frequency		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26		µs
t_{LOW}	LOW period of the SCL clock	0.5		µs
t_{HIGH}	HIGH period of the SCL clock	0.26		µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26		µs
$t_{HD;DAT}$	Data hold time: For I²C bus devices	0		µs
$t_{SU;DAT}$	Data set-up time	50		ns
t_r	SDA and SCL Rise Time		120	ns
t_f	SDA and SCL Fall Time		120	ns
$t_{SU;STO}$	Set-up time for STOP condition	0.26		µs
t_{BUF}	Bus free time between a STOP and START condition	0.5		µs
C_b	Capacitive load for each bus line		550	pF

6.7 TDM Port Timing Requirements

T_A = 25 °C, AVDD = IOVDD = 1.8 V, 20 pF load on all outputs(unless otherwise noted)

		MIN	MAX	UNIT
t_H(SBCLK)	SBCLK high period	20		ns
t_L(SBCLK)	SBCLK low period	20		ns

T_A = 25 °C, AVDD = IOVDD = 1.8 V, 20 pF load on all outputs(unless otherwise noted)

			MIN	MAX	UNIT
t_{SU}(FSYNC)	FSYNC setup time		8		ns
t_{HLD}(FSYNC)	FSYNC hold time		8		ns
t_{SU}(SDIN/ICC)	SDIN/ICC setup time		8		ns
t_{HLD}(SDIN/ICC)	SDIN/ICC hold time		8		ns
t_d(SBCLK_SDOUT/ICC)	SBCLK to SDOUT/ICC delay	50% of SBCLK to 50% of SDOUT/ICC, IOVDD = 1.8 V		30	ns
t_r(SBCLK)	SBCLK rise time	10 % - 90 % Rise Time		8	ns
t_f(SBCLK)	SBCLK fall time	90 % - 10 % Fall Time		8	ns

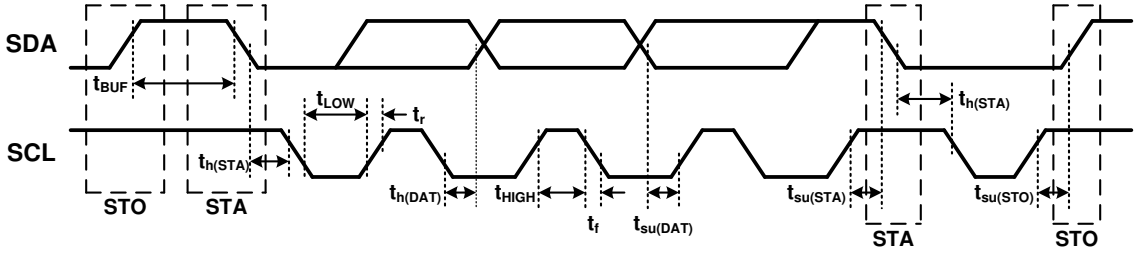


Figure 6-1. I²C Timing Diagram

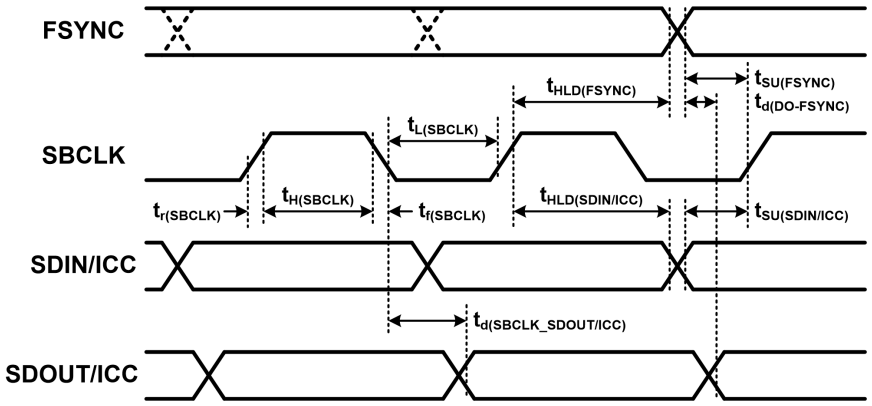
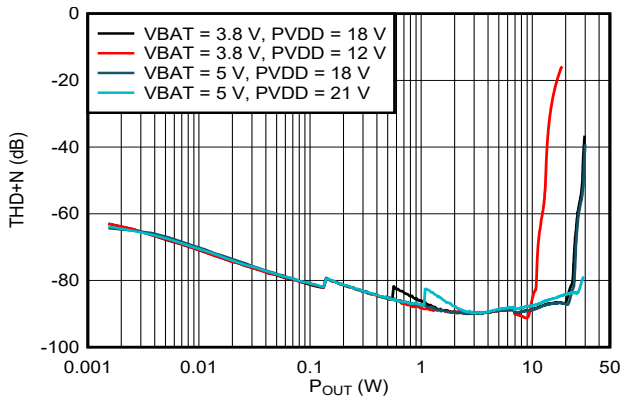


Figure 6-2. TDM and ICC Timing Diagram

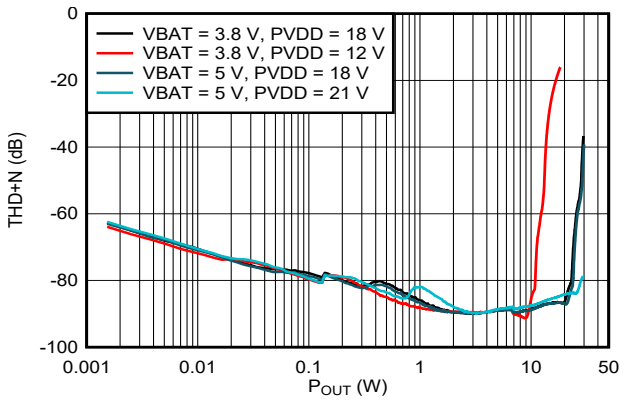
6.8 Typical Characteristics

At T_A = 25 ^{0}C, f_s = 48 kHz, Class-D Switching Frequency = 384 kHz, input signal f_{IN} = 1kHz - Sine, Load = 4Ω +15 µH, unless otherwise noted.



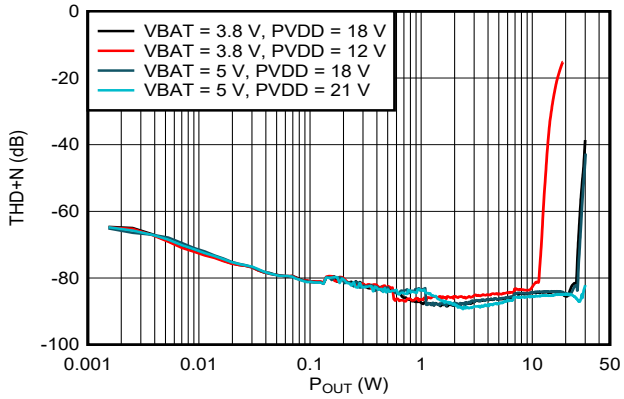
PWR_MODE1

Figure 6-3. THD+N vs Output Power



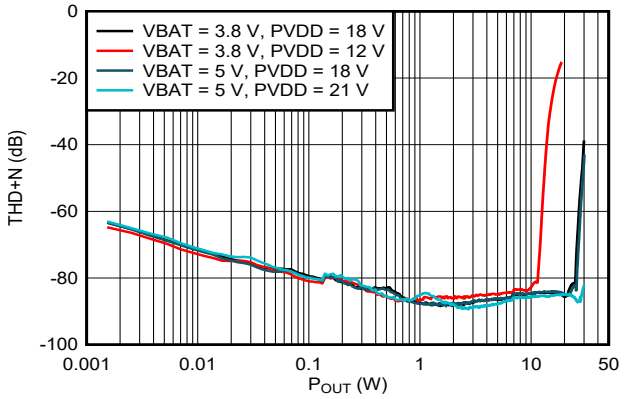
PWR_MODE0

Figure 6-4. THD+N vs Output Power



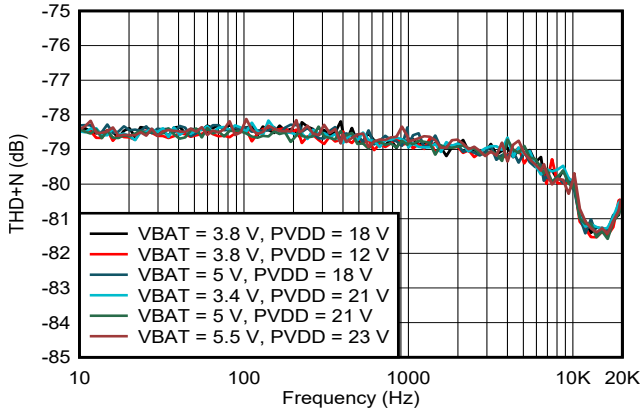
f_{IN}= 6.667 kHz PWR_MODE1

Figure 6-5. THD+N vs Output Power



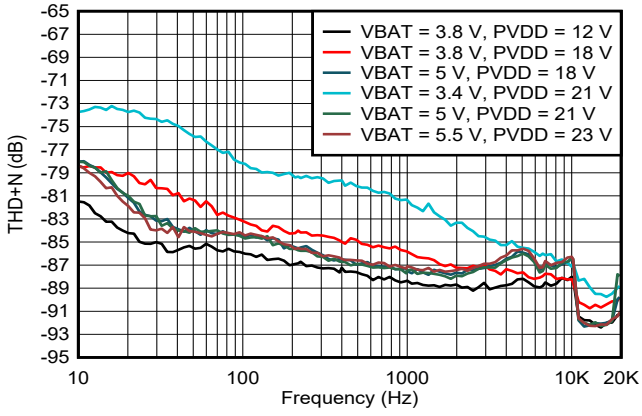
f_{IN}= 6.667 kHz PWR_MODE0

Figure 6-6. THD+N vs Output Power



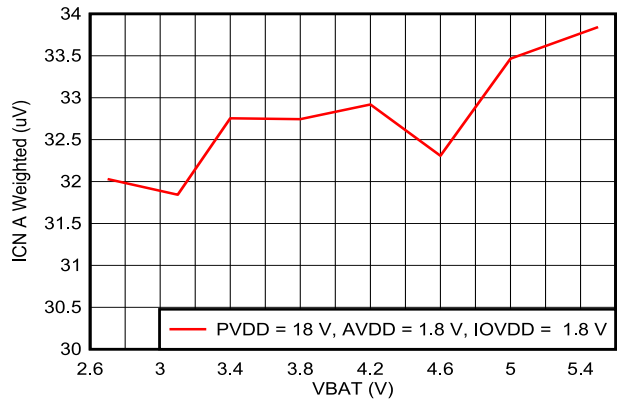
P_{OUT}= 0.1 W PWR_MODE1

Figure 6-7. THD+N vs Frequency



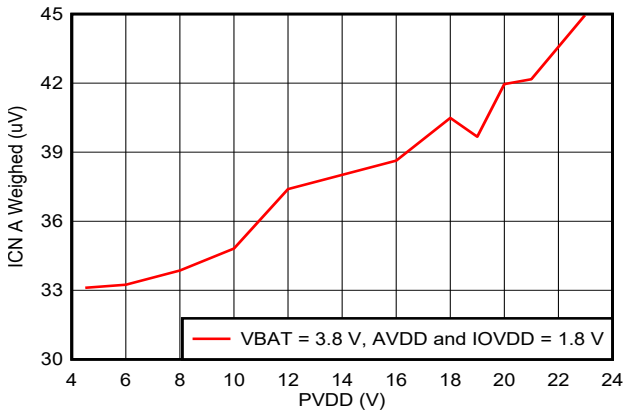
P_{OUT} = 1 W PWR_MODE1

Figure 6-8. THD+N vs Frequency



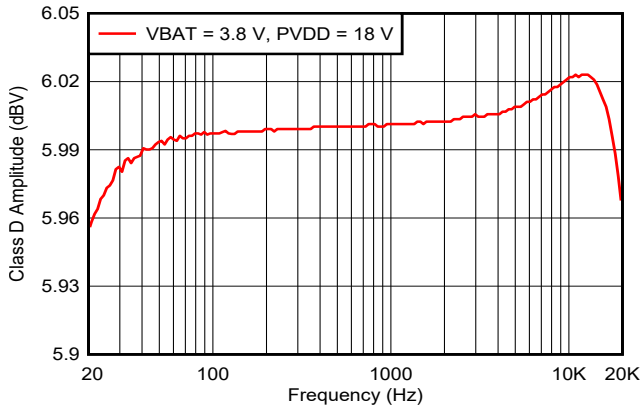
PWR_MODE1

Figure 6-9. ICN vs VBAT



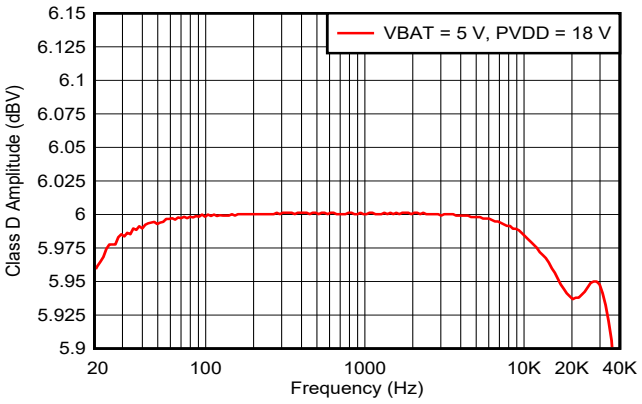
PWR_MODE0

Figure 6-10. ICN vs PVDD



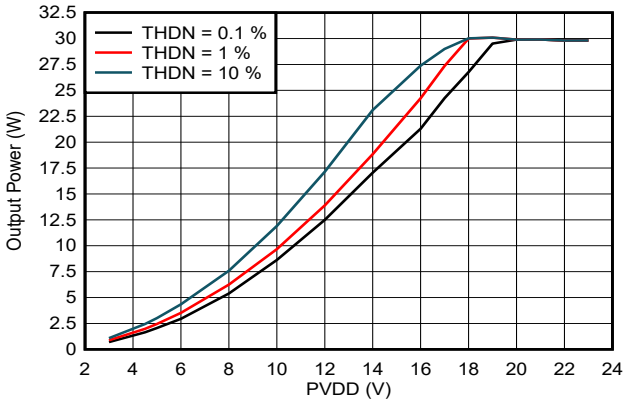
PWR_MODE1

Figure 6-11. Class-D Amplitude vs Frequency



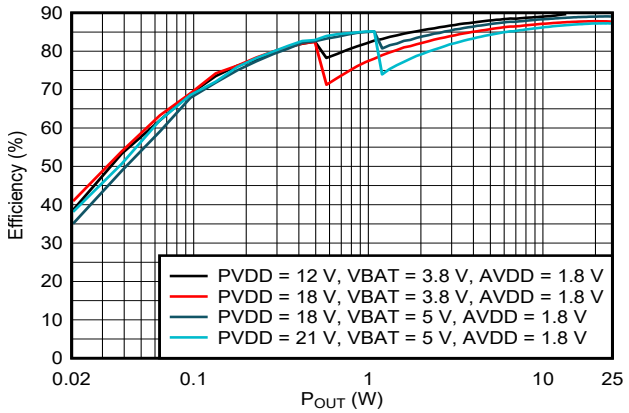
f_s = 96 kHz PWR_MODE3

Figure 6-12. Class-D Amplitude vs Frequency



VBAT1S = 5 V PWR_MODE0/ PWR_MODE1

Figure 6-13. Output Power vs PVDD



PWR_MODE1

Figure 6-14. Efficiency vs Output Power

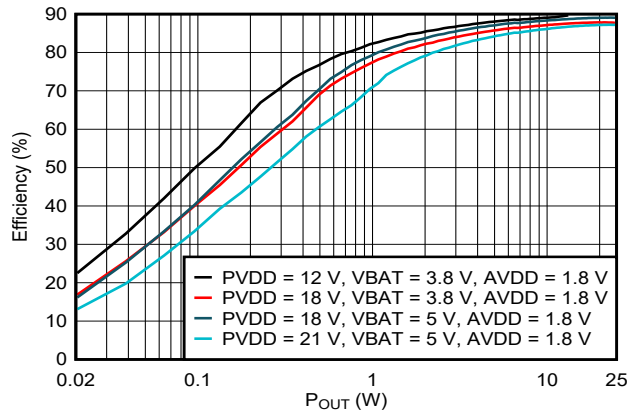


Figure 6-15. Efficiency vs Output Power

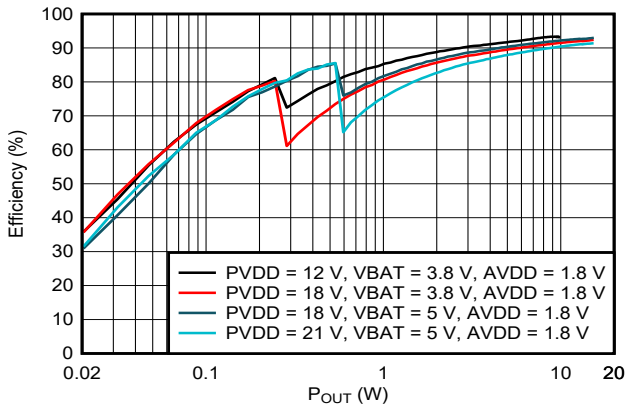


Figure 6-16. Efficiency vs Output Power

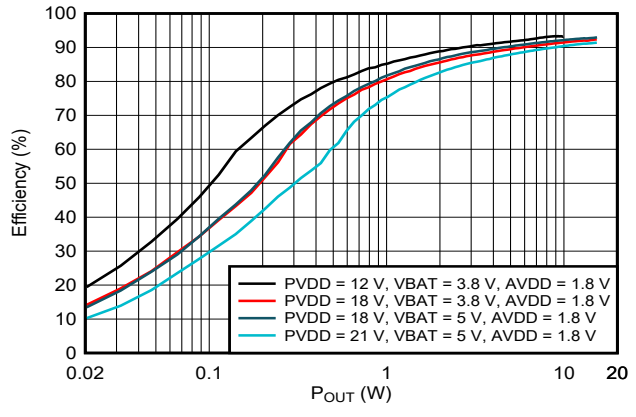


Figure 6-17. Efficiency vs Output Power

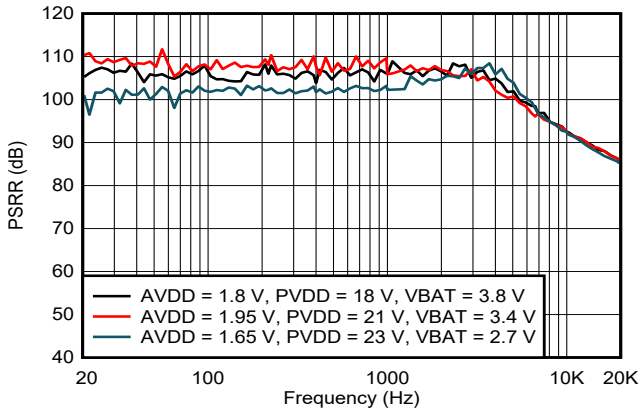


Figure 6-18. AVDD PSRR vs Frequency

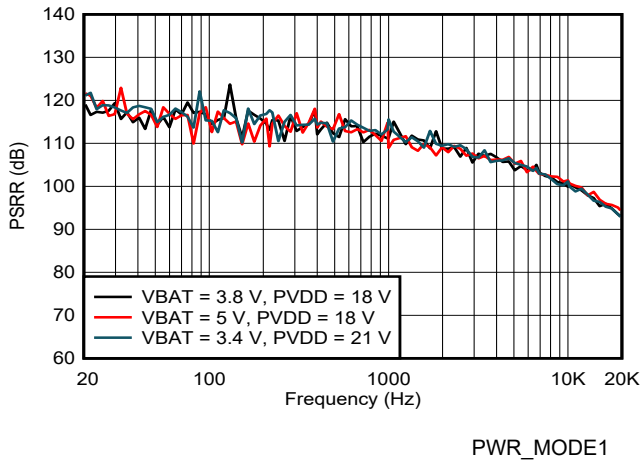


Figure 6-19. VBAT1S PSRR vs Frequency

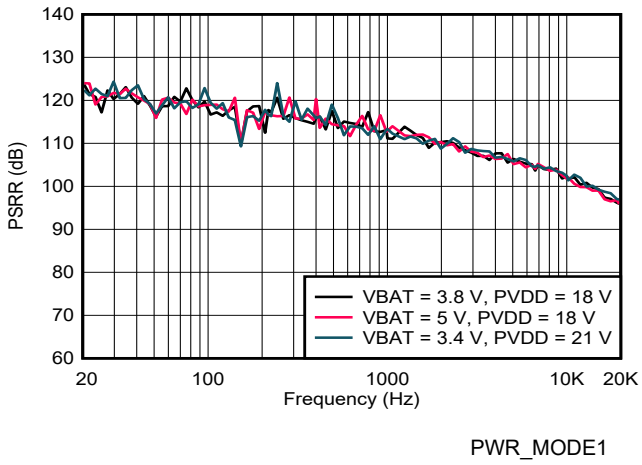


Figure 6-20. PVDD PSRR vs Frequency

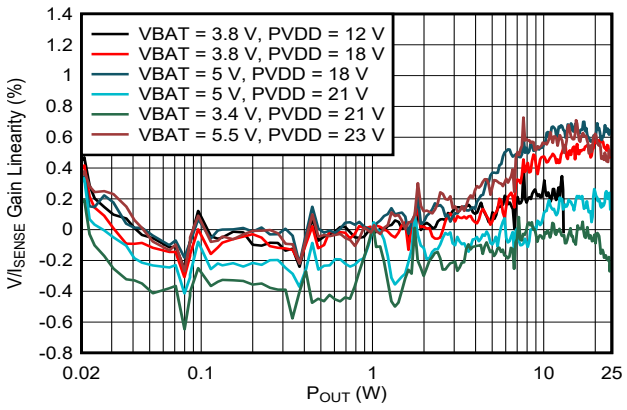


Figure 6-21. V/I Gain Linearity vs Output Power

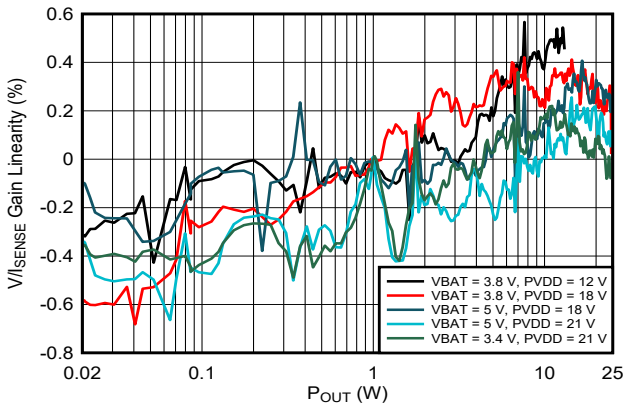


Figure 6-22. V/I Gain Linearity vs Output Power

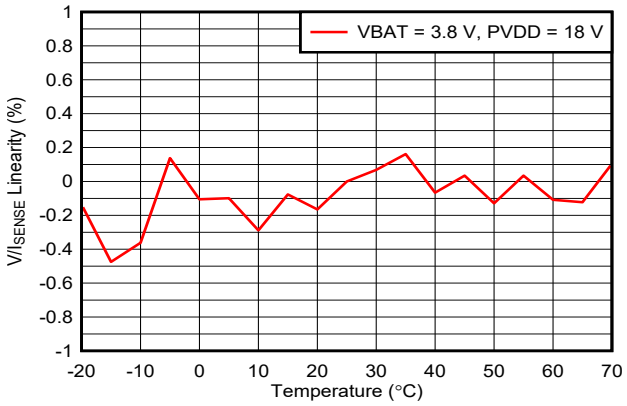


Figure 6-23. V/I Linearity vs Temperature

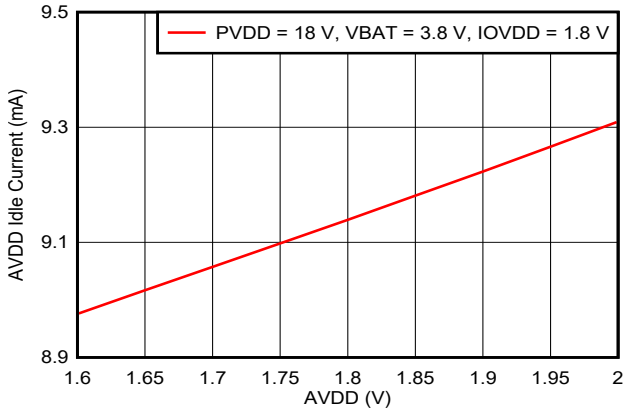


Figure 6-24. AVDD Idle Current vs AVDD

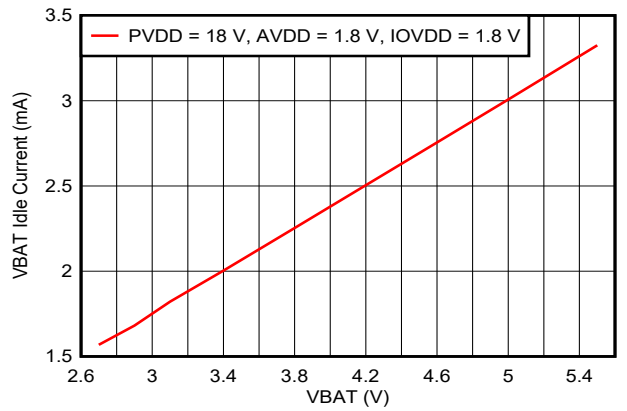


Figure 6-25. VBAT Idle Current vs VBAT

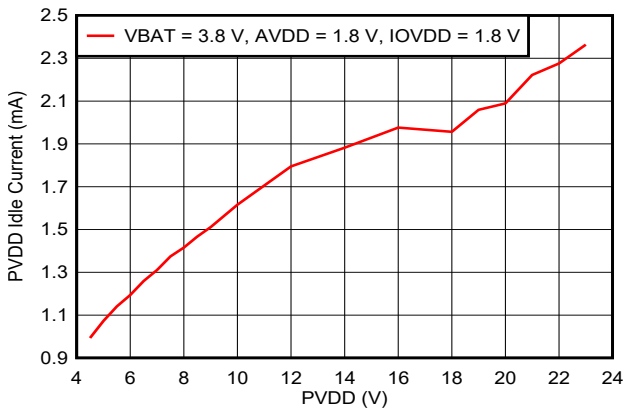


Figure 6-26. PVDD Idle Current vs PVDD

7 Parameter Measurement Information

The typical characteristics for the device are measured using the Bench Evaluation Module (EVM) and an Audio Precision Analyzer. A PSIA interface is used to allow the I²S interface to be driven directly into the Audio Precision Analyzer.

In some measurements (THD+N, ICN, DNR, and so forth), Class-D output terminals are connected to the Audio Precision Analyzer analog inputs through a Differential-to-Single Ended (D2S) filter as shown below. The D2S filter contains a second order passive pole at 120 kHz and an instrumenation amplifier. The D2S filter ensures the TAS2780 high performance Class-D amplifier has its outputs filtered and buffered before processed. This prevents measurement errors due to loading effects of AUX-00XX filter on the Class-D outputs.

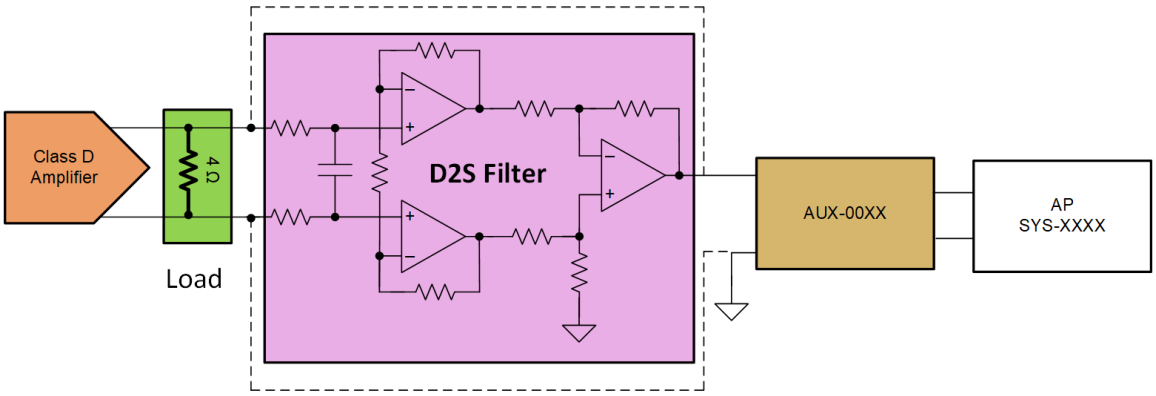


Figure 7-1. Differential to Single Ended (D2S) Filter

8 Detailed Description

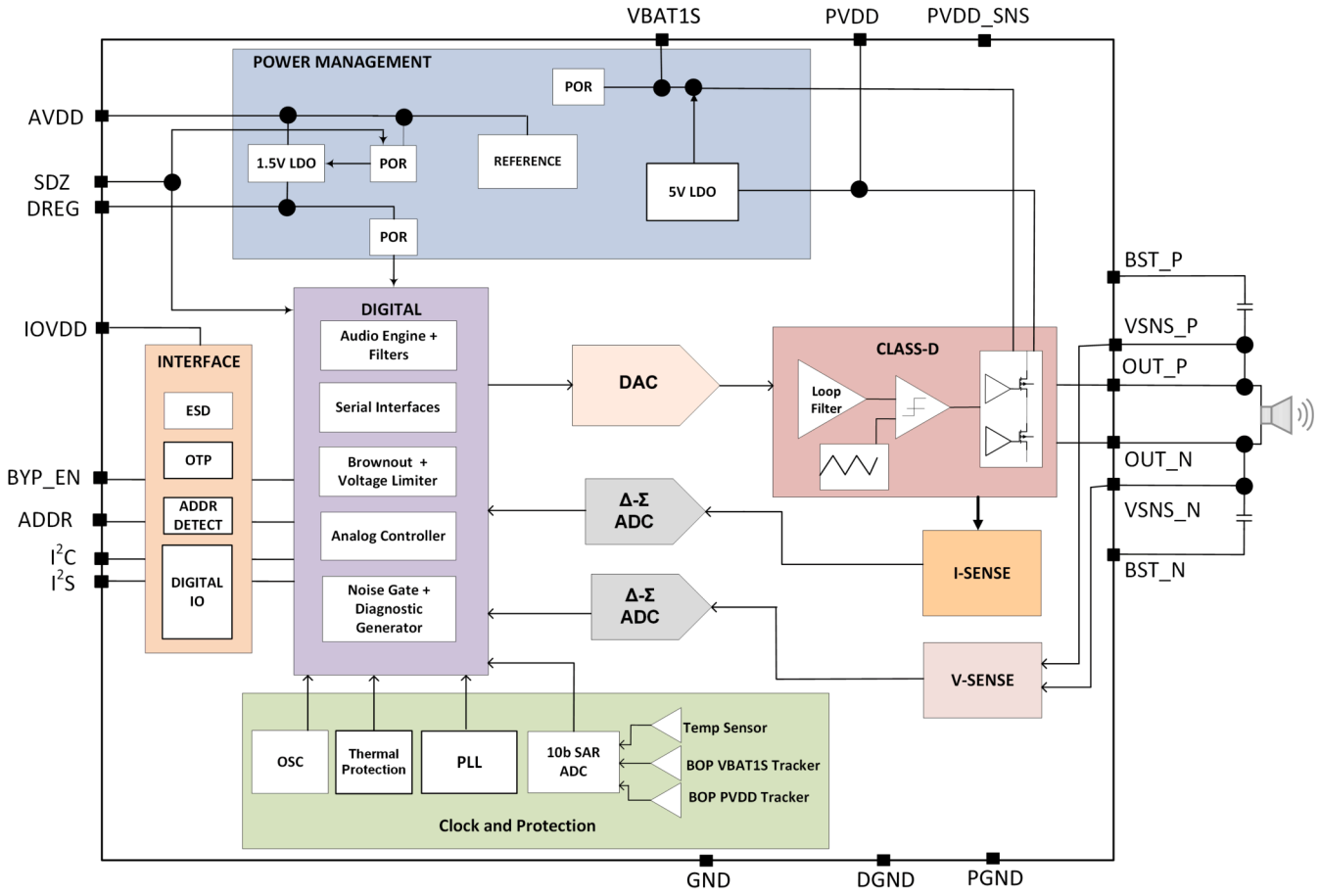
8.1 Overview

The TAS2780 is a mono digital input Class-D amplifier optimized for applications where efficient battery operation and small solution size are critical. It integrates speaker IV (current/voltage) sensing and battery tracking limiting with brown out prevention. The device operates using TDM/I²S and I²C interfaces.

Table 8-1. Full Scales

Input/Output Signal	Full Scale Value
Class-D Output	21 dBV
Voltage Monitor	23 V
Current Sense	5 A
Voltage Sense	16 Vpk

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Address Selection

The TAS2780 operates using a TDM/I^{2}S interface. Audio input and output are provided via the FSYNC, SBCLK, SDIN and SDOUT pins using formats including I^{2}S, Left Justified and TDM. Configuration and status are provided via the SDA and SCL pins using the I^{2}C protocol.

The table below illustrates how to configure the device for I^{2}C address . The peripheral addresses are shown left shifted by one bit with the R/W bit set to 0 (for example, {ADDR[6:0],1b0}). Resistors with tolerance better than 5% must be used for setting the address configuration.

Table 8-2. I^{2}C Address Selection

I^{2}C Address	0x70	0x72	0x74	0x76	0x78	0x7A	0x7C	0x7E
ADDR PIN	Short to GND	470 Ω to GND	470 Ω to AVDD	2.2 kΩ to GND	2.2 kΩ to AVDD	10 kΩ to GND	10 kΩ to AVDD	Short to AVDD

The TAS2780 has a global 7-bit I^{2}C address 0x80. When enabled, the device will additionally respond to I^{2}C commands at this address regardless of the ADDR pin settings. This is used to speed up device configuration when using multiple TAS2780 devices and programming similar settings across all devices. The I^{2}C ACK/ NACK cannot be used during the multi-device writes since multiple devices are responding to the I^{2}C command. The I^{2}C CRC function should be used to ensure each device properly received the I^{2}C commands. At the completion of writing multiple devices using the global address, the CRC at *I2C_CKSUM* register should be checked on each device using the local address for a proper value. The global I^{2}C address can be disabled using *I2C_GBL_EN* register bit. The I^{2}C address is detected by automatically sampling the ADDR pin when

SDZ pin is released. Additionally, the address may be re-detected by setting *I2C_AD_DET* register bit high after power up and the ADDR pin will be re-sampled.

8.3.2 Register Organization

Device configuration and coefficients are stored using a page and book scheme. Each page contains 128 bytes and each book contains 256 pages. All device configuration registers are stored in book 0 which is the default setting at power up and after a software reset. The book and page can be set by the *BOOK[7:0]* bits of register from and *PAGE[7:0]* bits of register from .

Note

Programming register bits from book 0x00, page 0x04 needs to be done in groups of four registers (32 bit format), each byte corresponding to a register and with less significant byte corresponding to the highest register address. For instance, when programing limiter maximum threshold, in registers 0x0C - 0x0F of page 0x04, the MSBs will be in register 0x0C and the LSBs in register 0x0F.

8.4 Device Functional Modes

8.4.1 TDM Port

The TAS2780 provides a flexible serial audio port. The port can be configured to support a variety of formats including stereo I^2S, Left Justified and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including speaker voltage and current sense, PVDD voltage, die temperature and channel gain.

The TDM serial audio port supports up to 16 of 32 bit time slots at 44.1/48 kHz or 8 of 32 bit time slots at a 88.2/96 kHz sample rate. Valid SBCLK to FSYNC ratios are 16, 24, 32, 48, 64, 96, 128, 192, 256, and 512. The device can automatically detect the number of time slots and it does not need to be programmed.

By default, the TAS2780 will automatically detect the PCM playback sample rate. This feature can be disabled and the device can manually be configured by setting the *AUTO_RATE* register bit high.

The *SAMP_RATE[2:0]* and *SAMP_RATIO[3:0]* register bits are used to configure the PCM audio sample rate when *AUTO_RATE* register bit is high (auto detection of TDM sample rate is disabled). The TAS2780 employs a robust clock fault detection engine that will automatically volume ramp down the playback path if FSYNC does not match the configured sample rate (if *AUTO_RATE* = 1) or the ratio of SBCLK to FSYNC is not supported (minimizing any audible artifacts). Once the clocks are detected to be valid in both frequency and ratio, the device will automatically volume ramp the playback path back to the configured volume and resume playback.

When using the auto rate detection the sampling rate and SBCLK to FSYNC ratio detected on the TDM bus are reported back on the read-only register bits *FS_RATE[2:0]* and *FS_RATIO[3:0]*.

The TAS2780 supports a 12 MHz SBCLK operation. The system will detect or should be manually configured for a ratio of 125 or 250. In this specific ratio the last 32 bit slot should not be used to transmit data over TDM (SDOUT) or ICC (Section 8.4.2.10.1), as data will be truncated.

Figure 8-1 and Figure 8-2 below illustrate the receiver frame parameters required to configure the port for playback. A frame begins with the transition of FSYNC from either high to low or low to high (set by the *FRAME_START* register bit). FSYNC and SDIN are sampled by SBCLK using either the rising or falling edge (set by the *RX_EDGE* register bit). The *RX_OFFSET[4:0]* register bits define the number of SBCLK cycles from the transition of FSYNC until the beginning of time slot 0. This is typically set to a value of 0 for Left Justified format and 1 for an I^2S format.

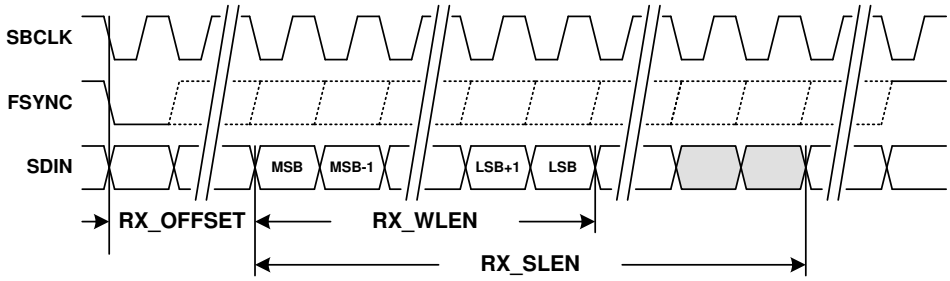


Figure 8-1. TDM RX Time Slot with Left Justification

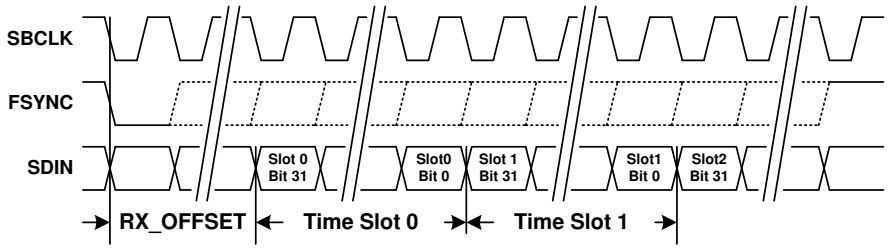


Figure 8-2. TDM RX Time Slots

The *RX_SLEN[1:0]* register bits set the length of the RX time slot to 16, 24 or 32 (default) bits. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits to 16, 20, 24 (default) or 32 bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit. The TAS2780 supports mono and stereo down mix playback ([L+R]/2). By default the device will playback mono from the time slot equal to the I^2C base address offset (set by the ADDR pin) for playback. The *RX_SCFG[1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_L[3:0]* and *RX_SLOT_R[3:0]* register bits.

If time slot selection places reception either partially or fully beyond the frame boundary, the receiver will return a null sample equivalent to a digitally muted sample.

The TDM port can transmit a number of sample streams on the SDOUT pin including speaker voltage sense, speaker current sense, interrupts and status, PVDD voltage, die temperature and channel gain. Figure 8-3 below illustrates the alignment of time slots to the beginning of a frame and how a given sample stream is mapped to time slots.

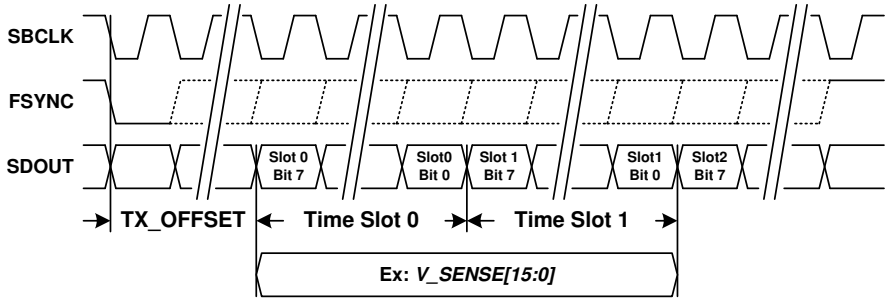


Figure 8-3. TDM Port TX Diagram

Either the rising or falling edge of SBCLK can be used to transmit data on the SDOUT pin. This can be configured by setting the *TX_EDGE* register bit. The *TX_OFFSET[2:0]* register bits define the number of SBCLK cycles between the start of a frame and the beginning of time slot 0. The TDM and ICC TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit. An optional bus keeper will weakly hold the state of SDOUT and ICC pins when all devices driving the bus are Hi-Z. Since only one bus keeper is required on SDOUT, this feature can be disabled via the *TX_KEEPEN* register bit. The bus keeper can be configured to hold the bus for only 1LSB or Always using *TX_KEEPLN* register bit. Additionally, the keeper LSB can be driven for a full cycle or half of cycle using *TX_KEEPCY* register bit.

TX_FILL register bit is used in mono systems where there is only one amplifier on I²S bus. All the slots unused by the amplifier will be filled with zeros when *TX_FILL* register bit is set to low.

The SDOUT_HIZ registers from page 0x01 are useful when multiple devices are on the same I²S bus. Each device does not know the configuration of slots in the other devices on the bus. It is required at the system level to program the SDOUT_HIZ registers appropriately, in such way that the settings are done correctly and do not create any contention, internally and externally.

Each sample stream is composed of either one or two 8 bit time slots. Speaker voltage sense and speaker current sense sample streams are 16 bit precision, so they will always utilize two TX time slots. The PVDD and VBAT1S voltage streams are 10 bit precision, and can either be transmitted left justified in a 16 bit word (using two time slots) or can be truncated to 8 bits (the top 8 MSBs) and be transmitted in a single time slot. This is configured by setting *PVDD_SLEN* and *VBAT1S_SLEN* register bits. The die temperature and the gain are both 8 bit precision and are transmitted in a single time slot.

The time slot register for each sample stream defines where the MSB transmission begins. By default *VSNS_SLOT[5:0]* register bits are set to 2 (decimal), the upper 8 MSBs will be transmitted in time slot 2 and the lower 8 LSBs will be transmitted in time slot 3. This sample stream can be individually enabled or disabled by using *VSNS_TX* register bit. The *ISNS_SLOT[5:0]* register bits are set by default to 0 (decimal) and the sample stream can be enabled or disabled by using *ISNS_TX* register bit. The enable/disable feature of the streams is useful to manage limited TDM bandwidth since it may not be necessary to transmit all streams for all devices on the bus.

It is important to ensure that time slot assignments for actively transmitted sample streams do not conflict. This will avoid producing unpredictable transmission results in the conflicting bit slots (i.e. the priority is not defined).

The current and voltage values are transmitted at the full 16 bit measured values by default. The *IVMON_LEN[1:0]* register bits can be used to transmit only the 8 MSB bits in one slot or 12 MSB bits values across multiple slots. The special 12 bit mode is used when only 24 bit I²S/ TDM data can be processed by the host processor. The device should be configured with the voltage-sense slot and current-sense slot off by 1 slot and will consume 3 consecutive 8 bit slots. In this mode the device will transmit the first 12 MSB bits followed by the second 12 MSB bits specified by the preceding slot.

If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

The time slots for VBAT1S, PVDD and temperature measurements are set using *VBAT1S_SLOT[5:0]*, *PVDD_SLOT[5:0]* and *TEMP_SLOT[5:0]* register bits. To enable each of the sample streams, register bits *VBAT1S_TX*, *PVDD_TX* and *TEMP_TX* must be set high. The slot length is selected by *VBAT1S_SLEN* and *PVDD_SLEN* register bits.

For TDM final processed audio slot, enable and length settings, use *AUDIO_SLOT[5:0]*, *AUDIO_TX* and *AUDIO_SLEN* register bits.

Information about status of slots can be find in *STATUS_SLOT[5:0]* register bits. *STATUS_TX* register bit set high enables the status transmit.

The slot configuration for the TX limiter gain reduction can be set between 0 (default) and 63 by setting *GAIN_SLOT[5:0]* register bits. It is used for ICC (Section 8.4.2.10) and can be either over the TDM bus or ICC bus. To use this feature, the register bit *GAIN_TX* needs to be set high.

8.4.2 Playback Signal Path

8.4.2.1 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers. The TAS2780 employs a high-pass filter (HPF) to prevent this from occurring for the PCM playback path. The *HPF_FREQ_PB[2:0]* register bits set the corner frequencies of HPF. The filter can be bypassed by setting the register bits to 3'b000.

8.4.2.2 Amplifier Inversion

The TAS2780 will output a non-inverted signal to the OUT_P and OUT_N pins. The output can be inverted with respect to the digital input value by setting the *AMP_INV* register bit to high.

8.4.2.3 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier output level and the digital volume control (DVC).

Amplifier output level settings are programmed using the *AMP_LVL[4:0]* register bits. The amplifier levels are presented in Section 8.9.9. The Digital Volume Control (DVC) is set by default to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used only to convey gain.

Equation (1) calculates amplifier output voltage:

$$V_{AMP} = INPUT + A_{DVC} + A_{AMP} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- *INPUT* is the digital input amplitude as a number of dB with respect to 0 dBFS
- A_{DVC} is the digital volume control setting as a number of dB
- A_{AMP} is the amplifier output level setting as a number of dBV

The DVC is configurable from 0 dB to -100 dB in 0.5 dB steps by setting the *DVC_LVL[7:0]* register bits. Settings greater than C8h are interpreted as mute. When a change in digital volume control occurs, the device ramps the volume to the new setting based on the *DVC_RAMP_RATE[1:0]* register bits status.

If *DVC_RAMP_RATE[1:0]* bits are set to 2'b11 the volume ramping is disabled. This setting can be used to speed up startup, shutdown and digital volume changes when volume ramping is handled by the system controller.

The Class-D amplifier uses a closed-loop architecture. The approximate threshold for output signal clipping is given by equation (2).

$$V_{PK} = V_{SUP} * \frac{R_L}{R_{FET} + R_P + R_L} \quad (2)$$

where:

- V_{PK} is the maximum peak un-clipped output voltage in V
- V_{SUP} is the power supply of Class-D output stage
- R_L is the speaker load in Ω
- R_P is the parasitic resistance on PCB (routing, filters) in Ω
- R_{FET} is the power stage total resistance (HS FET, LS FET, Sense Resistor, bonding, packaging) in Ω

When VBAT1S supplies Class-D output stage typical R_{FET} value is 0.5 Ω. For PVDD supply R_{FET} typical value is 0.25 Ω.

8.4.2.3.1 Safe Mode

The safe mode is a single bit that will enable an 18 dB attenuation in the forward path. It is similar to setting the *DVC_LVL[7:0]* register bits to 24h (-18 dB). When the *SMODE_EN* bit is set to high, the *DVC_LVL[7:0]* register bits will be ignored and volume ramping disabled.

8.4.2.4 VBAT1S Supply

The TAS2780 can operate with or without an external VBAT1S supply. When configured without an external VBAT1S supply, the PVDD voltage will be used with an internal LDO to generate this supply voltage. A

decoupling capacitor should still be populated as recommended in Table 9-1. In this case, *VBAT1S_MODE* bit should be set to high before transitioning from software shutdown. More details about VBAT1S supply modes of operation can be found in Section 11.1.

8.4.2.5 Low Voltage Signaling (LVS)

The TAS2780 monitors the absolute value of the audio stream.

When the input is initially above the programmed fixed threshold set by *LVS_FTH[4:0]* register bits, the Class-D is supplied by the PVDD rail. When the signal level drops below this threshold for longer than the hysteresis time defined by *LVS_HYS[3:0]* bits the Class-D supply will switch to VBAT1S (see Figure 8-4).

All values of *LVS_HYS[3:0]* bit settings will ensure the remaining samples will be output before BYP_EN pin is asserted (high). When multiple devices have BYP_EN pin connected together, any of the devices requiring a supply voltage higher than the threshold will pull the open drain output low.

When the signal level crosses above the programmed fixed threshold set by *LVS_FTH[4:0]* bits the Class-D supply will switch to PVDD.

The open-drain BYP_EN pin will be de-asserted (actively pulling the output low) after a delay programmed by the *LVS_DLY[1:0]* register bits . The Y Bridge will switch from the VBAT1S supply to the PVDD supply after a delay programmed by the *CDS_DLY[1:0]* register bits.

The fixed LVS threshold is set based on the output signal level and is measured in dBFS.

By default, the LVS threshold is configured to be a value relative to the VBAT1S voltage. The *LVS_TMODE* bit is set to high and the *LVS_RTH[3:0]* register bits are set to 3'b010 (0.7 V from VBAT1S).

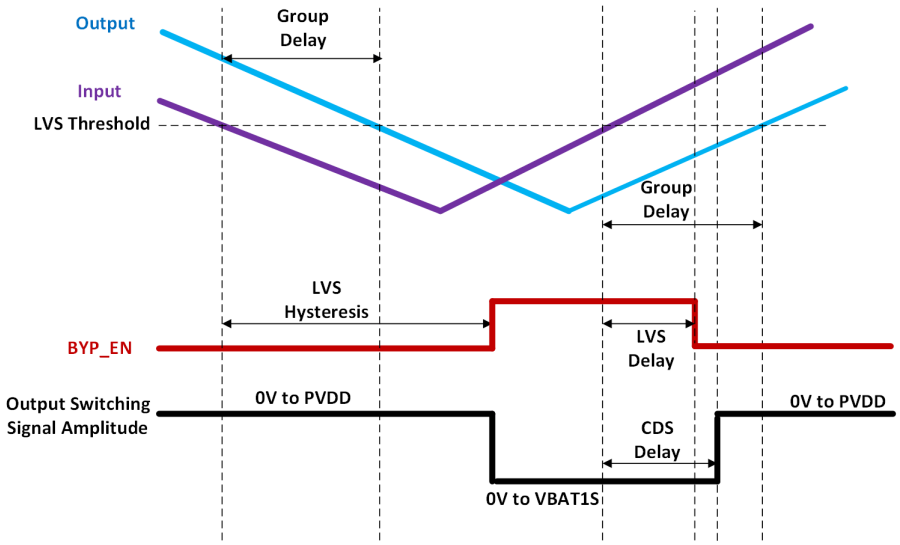


Figure 8-4. Low Voltage Signaling

The LVS fixed thresholds, when *CDS_MODE[1:0]=11* (PWR_MODE2 from Section 11.1), can be set using register bits *LVS_FTH_LOW[1:0]*. When *CDS_MODE[1:0]=00* (PWR_MODE1 from Section 11.1) the fixed thresholds should be set with register bits *LVS_FTH[4:0]*.

BOP, Limiter, Thermal Foldback and Thermal Gradient gain attenuations should not be taken into account for calculating LVS threshold.

8.4.2.6 Y-Bridge

The TAS2780 Class-D output uses a Y-Bridge configuration to improve efficiency during playback. The LVS (Section 8.4.2.5) is internally used to select between the PVDD and VBAT1S supplies. This feature is enabled by setting *CDS_MODE[1:0]* bits to 2'b00 when both PVDD and VBAT1S are supplied externally to the device. In this case the VBAT1S rail must be capable of delivering power (up to 1 W).

If not configured to Y-bridge mode the device will use only the selected supply for Class-D output even if clipping would occur. The device can operate using only PVDD to supply Class-D output. In this configuration the VBAT1S can be provided from external supply (register bit *VBAT1S_MODE*=0) or generated by an internal LDO (register bit *VBAT1S_MODE*=1). In this case *CDS_MODE[1:0]* bits should be set to 2'b10.

The TAS2780 Y-Bridge with low power on VBAT1S can be used to switch to the VBAT1S rail only at very low power when close to idle. This will reduce the Class-D output swing when near idle and limit the current requirements of the VBAT1S supply. Set the *CDS_MODE[1:0]* register to 2'b11 for this mode.

See Section 11.1 for details on programming the power mode of operation.

When in Y-Bridge mode, if the PVDD falls below (VBAT1S + 2.5 V) level the Y-bridge will stop switching between supplies and will remain on the PVDD supply.

8.4.2.7 Noise Gate

The TAS2780 has a noise-gate feature that monitors the input signal and powers down the Class-D when the signal goes below the set threshold set by *NG_LVL[1:0]* bits for longer than the time set by *NG_HYST[2:0]* register bits. When the signal goes above the threshold the Class-D will re-power in seven samples, before the samples applied to the audio input interface reach the Class-D bridge. This feature is enabled by setting *NG_EN* bit to high. Once enabled it is able to power up and down the channel within the device processing delay, with no additional external control. Volume ramping can be also used during noise gate operations by setting *NG_DVR_EN* bit to low.

The noise gate can be configured with finer resolution at the expense of additional I^2C writes. Use *NGFR_EN* bit to enable this mode and register bits *NGFR_LVL[23:0]* to set the fine resolution. The fine resolution hysteresis is set using *NGFR_HYST[18:3]* register bits.

8.4.2.8 Supply Tracking Limiter with Brown Out Prevention

The TAS2780 contains a supply tracking limiter to control distortion and brownout prevention to mitigate brownout events. The gain reduction that occurs due to this block can be aligned across multiple devices using the Inter Chip Gain Alignment (ICGA) (Section 8.4.2.10) feature. The maximum device attenuation set by *DEV_MAX_ATTN[6:0]* register bits can be used to limit the combination of the limiter and brownout attenuation.

The Supply Tracking Limiter (STL) (Section 8.4.2.8.1) and the Brownout Prevention (BOP) (Section 8.4.2.8.2) are configured independently. The ICGA, if enabled, keeps multiple device gains in sync if the STL and BOP need to reduce the gain. However, the BOP will take priority in the device. In order to prevent the STL and BOP from both making simultaneous adjustments to the system, the STL and ICGA will be paused once the BOP engages, until it fully releases.

The attenuation applied to the device can be selected to be either the sum of the limiter attenuation (ICLA) and Brownout attenuation (ICBA) or the maximum of the two of them by setting the *ICG_MODE* register bit.

8.4.2.8.1 Supply Tracking Limiter (STL)

The TAS2780 monitors PVDD supply voltage and the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions.

The Supply Tracking Limiter feature is enabled by setting the *LIM_EN* bit register to high.

Configurable attack rate, hold time and release rate are provided to shape the dynamic response of the limiter (*LIM_ATK_RT[3:0], LIM_HLD_TM[2:0]* and *LIM_RLS_RT [3:0]* register bits).

A maximum level of attenuation applied by the limiter is configurable via the *LIM_MAX_ATTN[3:0]* register bits. If the limiter mode is attacking and if it reaches the maximum attenuation, gain will not be reduced any further.

The limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track PVDD below a programmable inflection point with a minimum threshold value. Figure 8-5 below shows the limiter configured to limit to a constant level regardless of PVDD level. To achieve this behavior, set the limiter maximum threshold to the desired level via the *LIM_TH_MAX[31:0]* register bits. Set the

limiter inflection point (register bits *LIM_INF_PT[31:0]*) below the minimum allowable PVDD setting. The limiter minimum threshold, set by register bits *LIM_TH_MIN[31:0]*, does not impact limiter behavior in this use case.

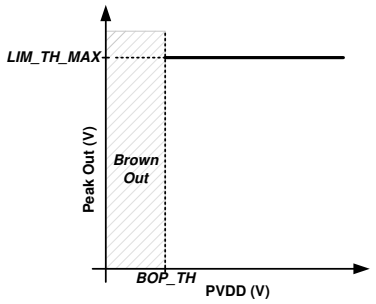


Figure 8-5. Limiter with Fixed Threshold

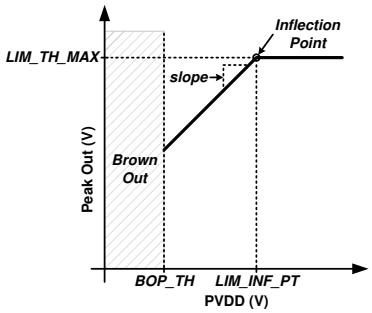


Figure 8-6. Limiter with Inflection Point

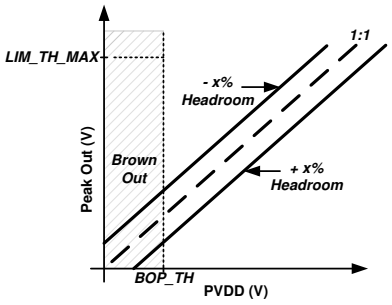


Figure 8-7. Limiter with Dynamic Threshold

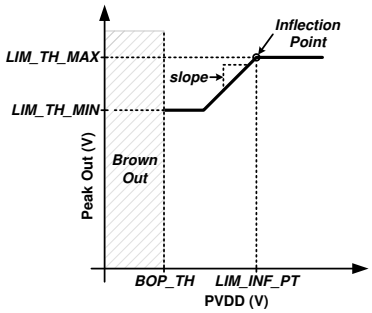


Figure 8-8. Limiter with Inflection Point and Minimum Threshold

Figure 8-6 shows how to configure the limiter to track PVDD supply below a certain level without setting a minimum threshold. Set the *LIM_TH_MAX[31:0]* register bits to the desired threshold and *LIM_INF_PT[31:0]* register bits to the desired inflection point where the limiter will begin reducing the threshold with PVDD. The *LIM_SLOPE[31:0]* register bits can be used to change the slope of the limiter tracking with PVDD. The default value of 1 V/V will reduce the threshold 1 V for every 1 V of drop in PVDD. More aggressive tracking slopes can be programmed if desired. Program the *LIM_TH_MIN[31:0]* bits below the minimum PVDD to prevent the limiter from having a minimum threshold reduction when tracking PVDD supply.

The limiter with a supply tracking slope can be configured in an alternate way. By setting *LIM_HR_EN* register bit to high , a headroom can be specified as a percentage of the supply voltage using a 1V/V slope by setting *LIM_DHR[4:0]* register bits. For example if a headroom of -10% is specified, the peak output voltage will be set to be 10% higher than PVDD. In this use case presented in Figure 8-7 the limiting begins for signals above the supply voltage and will result in a fixed clipping. If a positive headroom of +10% is specified the peak output voltage will be dynamically set 10% below the current PVDD. In this use case the limiting will begin at signal levels lower than the supply voltage and will prevent clipping from occurring.

To achieve a limiter that tracks PVDD only up to a minimum threshold, configure the limiter *LIM_TH_MAX [31:0]* and *LIM_SLOPE[31:0]* register bits as in the previous examples. Then, additionally set the *LIM_TH_MIN[31:0]* register bits to the desired minimum threshold. Supply voltage below this minimum threshold will not continue to decrease the signal output voltage. This is shown in Figure 8-8.

By setting register bit *LIM_HR_EN* to low the limiter mechanism depends on settings for maximum/minimum thresholds, inflection point and slope. Once this bit is set high the limiter dynamic headroom is enabled.

When a BOP (Brownout Prevention) event occurs the limiter updates can be paused (*LIM_PDB* register bit set to high) until the BOP fully releases. This can be used to prevent undesired interactions between both protection systems.

8.4.2.8.2 Brownout Prevention (BOP)

Brownout Prevention (BOP) feature provides a priority input to a dedicated limiter to generate a fast response to transient dips in the supply voltage at the end of charge conditions that can cause system level brownout. When supply voltage dips below the BOP threshold, the limiter begins reducing gain at a configurable attack rate. When supply voltage rises above the BOP threshold, the limiter will begin to release after a programmed hold time. The BOP feature can be enabled by setting the *BOP_EN* register bit high. The brownout supply source can be set using *BOP_SRC* register bit to either PVDD (*BOP_SRC =1*) or VBAT1S (*BOP_SRC =0*) depending on application need. It should be noted that the BOP feature is independent of the limiter and will function, if enabled, even if the Supply Tracking Limiter is disabled.

The BOP can be configured to attack the gain through four levels as the supply voltage continues to drop. The BOP threshold Level 3 is set using the *BOP_TH3[7:0]* register bits followed by threshold Level 2 using *BOP_TH2[7:0]* register bits, Level 1 threshold set by *BOP_TH1[7:0]* bits and finally crossing Level 0 set by *BOP_TH0[7:0]* register bits.

The BOP level that is not used can be disabled individually (register bits *BOP_DIS0*, *BOP_DIS1 , BOP_DIS2, BOP_DIS3*) providing flexibility from one to four levels. For proper operation levels should be disabled in order, starting with Level 3.

Each level has a separate attack rate (register bits *BOP_ATK_RT0[2:0]* to *BOP_ATK_RT3[2:0]*), attack step size (register bits *BOP_ATK_ST0[3:0]* to *BOP_ATK_ST3[3:0]*), release rate (register bits *BOP_RLS_RT0[2:0]* to *BOP_RLS_RT3[2:0]*), release step size (register bits *BOP_RLS_ST0[3:0]* to *BOP_RLS_ST3[3:0]*), dwell time (register bits *BOP_DT0[2:0]* to *BOP_DT3[2:0]*), hold time (register bits *BOP_HT0[2:0]* to *BOP_HT3[2:0]*), maximum attenuation (*BOP_MAX_ATTN0[4:0]* to *BOP_MAX_ATTN3[4:0]*).

For proper device operation the following conditions must be met:

- BOP_MAX_ATTN0 > BOP_MAX_ATTN1 > BOP_MAX_ATTN2 > BOP_MAX_ATTN3
- BOP_TH Level 3 > BOP_TH Level 2 > BOP_TH Level 1 > BOP_TH Level 0.

Use bits *BOP_MAX_ATTN* of registers *BOP_CFG4, BOP_CFG9, BOP_CFG14, BOP_CFG20* to program attenuation levels. Registers *BOP_CFG5, BOP_CFG10, BOP_CFG15, BOP_CFG21* will be used for setting the BOP threshold levels.

The TAS2780 can also immediately mute and then shutdown the device when a BOP event occurs by reaching Level 0 if the *BOP_SHDN* register bit is set high. For the device to continue playing audio again it must transition through a Software/Hardware Shutdown state. If the hold time set by *BOP_HT0÷4[2:0]* register bits is at 7h (Infinite) the device needs to transition through a Mute or Software/Hardware Shutdown state, or the register bit *BOP_HLD_CLR* can be set to high causing the device to exit the hold state and begin releasing. This bit is self clearing and will always read-back low.

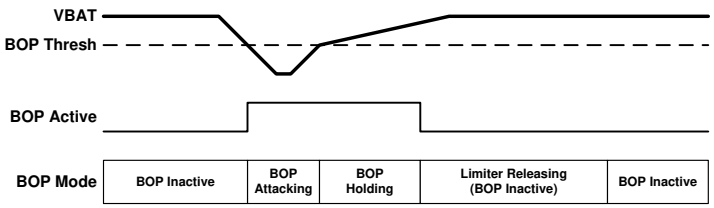


Figure 8-9. Brownout Prevention Event

The TAS2780 BOP engine will keep track of the current level state, the lowest BOP level that has been engaged and the lowest measued BOP supply voltage. This information is continuously updated until requested. To access this information the register *BOP_STAT_HLD* should be set high. This will pause the updates of the current state (*BOP_STAT_STATE[3:0]*) and lowest BOP level (*BOP_STAT_LLVL[2:0]*) registers bits allowing them to be read back. Once the read is complete the register bit *BOP_STAT_HLD* should be set low again clearing the current BOP status registers and re-enabling the updates based on current BOP state.

The lowest PVDD measurement since the last read is available in the register bits *BOP_STAT_PVDD[9:0]* if *BOP_STAT_HLD* register bit is set high before reading.

A hold condition (infinite or not) for a higher BOP level will not be reached if the supply ramps up faster than the lower levels release. Specifically, whether the infinite hold for a level is reached or not, it depends on the release rates of the lower levels, so even if infinite hold is set, it might not be reached.

8.4.2.9 Low Battery Tracking Limiter (LBTL)

The VBAT1S limiter attenuates the channel gain at lower VBAT1S voltages (< 3.2 V) to reduce the maximum power delivery and prevent thermal shutdown.

Using the SAR measurement on VBAT1S the limiter calculates its gain based on the equation below.

$$LBTL\_GAIN\ (dBV) = 21dBV + VBLIM\_GAIN\ (dBV) \quad (3)$$

If the programmed signal gain (amplifier level and DVC) meets the following condition:

$$A_{AMP} + A_{DVC} < LBTL\_GAIN, \quad (4)$$

the LBTL mechanism will not be activated.

The *VBLIM_GAIN* from equation (3) is dependent on VBAT1S level (see the table below).

Table 8-3. VBLIM_GAIN vs VBAT1S

VBAT1S [V]	VBLIM_GAIN [dBV]
3.2	0
3.1	-0.5
3	-0.75
2.9	-1.2
2.8	-1.56
2.7	-2

The overall gain in the signal chain will be the minimum of gains defined by SPL, BOP and LBTL.

8.4.2.10 Inter Chip Gain Alignment (ICGA)

The TAS2780 supports alignment of STL and brownout BOP dynamics across devices using the dedicated ICC feature (Section 8.4.2.10.1) or across the TDM output bus (SDOUT). This ensures consistent gain between channels during limiting or brownout events since these dynamics are dependent on audio content, which can vary across channels. Each device can be configured to align to a specified number of other devices, which allows creation of groupings of devices that align only to each other.

STL and BOP activity is optionally transmitted by each device on SDOUT pin or ICC pin in a 24-bit time slot. When both limiter and brownout are enabled, the data is comprised of an 11-bit word for limiter and a 13-bit word for brownout data. If only the limiter is enabled, the data will be 12-bit word for limiter data. Gain reduction should be transmitted in adjacent time slots for all devices that are to be aligned beginning with the first slot that is specified by the *ICGA_SLOT[5:0]* register bits. The order of the devices is not important as long as they are adjacent. The time slot for limiter gain reduction is configured by the *GAIN_SLOT[5:0]* register bits and enabled by the *GAIN_TX* register bit being set high. The *ICGA_SEN[7:0]* register bits specify which time slots should be listened to for gain alignment. This allows any number of devices between two and eight to be grouped together. At least two of these devices should be enabled for alignment to take place.

To enable the inter-chip limiter alignment the *ICLA_EN* register bit should be set to high. To enable the inter chip BOP alignment the *ICBA_EN* register bit should be set to high. All devices should be configured with identical limiter and brownout prevention settings.

8.4.2.10.1 Inter-Chip Communication (ICC) Pin

The TAS2780 has a dedicated ICC bus pin that enables gain alignment (ICGA) without consuming slots on the TDM bus. The ICC pin is connected to all TAS2780 devices in the system and slots are configured using register bits *GAIN_SLOT[5:0]*. This bus uses the TDM (Section 8.4.1) BCLK and FSYNC inputs and requires all devices to be configured using the same sampling clock. The ICC pin supports separate bus keeper configuration from

the SDOUT pin (TDM bus). If the ICC pin is disabled or used for GPIO functionality, the ICGA (Section 8.4.2.10) will occur on the TDM bus instead of the ICC pin. Register bits *ICC_MODE[2:0]* are used to set the ICC pin functionality.

8.4.2.11 Class-D Settings

8.4.2.11.1 Synchronization

The TAS2780 Class-D amplifier supports spread spectrum PWM modulation, which can be enabled by setting the *AMP_SS* register bit high. This can help reduce EMI in the system.

By default the Class-D amplifier switching frequency is based on the device trimmed internal oscillator. To synchronize switching to the audio sample rate, set the *CLASSD_SYNC* register bit high. When the Class-D is synchronized to the audio sample rate, the *RAMP_RATE* register bit must be set depending on the audio sample rate of either 44.1 kHz or 48 kHz based frequency.

For 44.1, 88.2 and 176.4 kHz, set *RAMP_RATE* bit high and for 48, 96 and 192 kHz, set this bit low. This ensures that the internal ramp generator has the appropriate slope.

8.4.2.11.2 Output Slew Rate Control

The output slew rate can be programmed using register bits *EDGE_CTRL[1:0]* form page 0x01, register 0x4C.

By default, if PVDD supply is below 20 V the output slew rate will be fast. If PVDD goes above 20 V the slew rate will be automatically change to slow.

Optionally, to improve EMI performance, is to set the slew rate to slow for the entire range of PVDD supply by setting the bits *EDGE_CTRL[1:0]* to 2'b11.

8.4.3 SAR ADC

A SAR ADC monitors PVDD voltage, VBAT1S voltage and die temperature. The results of these conversions are available via register readback (*PVDD_CNV[11:0]*, *VBAT1S_CNV[11:0]* and *TMP_CNV[7:0]* register bits). PVDD and VBAT1S voltage conversions are also used by the limiter and brown out prevention blocks.

By default, VBAT1S conversion is enabled along with PVDD and temperature in both cases, when BOP source is VBAT1S (*BOP_SRC*=0) or BOP source is PVDD (*BOP_SRC*=1). To disable VBAT1S conversion set the bit register *CONV_VBAT* to low.

The ADC runs at a fixed 192 kHz sample rate with a conversion time of 5.2 µs.

Sampling rate for temperature is 10K samples/sec.

PVDD and VBAT1S voltages and the die temperature are calculated using equations from Registers 0x52 to 0x56 of Page 0x00.

The register bits content should always be read from MSB to LSB.

8.4.4 Current and Voltage (IV) Sense

The TAS2780 provides speaker voltage and current sense measurements for real time monitoring of loudspeaker behavior. The VSNS_P and VSNS_N pins should be connected after any ferrite bead filter or directly to the OUT_P and OUT_N connections if no EMI filter is used. The V-Sense connections eliminate voltage drop error due to packaging, PCB interconnect or ferrite bead filter resistance. The V-sense connections are also used for Post Filter Feed-Back (Section 8.4.5) to correct for any voltage drop induced gain error or non-linearity due to the ferrite bead. It should be noted that any interconnect resistance after the VSNS terminals will not be corrected for, so it is advised to connect the VSNS pins as close to the load as possible.

The voltage and current sense ADCs have a DC blocking filter. This filter cut-off frequency can be adjusted, or the filter can be bypassed using the *HPF_FREQ_REC[2:0]* register bits.

I-Sense and V-Sense blocks can be powered up by programming to low the *ISNS_PD* and *VSNS_PD* register bits. When powered down, the device will return null samples for the powered down block.

8.4.5 Post Filter Feed-Back (PFFB)

The device supports post-filter feedback by closing the amplifier feedback loop after the external filter. The feedback is applied using the VSNS_N and VSNS_P terminals of the device. This feature can be disabled using the *PFFB_EN* register bit, for instance if an external filter that violates the amplifier loop stability is implemented. When PFFB is disabled, the feedback will be internally routed from the OUT_N and OUT_P pins of the device.

In the PFFB mode of operation the following conditions have to be met by the external filter: f_0 > 10 MHz and f_0/Q > 2.5 MHz (f_0 and Q are the cutoff frequency and the quality factor of the external filter).

8.4.6 Load Diagnostics

The TAS2780 can check the speaker terminal for open or short. This can be used to verify the continuity of the speaker or the traces to the speaker. The entire operation is performed by the TAS2780 and result is reported using the IRQZ pin or by reading over I^2C bus on completion. The load diagnostics can be performed using external audio clock (register bit *LDG_CLK=0*) or the internal oscillator (*LDG_CLK=1*).

The speaker open (upper - UT) and short (lower - LT) thresholds are configured using the *LDG_RES_UT[31:0]* and *LDG_RES_LT[31:0]* register bits. The diagnostic is run by selecting one of the load diagnostic modes set by *MODE[2:0]* register bits. The load diagnostic can be run before transitioning to active mode or stand-alone returning to software shutdown when complete. When the load diagnostics is run it will play a 22 kHz at -35 dBFS for 100 ms and measure the resistance of the speaker trace. The result is averaged over the time specified by the *LDG_AVG[1:0]* register bits. The measured speaker impedance can be read from *LDS_RES_VAL[31:0]* register bits.

8.4.7 Thermal Foldback

The TAS2780 monitors the die temperature and can automatically limit the audio signal when the die temperature reaches a set threshold. It is recommended to use the thermal fold-back registers to configure this protection mechanism as the internal DSP will perform the necessary calculation for each register.

Thermal fold-back can be disabled using *TFB_EN* register bit. If the die temperature reaches the value set by *TF_TEMP_TH[31:0]* register bits this feature will begin to attenuate the audio signal to prevent the device from shutting down due to over-temperature. It will attenuate the audio signal by a value set in *TF_LIMS[31:0]* register bits over a range of temperature set by *TF_TEMP_TH[31:0]* register bits. The thermal fold-back attack is at a fixed rate of 0.25dB/ms. A maximum attenuation can be specified using register bits *TF_MAX_ATTN[31:0]*. However, if the device continues to heat up, eventually the over-temperature will be triggered. The attenuation will be held for a number of samples set by register bits *TF_HOLD_CNT[31:0]*, before the attenuation will begin releasing.

8.4.8 Over Power Protection

The TAS2780 monitors the temperature of the internal power FETs. If the maximum continue power is high and power FETs temperature goes above a threshold, an internal protection circuit will trigger a thermal fold-back and, if temperature still increases, shutdown the device.

The protection mechanism is based on two thresholds TH1 and TH2. The TH1 threshold is set at a temperature 116^0C higher than the temperature measured by the internal bandgap but not less than 250^0C. The TH1 threshold triggers a thermal foldback.

The TH2 threshold is 40^0 C above TH1 and triggers thermal shutdown.

The two detection mechanisms can be disabled by setting bits *TG_TH2* and *TG_TH1* of register 0x47, page 0x01 to low.

8.4.9 Low Battery Protection

For VBAT1S supply below 3.4 V the power FETs can go into saturation at higher load currents which could result in device damage due to the FETs connected to PVDD going into thermal runaway.

To prevent the damage the OCP limit needs to be adjusted based on VBAT1S level measured by the internal SAR ADC. The table below presents the thresholds where the OCP will be adjusted and the settings of the registers to program these thresholds.

Once the VBAT1S supply is detected to a level below 3.4 V the device needs to be put in software shutdown or in idle mode before programming the registers.

Table 8-4. OCP Thresholds vs VBAT

VBAT1S Range	PVDD OCP Level	Book/Page/Register - New Setting
VBAT1S ≥ 3.4 V	6.6 A	NA
3.1 V ≤ VBAT1S < 3.4 V	6 A	B_0/P_0/R_6 - 01
2.9 V ≤ VBAT1S < 3.1 V	5.3 A	B_0/P_0/R_6 - 02
2.7 V ≤ VBAT1S < 2.9 V	4.3 A	B_0/P_FD/R_3A - 7D
		B_0/P_FD/R_3B - See Section 10.7
		B_0/P_FD/R_5C - C0

The control of OCP threshold from above is needed only in power modes where VBAT1S is supplied externaly and the Class-D outputs are switching on PVDD (PWR_MODE0, PWR_MODE1).

8.4.10 Clocks and PLL

The device clocking is derived from the SBCLK input clock. Table 8-5 and Table 8-6 show the valid SBCLK clock frequencies for each sample rate and SBCLK to FSYNC ratios.

Table 8-5. Supported SBCLK Frequencies (48 kHz based sample rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio						
	16	24	32	48	64	96	125
48 kHz	768 kHz	1.152 MHz	1.536 MHz	2.304 MHz	3.072 MHz	4.608 MHz	6 MHz
96 kHz	1.536 MHz	2.304 MHz	3.072 MHz	4.608 MHz	6.144 MHz	9.216 MHz	12 MHz
Sample Rate (kHz)	**SBCLK to FSYNC Ratio**						
	128	**192**	**250**	**256**	**384**	**500**	**512**
48 kHz	6.144 MHz	9.216 MHz	12 MHz	12.288 MHz	18.432 MHz	24 MHz	24.576 MHz
96 kHz	12.288 MHz	18.432 MHz	24 MHz	24.576 MHz	-	-	-

Table 8-6. Supported SBCLK Frequencies (44.1 kHz based sample rates)

Sample Rate (kHz)	SBCLK to FSYNC Ratio						
	16	24	32	48	64	96	125
44.1 kHz	705.6 kHz	1.0584 MHz	1.4112 MHz	2.1168 MHz	2.8224 MHz	4.2336 MHz	5.5125 MHz
88.2 kHz	1.4112 MHz	2.1168 MHz	2.8224 MHz	4.2336 MHz	5.6448 MHz	8.4672 MHz	11.025 MHz
Sample Rate (kHz)	**SBCLK to FSYNC Ratio**						
	128	**192**	**250**	**256**	**384**	**500**	**512**
44.1 kHz	5.6448 MHz	8.4672 MHz	11.025 MHz	11.2896 MHz	16.9344 MHz	22.05 MHz	22.5792 MHz
88.2 kHz	11.2896 MHz	16.9344 MHz	22.05 MHz	22.5792 MHz	-	-	-

If the sample rate is properly configured via the *SAMP_RATE[2:0]* register bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts. After the clock error is detected, the device will enter a low power halt mode after a time set by *CLK_HALT_TIMER[2:0]* register bits if *DIS_CLK_HALT* bit is low. Additionally, the device can automatically power up and down on valid clock signals if *CLK_PWR_UD_EN* register bit is set to high. The device sampling rate should not be changed while this feature is enabled. In this mode the *DIS_CLK_HALT* bit register should be set low in order for this feature to work properly.

8.4.11 Ultrasonic

The TAS2780 has a dedicated power mode (PWR_MODE3) to play ultasound in advanced ultrasonic applications like presence detection, gesture recognition, etc.

When playing ultrasound it is recommended to use settings from .

In PWR_MODE3 mode of operation the output stage of Class-D will be supplied by external VBAT1S rail.

8.4.12 Echo Reference

The TAS2780 can loop back the DSP output.

This feature allows user to do noise cancellation or echo correction algorithms.

A block diagram is presented in the figure below.

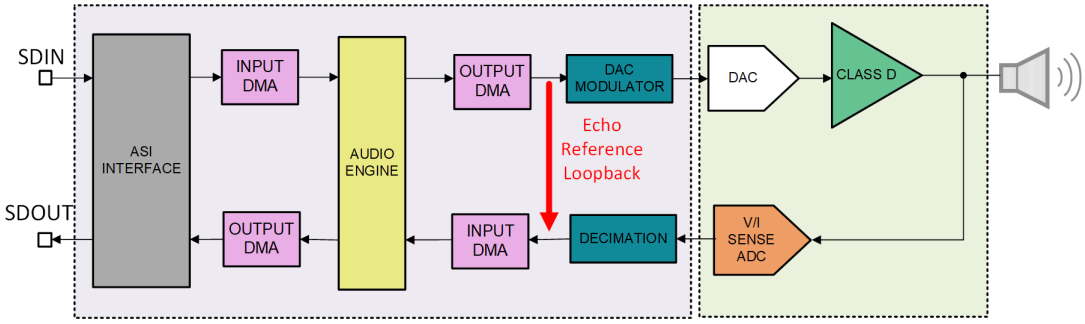


Figure 8-10. Echo Reference Loopback

The echo reference can be enabled by configuring *AUDIO_TX* register bit. The slot length and the time slot can be selected using *AUDIO_SLEN* and *AUDIO_SLOT[5:0]* register bits.

8.5 Operational Modes

8.5.1 Hardware Shutdown

The device enters Hardware Shutdown mode if the SDZ pin is asserted low. In Hardware Shutdown mode, the device consumes the minimum quiescent current from AVDD, IOVDD, PVDDPVDDH and VBAT1S supplies. All registers lose state in this mode and I^2C communication is disabled.

By default, when SDZ pin goes low, the device will force a hardware shutdown after a timeout set by the configurable shutdown timer (register bits SDZ_TIMEOUT[1:0]). If SDZ is asserted low while audio is playing, the device will ramp down volume of the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into Hardware Shutdown mode. The device can also be configured for forced hardware shutdown and in this case it will not attempt to gracefully disable the audio channel. The shutdown mode can be controlled using SDZ_MODE[1:0] register bits.

When SDZ is released, the device will sample the ADDR pin and enter the Software Shutdown mode.

8.5.2 Mode Control and Software Reset

The TAS2780 mode can be configured by writing the *MODE[2:0]* register bits.

A software reset can be accomplished by setting high the *SW_RESET* register bit. This bit is self clearing. Once enabled it will restore all registers to their default values.

8.5.3 Software Shutdown

Software Shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to lose register state.

The registers are available through I^2C interface.

Software Shutdown is enabled by asserting the *MODE[2:0]* register bits to 3'b010. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When de-asserted, the Class-D will begin switching and volume will ramp back to the programmed digital volume setting.

8.5.4 Mute Mode

The TAS2780 will ramp down volume of the Class-D amplifier to a mute state by setting the *MODE[2:0]* register bits to 3'b001. During mute the Class-D still switches but transmits no audio content. If mute is de-asserted, the device will ramp volume back to the programmed digital setting.

8.5.5 Active Mode

In Active Mode the Class-D switches and plays back audio. Speaker voltage and current sensing are operational if enabled. Set the *MODE[2:0]* register bits to 3'b000 to enter Active Mode.

8.5.6 Diagnostic Mode

The TAS2780 has a diagnostic generator that can be used without any PCM clocking to the device. If *DG_CLK* register bit is set low, an internal oscillator is used to generate the test patterns selected by *DG_SIG[4:0]* register bits. For sine-wave generation the sampling frequency f_s should be first set using the *SAMP_RATE[2:0]* register bits.

The programable DC level for diagnostic mode can be set using the *DG_DC_VAL[31:0]* register bits.

To play a DC diagnostic tone set the bits *HPF_FREQ_PB[2:0]* in register 0x04 to 0h (disabled DC blocker).

8.5.7 Noise Gate Mode

In this mode of operation described in section the TAS2780 monitors the signal and powers down the class-D when signal goes below a threshold.

8.6 Faults and Status

During the power-up sequence, the circuit monitoring the AVDD pin will hold the device in reset (including all configuration registers) until the supply is valid. The device will not exit hardware shutdown until AVDD is valid and the SDZ pin is released. Once SDZ is released, the digital core voltage regulator will power up, enabling detection of the operational mode. If AVDD dips below the under voltage threshold, the device will immediately be forced into a reset state.

The device also monitors the PVDD supply and holds the analog core in power down if the supply is below the PVDD under voltage threshold (set by register bits *PVDD_UVLO_TH[5:0]*). If the TAS2780 is in active operation and an under voltage fault occurs, the analog blocks will immediately be powered down to protect the device. These faults are latched and require a transition through Hardware or Software Shutdown to clear the fault. The latched registers will report under voltage faults.

The device transitions into Software Shutdown mode if it detects any faults with the TDM clocks such as:

- Invalid SBCLK to FSYNC ratio
- Invalid FSYNC frequency
- Halting of SBCLK or FSYNC clocks

Upon detection of a TDM clock error, the device transitions into Software Shutdown mode as quickly as possible to limit the possibility of audio artifacts. Once all TDM clock errors are resolved, the device volume ramps back to its previous playback state. During a TDM clock error, the IRQZ pin will assert low if the clock error interrupt mask register bit *IM_TDMCE* is set low. The clock fault is also available for read-back in the latched fault status register (bit *IR_TDMCE]*).

Note

It is mandatory to have TDM clocks available before programming I^2C to enter Active mode. Entering Active mode with no clocks present will trigger a clock error, device will go into Software Shutdown and the interrupts associated with the clock errors will be raised.

The TAS2780 also monitors die temperature and Class-D load current and will enter Software Shutdown mode if either of these exceed safe values. As with the TDM clock error, the IRQZ pin will assert low for these faults if the fault interrupt mask register bit is set low for over temperature and for over current. The fault status can also be monitored in the latched fault registers.

Die over temperature and Class-D over current errors can either be latching (for example, the device will enter Software Shutdown until a Hardware or Software Shutdown sequence is applied) or they can be programmed to automatically retry after a prescribed time. This behavior can be configured in the *OTE_RETRY, OCE_RETRY* register bits (for over temperature and over current respectively). Even in latched mode, the Class-D will not attempt to retry after an over temperature or over current error until the retry time period (1.5 s) has elapsed. This prevents applying repeated stress to the device in a rapid fashion that could lead to device damage. If the device has been cycled through a Hardware or Software Shutdown, it will only begin to operate after the retry time period.

By default all retry features are disabled.

When exiting Software Shutdown to Active mode (for example: *MODE[2:0]* bits from 010b to 000b), if PVDD under voltage is detected, the device will go back into Software Shutdown mode and an interrupt (*IL_PUVLO*) will be flagged. To exit this fault user needs to clear the interrupt and program the device in Software Shutdown using *MODE[2:0]* bits, before making another attempt to go to Active mode.

A similar situation might occur in PWR_MODE2, if internal VBAT1S LDO undervoltage is detected and *IL_LDO_UV* interrupt is flagged.

The status registers (and IRQZ pin, if enabled via the status mask register) also indicate limiter behavior including when the limiter is activated, when PVDD is below the inflection point, when maximum attenuation has been applied, when the limiter is in infinite hold and when the limiter has muted the audio.

In situations when the device operates in PWR_MODE2 the VBAT1S pin is supplied by an internal LDO. Protection circuits monitor this block and generate faults in case of under voltage, over voltage or if the LDO is over loaded. The device goes into Software Shutdown mode if one of these faults triggers.

The IRQZ pin is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal pull up resistor is provided and can be accessed (connected to the pin) by setting the *IRQZ_PU* register bit high.

The IRQZ interrupt configuration can be set using *IRQZ_PIN_CFG[1:0]* register bits. The *IRQZ_POL* register bit sets the interrupt polarity.

The *INT_LTCH_CLR* register bit allows to clear all the interrupt latch register bits.

Live flag registers are active only when the device is in Active mode of operation. If the device is shutdown by I^2C command or due to any fault condition described below, the live flags will be reset. Latched flags will not be reset in this condition and available for user to read their status.

Table 8-7. Fault Interrupt Mask

Interrupt	Live Register Bit	Latch Register Bit	Mask Register Bit	Default (1 = Mask)
Temp Over 105°C	IL_TO105	IR_TO105	IM_TO105	1
Temp Over 115°C	IL_TO115	IR_TO115	IM_TO115	1
Temp Over 125°C	IL_TO125	IR_TO125	IM_TO125	1
Temp Over 135°C	IL_TO135	IR_TO135	IM_TO135	1
Over Temp Error	Device in shutdown	IR_OT	IM_OT	0
Over Current Error	Device in shutdown	IR_OC	IM_OC	0
TDM Clock Error	Device in shutdown	IR_TDMCE	IM_TDMCE	1
TDM Clock Error: Invalid SBCLK ratio or FS rate		IR_TDMCEIR		
TDM Clock Error: FS changed on the fly		IR_TDNCEFC		
TDM Clock Error: SBCLK FS ratio changed on the fly		IR_TDMCERC		

Table 8-7. Fault Interrupt Mask (continued)

Interrupt	Live Register Bit	Latch Register Bit	Mask Register Bit	Default (1 = Mask)
BOP Active	IL_BOPA	IR_BOPA	IM_BOPA	0
BOP Level 0 Active	IL_BOPL0A	IR_BOPL0A	IM_BOPL0A	0
BOP Level 1 Active	IL_BOPL1A	IR_BOPL1A	IM_BOPL1A	0
BOP Level 2 Active	IL_BOPL2A	IR_BOPL2A	IM_BOPL2A	0
BOP Level 3 Active	IL_BOPL3A	IR_BOPL3A	IM_BOPL3A	0
BOP Infinite Hold	IL_BOPIH	IR_BOPIH	IM_BOPIH	1
BOP Mute	IL_BOPM	IR_BOPM	IM_BOPM	1
PVDD Below LImiter Inflection	IL_PBIP	IR_PBIP	IM_PBIP	1
Limiter Active	IL_LIMA	IR_LIMA	IM_LIMA	1
Limiter Max Atten	IL_LIMMA	IR_LIMMA	IM_LIMMA	1
PVDD UVLO	Device in shutdown	IR_PUVLO	IM_PUVLO	0
VBAT1S UVLO	Device in shutdown	IR_VBAT1S_UVLO	IM_VBAT1S_UVLO	0
OTP CRC Error	Device in shutdown	IR_OTPCRC		
VBAT Gain Limiter	IL_VBATLIM	IR_VBATLIM	IM_VBATLIM	1
Load Diagnostic Complete		IR_LDC	IM_LDC	1
Load Diagnostic Mode Fault		IR_LDMODE[1:0]	IM_LDMODE[1:0]	11
Internal PLL Clock Error	Device in shutdown	IR_PLL_CLK	IM_PLL_CLK	1
Noise Gate Active	IL_NGA			
PVDD-VBAT1S Below Threshold	IL_PVBT	IR_PVBT	IM_PVBT	0
Internal VBAT1S LDO Over Voltage	Device in shutdown	IR_LDO_OV	IM_LDO_OV	1
Internal VBAT1S LDO Under Voltage	Device in shutdown	IR_LDO_UV	IM_LDO_UV	0
Internal VBAT1S LDO Over Load	Device in shutdown	IR_LDO_OL	IM_LDO_OL	1
Thermal Detection Threshold 2	Device in shutdown	IR_TDTH2	IM_TDTH2	0
Thermal Detection Threshold 1	IL_TDTH1	IR_TDTH1	IM_TDTH1	0

8.6.1 Faults and Status Over TDM

Faults and device operation information can be sent over the TDM bus when *STATUS_TX* register bit is set high. The slot position in TDM bus can be configured using *STATUS_SLOT[5:0]* register bits.

Table 8-8. TDM Information Bits

TDM_STATUS[7:0] Bit	Bit Information	0 Value	1 Value
0	Power up state	Powered down(1)	Powered up
1	Y-Bridge	PVDD active	VBAT1S active
2	Noise-Gate Status	Normal operation	Noise gate active
3	Limiter Active	No Limiter or ICLA attn applied	Limiter or ICLA attn applied
4	BOP Active	No BOP attn applied	BOP attn applied
5	Over Temperature Error	No Over-temperature	Over-temperature detected(1)
6	Over Current Error	No Over-current	Over-current detected(1)
7	PVDD Status	No PVDD UVLO	PVDD UVLO detected(1)

(1) Can be read only during the transient shutdown phase. After shutdown the TDM bis are not available.

8.6.2 Temperature Warnings

The TAS2780 monitors the die temperature and flags warnings if the temperature is above 105 ºC, 115 ºC, 125 ºC and 135 ºC.

The warnings can be read live in Register 0x47 or latched in Register 0x4F, Page 0x00.

8.7 Power Sequencing Requirements

There are no power sequencing requirements for order of rate of ramping up or down as long as SDZ pin is kept low.

8.8 Digital Input Pull Downs

The I^2S/TDM interface pins and the ICC pin have optional weak pull down resistors to prevent the pins from floating. Register bits *DIN_PD[4:0]* are used to enable/disable pull downs. The pull downs are not enabled during Hardware Shutdown.

8.9 Register Map

8.9.1 Register Summary Table Page=0x00

Addr	Register	Description	Section
0x00	PAGE	Device Page	Section 8.9.6
0x01	SW_RESET	Software Reset	Section 8.9.7
0x02	MODE_CTRL	Device operational mode	Section 8.9.8
0x03	CHNL_0	Y Bridge and Channel settings	Section 8.9.9
0x04	DC_BLK0	SAR Filter and DC Path Blocker	Section 8.9.10
0x05	DC_BLK1	Record DC Blocker	Section 8.9.11
0x06	MISC_CFG1	Misc Configuration 1	Section 8.9.12
0x07	MISC_CFG2	Misc Configuration 2	Section 8.9.13
0x08	TDM_CFG0	TDM Configuration 0	Section 8.9.14
0x09	TDM_CFG1	TDM Configuration 1	Section 8.9.15
0x0A	TDM_CFG2	TDM Configuration 2	Section 8.9.16
0x0B	LIM_MAX_ATTN	Limiter	Section 8.9.17
0x0C	TDM_CFG3	TDM Configuration 3	Section 8.9.18
0x0D	TDM_CFG4	TDM Configuration 4	Section 8.9.19
0x0E	TDM_CFG5	TDM Configuration 5	Section 8.9.20
0x0F	TDM_CFG6	TDM Configuration 6	Section 8.9.21
0x10	TDM_CFG7	TDM Configuration 7	Section 8.9.22
0x11	TDM_CFG8	TDM Configuration 8	Section 8.9.23
0x12	TDM_CFG9	TDM Configuration 9	Section 8.9.24
0x13	TDM_CFG10	TDM Configuration 10	Section 8.9.25
0x14	TDM_CFG11	TDM Configuration 11	Section 8.9.26
0x15	ICC_CNFG2	ICC Mode	Section 8.9.27
0x16	TDM_CFG12	TDM Configuration 12	Section 8.9.28
0x17	ICLA_CFG0	Inter Chip Limiter Alignment 0	Section 8.9.29
0x18	ICLA_CFG1	Inter Chip Gain Alignment 1	Section 8.9.30
0x19	DG_0	Diagnostic Signal	Section 8.9.31
0x1A	DVC	Digital Volume Control	Section 8.9.32
0x1B	LIM_CFG0	Limiter Configuration 0	Section 8.9.33
0x1C	LIM_CFG1	Limiter Configuration 1	Section 8.9.34
0x1D	BOP_CFG0	Brown Out Prevention 0	Section 8.9.35
0x1E	BOP_CFG1	Brown Out Prevention 1	Section 8.9.36
0x1F	BOP_CFG2	Brown Out Prevention 2	Section 8.9.37
0x20	BOP_CFG3	Brown Out Prevention 3	Section 8.9.38
0x21	BOP_CFG4	Brown Out Prevention 4	Section 8.9.39

0x22	BOP_CFG5	BOP Configuration 5	Section 8.9.40
0x23	BOP_CFG6	Brown Out Prevention 6	Section 8.9.41
0x24	BOP_CFG7	Brown Out Prevention 7	Section 8.9.42
0x25	BOP_CFG8	Brown Out Prevention 8	Section 8.9.43
0x26	BOP_CFG9	Brown Out Prevention 9	Section 8.9.44
0x27	BOP_CFG10	BOP Configuration 10	Section 8.9.45
0x28	BOP_CFG11	Brown Out Prevention 11	Section 8.9.46
0x29	BOP_CFG12	Brown Out Prevention 12	Section 8.9.47
0x2A	BOP_CFG13	Brown Out Prevention 13	Section 8.9.48
0x2B	BOP_CFG14	Brown Out Prevention 14	Section 8.9.49
0x2C	BOP_CFG15	BOP Configuration 15	Section 8.9.50
0x2D	BOP_CFG17	Brown Out Prevention 17	Section 8.9.51
0x2E	BOP_CFG18	Brown Out Prevention 18	Section 8.9.52
0x2F	BOP_CFG19	Brown Out Prevention 19	Section 8.9.53
0x30	BOP_CFG20	Brown Out Prevention 20	Section 8.9.54
0x31	BOP_CFG21	BOP Configuration 21	Section 8.9.55
0x32	BOP_CFG22	Brown Out Prevention 22	Section 8.9.56
0x33	BOP_CFG23	Lowest PVDD Measured	Section 8.9.57
0x34	BOP_CFG24	Lowest BOP Attack Rate	Section 8.9.57
0x35	NG_CFG0	Noise Gate 0	Section 8.9.59
0x36	NG_CFG1	Noise Gate 1	Section 8.9.60
0x37	LVS_CFG0	Low Voltage Signaling	Section 8.9.61
0x38	DIN_PD	Digital Input Pin Pull Down	Section 8.9.62
0x3B	INT_MASK0	Interrupt Mask 0	Section 8.9.63
0x3C	INT_MASK1	Interrupt Mask 1	Section 8.9.64
0x3D	INT_MASK4	Interrupt Mask 4	Section 8.9.65
0x40	INT_MASK2	Interrupt Mask 2	Section 8.9.66
0x41	INT_MASK3	Interrupt Mask 3	Section 8.9.67
0x42	INT_LIVE0	Live Interrupt Read-back 0	Section 8.9.68
0x43	INT_LIVE1	Live Interrupt Read-back 1	Section 8.9.69
0x44	INT_LIVE1_0	Live Interrupt Read-back 1_0	Section 8.9.70
0x47	INT_LIVE2	Live Interrupt Read-back 2	Section 8.9.71
0x48	INT_LIVE3	Live Interrupt Read-back 3	Section 8.9.72
0x49	INT_LTCH0	Latched Interrupt Read-back 0	Section 8.9.73
0x4A	INT_LTCH1	Latched Interrupt Read-back 1	Section 8.9.74
0x4B	INT_LTCH1_0	Latched Interrupt Read-back 1_0	Section 8.9.75
0x4F	INT_LTCH2	Latched Interrupt Read-back 2	Section 8.9.76
0x50	INT_LTCH3	Latched Interrupt Read-back 3	Section 8.9.77
0x51	INT_LTCH4	Latched Interrupt Read-back 4	Section 8.9.78
0x52	VBAT_MSB	SAR VBAT1S 0	Section 8.9.79
0x53	VBAT_LSB	SAR VBAT1S 1	Section 8.9.80
0x54	PVDD_MSB	SAR PVDD 0	Section 8.9.81
0x55	PVDD_LSB	SAR PVDD 1	Section 8.9.82
0x56	TEMP	SAR ADC Conversion 2	Section 8.9.83
0x5C	INT_CLK_CFG	Clock Setting and IRQZ	Section 8.9.84
0x5D	MISC_CFG3	Misc Configuration 3	Section 8.9.85
0x60	CLOCK_CFG	Clock Configuration	Section 8.9.86
0x63	IDLE_IND	Idle channel current optimization	Section 8.9.87
0x64	SAR_SAMP	SAR Sampling Time	Section 8.9.88
0x65	MISC_CFG4	Misc Configuration 4	Section 8.9.89
0x67	TG_CFG0	Tone Generator	Section 8.9.90
0x68	CLK_CFG	Detect Clock Ration and Sample Rate	Section 8.9.91

0x6A	LV_EN_CFG	Class-D and LVS Delays	Section 8.9.92
0x6B	NG_CFG2	Noise Gate 2	Section 8.9.93
0x6C	NG_CFG3	Noise Gate 3	Section 8.9.94
0x6D	NG_CFG4	Noise Gate 4	Section 8.9.95
0x6E	NG_CFG5	Noise Gate 5	Section 8.9.96
0x6F	NG_CFG6	Noise Gate 6	Section 8.9.97
0x70	NG_CFG7	Noise Gate 7	Section 8.9.98
0x71	PVDD_UVLO	UVLO Threshold	Section 8.9.99
0x73	DMD	DAC Modulator Dither	Section 8.9.100
0x7E	I2C_CKSUM	I2C Checksum	Section 8.9.101
0x7F	BOOK	Device Book	Section 8.9.102

8.9.2 Register Summary Table Page=0x01

Addr	Register	Description	Section
0x17	INIT_0	Initialization	Section 8.9.103
0x19	LSR	Modulation	Section 8.9.104
0x21	INIT_1	Initialization	Section 8.9.105
0x35	INIT_2	Initialization	Section 8.9.106
0x36	INT_LDO	Internal LDO Setting	Section 8.9.107
0x3D	SDOUT_HIZ_1	Slots Control	Section 8.9.108
0x3E	SDOUT_HIZ_2	Slots Control	Section 8.9.109
0x3F	SDOUT_HIZ_3	Slots Control	Section 8.9.110
0x40	SDOUT_HIZ_4	Slots Control	Section 8.9.111
0x41	SDOUT_HIZ_5	Slots Control	Section 8.9.112
0x42	SDOUT_HIZ_6	Slots Control	Section 8.9.113
0x43	SDOUT_HIZ_7	Slots Control	Section 8.9.114
0x44	SDOUT_HIZ_8	Slots Control	Section 8.9.115
0x45	SDOUT_HIZ_9	Slots Control	Section 8.9.116
0x47	TG_EN	Thermal Detection Enable	Section 8.9.117
0x4C	EDGE_CTRL	Slew rate control	Section 8.9.118

8.9.3 Register Summary Table Page=0x04

Addr	Register	Description	Section
0x08	DG_DC_VAL1	Diagnostic DC Level	Section 8.9.119
0x09	DG_DC_VAL2	Diagnostic DC Level	Section 8.9.120
0x0A	DG_DC_VAL3	Diagnostic DC Level	Section 8.9.121
0x0B	DG_DC_VAL4	Diagnostic DC Level	Section 8.9.122
0x0C	LIM_TH_MAX1	Limiter Maximum Threshold	Section 8.9.123
0x0D	LIM_TH_MAX2	Limiter Maximum Threshold	Section 8.9.124
0x0E	LIM_TH_MAX3	Limiter Maximum Threshold	Section 8.9.125
0x0F	LIM_TH_MAX4	Limiter Maximum Threshold	Section 8.9.126
0x10	LIM_TH_MIN1	Limiter Minimum Threshold	Section 8.9.127
0x11	LIM_TH_MIN2	Limiter Minimum Threshold	Section 8.9.128
0x12	LIM_TH_MIN3	Limiter Minimum Threshold	Section 8.9.129
0x13	LIM_TH_MIN4	Limiter Minimum Threshold	Section 8.9.130
0x14	LIM_INF_PT1	Limiter Inflection Point	Section 8.9.131
0x15	LIM_INF_PT2	Limiter Inflection Point	Section 8.9.132
0x16	LIM_INF_PT3	Limiter Inflection Point	Section 8.9.133
0x17	LIM_INF_PT4	Limiter Inflection Point	Section 8.9.134
0x18	LIM_SLOPE1	Limiter Slope	Section 8.9.135
0x19	LIM_SLOPE2	Limiter Slope	Section 8.9.136

0x1A	LIM_SLOPE3	Limiter Slope	Section 8.9.137
0x1B	LIM_SLOPE4	Limiter Slope	Section 8.9.138
0x1C	TF_HLD1	TFB Maximum Hold	Section 8.9.139
0x1D	TF_HLD2	TFB Maximum Hold	Section 8.9.140
0x1E	TF_HLD3	TFB Maximum Hold	Section 8.9.141
0x1F	TF_HLD4	TFB Maximum Hold	Section 8.9.142
0x20	TF_RLS1	TFB Release Rate	Section 8.9.143
0x21	TF_RLS2	TFB Release Rate	Section 8.9.144
0x22	TF_RLS3	TFB Release Rate	Section 8.9.145
0x23	TF_RLS4	TFB Release Rate	Section 8.9.146
0x24	TF_SLOPE1	TFB Limiter Slope	Section 8.9.147
0x25	TF_SLOPE2	TFB Limiter Slope	Section 8.9.148
0x26	TF_SLOPE3	TFB Limiter Slope	Section 8.9.149
0x27	TF_SLOPE4	TFB Limiter Slope	Section 8.9.150
0x28	TF_TEMP_TH1	TFB Threshold	Section 8.9.151
0x29	TF_TEMP_TH2	TFB Threshold	Section 8.9.152
0x2A	TF_TEMP_TH3	TFB Threshold	Section 8.9.153
0x2B	TF_TEMP_TH4	TFB Threshold	Section 8.9.154
0x2C	TF_MAX_ATTN1	TFB Gain Reduction	Section 8.9.155
0x2D	TF_MAX_ATTN2	TFB Gain Reduction	Section 8.9.156
0x2E	TF_MAX_ATTN3	TFB Gain Reduction	Section 8.9.157
0x2F	TF_MAX_ATTN4	TFB Gain Reduction	Section 8.9.158
0x40	LD_CFG0	Load Diagnostics Resistance Upper Threshold	Section 8.9.159
0x41	LD_CFG1	Load Diagnostics Resistance Upper Threshold	Section 8.9.160
0x42	LD_CFG2	Load Diagnostics Resistance Upper Threshold	Section 8.9.161
0x43	LD_CFG3	Load Diagnostics Resistance Upper Threshold	Section 8.9.162
0x44	LD_CFG4	Load Diagnostics Resistance Lower Threshold	Section 8.9.163
0x45	LD_CFG5	Load Diagnostics Resistance Lower Threshold	Section 8.9.164
0x46	LD_CFG6	Load Diagnostics Resistance Lower Threshold	Section 8.9.165
0x47	LD_CFG7	Load Diagnostics Resistance Lower Threshold	Section 8.9.166
0x48	CLD_EFF_1	Class D Efficiency	Section 8.9.167
0x49	CLD_EFF_2	Class D Efficiency	Section 8.9.168
0x4A	CLD_EFF_3	Class D Efficiency	Section 8.9.169
0x4B	CLD_EFF_4	Class D Efficiency	Section 8.9.170
0x4C	LDG_RES1	Load Diagnostics Resistance Value	Section 8.9.171
0x4D	LDG_RES2	Load Diagnostics Resistance Value	Section 8.9.172
0x4E	LDG_RES3	Load Diagnostics Resistance Value	Section 8.9.173
0x4F	LDG_RES4	Load Diagnostics Resistance Value	Section 8.9.174

8.9.4 Register Summary Table Page=0xFD

Addr	Register	Description	Section
0x3E	INIT_3	Initialization	Section 8.9.175

8.9.5 Note and Legend

NOTE: all register bits described in italic font can be programmed in Active mode.

LEGEND: R/W = Read/Write, R = Read only; -n = Value after reset

8.9.6 PAGE (page=0x00 address=0x00) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	RW	0h	Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255

8.9.7 SW_RESET (page=0x00 address=0x01) [reset=00h]

Bit	Field	Type	Reset	Description
7-1	Reserved	R	0h	Reserved
0	*SW_RESET*	RW	0h	Software reset. Bit is self clearing. 0b = Do not reset 1b = Reset

8.9.8 MODE_CTRL (page=0x00 address=0x02) [reset=1Ah]

Bit	Field	Type	Reset	Description
7	BOP_SRC	RW	0h	BOP input source and PVDD UVLO 0b = VBAT1S input and PVDD UVLO disabled. 1b = PVDD input and PVDD UVLO enabled.
6-5	Reserved	RW	0h	Reserved
4	*ISNS_PD*	RW	1h	Current sense is 0b = Active 1b = Powered down
3	*VSNS_PD*	RW	1h	Voltage sense is 0b = Active 1b = Powered down
2-0	*MODE[2:0]*	RW	2h	Device operational mode. 000b = Active without Mute 001b = Active with Mute 010b = Software Shutdown 011b = Load Diagnostics followed by normal device power up 100b = Standalone Load Diagnostic, after completion these bits are self reset to 010b 101b = Diagnostic Generator Mode 110b -111b = Reserved

8.9.9 CHNL_0 (page=0x00 address=0x03) [reset=28h]

Bit	Field	Type	Reset	Description
7-6	CDS_MODE[1:0]	RW	0h	Class-D switching mode 00b = Y-Bridge, high power on VBAT1S 01b = VBAT1S Only Supply of Class D 10b = PVDD Only Supply of Class D 11b = Y-Bridge, low power on VBAT1S

Bit	Field	Type	Reset	Description		
5-1	*AMP_LEVEL[4:0]*	RW	14h	Setting	@48ksps	@96 ksps
				00h	11 dBV	9 dBV
				01h	11.5 dBV	9.5 dBV
				02h	12.0 dBV	10 dBV
				03h	12.5 dBV	10.5 dBV
				04h	13.0 dBV	11 dBV
				05h	13.5 dBV	11.5 dBV
				06h	14.0 dBV	12 dBV
				07h	14.5 dBV	12.5 dBV
				08h	15.0 dBV	13 dBV
				09h	15.5 dBV	13.5 dBV
				0Ah	16.0 dBV	14 dBV
				0Bh	16.5 dBV	14.5 dBV
				0Ch	17.0 dBV	15 dBV
				0Dh	17.5 dBV	15.5 dBV
				0Eh	18.0 dBV	16 dBV
				0Fh	18.5 dBV	16.5 dBV
				10h	19 dBV	17 dBV
				11h	19.5 dBV	17.5 dBV
				12h	20 dBV	18 dBV
				13h	20.5 dBV	18.5 dBV
				14h	21 dBV	19 dBV
				Others : Reserved		
0	Reserved	RW	0h	Reserved		

8.9.10 DC_BLK0 (page=0x00 address=0x04) [reset=21h]

Bit	Field	Type	Reset	Description
7	VBAT1S_MODE	RW	0h	VBAT1S supply 0b = Supplied externally 1b = Internally generated from PVDD
6	IRQZ_PU	RW	0h	IRQZ internal pull up enable. 0b = Disabled 1b = Enabled
5	AMP_SS **When Spread Spectrum and Sync Mode are both enabled, Sync Mode takes priority*	RW	1h	Low EMI spread spectrum is 0b = Disabled 1b = Enabled
4-3	Reserved	R	0h	Reserved
2-0	*HPF_FREQ_PB[2:0]*	RW	1h	Forward Path DC blocker 0h = Disabled (filter bypassed) 1h = 2 Hz 2h = 50 Hz 3h = 100 Hz 4h = 200 Hz 5h = 400 Hz 6h = 800 Hz 7h = Reserved * For 44.1/88.2 kHz sampling rates divide the values from above by 1.0884

8.9.11 DC_BLK1 (page=0x00 address=0x05) [reset=41h]

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	4h	Reserved
3	*TFB_EN*	RW	0h	Thermal Foldback is 0b = Disabled 1b = Enabled
2-0	*HPF_FREQ_REC[2:0]*	RW	1h	Record Path DC blocker 0h = Disabled (filter bypassed) 1h = 2 Hz 2h = 50 Hz 3h = 100 Hz 4h = 200 Hz 5h = 400 Hz 6h = 800 Hz 7h = Reserved * For 44.1/88.2 kHz sampling rates divide the values from above by 1.0884

8.9.12 MISC_CFG1 (page=0x00 address=0x06) [reset=00h]

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	0h	Reserved
5	OCE_RETRY	RW	0h	Retry after over current event. 0b = Disabled 1b = Enabled, retry after timer.
4	OTE_RETRY	RW	0h	Retry after over temperature event. 0b = Disabled 1b = Enabled, retry after timer.
3	PFFB_EN	RW	0h	Post-Filter Feedback is 0b = Disabled (uses OUT_N and OUT_P pins) 1b = Enabled (uses VSNS_N and VSNS_P pins)
2	*SMODE_EN*	RW	0h	When safe mode is enabled adds 18dB attenuation on channel gain. Safe mode is 0b = Disabled 1b = Enabled
1-0	*OC_CTRL[1:0]*	RW	0h	OC Threshold Control 0h = Nominal Value 1h = 10% below Nominal Value 2h = 20% below Nominal Value 3h = 30% below Nominal Value

8.9.13 MISC_CFG2 (page=0x00 address=0x07) [reset=20h]

Bit	Field	Type	Reset	Description
7-6	*SDZ_MODE[1:0]*	RW	0h	SDZ Mode configuration. 00b = Shutdown after timeout 01b = Immediate forced shutdown 10b - 11b = Reserved
5-4	*SDZ_TIMEOUT[1:0]*	RW	2h	SDZ Timeout value 00b = 2 ms 01b = 4 ms 10b = 6 ms 11b = 23.8 ms
3-2	DVC_RAMP_RATE[1:0]	RW	0h	Digital volume control ramp rate 00b = 0.5 dB per 1 sample 01b = 0.5 dB per 4 samples 10b = 0.5 dB per 8 samples 11b = Volume ramping disabled

Bit	Field	Type	Reset	Description
1	*I2C_GBL_EN*	RW	0h	I²C global address is 0b = Disabled 1b = Enabled
0	*I2C_AD_DET*	RW	0h	Re-detect I²C peripheral address (self clearing bit). 0b = Normal detection 1b = Re-detect address after power up

8.9.14 TDM_CFG0 (page=0x00 address=0x08) [reset=09h]

Bit	Field	Type	Reset	Description
7	AMP_INV	RW	0h	Invert audio amplifier ouput 0b = Normal 1b = Invert
6	CLASSD_SYNC **When Spread Spectrum and Sync Mode are both enabled, Sync Mode takes priority*	RW	0h	Class-D synchronization mode 0b = Not synchronized to audio clocks 1b = Synchronized to audio clocks
5	RAMP_RATE	RW	0h	Sample rate based on 44.1 kHz or 48 kHz when CLASSD_SYNC = 1 0b = 48 kHz 1b = 44.1 kHz
4	AUTO_RATE	RW	0h	Auto detection of TDM sample rate 0b = Enabled 1b = Disabled
3-1	SAMP_RATE[2:0]	RW	4h	Sample rate of the TDM bus 000b - 011b = Reserved 100b = 44.1/48 kHz 101b = 88.2/96 kHz 110b - 111b = Reserved
0	FRAME_START	RW	1h	TDM frame start polarity 0b = Low to High on FSYNC 1b = High to Low on FSYNC

8.9.15 TDM_CFG1 (page=0x00 address=0x09) [reset=02h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	RX_JUSTIFY	RW	0h	TDM RX sample justification within the time slot 0b = Left 1b = Right
5-1	RX_OFFSET[4:0]	RW	1h	TDM RX start of frame to time slot 0 offset - number of SBCLK cycles from transiton of FSYNC
0	RX_EDGE	RW	0h	TDM RX capture clock polarity 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK

8.9.16 TDM_CFG2 (page=0x00 address=0x0A) [reset=0Ah]

Bit	Field	Type	Reset	Description
7-6	IVMON_LEN[1:0]	RW	0h	Sets the current and voltage data to length of 00b = 16 bits 01b = 12 bits 10b = 8 bits 11b = Reserved
5-4	RX_SCFG[1:0]	RW	0h	TDM RX time slot select config 00b = Mono with time slot equal to I²C address offset 01b = Mono left channel 10b = Mono right channel 11b = Stereo downmix (L+R)/2

Bit	Field	Type	Reset	Description
3-2	RX_WLEN[1:0]	RW	2h	TDM RX word length 00b = 16 bits 01b = 20 bits 10b = 24 bits 11b = 32 bits
1-0	RX_SLEN[1:0]	RW	2h	TDM RX time slot length 00b = 16 bits 01b = 24 bits 10b = 32 bits 11b = Reserved

8.9.17 LIM_MAX_ATTN (page=0x00 address=0x0B) [reset=80h]

Bit	Field	Type	Reset	Description
7-4	LIM_MAX_ATTN[3:0]	RW	8h	Limiter Maximum Attenuation 0h = 1 dB 1h = 2 dB 2h = 3 dB ... 0Eh = 15 dB 0Fh = Reserved
3-0	Reserved	R	0h	Reserved

8.9.18 TDM_CFG3 (page=0x00 address=0x0C) [reset=10h]

Bit	Field	Type	Reset	Description
7-4	RX_SLOT_R[3:0]	RW	1h	TDM RX Right Channel Time Slot.
3-0	RX_SLOT_L[3:0]	RW	0h	TDM RX Left Channel Time Slot.

8.9.19 TDM_CFG4 (page=0x00 address=0x0D) [reset=13h]

Bit	Field	Type	Reset	Description
7	TX_KEEPCY	RW	0h	TDM and ICC TX SDOUT LSB data will be driven for full/half cycles when TX_KEEPEN is enabled 0b = Full-cycle 1b = Half-cycle
6	TX_KEEPLN	RW	0h	TDM and ICC TX SDOUT will hold the bus for the following when TX_KEEPEN is enabled 0b = 1 LSB cycle 1b = Always
5	TX_KEEPEN	RW	0h	TDM and ICC TX SDOUT bus keeper enable 0b = Disable bus keeper 1b = Enable bus keeper
4	TX_FILL	RW	1h	TDM and ICC TX SDOUT unused bit field fill 0b = Transmit 0 1b = Transmit Hi-Z
3-1	TX_OFFSET[2:0]	RW	1h	TDM TX start of frame to time slot 0 offset
0	TX_EDGE	RW	1h	TDM TX launch clock polarity 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK

8.9.20 TDM_CFG5 (page=0x00 address=0x0E) [reset=42h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	VSNS_TX	RW	1h	TDM TX voltage sense transmit 0b = Disabled 1b = Enabled

Bit	Field	Type	Reset	Description
5-0	VSNS_SLOT[5:0]	RW	2h	TDM TX voltage sense time slot

8.9.21 TDM_CFG6 (page=0x00 address=0x0F) [reset=40h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	ISNS_TX	RW	1h	TDM TX current sense transmit 0b = Disabled 1b = Enabled
5-0	ISNS_SLOT[5:0]	RW	0h	TDM TX current sense time slot

8.9.22 TDM_CFG7 (page=0x00 address=0x10) [reset=04h]

Bit	Field	Type	Reset	Description
7	VBAT1S_SLEN	RW	0h	TDM TX VBAT1S time slot length 0b = Truncate to 8 bits 1b = Left justify to 16 bits
6	VBAT1S_TX	RW	0h	TDM TX VBAT1S transmit 0b = Disabled 1b = Enabled
5-0	VBAT1S_SLOT[5:0]	RW	4h	TDM TX VBAT1S time slot

8.9.23 TDM_CFG8 (page=0x00 address=0x11) [reset=05h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	TEMP_TX	RW	0h	TDM TX temp sensor transmit 0b = Disabled 1b = Enabled
5-0	TEMP_SLOT[5:0]	RW	5h	TDM TX temp sensor time slot

8.9.24 TDM_CFG9 (page=0x00 address=0x12) [reset=06h]

Bit	Field	Type	Reset	Description
7	PVDD_SLEN	RW	0h	TDM TX PVDD time slot length 0b = Truncate to 8 bits 1b = Left justify to 16 bits
6	PVDD_TX	RW	0h	TDM TX PVDD transmit 0b = Disabled 1b = Enabled
5-0	PVDD_SLOT[5:0]	RW	6h	TDM TX PVDD time slot

8.9.25 TDM_CFG10 (page=0x00 address=0x13) [reset=08h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	STATUS_TX	RW	0h	TDM TX status transmit 0b = Disabled 1b = Enabled

Bit	Field	Type	Reset	Description
5-0	STATUS_SLOT[5:0]	RW	8h	TDM TX status time slot Status slot bit description: ***Bit7**- PVDD status(Cannot be read post analog blocks shutdown) 0b = PVDD UVLO not detected 1b = PVDD UVLO detected ***Bit6** -Over Current status(Cannot be read post analog blocks shutdown) 0b = No OC detected 1b = OC detected ***Bit5**- Over Temp status(Cannot be read post analog blocks shutdown) 0b = No OT detected 1b = OT detected ***Bit4**- BOP status 0b = BOP not detected 1b = BOP detected ***Bit3**- Signal distortion limiter status 0b = No distortion limiter or ICLA gain applied 1b = Gain attenuation done due to distortion limiter/ICLA ***Bit2**- Noise Gate status 0b = Device in normal mode 1b = Device in Noise Gate mode ***Bit1**- Class D Power Stage status 0b = Class D Power switch connected to PVDD 1b = Class D Power switch connected to VBAT1S ***Bit0**- Power Up state (Cannot be read post analog blocks shutdown) 0b = Device is powered down 1b = Device is in active state

8.9.26 TDM_CFG11 (page=0x00 address=0x14) [reset=0Ah]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	GAIN_TX	RW	0h	TDM/ICC TX limiter gain reduction transmit 0b = Disabled 1b = Enabled
5-0	GAIN_SLOT[5:0]	RW	Ah	TDM/ICC TX limiter gain reduction time slot

8.9.27 ICC_CNFG2 (page=0x00 address=0x15) [reset=00h]

Bit	Field	Type	Reset	Description
7-5	Reserved	R	0h	Reserved
4-2	ICC_MODE[2:0]	RW	0h	Selects ICC pin function 0h = Gain alignment on ICC pin 1h = Reserved 2h = ICC pin buffers disabled 3h = ICC pin is a general purpose input 4h = ICC pin is a general purpose output 5h - 7h = Reserved
1-0	Reserved	R	0h	Reserved

8.9.28 TDM_CFG12 (page=0x00 address=0x16) [reset=12h]

Bit	Field	Type	Reset	Description
7	AUDIO_SLEN	RW	0h	TDM audio slot length 0b = 16 bits 1b = 24 bits
6	AUDIO_TX	RW	0h	TDM audio output transmit 0b = Disabled 1b = Enabled
5-0	AUDIO_SLOT[5:0]	RW	12h	TDM TX status time slot

8.9.29 ICLA_CFG0 (page=0x00 address=0x17) [reset=0Ch]

Bit	Field	Type	Reset	Description
7	ICBA_EN	RW	0h	Inter chip brownout gain alignment 0b = Disabled 1b = Enabled
6-1	ICGA_SLOT[5:0]	RW	6h	Inter chip gain alignment starting time slot
0	ICLA_EN	RW	0h	Inter chip limiter alignment gain 0b = Disabled 1b = Enabled

8.9.30 ICLA_CFG1 (page=0x00 address=0x18) [reset=00h]

Bit	Field	Type	Reset	Description
7	ICGA_SEN[7]	RW	0h	Time slot equals ICGA_SLOT[5:0]+7*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
6	ICGA_SEN[6]	RW	0h	Time slot equals ICGA_SLOT[5:0]+6*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
5	ICGA_SEN[5]	RW	0h	Time slot equals ICGA_SLOT[5:0]+5*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
4	ICGA_SEN[4]	RW	0h	Time slot equals ICGA_SLOT[5:0]+4*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
3	ICGA_SEN[3]	RW	0h	Time slot equals ICGA_SLOT[5:0]+3*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
2	ICGA_SEN[2]	RW	0h	Time slot equals ICGA_SLOT[5:0]+2*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
1	ICGA_SEN[1]	RW	0h	Time slot equals ICGA_SLOT[5:0]+1*3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled
0	ICGA_SEN[0]	RW	0h	Time slot equals ICGA_SLOT[5:0]+0. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled

8.9.31 DG_0 (page=0x00 address=0x19) [reset=0Dh]

Bit	Field	Type	Reset	Description
7	ICGA_NG_EN	RW	0h	Recommended with ICGA feature when Noise gate is enabled 0b = Feature disabled 1b = Feature enabled
6	DG_CLK	RW	0h	Diagnostic generated clock source 0b = Internal osscilator 1b = External SBCLK and FSYNC
5	ICG_MODE	RW	0h	Device attenuation 0b = BOP and Limiter attenuation added together 1b = Max attenuation of either BOP or Limiter
4-0	*DG_SIG[4:0]*	RW	Dh	Selects Tone Freq for DG MODE 00h = Zero input (Idle channel) 01h = -6 dBFS positive DC 02h = -6 dBFS negative DC 03h = -12 dBFS positive DC 04h = -12 dBFS negative DC 05h = -18 dBFS positive DC 06h = -18 dBFS negative DC 07h = -24 dBFS positive DC 08h = -24 dBFS negative DC 09h = -30 dBFS positive DC 0Ah = -30 dBFS negative DC 0Bh = -6 dBFS $f_s/4$ 0Ch = -4.8 dBFS $f_s/6$ 0Dh = 0 dBFS 1 kHz sine 0Eh = Programmable DC using B0_P4, registers 0x08 to 0x0B 0Fh-1Fh = Reserved

8.9.32 DVC (page=0x00 address=0x1A) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	*DVC_LVL[7:0]*	RW	0h	Digital volume control 00h = 0 dB 01h = -0.5 dB 02h = -1 dB ... C8h = -100 dB Others : Mute

8.9.33 LIM_CFG0 (page=0x00 address=0x1B) [reset=62h]

Bit	Field	Type	Reset	Description
7 - 6	Reserved	R	1h	Reserved
5	LIM_HR_EN	RW	1h	Limiter dynamic headroom 0b = Disabled 1b = Enabled

Bit	Field	Type	Reset	Description
4-1	LIM_ATK_RT[3:0]	RW	1h	Limiter attack rate 00h = 20 µs/dB 01h = 40 µs/dB 02h = 80 µs/dB 03h = 160 µs/dB 04h = 320 µs/dB 05h = 640 µs/dB 06h = 1280 µs/dB 07h = 2560 µs/dB 08h = 5120 µs/dB 09h = 10240 µs/dB 10h = 20480 µs/dB 11h = 40960 µs/dB 12h = 81920 µs/dB 13h = 163840 µs/dB Others : Reserved
0	LIM_EN	RW	0h	Limiter is 0b = Disabled 1b = Enabled

8.9.34 LIM_CFG1 (page=0x00 address=0x1C) [reset=32h]

Bit	Field	Type	Reset	Description
7	LIM_PDB	RW	0h	During BOP the limiter will be 0b =Running 1b = Paused
6-3	LIM_RLS_RT[3:0]	RW	6h	Limter release rate 0h = Reserved 1h = 4 ms/dB 2h = 8 ms/dB 3h = 16 ms/dB 4h = 32 ms/dB 5h = 64 ms/dB 6h = 128 ms/dB 7h = 256 ms/dB 8h = 512 ms/dB 9h = 1024 ms/dB Ah = 2048 ms/dB Bh = 4096 ms/dB Ch = 8192 ms/dB Others : reserved
2-0	LIM_HLD_TM[2:0]	RW	2h	Limiter hold time 0h = Reserved 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms

8.9.35 BOP_CFG0 (page=0x00 address=0x1D) [reset=40h]

Bit	Field	Type	Reset	Description
7-3	LIM_DHR[4:0]	RW	8h	Limiter Maximum Headroom as % of PVDD 00h = -20 01h = -17.5 02h = -15 .. 0Fh = 17.5 10h = 20 Others = Reserved
2	Reserved	R	0h	Reserved

Bit	Field	Type	Reset	Description
1	BOP_SHDN	RW	0h	When BOP level 0 is reached device 0b = Attenuates based on level 0 setttings 1b = Mutes followed by device shutdown
0	BOP_EN	RW	0h	Brown out prevention 0b = Disabled 1b = Enabled

8.9.36 BOP_CFG1 (page=0x00 address=0x1E) [reset=32h]

Bit	Field	Type	Reset	Description
7	BOP_HLD_CLR	RW	0h	BOP infinite hold clear (self clearing) 0b = Do not clear 1b = Clear
6-0	DEV_MAX_ATTN[6:0]	RW	32h	Device maximum attenuation of limiter and BOP combined 00h = 0 dB 01h = -1 dB 02h = -2 dB 03h = -3 dB .. 2Eh = -46 dB 2Fh-7Fh = Disabled

8.9.37 BOP_CFG2 (page=0x00 address=0x1F) [reset=02h]

Bit	Field	Type	Reset	Description
7-5	BOP_DT3[2:0]	RW	0h	BOP level 3 dwell time 0h= 0 µs 1h = 100 µs 2h = 250 µs 3h = 500 µs 4h = 1000 µs 5h = 2000 µs 6h = 4000 µs 7h = 8000 µs
4-1	BOP_ATK_ST3[3:0]	RW	1h	BOP level 3 attack step size 0h = -0.0625 dB 1h = -0.5 dB 2h = -0.8958 dB 3h = -1.2916 dB 4h = -1.6874 dB 5h = -2.0832 dB 6h = -2.479 dB 7h = -2.8748 dB 8h = -3.2706 dB 9h = -3.6664 dB Ah = -4.0622 dB Bh = -4.458 dB Ch = -4.8538 dB Dh = -5.2496 dB Eh = -5.6454 dB Fh = -6 dB
0	Reserved	R	0h	Reserved

8.9.38 BOP_CFG3 (page=0x00 address=0x20) [reset=06h]

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT3[2:0]	RW	0h	BOP level 3 attack rate 0h= 2.5 µs 1h = 5 µs 2h = 10 µs 3h = 25 µs 4h = 50 µs 5h = 100 µs 6h = 250 µs 7h = 500 µs
4-1	BOP_RLS_ST3[3:0]	RW	3h	BOP level 3 release step size 0h = 0.0625 dB 1h = 0.5 dB 2h = 0.8958 dB 3h = 1.2916 dB 4h = 1.6874 dB 5h = 2.0832 dB 6h = 2.479 dB 7h = 2.8748 dB 8h = 3.2706 dB 9h = 3.6664 dB 0Ah = 4.0622 dB 0Bh = 4.458 dB 0Ch = 4.8538 dB 0Dh = 5.2496 dB 0Eh = 5.6454 dB 0Fh = 6 dB
0	Reserved	R	0h	Reserved

8.9.39 BOP_CFG4 (page=0x00 address=0x21) [reset=2Ch]

Bit	Field	Type	Reset	Description
7-5	BOP_RLS_RT3[2:0]	RW	1h	BOP level 3 release rate time 0h= 5 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
4-0	BOP_MAX_ATTN3[4:0]	RW	0Ch	BOP level 3 maximum attenuation 00h = 0 dB 01h = -1 dB 02h = -2 dB .. 0Ch = -12 dB .. 1Eh = -30 dB 1Fh = -31 dB

8.9.40 BOP_CFG5 (page=0x00 address=0x22) [reset=4Ch]

Bit	Field	Type	Reset	Description		
7-0	BOP_TH3[7:0]	RW	4Ch	BOP level 3 threshold (V)		
				Setting	BOP_SRC=0 (VBAT1S Source)	BOP_SRC=1 (PVDD Source)
				00h	2.7	5.5
				01h	2.75	5.55
				02h	2.8	5.6
				.....	.....	.....
				38h	5.5	8.3
				39h	Reserved	8.35
				.....	Reserved	.....
				5Ah	Reserved	10
				.....	Reserved	.....
				FDh	Reserved	18.15
				FEh	Reserved	18.2
				FFh	Reserved	18.25

8.9.41 BOP_CFG6 (page=0x00 address=0x23) [reset=20h]

Bit	Field	Type	Reset	Description
7-5	BOP_HT3[2:0]	RW	1h	BOP level 3 hold time 0h = 0 ms 1h = 10 ms 2h = 100 ms 3h = 250 ms 4h = 500ms 5h = 1000 ms 6h = 2000 ms 7h = Infinte (This can be exited using BOP_HLD_CLR bit)
4	BOP_DIS3	RW	0h	BOP level 3 0b = Enabled 1b = Disabled
3-0	BOP_STAT_STATE[3:0]	R	0h	BOP current state - set BOP_STAT_HLD bit high to hold update and valid readack 0h = Idle 1h = Attacking Level 3 2h = Attacking Level 2 3h = Attacking Level 1 4h = Attacking Level 0 5h = Holding Level 3 6h = Holding Level 2 7h = Holding Level1 8h = Holding Level 0 9h = Releasing Level 3 Ah = Releasing Level 2 Bh = Releasing Level 1 Ch = Releasing Level 0 Dh-Fh = Reserved

8.9.42 BOP_CFG7 (page=0x00 address=0x24) [reset=02h]

Bit	Field	Type	Reset	Description
7-5	BOP_DT2[2:0]	RW	0h	BOP level 2 dwell time 0h= 0 µs 1h = 100 µs 2h = 250 µs 3h = 500 µs 4h = 1000 µs 5h = 2000 µs 6h = 4000 µs 7h = 8000 µs
4-1	BOP_ATK_ST2[3:0]	RW	1h	BOP level 2 attack step size 0h = -0.0625 dB 1h = -0.5 dB 2h = -0.8958 dB 3h = -1.2916 dB 4h = -1.6874 dB 5h = -2.0832 dB 6h = -2.479 dB 7h = -2.8748 dB 8h = -3.2706 dB 9h = -3.6664 dB Ah = -4.0622 dB Bh = -4.458 dB Ch = -4.8538 dB Dh = -5.2496 dB Eh = -5.6454 dB Fh = -6 dB
0	Reserved	R	0h	Reserved

8.9.43 BOP_CFG8 (page=0x00 address=0x25) [reset=06h]

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT2[2:0]	RW	0h	BOP level 2 attack rate 0h= 2.5 µs 1h = 5 µs 2h = 10 µs 3h = 25 µs 4h = 50 µs 5h = 100 µs 6h = 250 µs 7h = 500 µs
4-1	BOP_RLS_ST2[3:0]	RW	3h	BOP level 2 release step size 0h = 0.0625 dB 1h = 0.5 dB 2h = 0.8958 dB 3h = 1.2916 dB 4h = 1.6874 dB 5h = 2.0832 dB 6h = 2.479 dB 7h = 2.8748 dB 8h = 3.2706 dB 9h = 3.6664 dB Ah = 4.0622 dB Bh = 4.458 dB Ch = 4.8538 dB Dh = 5.2496 dB Eh = 5.6454 dB Fh = 6 dB
0	Reserved	R	0h	Reserved

8.9.44 BOP_CFG9 (page=0x00 address=0x26) [reset=32h]

Bit	Field	Type	Reset	Description
7-5	BOP_RLS_RT2[2:0]	RW	1h	BOP level 2 release rate time 0h= 5 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
4-0	BOP_MAX_ATTN2[4:0]	RW	12h	BOP level 2 maximum attenuation 00h = 0 dB 01h = -1 dB 02h = -2 dB .. 12h = -18 dB .. 1Eh = -30 dB 1Fh = -31 dB

8.9.45 BOP_CFG10 (page=0x00 address=0x27) [reset=46h]

Bit	Field	Type	Reset	Description		
7-0	BOP_TH2[7:0]	RW	46h	BOP level 2 threshold (V)		
				Setting	BOP_SRC=0 (VBAT1S Source)	BOP_SRC=1 (PVDD Source)
				00h	2.7	5.5
				01h	2.75	5.55
				02h	2.8	5.6
				.....	.....	.....
				38h	5.5	8.3
				39h	Reserved	8.35
				.....	Reserved	.....
				5Ah	Reserved	10
				.....	Reserved	.....
				FDh	Reserved	18.15
				FEh	Reserved	18.2
				FFh	Reserved	18.25

8.9.46 BOP_CFG11 (page=0x00 address=0x28) [reset=20h]

Bit	Field	Type	Reset	Description
7-5	BOP_HT2[2:0]	RW	1h	BOP level 2 hold time 0h = 0 ms 1h = 10 ms 2h = 100 ms 3h = 250 ms 4h = 500ms 5h = 1000 ms 6h = 2000 ms 7h = Infinte (This can be exited using BOP_HLD_CLR bit)
4	BOP_DIS2	RW	0h	BOP level 2 0b = Enabled 1b = Disabled
3-0	Reserved	R	0h	Reserved

8.9.47 BOP_CFG12 (page=0x00 address=0x29) [reset=02h]

Bit	Field	Type	Reset	Description
7-5	BOP_DT1[2:0]	RW	0h	BOP level 1 dwell time 0h= 0 µs 1h = 100 µs 2h = 250 µs 3h = 500 µs 4h = 1000 µs 5h = 2000 µs 6h = 4000 µs 7h = 8000 µs
4-1	BOP_ATK_ST1[3:0]	RW	1h	BOP level 1 attack step size 0h = -0.0625 dB 1h = -0.5 dB 2h = -0.8958 dB 3h = -1.2916 dB 4h = -1.6874 dB 5h = -2.0832 dB 6h = -2.479 dB 7h = -2.8748 dB 8h = -3.2706 dB 9h = -3.6664 dB Ah = -4.0622 dB Bh = -4.458 dB Ch = -4.8538 dB Dh = -5.2496 dB Eh = -5.6454 dB Fh = -6 dB
0	Reserved	R	0h	Reserved

8.9.48 BOP_CFG13 (page=0x00 address=0x2A) [reset=06h]

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT1[2:0]	RW	0h	BOP level 1 attack rate 0h= 2.5 µs 1h = 5 µs 2h = 10 µs 3h = 25 µs 4h = 50 µs 5h = 100 µs 6h = 250 µs 7h = 500 µs
4-1	BOP_RLS_ST1[3:0]	RW	3h	BOP level 1 release step size 0h = 0.0625 dB 1h = 0.5 dB 2h = 0.8958 dB 3h = 1.2916 dB 4h = 1.6874 dB 5h = 2.0832 dB 6h = 2.479 dB 7h = 2.8748 dB 8h = 3.2706 dB 9h = 3.6664 dB Ah = 4.0622 dB Bh = 4.458 dB Ch = 4.8538 dB Dh = 5.2496 dB Eh = 5.6454 dB Fh = 6 dB
0	Reserved	R	0h	Reserved

8.9.49 BOP_CFG14 (page=0x00 address=0x2B) [reset=38h]

Bit	Field	Type	Reset	Description
7-5	BOP_RLS_RT1[2:0]	RW	1h	BOP level 1 release rate time 0h= 5 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
4-0	BOP_MAX_ATTN1[4:0]	RW	18h	BOP level 1 maximum attenuation 0h = 0 dB 1h = -1 dB 2h = -2 dB .. 18h = -24 dB .. 1Eh = -30 dB 1Fh = -31 dB

8.9.50 BOP_CFG15 (page=0x00 address=0x2C) [reset=40h]

Bit	Field	Type	Reset	Description		
7-0	BOP_TH1[7:0]	RW	40h	BOP level 1 threshold (V)		
				Setting	BOP_SRC=0 (VBAT1S Source)	BOP_SRC=1 (PVDD Source)
				00h	2.7	5.5
				01h	2.75	5.55
				02h	2.8	5.6
				.....	.....	.....
				38h	5.5	8.3
				39h	Reserved	8.35
				.....	Reserved	.....
				5Ah	Reserved	10
				.....	Reserved	.....
				FDh	Reserved	18.15
				FEh	Reserved	18.2
				FFh	Reserved	18.25

8.9.51 BOP_CFG17 (page=0x00 address=0x2D) [reset=20h]

Bit	Field	Type	Reset	Description
7-5	BOP_HT1[2:0]	RW	1h	BOP level 1 hold time 0h = 0 ms 1h = 10 ms 2h = 100 ms 3h = 250 ms 4h = 500ms 5h = 1000 ms 6h = 2000 ms 7h = Infinte (This can be exited using BOP_HLD_CLR bit)
4	BOP_DIS1	RW	0h	BOP level 1 0b = Enabled 1b = Disabled
3-0	Reserved	R	0h	Reserved

8.9.52 BOP_CFG18 (page=0x00 address=0x2E) [reset=02h]

Bit	Field	Type	Reset	Description
7-5	BOP_DT0[2:0]	RW	0h	BOP level 0 dwell time 0h= 0 µs 1h = 100 µs 2h = 250 µs 3h = 500 µs 4h = 1000 µs 5h = 2000 µs 6h = 4000 µs 7h = 8000 µs
4-1	BOP_ATK_ST0[3:0]	RW	1h	BOP level 0 attack step size 0h = -0.0625 dB 1h = -0.5 dB 2h = -0.8958 dB 3h = -1.2916 dB 4h = -1.6874 dB 5h = -2.0832 dB 6h = -2.479 dB 7h = -2.8748 dB 8h = -3.2706 dB 9h = -3.6664 dB Ah = -4.0622 dB Bh = -4.458 dB Ch = -4.8538 dB Dh = -5.2496 dB Eh = -5.6454 dB Fh = -6 dB
0	Reserved	R	0h	Reserved

8.9.53 BOP_CFG19 (page=0x00 address=0x2F) [reset=06h]

Bit	Field	Type	Reset	Description
7-5	BOP_ATK_RT0[2:0]	RW	0h	BOP level 0 attack rate 0h= 2.5 µs 1h = 5 µs 2h = 10 µs 3h = 25 µs 4h = 50 µs 5h = 100 µs 6h = 250 µs 7h = 500 µs
4-1	BOP_RLS_ST0[3:0]	RW	3h	BOP level 0 release step size 0h = 0.0625 dB 1h = 0.5 dB 2h = 0.8958 dB 3h = 1.2916 dB 4h = 1.6874 dB 5h = 2.0832 dB 6h = 2.479 dB 7h = 2.8748 dB 8h = 3.2706 dB 9h = 3.6664 dB Ah = 4.0622 dB Bh = 4.458 dB Ch = 4.8538 dB Dh = 5.2496 dB Eh = 5.6454 dB Fh = 6 dB
0	Reserved	R	0h	Reserved

8.9.54 BOP_CFG20 (page=0x00 address=0x30) [reset=3Eh]

Bit	Field	Type	Reset	Description
7-5	BOP_RLS_RT0[2:0]	RW	1h	BOP level 0 release rate time 0h= 5 ms 1h = 10 ms 2h = 25 ms 3h = 50 ms 4h = 100 ms 5h = 250 ms 6h = 500 ms 7h = 1000 ms
4-0	BOP_MAX_ATTN0[4:0]	RW	1Eh	BOP level 0 maximum attenuation. 0h = 0 dB 1h = -1 dB 2h = -2 dB .. Ch = -12 dB .. 1Eh = -30 dB 1Fh = -31 dB

8.9.55 BOP_CFG21 (page=0x00 address=0x31) [reset=37h]

Bit	Field	Type	Reset	Description		
7-0	BOP_TH0[7:0]	RW	37h	BOP level 0 threshold (V)		
				Setting	BOP_SRC=0 (VBAT1S Source)	BOP_SRC=1 (PVDD Source)
				00h	2.7	5.5
				01h	2.75	5.55
				02h	2.8	5.6
				.....	.....	.....
				38h	5.5	8.3
				39h	Reserved	8.35
				.....	Reserved	.....
				5Ah	Reserved	10
				.....	Reserved	.....
				FDh	Reserved	18.15
				FEh	Reserved	18.2
				FFh	Reserved	18.25

8.9.56 BOP_CFG22 (page=0x00 address=0x32) [reset=20h]

Bit	Field	Type	Reset	Description
7-5	BOP_HT0[2:0]	RW	1h	BOP level 0 hold time 0h = 0 ms 1h = 10 ms 2h = 100 ms 3h = 250 ms 4h = 500ms 5h = 1000 ms 6h = 2000 ms 7h = Infinte (This can be exited using BOP_HLD_CLR bit)
4	BOP_DIS0	RW	0h	BOP level 0 0b = Enabled 1b = Disabled
3-1	Reserved	RW	0h	Reserved

Bit	Field	Type	Reset	Description
0	BOP_STAT_HLD	RW	0h	Hold BOP status for BOP_STAT_STATE[3:0], BOP_STAT_LLVL[2:0], and BOP_STAT_PVDD[9:0] register bits. When this bit is set back to low the status registers will be reset and updating will resume. 0b= Hold update disabled, status register readback invalid 1b= Hold update enabled, status register readback valid

8.9.57 BOP_CFG23 (page=0x00 address=0x33) [reset=FFh]

Bit	Field	Type	Reset	Description
7-0	BOP_STAT_PVDD[9:2]	R	FFh	Lowest PVDD measured since last read. Set BOP_STAT_HLD high before reading.Till the time SAR does not get enabled in device, this register wll readback default value on PVDD (FFh) if device is in PWR_MODE2, else it will readback default value on VBAT (FFh) when device is in PWR_MODE1. Note: default value of PVDD is 23V and of VBAT1S is 6V.

8.9.58 BOP_CFG24 (page=0x00 address=0x34) [reset=E6h]

Bit	Field	Type	Reset	Description
7-6	BOP_STAT_PVDD[1:0]	R	3h	Lowest PVDD measured since last read. Set BOP_STAT_HLD high before reading.Till the time SAR does not get enabled in device, this register wll readback default value on PVDD (3h) if device is in PWR_MODE2, else it will readback default value on VBAT (3h) when device is in PWR_MODE1. Note: default value of PVDD is 23V and of VBAT1S is 6V.
5-3	BOP_STAT_LLVL[2:0]	R	4h	Lowest BOP level attacked since last read. Set BOP_STAT_HLD high before reading. 0h = Attack level 0 was lowest attack level 1h = Attack level 1 was lowest attack level 2h = Attack level 2 was lowest attack level 3h = Attack level 3 was lowest attack level 4h = No BOP attacked since last read 5h - 7h = Reserved
2-1	LVS_FTH_LOW[1:0]	RW	3h	Threshold for LVS when CDS_MODE = 3h 0h = -121.5 dBFS 1h= -101.5 dBFS (default) 2h= -81.5 dBFS 3h = -71.5 dBFS
0	Reserved	R	0h	Reserved

8.9.59 NG_CFG0 (page=0x00 address=0x35) [reset=BDh]

Bit	Field	Type	Reset	Description
7-5	NG_HYST[2:0]	RW	5h	Noise Gate entry hysteris timer 0h = 400 µs 1h = 600 µs 2h = 800 µs 3h = 2 ms 4h = 10 ms 5h = 50 ms 6h = 100 ms 7h = 1000 ms
4-3	NG_LVL[1:0]	RW	3h	Noise Gate audio threshold level 0h = -90 dBFS 1h= -100 dBFS 2h = -110 dBFS 3h = -120 dBFS
2	NG_EN	RW	1h	Noise Gate 0b = Disabled 1b= Enabled

Bit	Field	Type	Reset	Description
1-0	Reserved	RW	1h	Reserved

8.9.60 NG_CFG1 (page=0x00 address=0x36) [reset=ADh]

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	2h	Reserved
5	NG_DVR_EN	RW	1h	Volume ramping on Noise Gate control 0b = Enabled 1b = Disabled
4	Reserved	R	0h	Reserved
3-0	LVS_HYS[3:0]	RW	Dh	PVDD to VBAT1S hysteresis time 0h - 9h = Reserved Ah = 1 ms Bh = 10 ms Ch = 20 ms Dh = 50 ms Eh = 75 ms Fh = 100 ms

8.9.61 LVS_CFG0 (page=0x00 address=0x37) [reset=A8h]

Bit	Field	Type	Reset	Description
7	LVS_TMODE	RW	1h	Low Voltage Signaling detection threshold 0b = Fixed 1b = Relative to VBAT1S voltage
6	Reserved	RW	1h	Reserved
4-0	LVS_FTH[4:0]	RW	8h	Threshold for LVS when CDS_MODE = 0h 00h = -18.5 dBFS 01h = -18.25 dBFS (default) 02h = -18 dBFS 03h = -17.75 dBFS 04h = -17.5 dBFS .. 08h = -16.5 dBFS .. 1Eh = -11 dBFS 1Fh = -10.75 dBFS

8.9.62 DIN_PD (page=0x00 address=0x38) [reset=03h]

Bit	Field	Type	Reset	Description
7	Reserved	RW	0h	Reserved
6	DIN_PD[4]	RW	0h	Weak pull down for ICC 0b = Disabled 1b = Enabled
5	DIN_PD[3]	RW	0h	Weak pull down for SDOUT 0b = Disabled 1b = Enabled
4	DIN_PD[2]	RW	0h	Weak pull down for SDIN 0b = Disabled 1b = Enabled
3	DIN_PD[1]	RW	0h	Weak pull down for FSYNC 0b = Disabled 1b = Enabled
2	DIN_PD[0]	RW	0h	Weak pull down for SBCLK 0b = Disabled 1b = Enabled
1-0	Reserved	RW	3h	Reserved

8.9.63 INT_MASK0 (page=0x00 address=0x3B) [reset=FCh]

Bit	Field	Type	Reset	Description
7	*IM_BOPM*	RW	1h	BOP mute interrupt 0b = No Mask 1b = Mask
6	*IM_BOPIH*	RW	1h	Bop infinite hold interrupt. 0b = No Mask 1b = Mask
5	*IM_LIMMA*	RW	1h	Limiter max attenuation interrupt 0b = No Mask 1b = Mask
4	*IM_PBIP*	RW	1h	PVDD below limiter inflection point interrupt 0b = No Mask 1b = Mask
3	*IM_LIMA*	RW	1h	Limiter active interrupt 0b = No Mask 1b = Mask
2	*IM_TDMCE*	RW	1h	TDM clock error interrupt 0b = No Mask 1b = Mask
1	*IM_OC*	RW	0h	Over current error interrupt 0b = No Mask 1b = Mask
0	*IM_OT*	RW	0h	Over temp error interrupt 0b = No Mask 1b = Mask

8.9.64 INT_MASK1 (page=0x00 address=0x3C) [reset=BFh]

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	2h	Reserved
5	*IM_LDC*	RW	1h	Load diagnostic completion 0h = No Mask 1h = Mask
4-3	*IM_LDMODE[1:0]*	RW	3h	Speaker Load 0h = No Mask 1h = Mask Open Load Detection 2h = Mask Short Load Detection 3h = Mask Both
2-11	Reserved	RW	1h	Reserved
0	*IM_VBATLIM*	RW	1h	Gain limiter active interrupt 0h = No Mask 1h = Mask

8.9.65 INT_MASK4 (page=0x00 address=0x3D) [reset=DFh]

Bit	Field	Type	Reset	Description
7	*IM_PLL_CLK*	RW	1h	Internal PLL Derived Clock Error Mask 0h = No Mask 1h = Mask
6	Reserved	RW	1h	Reserved
5	*IM_VBAT1S_UVLO*	RW	0h	VBAT1S Under Voltage 0h = No Mask 1h = Mask
4-0	Reserved	RW	1Fh	Reserved

8.9.66 INT_MASK2 (page=0x00 address=0x40) [reset=F6h]

Bit	Field	Type	Reset	Description
7	*IM_TO105*	RW	1h	Temperature over 105 ºC interrupt. 0h = No Mask 1h = Mask
6	*IM_TO115*	RW	1h	Temperature over 115 ºC interrupt. 0h = No Mask 1h = Mask
5	*IM_TO125*	RW	1h	Temperature over 125 ºC interrupt. 0h = No Mask 1h = Mask
4	*IM_TO135*	RW	1h	Temperature over 135 ºC interrupt. 0h = No Mask 1h = Mask
3	*IM_LDO_UV*	RW	0h	Internal VBAT1S LDO Under Voltage 0h = No Mask 1h = Mask
2	*IM_LDO_OV*	RW	1h	Internal VBAT1S LDO Over Voltage 0h = No Mask 1h = Mask
1	*IM_LDO_OL*	RW	1h	Internal VBAT1S LDO Over Load 0h = No Mask 1h = Mask
0	*IM_PUVLO*	RW	0h	PVDD UVLO interrupt. 0h = No Mask 1h = Mask

8.9.67 INT_MASK3 (page=0x00 address=0x41) [reset=00h]

Bit	Field	Type	Reset	Description
7	*IM_TDTH2*	RW	0h	Thermal Detection threshold 2 0h = No Mask 1h = Mask
6	*IM_TDTH1*	RW	0h	Thermal Detection threshold 1 0h = No Mask 1h = Mask
5	*IM_PVBT*	RW	0h	PVDD - VBAT1S below threshold 0h = No Mask 1h = Mask
4	*IM_BOPA*	RW	0h	BOP active interrupt 0h = No mask 1h = Mask
3	*IM_BOPL3A*	RW	0h	BOP level 3 detected interrupt 0h = No Mask 1h = Mask
2	*IM_BOPL2A*	RW	0h	BOP level 2 detected interrupt 0h = No Mask 1h = Mask
1	*IM_BOPL1A*	RW	0h	BOP level 1 detected interrupt 0h = No Mask 1h = Mask
0	*IM_BOPL0A*	RW	0h	BOP level 0 detected interrupt 0h = No mask 1h = Mask

8.9.68 INT_LIVE0 (page=0x00 address=0x42) [reset=00h]

Bit	Field	Type	Reset	Description
7	IL_BOPM	R	0h	Interrupt due to bop mute 0h = No interrupt 1h = Interrupt
6	IL_BOPIH	R	0h	Interrupt due to bop infinite hold 0h = No interrupt 1h = Interrupt
5	IL_LIMMA	R	0h	Interrupt due to limiter max attenuation 0h = No interrupt 1h = Interrupt
4	IL_PBIP	R	0h	Interrupt due to PVDD below limiter inflection point 0h = No interrupt 1h = Interrupt
3	IL_LIMA	R	0h	Interrupt due to limiter active 0h = No interrupt 1h = Interrupt
2	IL_TDMCE	R	0h	Interrupt due to TDM clock error 0h = No interrupt 1h = Interrupt ***- Device in shutdown***
1	IL_OC	R	0h	Interrupt due to over current error 0h = No interrupt 1h = Interrupt ***- Device in shutdown***
0	IL_OT	R	0h	Interrupt due to over temp error 0h = No interrupt 1 = Interrupt ***- Device in shutdown***

8.9.69 INT_LIVE1 (page=0x00 address=0x43) [reset=00h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	IL_OTPCRC	R	0h	Interrupt due to OTP CRC Error Flag 0h = No interrupt 1h = Interrupt ***- Device in shutdown***
5-3	Reserved	R	0h	Reserved
2	IL_NGA	R	0h	Noise Gate active flag 0h = Noise Gate not detected 1h = Noise Gate detected
1	Reserved	R	0h	Reserved
0	IL_VBATLIM	R	0h	Gain Limiter 0h = No interuupt 1h = Interrupt

8.9.70 INT_LIVE1_0 (page=0x00 address=0x44) [reset=00h]

Bit	Field	Type	Reset	Description
7	IL_PLL_CLK	R	0h	Internal PLL Clock Error 0h = No interrupt 1h = Interrupt ***- Device in shutdown***
6	Reserved	R	0h	Reserved
5	IL_VBAT1S_UVLO	R	0h	VBAT1S Under Voltage 0h = No interrupt 1h = Interrupt ***- Device in shutdown***
4-0	Reserved	R	0h	Reserved

8.9.71 INT_LIVE2 (page=0x00 address=0x47) [reset=00h]

Bit	Field	Type	Reset	Description
7	IL_TO105	R	0h	Temperature over 105 ºC 0h = No Interrupt 1h = Interrupt
6	IL_TO115	R	0h	Temperature over 115 ºC 0h = No Interrupt 1h = Interrupt
5	IL_TO125	R	0h	Temperature over 125 ºC 0h = No Interrupt 1h = Interrupt
4	IL_TO135	R	0h	Temperature over 135 ºC 0h = No Interrupt 1h = Interrupt
3	IL_LDO_UV	R	0h	VBAT1S Internal LDO Under Voltage 0h = No Interrupt 1h = Interrupt ***- Device in shutdown***
2	IL_LDO_OV	R	0h	VBAT1S Internal LDO Over Voltage 0h = No Interrupt 1h = Interrupt ***- Device in shutdown***
1	IL_LDO_OL	R	0h	VBAT1S Internal LDO Over Load 0h = No Interrupt 1h = Interrupt ***- Device in shutdown***
0	IL_PUVLO	R	0h	PVDD UVLO 0h = No Interrupt 1h = Interrupt ***- Device in shutdown***

8.9.72 INT_LIVE3 (page=0x00 address=0x48) [reset=00h]

Bit	Field	Type	Reset	Description
7	IL_TDTH2	R	0h	Thermal Detection Threshold 2 active flag 0h = No interrupt 1h = Interrupt - ***Device in shutdown***
6	IL_TDTH1	R	0h	Thermal Detection Threshold 1 active flag 0h = No interrupt 1h = Interrupt
5	IL_PVBT	R	0h	PVDD -VBAT1S going below the threshold flag 0h = No interrupt 1h = Interrupt
4	IL_BOPA	R	0h	BOP active flag 0h = No interrupt 1h = Interrupt
3	IL_BOPL3A	R	0h	BOP level 3 detected flag 0h = No interrupt 1h = Interrupt
2	IL_BOPL2A	R	0h	BOP level 2 detected flag 0h = No interrupt 1h = Interrupt
1	IL_BOPL1A	R	0h	BOP level 1 detected flag 0h = No interrupt 1h = Interrupt
0	IL_BOPL0A	R	0h	BOP level 0 detected flag 0h = No interrupt 1h = Interrupt

8.9.73 INT_LTCH0 (page=0x00 address=0x49) [reset=00h]

Bit	Field	Type	Reset	Description
7	IR_BOPM	R	0h	Interrupt due to bop mute 0h = No interrupt 1h = Interrupt
6	IR_BOPIH	R	0h	Interrupt due to BOP infinite hold 0h = No interrupt 1h = Interrupt
5	IR_LIMMA	R	0h	Interrupt due to limiter max attenuation 0h = No interrupt 1h = Interrupt
4	IR_PBIP	R	0h	Interrupt due to PVDD below limiter inflection point 0h = No interrupt 1h = Interrupt
3	IR_LIMA	R	0h	Interrupt due to limiter active 0h = No interrupt 1h = Interrupt
2	IR_TDMCE	R	0h	Interrupt due to TDM clock error (type of clock error can be seen in INT_LTCH4 register) 0h = No interrupt 1h = Interrupt
1	IR_OC	R	0h	Interrupt due to over current error 0h = No interrupt 1h = Interrupt
0	IR_OT	R	0h	Interrupt due to over temp error 0h = No interrupt 1h = Interrupt

8.9.74 INT_LTCH1 (page=0x00 address=0x4A) [reset=00h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	IR_OTPCRC	R	0h	Interrupt due to OTP CRC error flag 0h = No interrupt 1h = Interrupt
5	IR_LDC	R	0h	Interrupt due to load diagnostic completion 0h = Not completed 1h = Completed
4-3	IR_LDMODE[1:0]	R	0h	Interrupt due to Load Diagnostic mode fault status 0h = Normal Load 1h = Open Load Detected 2h =Short Load Detected 3h =Reserved
2-1	Reserved	R	0h	Reserved
0	IR_VBATLIM	R	0h	Gain Limiter interrupt 0h = No interrupt 1h = Interrupt

8.9.75 INT_LTCH1_0 (page=0x00 address=0x4B) [reset=00h]

Bit	Field	Type	Reset	Description
7	IR_PLL_CLK	R	0h	Internal PLL Clock Error 0h = No interrupt 1h = Interrupt
6	Reserved	R	0h	Reserved
5	IR_VBAT1S_UVLO	R	0h	VBAT1S Under Voltage 0h = No interrupt 1h = Interrupt

Bit	Field	Type	Reset	Description
4-0	Reserved	R	0h	Reserved

8.9.76 INT_LTCH2 (page=0x00 address=0x4F) [reset=00h]

Bit	Field	Type	Reset	Description
7	IR_TO105	R	0h	Temperature over 105 ºC 0h = No Interrupt 1h = Interrupt
6	IR_TO115	R	0h	Temperature over 115 ºC 0h = No Interrupt 1h = Interrupt
5	IR_TO125	R	0h	Temperature over 125 ºC 0h = No Interrupt 1h = Interrupt
4	IR_TO135	R	0h	Temperature over 135 ºC 0h = No Interrupt 1h = Interrupt
3	IR_LDO_UV	R	0h	Internal VBAT1S LDO Under Voltage 0h = No Interrupt 1h = Interrupt
2	IR_LDO_OV	R	0h	Internal VBAT1S LDO Over Voltage 0h = No Interrupt 1h = Interrupt
1	IR_LDO_OL	R	0h	Internal VBAT1S LDO Over Load 0h = No Interrupt 1h = Interrupt
0	IR_PUVLO	R	0h	PVDD UVLO 0h = No Interrupt 1h = Interrupt

8.9.77 INT_LTCH3 (page=0x00 address=0x50) [reset=00h]

Bit	Field	Type	Reset	Description
7	IR_TDTH2	R	0h	Thermal Detection Threshold 2 0h = No interrupt 1h = Interrupt
6	IR_TDTH1	R	0h	Thermal Detection Threshold 1 0h = No interrupt 1h = Interrupt
5	IR_PVBT	R	0h	Interrupt due to PVDD-VBAT1S going below the threshold 0h = No interrupt 1h = Interrupt
4	IR_BOPA	R	0h	BOP active flag 0h = No interrupt 1h = Interrupt
3	IR_BOPL3A	R	0h	BOP level 3 detected 0h = No interrupt 1h = Interrupt
2	IR_BOPL2A	R	0h	BOP level 2 detected 0h = No interrupt 1h = Interrupt
1	IR_BOPL1A	R	0h	BOP level 1 detected 0h = No interrupt 1h = Interrupt
0	IR_BOPL0A	R	0h	BOP level 0 detected 0h = No interrupt 1h = Interrupt

8.9.78 INT_LTCH4 (page=0x00 address=0x51) [reset=00h]

Bit	Field	Type	Reset	Description
7-3	Reserved	R	0h	Reserved
2	IR_TDMCEIR	R	0h	TDM clock error type = Invalid SBCLK ratio or sampling rate 0b = Not detected during TDM clock error 1b = Detected during TDM clock error
1	IR_TDMCEFC	R	0h	TDM clock error type = Sampling rate changed on the fly 0b = Detected during TDM clock error 1b = Not detected during TDM clock error
0	IR_TDMCERC	R	0h	TDM clock error type = SBCLK ratio changed on the fly 0b = Not detected during TDM clock error 1b = Detected during TDM clock error

8.9.79 VBAT_MSB (page=0x00 address=0x52) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	VBAT1S_CNV[11:4]	R	0h	Returns SAR ADC VBAT1S conversion MSBs. {hex2dec(VBAT1S_CNV[11:0])}/128

8.9.80 VBAT_LSB (page=0x00 address=0x53) [reset=00h]

Bit	Field	Type	Reset	Description
7-4	VBAT1S_CNV[3:0]	R	0h	Returns SAR ADC VBAT1S conversion LSBs. {hex2dec(VBAT1S_CNV[11:0])}/128
3-0	Reserved	R	0h	Reserved

8.9.81 PVDD_MSB (page=0x00 address=0x54) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	PVDD_CNV[11:4]	R	0h	Returns SAR ADC PVDD conversion MSBs. {hex2dec(PVDD_CNV[11:0])}/64

8.9.82 PVDD_LSB (page=0x00 address=0x55) [reset=00h]

Bit	Field	Type	Reset	Description
7-4	PVDD_CNV[3:0]	R	0h	Returns SAR ADC PVDD conversion LSBs. {hex2dec(PVDD_CNV[11:0])}/64
3-0	Reserved	R	0h	Reserved

8.9.83 TEMP (page=0x00 address=0x56) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	TMP_CNV[7:0]	R	0h	Returns SAR ADC temp sensor conversion. {hex2dec(TMP_CNV[7:0])} - 95

8.9.84 INT_CLK_CFG (page=0x00 address=0x5C) [reset=19h]

Bit	Field	Type	Reset	Description
7	CLK_PWR_UD_EN	RW	0h	Clock based device power up/power down feature 0h = Disabled 1h = Enabled
6	DIS_CLK_HALT	RW	0h	Clock halt timer 0h = Enable clock halt detection, after clock error detected 1h = Disable clock halt detection, after clock error detected

Bit	Field	Type	Reset	Description
5-3	CLK_HALT_TIMER[2:0]	RW	3h	Clock halt timer values 0h = 820 µs 1h = 3.27 ms 2h = 26.21 ms 3h = 52.42 ms 4h = 104.85 ms 5h = 209.71 ms 6h = 419.43 ms 7h = 838.86 ms
2	INT_LTCH_CLR	RW	0h	Clear interrupt latch registers 0h = Don't clear 1h = Clear (self clearing bit)
1-0	IRQZ_PIN_CFG[1:0]	RW	1h	IRQZ interrupt configuration. IRQZ will assert 0h = On any unmasked live interrupts 1h = On any unmasked latched interrupts 2h = For 2 - 4 ms one time on any unmasked live interrupt event 3h = For 2 - 4 ms every 4 ms on any unmasked latched interrupts

8.9.85 MISC_CFG3 (page=0x00 address=0x5D) [reset=80h]

Bit	Field	Type	Reset	Description
7	IRQZ_POL	RW	1h	IRQZ pin polarity for interrupt 0h = Active high (IRQ) 1h = Active low (IRQZ)
6-4	Reserved	RW	0h	Reserved
3-2	YB_BOP_CTRL[1:0]	RW	0h	This register selects on which BOP level, Y-bridge and BYP_EN pad need to shift to PVDD when BOP_SRC=0 0h = shift to PVDD when BOP LVL0 is detected 1h = shift to PVDD when BOP LVL1 or LVL0 is detected 2h = shift to PVDD when BOP LVL2 or LVL1 or LVL0 is detected 3h = shift to PVDD when BOP LVL3 or LVL2 or LVL1 or LVL0 is detected
1-0	Reserved	RW	0h	Reserved

8.9.86 CLOCK_CFG (page=0x00 address=0x60) [reset=0Dh]

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0h	Reserved
5-2	SAMP_RATIO[3:0]	RW	3h	SBCLK to FSYNC ratio when AUTO_RATE = 1 (disabled) 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 0Bh = 125 0Ch = 250 0Dh = 500 0Eh - 0Fh = Reserved
1-0	Reserved	RW	1h	Reserved

8.9.87 IDLE_IND (page=0x00 address=0x63) [reset=48]

Bit	Field	Type	Reset	Description
7	IDLE_IND	RW	0h	Idle channel Class D output current optimization 0h = Used for inductors 15 µH and higher 1h = Used for 5 µH inductors
6-0	Reserved	RW	48h	Reserved

8.9.88 SAR_SAMP (page=0x00 address=0x64) [reset=84h]

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	2h	Reseved
5-4	SAR_SAMP_TIME[1:0]	RW	0h	Sampling time and ADC filter frequency 0h = 1.3 µs, filter disabled 1h = 4.1 µs, 300 kHz 2h = 12.1 µs, 150 KHz 3h = 24.2 µs, 50 KHz
3-0	Reserved	RW	4h	Reserved

8.9.89 MISC_CFG4 (page=0x00 address=0x65) [reset=08]

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	0h	Reserved
3	LDG_CLK	RW	1h	Clock source for load diagnostic 0h = External TDM 1h = Internal oscillator
2-1	LDG_AVG[1:0]	RW	0h	Duration of averaging on V/I data 0h = 5 ms 1h = 10 ms 2h = 50 ms 3h =100 ms
0	Reserved	RW	0h	Reserved

8.9.90 IDLE_CFG (page=0x00 address=0x67) [reset=00h]

Bit	Field	Type	Reset	Description
7-2	Reserved	R	00h	Reserved
1-0	ID_CH_HYST_TIME[1:0]	RW	0h	Idle channel hysteresis timer. 0h = 50 ms 1h = 100 ms 2h = 200 ms 3h = 1000 ms

8.9.91 CLK_CFG (page=0x00 address=0x68) [reset=7Fh]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved

Bit	Field	Type	Reset	Description
6-3	FS_RATIO[3:0]	R	Fh	Detected SBCLK to FSYNC ratio. 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 0Bh = 125 0Ch = 250 0Dh = 500 0Eh = Reserved 0F = Invalid ratio
2-0	FS_RATE[2:0]	R	7h	Detected sample rate of TDM bus. 0h - 3h = Reserved 4h = 44.1/48 kHz 5h = 88.2/96 kHz 6h = Reserved 7h = Error condition

8.9.92 LV_EN_CFG (page=0x00 address=0x6A) [reset=12h]

Bit	Field	Type	Reset	Description
7-6	CDS_DLY[1:0]	RW	0h	Delay ($1/f_s$) of the Class-D Y-bridge switching with respect to the input signal 0h = 8.1(NG enabled,48ksps), 6.1(NG disabled,48ksps) 0h = 12.6(NG enabled,96ksps), 9.6(NG disabled,96ksps) 1h = 7.1(NG enabled,48ksps), 5.1(NG disabled,48ksps), 1h = 10.6(NG enabled,96ksps), 7.6(NG disabled,96ksps) 2h = 6.1(NG enabled,48ksps), 4.1(NG disabled,48ksps) 2h = 8.5(NG enabled,96ksps), 5.6(NG disabled,96ksps) 3h = 5.6(NG enabled,48ksps), 3.6(NG disabled,48ksps 3h = 7.6(NG enabled,96ksps), 4.6(NG disabled,96ksps)
5-4	LVS_DLY[1:0]	RW	1h	Delay ($1/f_s$) of the BYP_EN signaling with respect to the input signal 0h = 7.8(NG enabled,48ksps), 5.8(NG disabled,48ksps) 0h = 12.1(NG enabled,96ksps), 9.1(NG disabled,96ksps) 1h = 6.8(NG enabled,48ksps), 4.8(NG disabled,48ksps), 1h = 10.1(NG enabled,96ksps), 7.1(NG disabled,96ksps) 2h = 5.8(NG enabled,48ksps), 3.8(NG disabled,48ksps) 2h = 8.1(NG enabled,96ksps), 5.1(NG disabled,96ksps) 3h = 5.1(NG enabled,48ksps), 3.1(NG disabled,48ksps 3h = 6.6(NG enabled,96ksps), 3.6(NG disabled,96ksps)
3-0	LVS_RTH[3:0]	RW	2h	Relative threshold for Low Voltage Signaling (LVS). The headroom is from VBAT1S supply. 0h = 0.5 V 1h = 0.6 V 2h = 0.7 V ... Eh = 1.9 V Fh = 2 V

8.9.93 NG_CFG2 (page=0x00 address=0x6B) [reset=43h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0h	Reserved
6	CONV_VBAT	RW	1h	Convert the VBAT1S when BOP source is PVDD 0h = No VBAT1S conversion 1h = VBAT1S conversion is performed by SAR

Bit	Field	Type	Reset	Description
5-3	Reserved	RW	0h	Reserved
2	NGFR_EN	RW	0h	Noise Gate fine resolution register mode 0h = Disabled 1h = Enabled
1-0	Reserved	RW	3h	Reserved

8.9.94 NG_CFG3 (page=0x00 address=0x6C) [reset=00h]

Programmable bits for Noise Gate fine resolution threshold to a level **NGLVL**(dBFS); default is -110dBFS.

Bit	Field	Type	Reset	Description
7-0	NGFR_LVL[23:16]	RW	00h	dec2hex{round{ 10^(**NGLVL**/20)]*2^23}

8.9.95 NG_CFG4 (page=0x00 address=0x6D) [reset=00h]

Programmable bits for Noise Gate fine resolution threshold to a level **NGLVL**(dBFS); default is -110dBFS.

Bit	Field	Type	Reset	Description
7-0	NGFR_LVL[15:8]	RW	00h	dec2hex{round{ 10^(**NGLVL**/20)]*2^23}

8.9.96 NG_CFG5 (page=0x00 address=0x6E) [reset=1Ah]

Programmable bits for Noise Gate fine resolution threshold to a level **NGLVL**(dBFS); default is -110dBFS.

Bit	Field	Type	Reset	Description
7-0	NGFR_LVL[7:0]	RW	1Ah	dec2hex{round{ 10^(**NGLVL**/20)]*2^23}

8.9.97 NG_CFG6 (page=0x00 address=0x6F) [reset=00h]

Programmable bits for Noise Gate fine resolution hysteresis to a value **NGHYS**(ms).

Recommended to be set above 1ms.

Bit	Field	Type	Reset	Description
7-0	NGFR_HYST[18:11]	RW	0h	dec2bin[(**NGHYS***f_s),19] f_s=sampling rate in kHz

8.9.98 NG_CFG7 (page=0x00 address=0x70) [reset=96h]

Programmable bits for Noise Gate fine resolution hysteresis to a value **NGHYS**(ms).

Recommended to be set above 1ms.

Bit	Field	Type	Reset	Description
7-0	NGFR_HYST[10:3]	RW	96h	dec2bin[(**NGHYS***f_s),19] f_s=sampling rate in kHz

Example:

NGFR_HYST[15:0] is the result of 19 bits processing with last three bits thrown away (000)

For 50 ms and 48ksps formula is:

*dec2bin[50*48,19]=dec2bin[2400,19]=0000000100101100**000*** (5)

Result: 01h in register 0x6F and 2Ch in register 0x70.

8.9.99 PVDD_UVLO (page=0x00 address=0x71) [reset=02h]

When Y bridge is used (eg. PWR_MODE1) PVDD UVLO threshold needs to be set 2.5 V above VBAT1S level.

Bit	Field	Type	Reset	Description
7-6	Reserved	RW	0h	Reserved
5-0	PVDD_UVLO_TH[5:0]	RW	02h	PVDD UVLO threshold 00h = 1.753 V 01h = 2.09 V 02h = 2.428 V ..... 3Fh = 23 V

8.9.100 DMD (page=0x00 address=0x73) [reset=00h]

Bit	Field	Type	Reset	Description
7-6	DEM_CTRL[1:0]	R	0h	DAC MSB and LSB DEM enable/disable control 0h = MSB Enabled, LSB = Enabled 1h = MSB Enabled, LSB = Disabled 2h = MSB Disabled, LSB = Enabled 3h = MSB Disabled, LSB = Disabled - *Recommended for ultrasonic use case*
5	DIS_DITH	RW	0h	DAC MSB modulator dither control 0h = Enabled 1h = Disabled - *Recommended for ultrasonic use case*
4-0	Reserved	R	00	Reserved

8.9.101 I2C_CKSUM (page=0x00 address=0x7E) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	RW	0h	Returns I^2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages.

8.9.102 BOOK (page=0x00 address=0x7F) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	BOOK[7:0]	RW	0h	Sets the device book. 00h = Book 0 01h = Book 1 ... FFh = Book 255

8.9.103 INIT_0 (page=0x01 address=0x17) [reset=D0h]

Bit	Field	Type	Reset	Description
7-5	Reserved	RW	6h	Reserved
4	CMP_HYST_LP	RW	1h	Class D comparator dependancy of low power 0h = Disabled 1h = Enabled
3	SAR_IDLE	RW	0h	Idle channel interraction to SAR 0h = Enabled 1h = Disabled
2-0	Reserved	RW	0h	Reserved

8.9.104 LSR (page=0x01 address=0x19) [reset=40h]

Bit	Field	Type	Reset	Description
7	Reserved	R	0b	Reserved
6	EN_LLSR	RW	1h	Modulation 0h = LSR 1h = Linear LSR

Bit	Field	Type	Reset	Description
5-0	Reserved	R	00h	Reserved

8.9.105 INIT_1 (page=0x01 address=0x21) [reset=08h]

Bit	Field	Type	Reset	Description
7-4	Reserved	R	0h	Reserved
3	HSCMP_EN	RW	0h	Class D comparator voltage hysterisis 0h = Enabled 1h = Disabled
2-0	Reserved	R	0h	Reserved

8.9.106 INIT_2 (page=0x01 address=0x35) [reset=75h]

Bit	Field	Type	Reset	Description
7-4	Reserved	R	7h	Reserved
3-0	BIAS_NOISE	RW	5h	Settings for noise improvement

8.9.107 INT_LDO (page=0x01 address=0x36) [reset=08h]

Bit	Field	Type	Reset	Description
7-6	INT_LDO_SET[1:0]	RW	0h	Internal LDO Setting 0h = Setting done through register 04h of page 0x00h 1h = Force external supply, VBAT1S LDO is disabled 2h = Force internal LDO to be used 3h = Reserved
5-0	Reserved	R	08h	Reserved

8.9.108 SDOUT_HIZ_1 (page=0x01 address=0x3D) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ1[7:0]	RW	00h	Force '0' output control for slots 7 down to 0. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.109 SDOUT_HIZ_2 (page=0x01 address=0x3E) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ2[7:0]	RW	00h	Force '0' output control for slots 15 down to 8. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.110 SDOUT_HIZ_3 (page=0x01 address=0x3F) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ3[7:0]	RW	00h	Force '0' output control for slots 23 down to 16. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.111 SDOUT_HIZ_4 (page=0x01 address=0x40) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ4[7:0]	RW	00h	Force '0' output control for slots 31 down to 24. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.112 SDOUT_HIZ_5 (page=0x01 address=0x41) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ5[7:0]	RW	00h	Force '0' output control for slots 39 down to 32. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.113 SDOUT_HIZ_6 (page=0x01 address=0x42) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ6[7:0]	RW	00h	Force '0' output control for slots 47 down to 40. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.114 SDOUT_HIZ_7 (page=0x01 address=0x43) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ7[7:0]	RW	00h	Force '0' output control for slots 55 down to 48. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.115 SDOUT_HIZ_8 (page=0x01 address=0x44) [reset=00h]

Bit	Field	Type	Reset	Description
7-0	SDOUT_HIZ8[7:0]	RW	00h	Force '0' output control for slots 63 down to 56. This register to be programmed to zero in case the slot is not valid as per SBLK to FSYNC ratio.

8.9.116 SDOUT_HIZ_9 (page=0x01 address=0x45) [reset=00h]

Bit	Field	Type	Reset	Description
7	SDOUT_FORCE_0_CNT_EN	RW	0h	Control over sending "0" to un-used slots 0h = All unused slots will have 'Hi-Z' transmitted 1h = Unused slots can transmit '0' base on programming in registers 0x3D to 0x44 of Page 0x01
6-0	Reserved	RW	00h	Reserved

8.9.117 TG_EN (page=0x01 address=0x47) [reset=AB]

Bit	Field	Type	Reset	Description
7-2	Reserved	R	2Ah	Reserved
1	TG_TH2	RW	1h	Thermal threshold 2 0h = Disabled 1h = Enabled
0	TG_TH1	RW	1h	Thermal threshold 1 0h = Disabled 1h = Enabled

8.9.118 EDGE_CTRL (page=0x01 address=0x4C) [reset=00h]

Bit	Field	Type	Reset	Description
7-3	Reserved		0h	Reserved
2-1	EDGE_CTRL[1:0]	RW	0h	Output slew rate 00b = Auto adjust slew rate based on PVDD range 01b = Reserved 10b = Reserved 11b = Slow slew rate for full range of PVDD
0	Reserved	RW	0h	Reserved

8.9.119 DG_DC_VAL1 (page=0x04 address=0x08) [reset=40h]

Programmable DG bits for a **DC_VAL**(dBFS) desired level.

Bit	Field	Type	Reset	Description
7-0	DG_DC_VAL [31:24]	RW	40h	dec2hex{256*round[10^(**DC_VAL**/20)*2^23]}

8.9.120 DG_DC_VAL2 (page=0x04 address=0x09) [reset=26h]

Programmable DG bits for a **DC_VAL**(dBFS) desired level.

Bit	Field	Type	Reset	Description
7-0	DG_DC_VAL [23:16]	RW	26h	dec2hex{256*round[10^(**DC_VAL**/20)*2^23]}

8.9.121 DG_DC_VAL3 (page=0x04 address=0x0A) [reset=40h]

Programmable DG bits for a **DC_VAL**(dBFS) desired level.

Bit	Field	Type	Reset	Description
7-0	DG_DC_VAL [15:8]	RW	40h	dec2hex{256*round[10^(**DC_VAL**/20)*2^23]}

8.9.122 DC_DG_VAL4 (page=0x04 address=0x0B) [reset=00h]

Programmable DG bits for a **DC_VAL**(dBFS) desired level.

Bit	Field	Type	Reset	Description
7-0	DG_DC_VAL [7:0]	RW	00h	dec2hex{256*round[10^(**DC_VAL**/20)*2^23]}

8.9.123 LIM_TH_MAX1 (page=0x04 address=0x0C) [reset=68h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MAX**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MAX[31:24]	RW	68h	dec2hex{256*round [**LIM_TH_MAX***2^18]}

8.9.124 LIM_TH_MAX2 (page=0x04 address=0x0D) [reset=00h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MAX**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MAX[23:16]	RW	00h	dec2hex{256*round [**LIM_TH_MAX***2^18]}

8.9.125 LIM_TH_MAX3 (page=0x04 address=0x0E) [reset=00h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MAX**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MAX[15:8]	RW	00h	dec2hex{256*round [**LIM_TH_MAX***2^18]}

8.9.126 LIM_TH_MAX4 (page=0x04 address=0x0F) [reset=00h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MAX**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MAX[7:0]	RW	00h	dec2hex{256*round [**LIM_TH_MAX***2^18]}

8.9.127 LIM_TH_MIN1 (page=0x04 address=0x10) [reset=28h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MIN**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MIN[31:24]	RW	28h	dec2hex{256*round [**LIM_TH_MIN***2^18]}

8.9.128 LIM_TH_MIN2 (page=0x04 address=0x11) [reset=00h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MIN**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MIN[23:16]	RW	00h	dec2hex{256*round [**LIM_TH_MIN***2^18]}

8.9.129 LIM_TH_MIN3 (page=0x04 address=0x12) [reset=00h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MIN**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MIN[15:8]	RW	00h	dec2hex{256*round [**LIM_TH_MIN***2^18]}

8.9.130 LIM_TH_MIN4 (page=0x04 address=0x13) [reset=00h]

Programmable bits to set limiter maximum threshold to a **LIM_TH_MIN**(V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_TH_MIN[7:0]	RW	0h	dec2hex{256*round [**LIM_TH_MIN***2^18]}

8.9.131 LIM_INF_PT1 (page=0x04 address=0x14) [reset=56h]

Programmable bits to set limiter inflection point to a value of **LIM_INF_P**T(V).Sets limiter inflection point.

Bit	Field	Type	Reset	Description
7-0	LIM_INF_PT[31:24]	RW	56h	dec2hex{256*round [**LIM_IN_PT***2^18]}}

8.9.132 LIM_INF_PT2 (page=0x04 address=0x15) [reset=66h]

Programmable bits to set limiter inflection point to a value of **LIM_INF_P**T(V).Sets limiter inflection point.

Bit	Field	Type	Reset	Description
7-0	LIM_INF_PT[23:16]	RW	66h	dec2hex{256*round [**LIM_IN_PT***2^18]}}

8.9.133 LIM_INF_PT3 (page=0x04 address=0x16) [reset=66h]

Programmable bits to set limiter inflection point to a value of **LIM_INF_P**T(V).Sets limiter inflection point.

Bit	Field	Type	Reset	Description
7-0	LIM_INF_PT[15:8]	RW	66h	dec2hex{256*round [**LIM_IN_PT***2^18]}}

8.9.134 LIM_INF_PT4 (page=0x04 address=0x17) [reset=00h]

Programmable bits to set limiter inflection point to a value of **LIM_INF_P**T(V).Sets limiter inflection point.

Bit	Field	Type	Reset	Description
7-0	LIM_INF_PT[7:0]	RW	0h	dec2hex{256*round [**LIM_IN_PT***2^18]}}

8.9.135 LIM_SLOPE1 (page=0x04 address=0x18) [reset=10h]

Programmable bits to set limiter slope to a **LIM_SLOPE** (V/V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_SLOPE[31:24]	RW	10h	dec2hex{256*round [**LIM_SLOPE***2^20]}

8.9.136 LIM_SLOPE2 (page=0x04 address=0x19) [reset=00h]

Programmable bits to set limiter slope to a **LIM_SLOPE** (V/V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_SLOPE[23:16]	RW	00h	dec2hex{256*round [**LIM_SLOPE***2^20]}

8.9.137 LIM_SLOPE3 (page=0x04 address=0x1A) [reset=00h]

Programmable bits to set limiter slope to a **LIM_SLOPE** (V/V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_SLOPE[15:8]	RW	00h	dec2hex{256*round [**LIM_SLOPE***2^20]}

8.9.138 LIM_SLOPE4 (page=0x04 address=0x1B) [reset=00h]

Programmable bits to set limiter slope to a **LIM_SLOPE** (V/V) value.

Bit	Field	Type	Reset	Description
7-0	LIM_SLOPE[7:0]	RW	00h	dec2hex{256*round [**LIM_SLOPE***2^20]}

8.9.139 TF_HLD1 (page=0x04 address=0x1C) [reset=00h]

Programmable bits for thermal fold-back hold count set to a **TF_HLD**[s] value.

Bit	Field	Type	Reset	Description
7-0	TF_ HOLD_CNT[31:24]	RW	00h	dec2hex[256*round (**TF_HLD***9600)]

8.9.140 TF_HLD2 (page=0x04 address=0x1D) [reset=00h]

Programmable bits for thermal fold-back hold count set to a **TF_HLD**[s] value.

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT23:16]	RW	00h	dec2hex[256*round (**TF_HLD***9600)]

8.9.141 TF_HLD3 (page=0x04 address=0x1E) [reset=64h]

Programmable bits for thermal fold-back hold count set to a **TF_HLD**[s] value.

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT[15:8]	RW	64h	dec2hex[256*round (**TF_HLD***9600)]

8.9.142 TF_HLD4 (page=0x04 address=0x1F) [reset=00h]

Programmable bits for thermal fold-back hold count set to a **TF_HLD**[s] value.

Bit	Field	Type	Reset	Description
7-0	TF_HOLD_CNT[7:0]	RW	00h	dec2hex[256*round (**TF_HLD***9600)]

8.9.143 TF_RLS1 (page=0x04 address=0x20) [reset=40h]

Programmable bits for thermal fold-back limiter release rate set to a value **TF_RLS**[dB/100us].

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[31:24]	RW	40h	dec2hex{256*round[10^(**TF_RLS**/20)*2^22]}

8.9.144 TF_RLS2 (page=0x04 address=0x21) [reset=BDh]

Programmable bits for thermal fold-back limiter release rate set to a value **TF_RLS**[dB/100us].

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[23:16]	RW	BDh	dec2hex{256*round[10^(**TF_RLS**/20)*2^22]}

8.9.145 TF_RLS3 (page=0x04 address=0x22) [reset=B8h]

Programmable bits for thermal fold-back limiter release rate set to a value **TF_RLS**[dB/100us].

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[15:8]	RW	B8h	dec2hex{256*round[10^(**TF_RLS**/20)*2^22]}

8.9.146 TF_RLS4 (page=0x04 address=0x23) [reset=00h]

Programmable bits for thermal fold-back limiter release rate set to a value **TF_RLS**[dB/100us].

Bit	Field	Type	Reset	Description
7-0	TF_REL_RATE[7:0]	RW	0h	dec2hex{256*round[10^(**TF_RLS**/20)*2^22]}

8.9.147 TF_SLOPE1 (page=0x04 address=0x24) [reset=04h]

Programmable bits for thermal fold-back limiter attenuation slope set to value **TF_SLOPE**(V/^{0}C).

Input level is assumed 0dB and gain is 21dB. An extra 3dB (total of 24dB) is due to rms to peak conversion.

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[31:24]	RW	04h	dec2hex{256*round {[**TF_SLOPE**/(10^24/20)]*2^23}

8.9.148 TF_SLOPE2 (page=0x04 address=0x25) [reset=08h]

Programmable bits for thermal fold-back limiter attenuation slope set to value **TF_SLOPE**(V/^{0}C).

Input level is assumed 0dB and gain is 21dB. An extra 3dB (total of 24dB) is due to rms to peak conversion.

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[23:16]	RW	08h	dec2hex{256*round {[**TF_SLOPE**/(10^24/20)]*2^23}

8.9.149 TF_SLOPE3 (page=0x04 address=0x26) [reset=89h]

Programmable bits for thermal fold-back limiter attenuation slope set to value **TF_SLOPE**(V/^{0}C).

Input level is assumed 0dB and gain is 21dB. An extra 3dB (total of 24dB) is due to rms to peak conversion.

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[15:8]	RW	89h	dec2hex{256*round {[**TF_SLOPE**/(10^24/20)]*2^23}

8.9.150 TF_SLOPE4 (page=0x04 address=0x27) [reset=00h]

Programmable bits for thermal fold-back limiter attenuation slope set to value **TF_SLOPE**(V/^{0}C).

Input level is assumed 0dB and gain is 21dB. An extra 3dB (total of 24dB) is due to rms to peak conversion.

Bit	Field	Type	Reset	Description
7-0	TF_LIMS[7:0]	RW	0h	dec2hex{256*round {[**TF_SLOPE**/(10^24/20)]*2^23}

8.9.151 TF_TEMP_TH1 (page=0x04 address=0x28) [reset=39h]

Programmable bits for thermal fold-back temperature threshold set to **TF_TEMP**(^{0}C) value.

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[31:24]	RW	39h	dec2hex{256*round [**TF_TEMP***(2^15)]}

8.9.152 TF_TEMP_TH2 (page=0x04 address=0x29) [reset=80h]

Programmable bits for thermal fold-back temperature threshold set to **TF_TEMP**(^{0}C) value.

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[23:16]	RW	80h	dec2hex{256*round [**TF_TEMP***(2^15)]}

8.9.153 TF_TEMP_TH3 (page=0x04 address=0x2A) [reset=00h]

Programmable bits for thermal fold-back temperature threshold set to **TF_TEMP**(^{0}C) value.

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[15:8]	RW	00h	dec2hex{256*round [**TF_TEMP***(2^15)]}

8.9.154 TF_TEMP_TH4 (page=0x04 address=0x2B) [reset=00h]

Programmable bits for thermal fold-back temperature threshold set to **TF_TEMP**(^{0}C) value.

Bit	Field	Type	Reset	Description
7-0	TF_TEMP_TH[7:0]	RW	0h	dec2hex{256*round [**TF_TEMP***(2^15)]}

8.9.155 TF_MAX_ATTN1 (page=0x04 address=0x2C) [reset=2Dh]

Programmable bits for thermal fold-back maximum gain reduction set to **TF_ATTN**(dB) value of attenuation.

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[31:24]	RW	2Dh	dec2hex{256*round [(10^(-**TF_ATTN**/20)*2^23]}

8.9.156 TF_MAX_ATTN2 (page=0x04 address=0x2D) [reset=6Ah]

Programmable bits for thermal fold-back maximum gain reduction set to **TF_ATTN**(dB) value of attenuation.

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN(23:16]	RW	6Ah	dec2hex{256*round [(10^(-**TF_ATTN**/20)*2^23]}

8.9.157 TF_MAX_ATTN3 (page=0x04 address=0x2E) [reset=86h]

Programmable bits for thermal fold-back maximum gain reduction set to **TF_ATTN**(dB) value of attenuation.

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[15:7]	RW	86h	dec2hex{256*round [(10^(-**TF_ATTN**/20)*2^23]}

8.9.158 TF_MAX_ATTN4 (page=0x04 address=0x2F) [reset=00h]

Programmable bits for thermal fold-back maximum gain reduction set to **TF_ATTN**(dB) value of attenuation.

Bit	Field	Type	Reset	Description
7-0	TF_MAX_ATTN[7:0]	RW	0h	dec2hex{256*round [(10^(-**TF_ATTN**/20)*2^23]}

8.9.159 LD_CFG0 (page=0x04 address=0x40) [reset=03h]

Programmable bits for load diagnostic resistance upper threshold set to a **LD_RES_UT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[31:24]	RW	03h	dec2hex{256*round (**LDG_RES_UT***(5/16)*2^14)}

8.9.160 LD_CFG1 (page=0x04 address=0x41) [reset=20h]

Programmable bits for load diagnostic resistance upper threshold set to a **LD_RES_UT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[23:16]	RW	20h	dec2hex{256*round (**LDG_RES_UT***(5/16)*2^14)}

8.9.161 LD_CFG2 (page=0x04 address=0x42) [reset=00h]

Programmable bits for load diagnostic resistance upper threshold set to a **LD_RES_UT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[15:7]	RW	00h	dec2hex{256*round (**LDG_RES_UT***(5/16)*2^14)}

8.9.162 LD_CFG3 (page=0x04 address=0x43) [reset=00h]

Programmable bits for load diagnostic resistance upper threshold set to a **LD_RES_UT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_UT[7:0]	RW	0h	dec2hex{256*round (**LDG_RES_UT***(5/16)*2^14)}

8.9.163 LD_CFG4 (page=0x04 address=0x44) [reset=00h]

Programmable bits for load diagnostic resistance lower threshold set to a **LD_RES_LT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[31:24]	RW	0h	dec2hex{256*round (**LDG_RES_LT***(5/16)*2^14)}

8.9.164 LD_CFG5 (page=0x04 address=0x45) [reset=20h]

Programmable bits for load diagnostic resistance lower threshold set to a **LD_RES_LT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[23:16]	RW	20h	dec2hex{256*round (**LDG_RES_LT***(5/16)*2^14)}

8.9.165 LD_CFG6 (page=0x04 address=0x46) [reset=00h]

Programmable bits for load diagnostic resistance lower threshold set to a **LD_RES_LT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[15:8]	RW	00h	dec2hex{256*round (**LDG_RES_LT***(5/16)*2^14)}

8.9.166 LD_CFG7 (page=0x04 address=0x47) [reset=00h]

Programmable bits for load diagnostic resistance lower threshold set to a **LD_RES_LT**(Ω) value.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_LT[7:0]	RW	0h	dec2hex{256*round (**LDG_RES_LT***(5/16)*2^14)}

8.9.167 CLD_EFF_1 (page=0x04 address=0x48) [reset=6Ch]

Programmable bits for Class D efficiency for LV_EN relative threshold. It is expressed as a fraction (**EFF**) and default is 0.85.

Bit	Field	Type	Reset	Description
7-0	ClassD Efficiency [31:24]	RW	6Ch	dec2hex[256*round (**EFF***2^23)]

8.9.168 CLD_EFF_2 (page=0x04 address=0x49) [reset=CCh]

Programmable bits for Class D efficiency for LV_EN relative threshold. It is expressed as a fraction (**EFF**) and default is 0.85.

Bit	Field	Type	Reset	Description
7-0	ClassD Efficiency [23:16]	RW	CCh	dec2hex[256*round (**EFF***2^23)]

8.9.169 CLD_EFF_3 (page=0x04 address=0x4A) [reset=CDh]

Programmable bits for Class D efficiency for LV_EN relative threshold. It is expressed as a fraction (**EFF**) and default is 0.85.

Bit	Field	Type	Reset	Description
7-0	ClassD Efficiency [15:8]	RW	CDh	dec2hex[256*round (**EFF***2^23)]

8.9.170 CLD_EFF_4 (page=0x04 address=0x4B) [reset=00h]

Programmable bits for Class D efficiency for LV_EN relative threshold. It is expressed as a fraction (**EFF**) and default is 0.85.

Bit	Field	Type	Reset	Description
7-0	ClassD Efficiency [7:0]	RW	00h	dec2hex[256*round (**EFF***2^23)]

8.9.171 LDG_RES1 (page=0x04 address=0x4C) [reset=00h]

Diagnostic mode load resistance measured value expresed in Ω. Read value is 0x**UUVVXXYY** and the last byte will be dropped.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_VAL[31:24]	R	0h	(16/5)*{hex2dec (0x**UUVVXX**)}/2^14}

8.9.172 LDG_RES2 (page=0x04 address=0x4D) [reset=00h]

Diagnostic mode load resistance measured value expresed in Ω. Read value is 0x**UUVVXXYY** and the last byte will be dropped.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_VAL[23:16]	R	0h	(16/5)*{hex2dec (0x**UUVVXX**)}/2^14}

8.9.173 LDG_RES3 (page=0x04 address=0x4E) [reset=00h]

Diagnostic mode load resistance measured value expresed in Ω. Read value is 0x**UUVVXXYY** and the last byte will be dropped.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_VAL[15:7]	R	0h	(16/5)*{hex2dec (0x**UUVVXX**)}/2^14}

8.9.174 LDG_RES4 (page=0x04 address=0x4F) [reset=00h]

Diagnostic mode load resistance measured value expresed in Ω. This last byte will be dropped.

Bit	Field	Type	Reset	Description
7-0	LDG_RES_VAL[7:0]	R	0h	Drop this byte

8.9.175 INIT_3 (page=0xFD address=0x3E) [reset=45h]

Bit	Field	Type	Reset	Description
7-4	Reserved	RW	4h	Reserved
3-0	OPT_DMIN[3:0]	RW	5h	DMIN optimization settings

8.10 SDOUT Equations

The following equations will alow to convert data read on SDOUT.

$$PVDD\ (V) = 23 * [Hex2Dec(SDOUTdata)]/2^{PVDD\_SlotLength} \quad (6)$$

By default, PVDD_SlotLength = 8.

VBAT1S (V)= 8 [Hex2Dec(SDOUTdata)]/2^VBAT1S_SlotLength* (7)

By default, VBAT1S_SlotLength = 8.

TEMP (^{0}C)= 256[Hex2Dec(SDOUTdata)]/2^TEMP_SlotLength - 95* (8)

TEMP_SlotLength = 8.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TAS2780 is a digital input Class-D audio power amplifier with integrated I/V sense. I²S audio data is supplied by host processor. The device provides I/V data in I²S format. I²C bus is used for configuration and control.

9.2 Typical Application

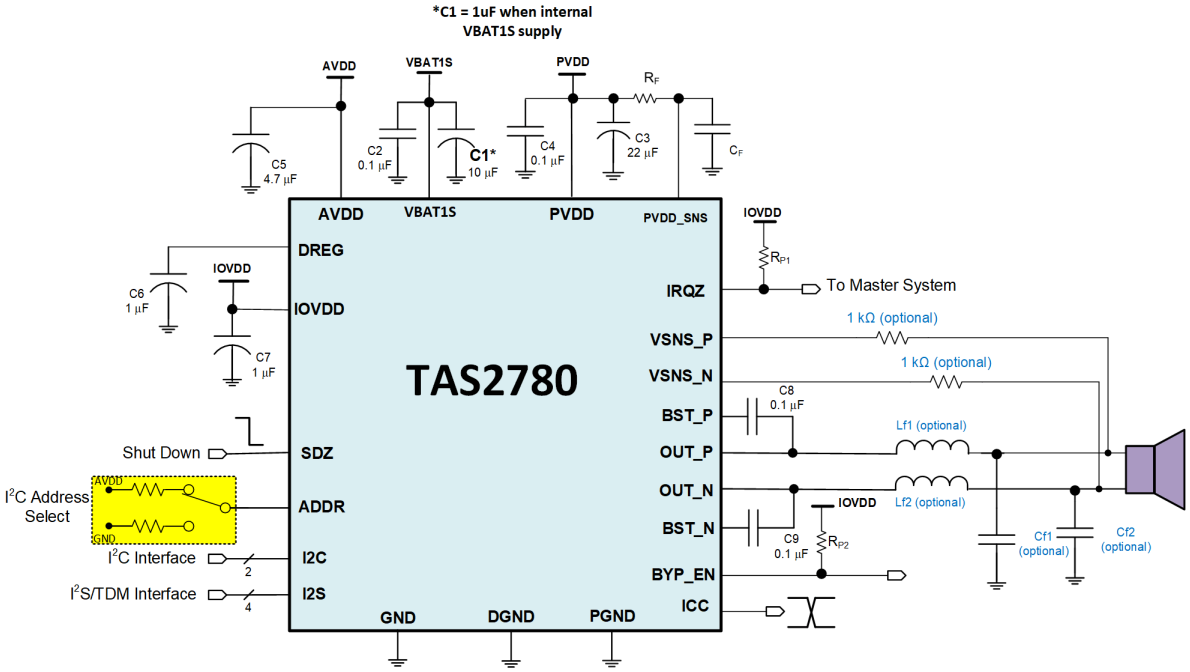


Figure 9-1. Typical Application - Digital Audio Input

Table 9-1. Recommended External Components

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
C1	VBAT1S Decoupling Capacitor - VBAT1S External Supply (PWR_MODE0/1/3)	Type	X7R			
		Capacitance, 20% Tolerance		10		µF
		Rated Voltage		10		V
	VBAT1S Decoupling Capacitor - VBAT1S Internally Generated (PWR_MODE2)	Type	X7R			
		Capacitance, 20% Tolerance		1		µF
		Rated Voltage		10		V
C2	VBAT1S Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		100		nF
		Rated Voltage		10		V
C3	PVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	22			µF
		Rated Voltage	30			V

Table 9-1. Recommended External Components (continued)

COMPONENT	DESCRIPTION	SPECIFICATION	MIN	TYP	MAX	UNIT
C4	PVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		100		nF
		Rated Voltage	30			V
C5	AVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance	4.7			µF
		Rated Voltage	6			V
C6	DREG Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		1		µF
		Rated Voltage	6			V
C7	IOVDD Decoupling Capacitor	Type	X7R			
		Capacitance, 20% Tolerance		1		µF
		Rated Voltage	6			V
C8, C9	Bootstrap Capacitors	Type	X7R			
		Capacitance, 20% Tolerance		100		nF
		Rated Voltage	6			V
Lf1, Lf2 **(optional)**	EMI filter inductors are optional. TAS2780 device support filter less Class-D operation. PFFB feature is recommended if ferrite bead EMI filters are used.	Impedance at 100MHz		120		Ω
		DC Resistance			0.095	Ω
		DC Current	7			A
Cf1, Cf2 **(optional)**	EMI filter capacitors are optional. Design must use Lf2, Lf3 if Cf1, Cf2 are used	Capacitance		1		nF
R_F	Filter resistor for noise reduction	Resistor, 20% Tolerance	1			kΩ
C_F	Filter capacitor for noise reduction	Capacitance, 20% Tolerance			$10/R_F(k\Omega)$	nF
		Rated Voltage	30			V

9.3 Design Requirements

For this design example, use the parameters shown in Section 9.2.

Table 9-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Audio Input	Digital Audio, I^2S
Current and Voltage Data Stream	Digital Audio, I^2S
Mono or Stereo Configuration	Mono
Max Output Power at 1% THD+N, R_L = 4 Ω	25 W

9.4 Detailed Design Procedure

9.4.1 Mono/Stereo Configuration

In applications the device is assumed to be operating in mono mode. See *Section 8.3.1* for information on changing the I^2C address of the TAS2780 to support stereo operation. Mono or stereo configuration does not impact the device performance.

9.4.2 EMI Passive Devices

The TAS2780 supports spread spectrum to minimize EMI. It is allowed to include passive devices on the Class-D outputs. The passive devices Lf1, Lf2, Cf1 and Cf2 from Figure 9-1 have recommended specifications provided in Table 9-1. The passive devices of the output filter have to be properly selected to maintain the stability of the amplifier. See Section 8.4.5 for details.

9.5 Application Curves

At T_A = 25 ^{0}C, f_{SPK_AMP} = 384 kHz, input signal f_{IN} = 1kHz - Sine, Load = 4Ω + 15µH, unless otherwise noted.

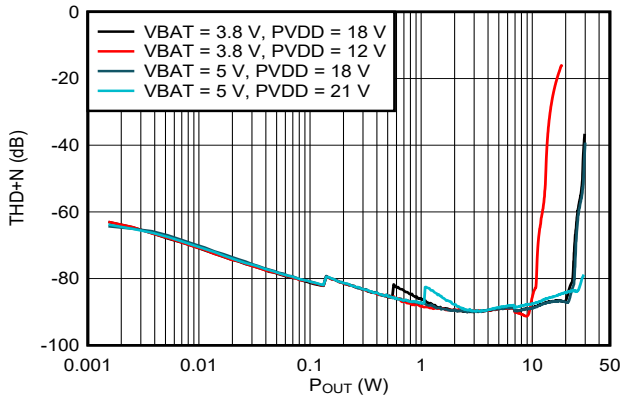


Figure 9-2. THD+N vs Output Power

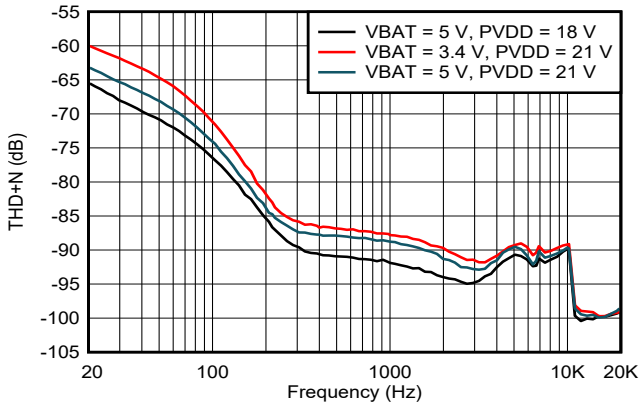


Figure 9-3. THD+N vs Output Power

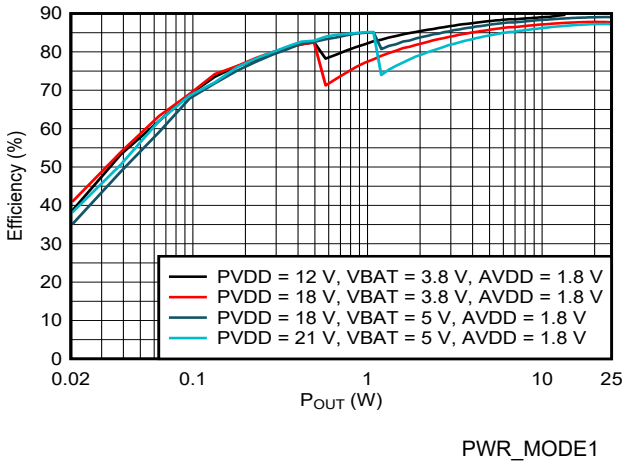


Figure 9-4. Efficiency vs Output Power

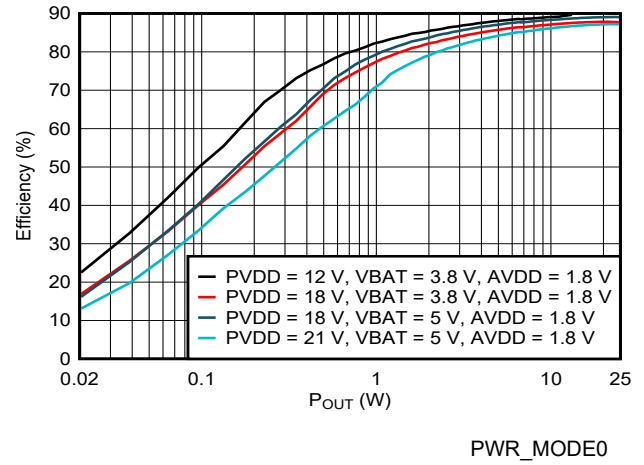


Figure 9-5. Efficiency vs Output Power

10 Initialization Set Up

10.1 Initial Device Configuration - Power Up and Software Reset

The following I²C sequence needs to be used:

- At power up, when SDZ = 1 (out of Hardware Shutdown into Software Shutdown);
- when device is in Software Shutdown or Active mode and user runs a Software Reset command: bit[0] of register 0x01 = 1.

```
###### Pre-Reset Configuration
w 70 00 01 #Page 0x01
w 70 37 3A #Bypass

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access page
w 70 06 C1 #Set Dmin

w 70 00 01 #Page 0x01
 w 70 19 C0 #Force modulation
w 70 00 FD #Page 0xFD
w 70 0D 0D #Access page
w 70 06 D5 #Set Dmin

###### Software Reset
w 70 00 00 #Page 0x00
w 70 7F 00 #Book 0x00
w 70 01 01 #Software Reset
d 01 #1 ms Delay

###### Post-Reset Configuration
w 70 00 01 #Page 0x01
w 70 37 3A #Bypass

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access page
w 70 06 C1 #Set Dmin
w 70 06 D5 #Set Dmin
```

10.2 Initial Device Configuration - PWR_MODE0

The following I²C sequence is an example of initializing the device in PWR_MODE0.

```
w 70 00 00 # Page 0x00
w 70 0E 44 #TDM tx vsns transmit enable with slot 4
w 70 0F 40 #TDM tx isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 21 00 #Disable Comparator Hysterisis
w 70 17 C8 #SARBurstMask=0
w 70 19 00 #LSR Mode
w 70 35 74 #Noise minimized

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page 0xFD
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access Page 0xFD

w 70 00 00 #Page 0x00
w 70 03 A8 #PWR_MODE0 selected
w 70 71 03 #PVDD UVLO set to 2.76V
w 70 02 80 #Play audio, power up with playback, IV enabled
```

10.3 Initial Device Configuration - PWR_MODE1

The following I²C sequence is an example of initializing the device in PWR_MODE1.

```
w 70 00 00 # Page 0x00
w 70 0E 44 #TDM tx vsns transmit enable with slot 4
w 70 0F 40 #TDM tx isns transmit enable with slot 0
```

```
w 70 00 01 #Page 0x01
w 70 17 C8 #SARBurstMask=0
w 70 21 00 #Disable Comparator Hysterisis
w 70 19 00 #LSR Mode
w 70 35 74 #Noise minimized

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page 0xFD
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access Page 0xFD

w 70 00 00 #Page 0x00
w 70 02 00 #Play audio, power up with playback, IV enabled
```

10.4 Initial Device Configuration - PWR_MODE2

The following I²C sequence is an example of initializing the device in PWR_MODE2.

```
w 70 00 00 #Page 0x00
w 70 0E 44 #TDM tx vsns transmit enable with slot 4
w 70 0F 40 #TDM tx isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 17 C0 #SARBurstMask=0
w 70 19 00 #LSR Mode
w 70 21 00 #Disable Comparator Hysterisis
w 70 35 74 #Noise minimized

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page 0xFD
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access Page 0xFD

w 70 00 00 #Page 0x00
w 70 03 E8 #PWR_MODE2
w 70 04 A1 #Int LDO mode
w 70 71 0E #PVDD UVLO 6.5V
w 70 02 80 #Power up audio playback with I,V enabled
```

10.5 Initial Device Configuration - PWR_MODE3

The following I²C sequence is an example of initializing the device in PWR_MODE3, for ultrasonic applications.

```
w 70 00 00 #Page 0x00
w 70 0E 44 #TDM tx vsns transmit enable with slot 4
w 70 0F 40 #TDM tx isns transmit enable with slot 0

w 70 00 01 #Page 0x01
w 70 17 C8 #SARBurstMask=0
w 70 19 00 #LSR Mode
w 70 21 00 #Disable Comparator Hysterisis

w 70 00 FD #Page 0xFD
w 70 0D 0D #Access Page 0xFD
w 70 3E 4A #Optimal Dmin
w 70 0D 00 #Remove access Page 0xFD

w 70 00 00 #Page 0x00
w 70 03 68 #PWR_MODE3
w 70 73 E0 #DEM dither disable
w 70 02 00 #Play audio, power up with playback, IV enabled
```

10.6 Device Configuration - 44.1 kHz

The following I²C sequence is an example of initializing a TAS2780 device into 44.1 kHz sampling rate.

```
###### Configure Channel
w 70 60 21 # SBLK to Fs ratio = 256 / 8 TDM Slots
w 70 08 39 # 44.1KHz, Auto TDM off, Frame start High to Low
w 70 09 03 # Offset = 1, Sync on BCLK falling edge
w 70 0A 0A # TDM slot by address, Word = 24 bit, Frame = 32 bit
```

```
w 70 0C 20 # Right Ch = TDM slot 2, Left Ch = TDM slot 0
w 70 0D 33 # TX bus keeper, Hi-Z, Offset 1, TX on Falling edge
```

10.7 Over Power Protection - OCP Programming

The following I²C sequence will program the over current protection in the case 2.7V ≤ VBAT1S≤ 2.9V.

```
w 70 00 FD #
w 70 0D 0D #
w 70 5C C0 #
w 70 3A 7D #
r 70 3B 01 #
#Record the value read from register 3B: XY
w 70 3B XZ # Z=Y-2
w 70 0D 00 #
w 70 00 00 #
```

10.8 DSP Loopback

The following I²C sequence will enable the DSP loopback for echo reference.

```
#####DSP Echo Reference Loopback
w 70 00 00 #Page 0x00
w 70 7F 00
w 70 16 C0 #Audio TX slot programmed to 0
w 70 0E 00 #Disable V sense
w 70 0F 00 #Disable I sense
```

11 Power Supply Recommendations

The power sequence between the supply rails can be applied in any order as long as SDZ pin is held low. Once all supplies are stable the SDZ pin can be set high to initialize the part. After a hardware or software reset additional commands to the device should be delayed for at least 1 ms to allow the OTP memory to load (see section Section 10).

When VBAT1S is internally generated (see Section 11.1) it is recommended that the device enters Software Shutdown mode before entering Hardware Shutdown mode. This ensures that VBAT1S pin is discharged using the internal 5 kOhms pull down resistor (not present in Hardware Shutdown mode).

11.1 Power Supply Modes

The TAS2780 can operate with both VBAT1S and PVDD as supplies or with only PVDD or VBAT1S as supply. The table below shows different power supply modes of operation depending on the user need.

Table 11-1. Device Configuration and Power Supply Modes

Supply Power Mode	Output Switching Mode	Supply Condition	VBAT1S Mode	Device Configurations	Use Case and Device Functionality
PWR_MODE0	High Power on PVDD	PVDD>VBAT1S	External	VBAT1S_MODE=0 CDS_MODE[1:0]=10	PVDD is the only supply used to deliver output power.
PWR_MODE1	Y Bridge - High Power on VBAT1S	PVDD	External	VBAT1S_MODE=0 CDS_MODE[1:0]=00	VBAT1S is used to deliver output power based on level and headroom configured. When audio signal crosses a programmed threshold Class-D output is switched over PVDD.
PWR_MODE2	Y Bridge - Low Power on VBAT1S	PVDD	Internal	VBAT1S_MODE=1 CDS_MODE[1:0]=11	PVDD is the only supply. VBAT1S is delivered by an internal LDO and used to supply at signals close to idle channel levels. When audio signal levels crosses -100dBFS (default), Class-D output switches to PVDD.
PWR_MODE3	VBAT1S	VBAT1S	External	VBAT1S_MODE=0 CDS_MODE[1:0]=01	The device can be forced to work out of a low power rail mode of operation. For example this can be used for a low power ultrasonic chirp when audio is not played.

When VBAT1S is external (PWR_MODE0, PWR_MODE1), if PVDD falls below (VBAT1S + 2.5 V) level, the Y-bridge will stop switching between supplies and will remain on the PVDD supply.

In PWR_MODE2 user needs to ensure that PVDD supply level is at least 2.5 V above the VBAT1S voltage generated internally in order to take advantage of Y bridge mode of operation. To enable voltage protection the under voltage threshold of PVDD supply should be set above 7.3 V by using register bits *PVDD_UVLO[5:0]*. This will ensure that, with an internally generated VBAT1S of 4.8 V, PVDD supply is at least 2.5 V higher than VBAT1S.

12 Layout

12.1 Layout Guidelines

All supply rails should be bypassed by low-ESR ceramic capacitors as shown and described in Section 9.2.

To create a low impedance connection to PGND, DGND and GND and minimize the ground noise, ground planes with multiple conductive epoxy filled vias should be used in layout.

Specific layout design recommendations should be followed for this device:

- Use wide traces for signals that carry high current: PVDD, VBAT1S, PGND, DGND, GND and the speaker OUT_P, OUT_N.
- PGND pin should be directly connected and shorted to the ground plane.
- DGND pin should be directly connected to the ground plane.
- Connect VSNS_P and VSNS_N as close as possible to the speaker.
- VSNS_P and VSNS_N should be connected between the EMI ferrite filter and the speaker if EMI ferrites are used at the outputs.
- VSNS_P and VSNS_N routing should be separated and shielded from switching signals (interface signals, speaker outputs, bootstrap pins).
- Place bootstrap capacitors as close as possible to the BST pins.
- Place decoupling capacitors of PVDD and VBAT1S as close as possible to the pins (see Figure 12-1).

12.2 Layout Example

The figure below describes the placement of critical components as assigned in Figure 9-1.

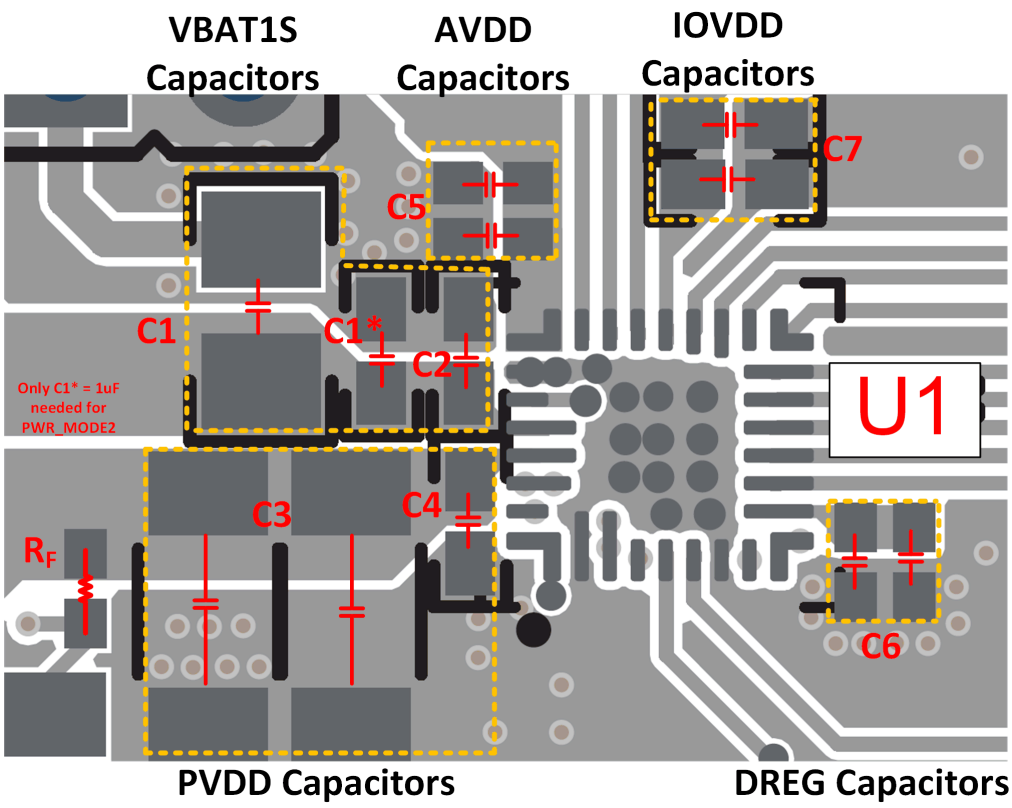


Figure 12-1. Layout and Component Placement - Top Layer

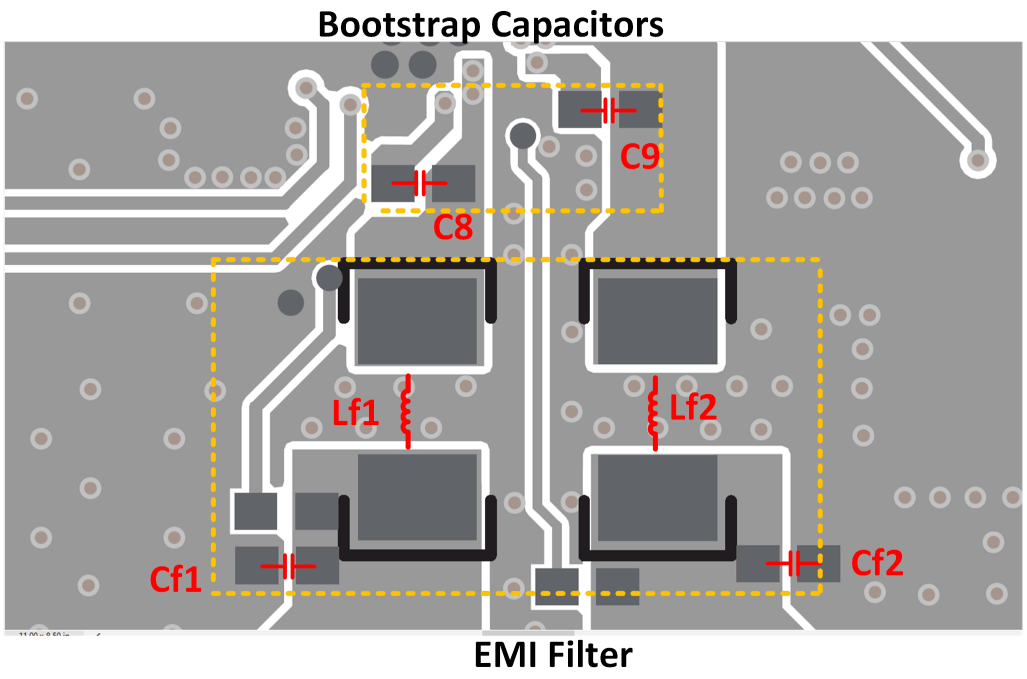


Figure 12-2. Layout and Component Placement - Bottom Layer

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

13.3 Trademarks

All trademarks are the property of their respective owners.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS2780RYAR	ACTIVE	VQFN-HR	RYA	30	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	TAS2780	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

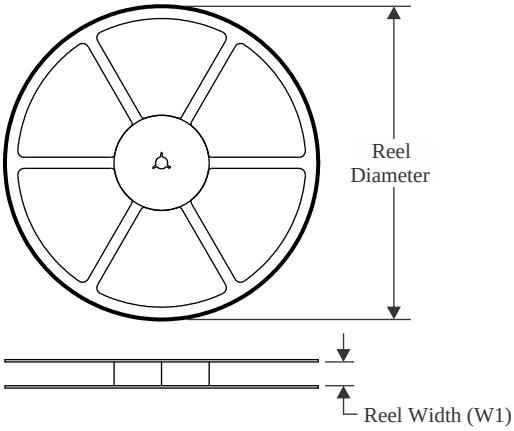
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

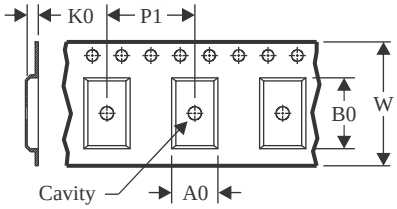
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

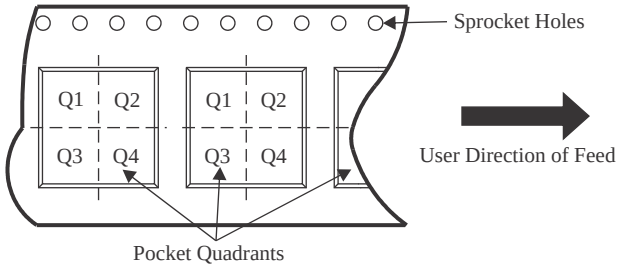


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

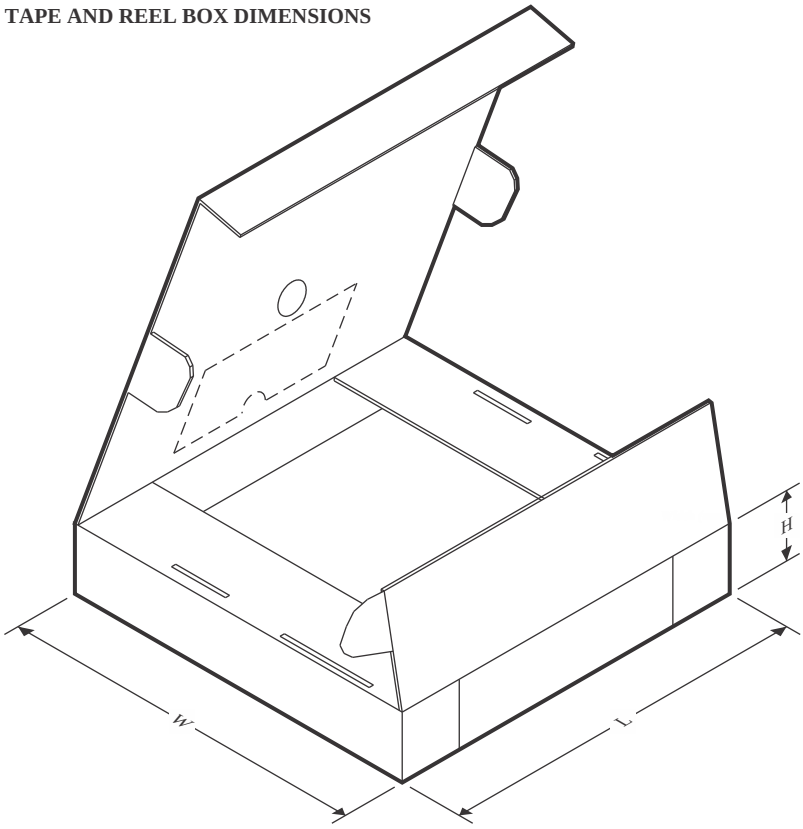
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS2780RYAR	VQFN-HR	RYA	30	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

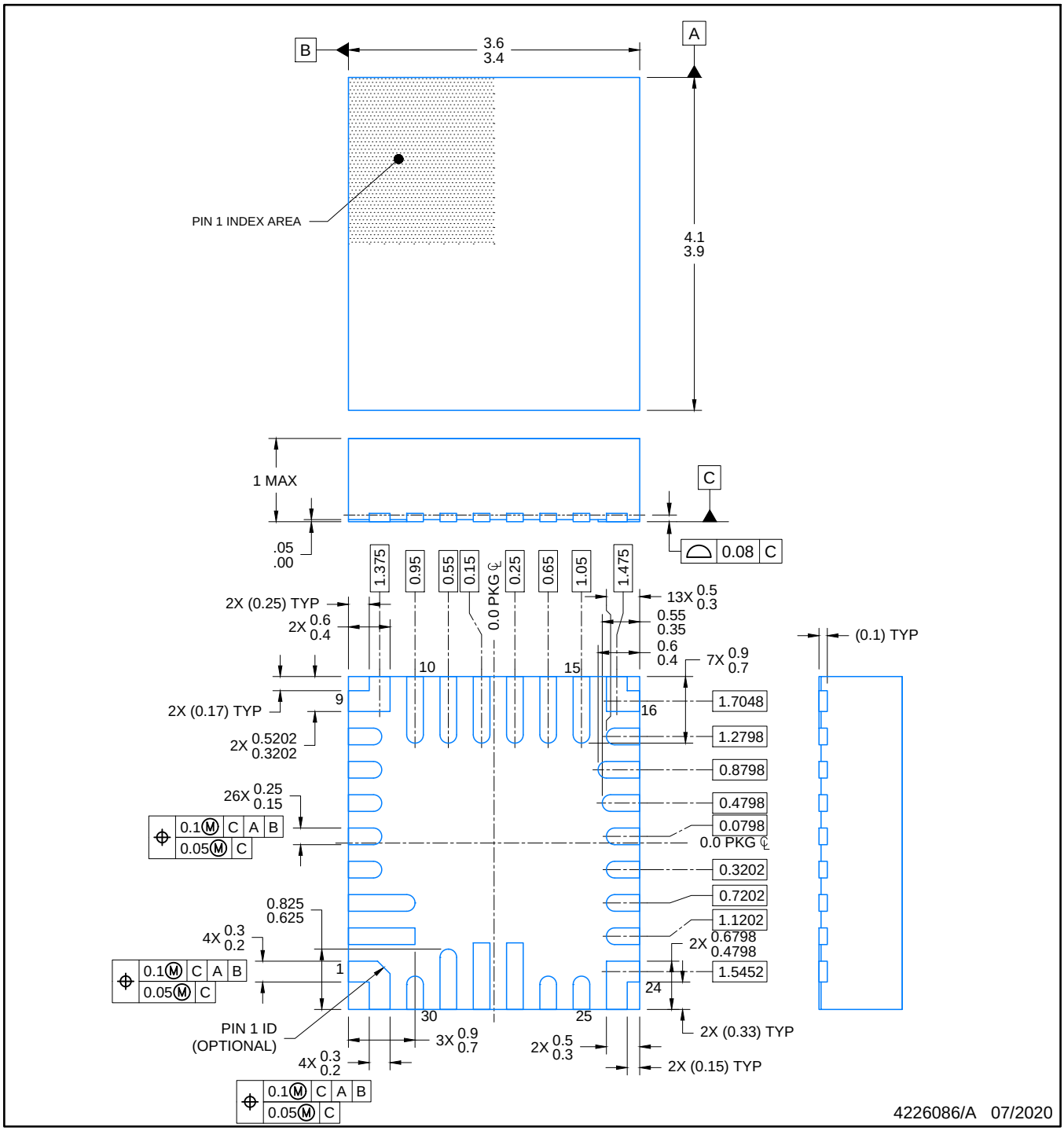
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS2780RYAR	VQFN-HR	RYA	30	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RYA0030A

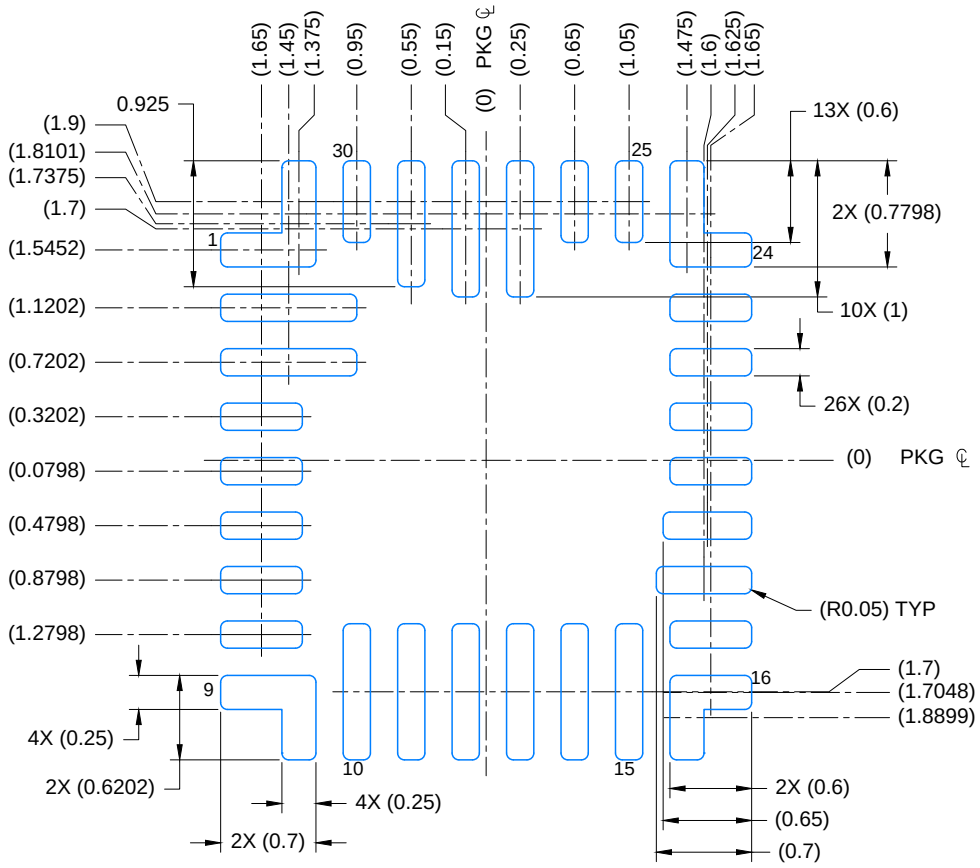
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

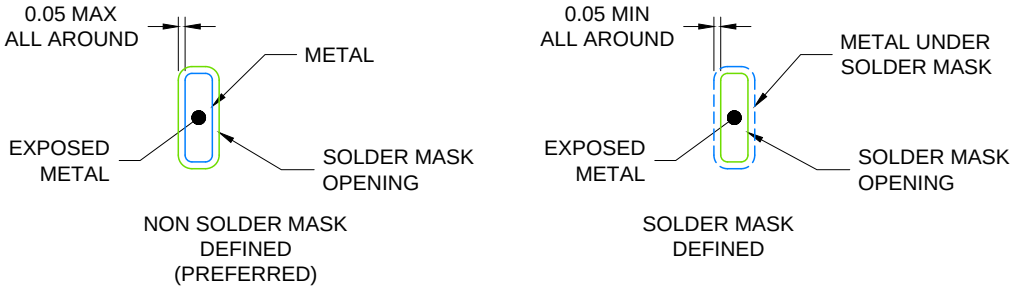
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 18X

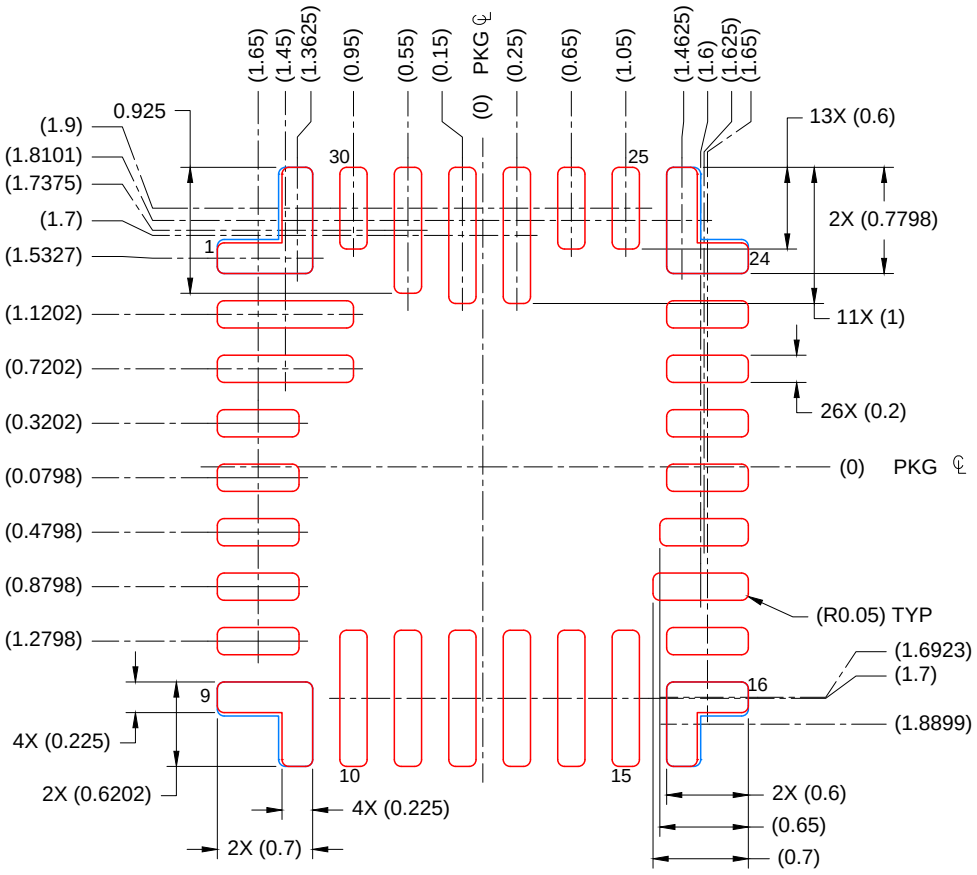


SOLDER MASK DETAILS

4226086/A 07/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1,9, 16, 24: 92%
SCALE: 18X

4226086/A 07/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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