LM4980 Boomer™ Audio Power Amplifier Series 2 Cell Battery, 1mA, 42mW Per Channel High Fidelity Stereo Headphone Audio Amplifier for MP3 players

Check for Samples: LM4980

FEATURES

- **2-Cell 1.5V to 3.3V Battery Operation**
- **Unity-Gain Stable**
- **"Click and Pop" Suppression Circuitry for Shutdown and Power On/Off Transient with Headphone Loads**
- **Active Low Micro-Power Shutdown**
- **Thermal Shutdown Protection Circuitry**

APPLICATIONS

- **Portable Two-Cell Audio Products**
- **Portable Two-Cell Electronic Devices**
- **Portable MP3 Player/Recorders**

KEY SPECIFICATIONS

- **Output Power (RL = 16Ω, V_{DD} = 3.0V, THD+N = 1%), 42mW (Typ)**
- **Quiescent current (V_{DD} = 3V), 1mA (Typ)**
- **Micropower Shutdown Current, 0.1µA (Typ)**
- **Supply Voltage Operating Range. 1.5V < V_{DD} < 3.3V**
- **PSRR @ 1kHz, V_{DD} = 3.0V, 90dB (Typ)**
- **PSRR @ 217Hz, V_{DD} = 3.0V, 100 (Typ)**

DESCRIPTION

The LM4980 is a stereo headphone audio amplifier, which when connected to a 3.0V supply, delivers 42mW to a 16Ω load with less than 1% THD+N. With the LM4980 packaged in the SON package, the customer benefits include low profile and small size. This package minimizes PCB area and maximizes output power.

The LM4980 features circuitry that significantly reduces output transients ("clicks" and "pops") while driving headphones during device turn-on and turn-off without costly external additional circuitry. The LM4980 also includes an externally controlled low-power consumption active-low shutdown mode, and thermal shutdown. Boomer audio power amplifiers are designed specifically to use few external components and provide high quality output power in a surface mount package.

Typical Application

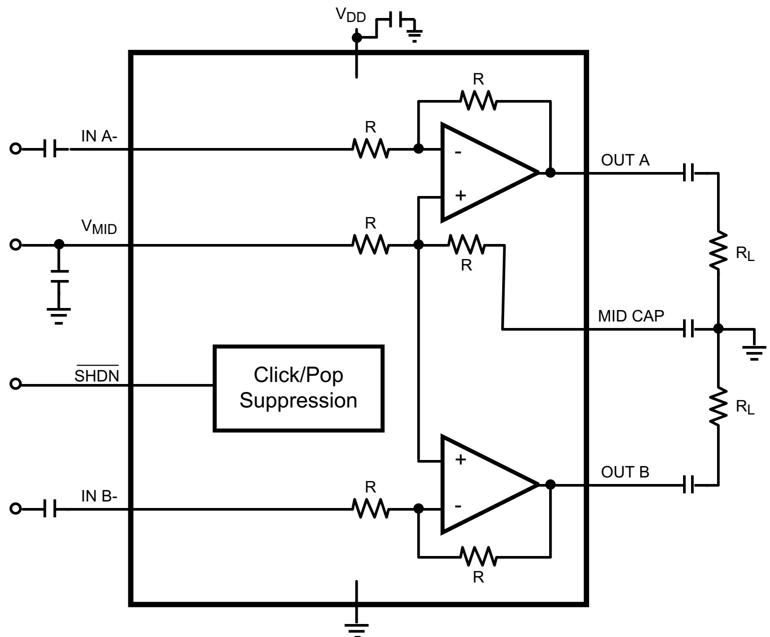

Figure 1. Block Diagram

Connection Diagram

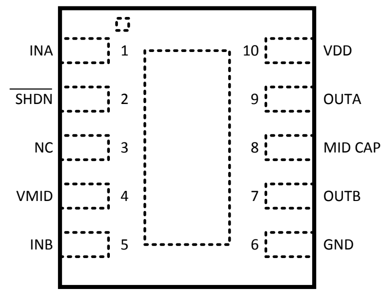

Figure 2. SON Package
Top View
See Package Number DSC0010A

Typical Connection

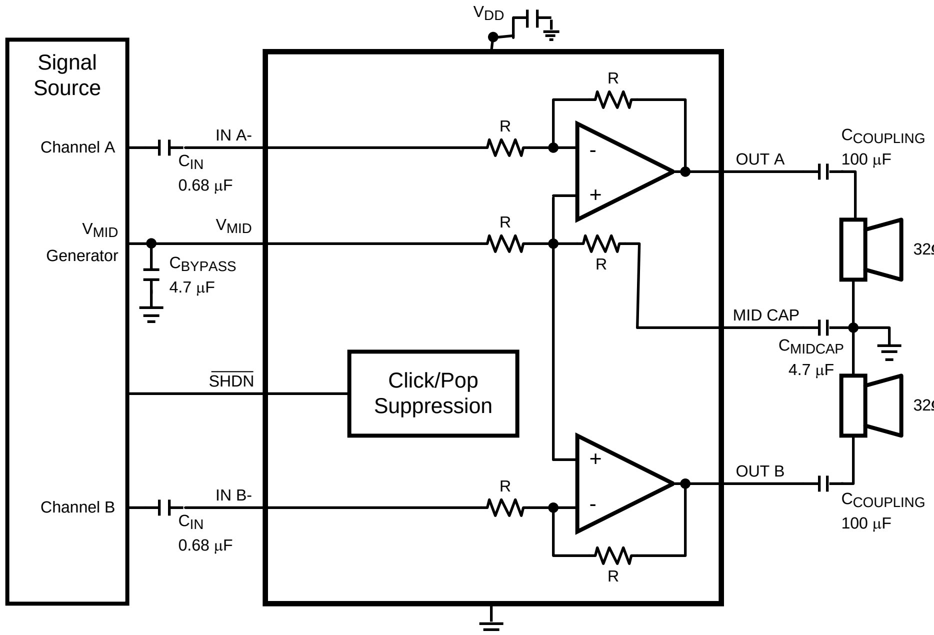

Figure 3. Typical Application Circuit

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Supply Voltage		3.6V
Storage Temperature		−65°C to +150°C
Input Voltage		−0.3V to V_{DD} +0.3V
Power Dissipation (3)		Internally limited
ESD Susceptibility (4)		2000V
ESD Susceptibility (5)		200V
Junction Temperature		150°C
Solder Information	Small Outline Package Vapor Phase (60sec)	215°C
	Infrared (15 sec)	220°C
Thermal Resistance	θ_{JA} (typ) DSC0010A	73°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The maximum power dissipation is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A must be derated at elevated temperatures. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} − T_A) / \theta_{JA}$. For the LM4980, T_{JMAX} = 150°C. For the θ_{JA}s, please see the Application Information section or the Absolute Maximum Ratings section.
(4) Human body model, 100pF discharged through a 1.5kΩ resistor.
(5) Machine model, 200pF – 220pF discharged through all pins.

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$	$−40°C \le T_A \le +85°C$
Supply Voltage		$1.5V \le V_{DD} \le 3.3V$

Electrical Characteristics V_{DD} = 3.0V(1)(2)

The following specifications apply for the circuit shown in Figure 3, unless otherwise specified. A_V = 0dB, R_L = 32Ω. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4980		Units (Limits)
			Typical(3)	Limit(4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞(5)	1.0	1.5	mA (max)
I_{SD}	Shutdown Current	$V_{\overline{SHDN}}$ = GND	0.1	1	μA (max)
V_{OS}	Output Offset Voltage		1	5	mV
P_O	Output Power(6)	R_L = 16Ω, THD+N = 1%, f = 1kHz, per channel	42	35	mW (min)
		R_L = 32Ω, THD+N = 1%, f = 1kHz, per channel	28		mW (min)
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Fig. 2	10		$μV_{RMS}$
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, P_{OUT} = 10mW, f = 1kHz	0.02		%
Crosstalk		Freq = 1kHz, P_{OUT} = 28mW, R_L = 32Ω	77		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} sine wave f_{RIPPLE} = 1kHz, C_{MIDCAP} = 4.7μF, V_{MID} Voltage is Ripple-Free	90		dB
		V_{RIPPLE} = 200mV_{P-P} sine wave f_{RIPPLE} = 217Hz, C_{MIDCAP} = 4.7μF, V_{MID} Voltage is Ripple-Free	100		dB
CMRR	Common-Mode Rejection Ratio	Input coupling capacitors with 5% tolerance, V_{IN} = V_{MID}, f_{RIPPLE} = 1kHz	47		dB
$T_{WAKE-UP}$	Wake-up Time	C_{MIDCAP} = 4.7μF, Fig 2.	250		ms
V_{IH}	Control Logic High	1.5V ≤ V_{DD} ≤ 3.3V		1.4V	V (min)
V_{IL}	Control Logic Low	1.5V ≤ V_{DD} ≤ 3.3V		0.4V	V (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

Electrical Characteristics V_{DD} = 1.8V (1) (2)

The following specifications apply for the circuit shown in Figure 3, unless otherwise specified. A_V = 0dB, R_L = 32Ω. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM4980		Units (Limits)
			Typical (3)	Limit (4)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A, R_L = ∞ (5)	0.9		mA
I_{SD}	Shutdown Current	$V_{\overline{SHDN}}$ = GND	0.1		µA
V_{OS}	Output Offset Voltage		1		mV
P_O	Output Power (6)	R_L = 16Ω, THD+N = 1%, f = 1kHz, per channel	11		mW (min)
		R_L = 32Ω, THD+N = 1%, f = 1kHz, per channel	9		mW (min)
V_{NO}	Output Voltage Noise	20Hz to 20kHz, A-weighted, Fig. 2	9		$µV_{RMS}$
THD+N	Total Harmonic Distortion + Noise	R_L = 32Ω, P_{OUT} = 10mW, f = 1kHz	0.03		%
Crosstalk		Freq = 1kHz, P_{OUT} = 9mW, R_L = 32Ω	79		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} sine wave f_{RIPPLE} = 1kHz, C_{MIDCAP} = 4.7µF, V_{MID} Voltage is Ripple-Free	78		dB
		V_{RIPPLE} = 200mV_{P-P} sine wave f_{RIPPLE} = 217Hz, C_{MIDCAP} = 4.7µF, V_{MID} Voltage is Ripple-Free	85		dB
CMRR	Common-Mode Rejection Ratio	Input coupling capacitors with 5% tolerance, V_{IN} = V_{MID}, f_{RIPPLE} = 1kHz	47		dB
$T_{WAKE-UP}$	Wake-up Time	C_{MIDCAP} = 4.7µF, Fig 2.	320		ms
V_{IH}	Control Logic High	1.5V ≤ V_{DD} ≤ 3.3V		1.4V	V (min)
V_{IL}	Control Logic Low	1.5V ≤ V_{DD} ≤ 3.3V		0.4V	V (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the ground (GND) pins unless otherwise specified.
(3) Typicals are measured at 25°C and represent the parametric norm.
(4) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(5) The quiescent power supply current depends on the offset voltage when a practical load is connected to the amplifier.
(6) Output power is measured at the device terminals.

Typical Performance Characteristics (T_A = 25°C)

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, P_O = 7.3mW

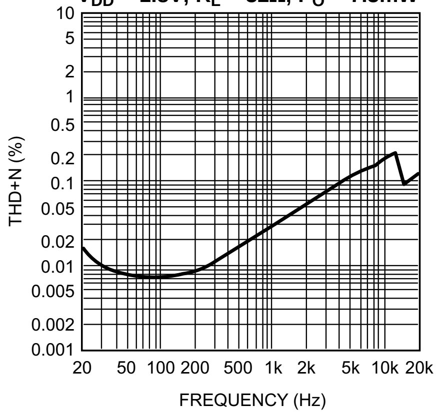

Figure 4.

THD+N vs Frequency
V_{DD} = 2.4V, R_L = 32Ω, P_{OUT} = 14mW

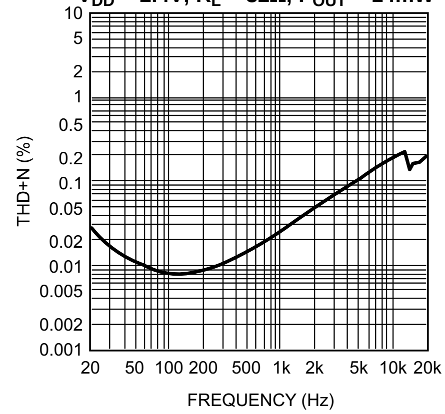

Figure 5.

THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, P_{OUT} = 23mW

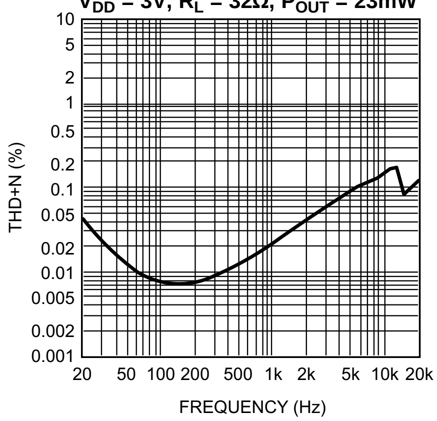

Figure 6.

THD+N vs Frequency
V_{DD} = 1.8V, R_L = 16Ω, P_{OUT} = 9.3mW

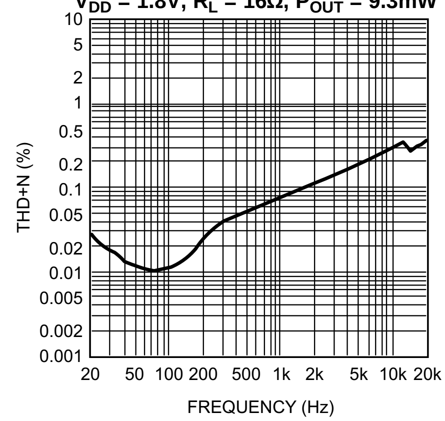

Figure 7.

THD+N vs Frequency
V_{DD} = 2.4V, R_L = 16Ω, P_{OUT} = 20mW

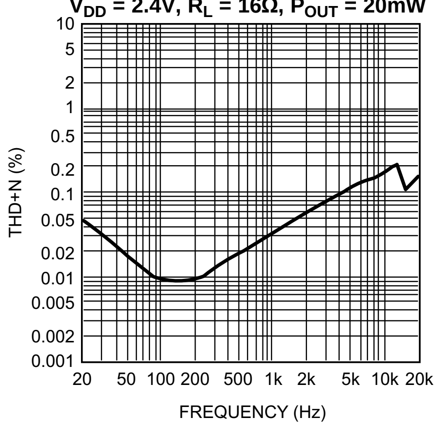

Figure 8.

THD+N vs Frequency
V_{DD} = 3V, R_L = 16Ω, P_{OUT} = 27mW

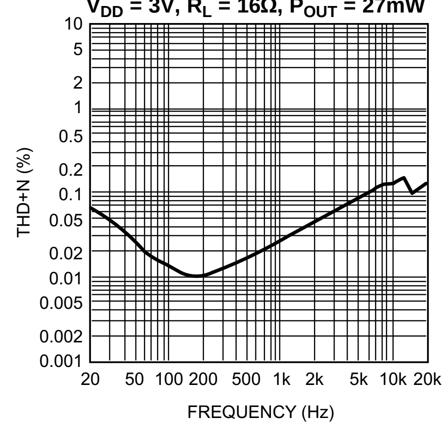

Figure 9.

Typical Performance Characteristics (T_A = 25°C) (continued)

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 32Ω

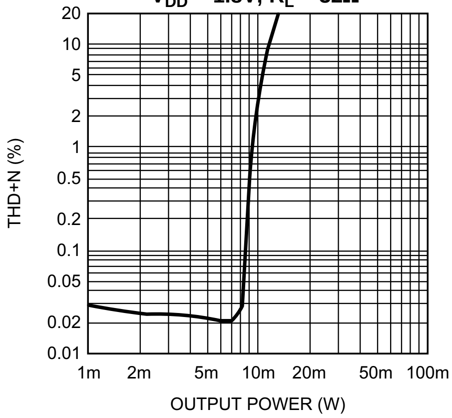

Figure 10.

THD+N vs Output Power
V_{DD} = 2.4V, R_L = 32Ω

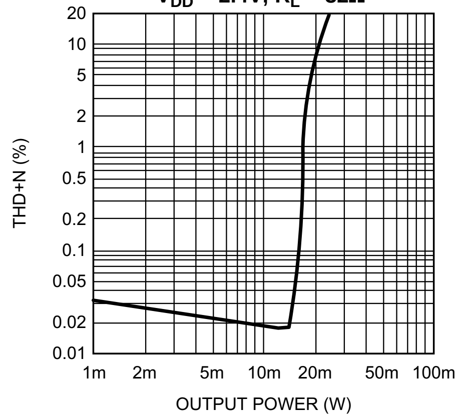

Figure 11.

THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω

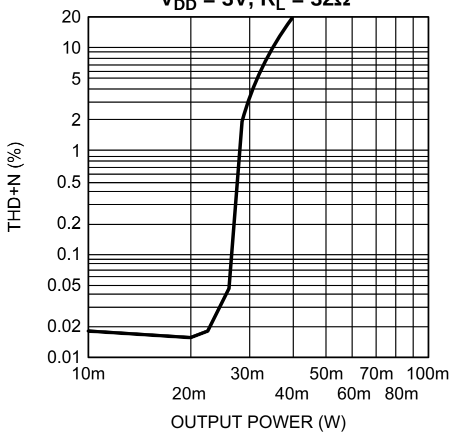

Figure 12.

THD+N vs Output Power
V_{DD} = 1.8V, R_L = 16Ω

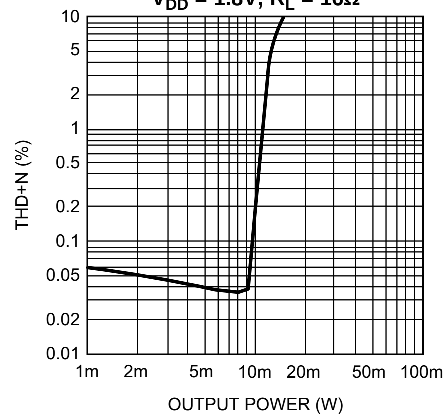

Figure 13.

THD+N vs Output Power
V_{DD} = 2.4V, R_L = 16Ω

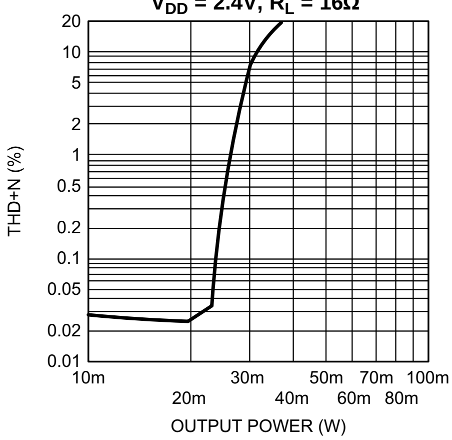

Figure 14.

THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω

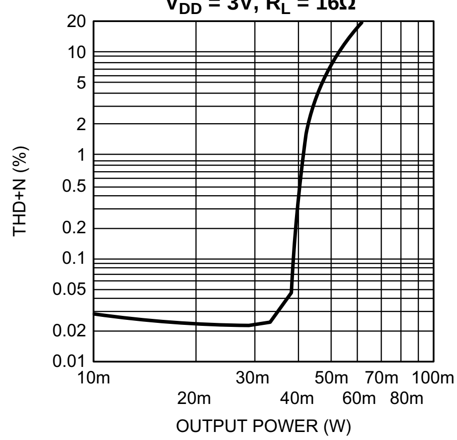

Figure 15.

Typical Performance Characteristics (T_A = 25°C) (continued)

PSRR vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, 4.7µ

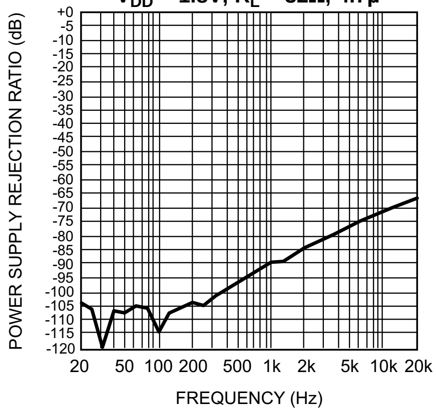

Figure 16.

PSRR vs Frequency
V_{DD} = 2.4V, R_L = 32Ω, 4.7µ

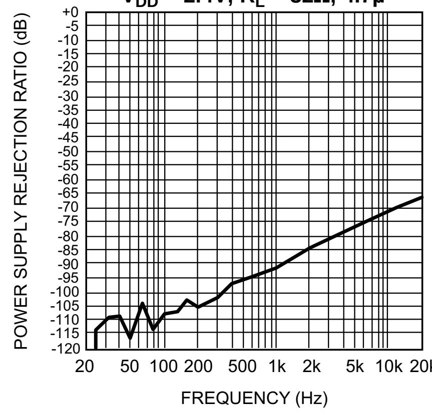

Figure 17.

PSRR vs Frequency
V_{DD} = 3V, R_L = 32Ω, 4.7µ

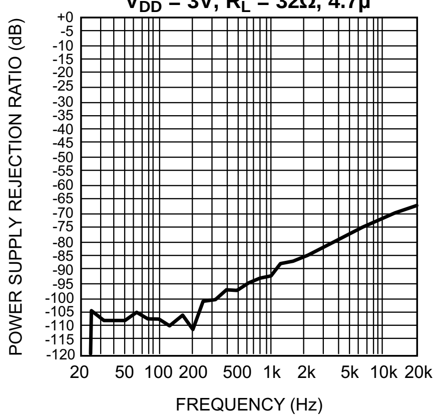

Figure 18.

PSRR vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, 1µ

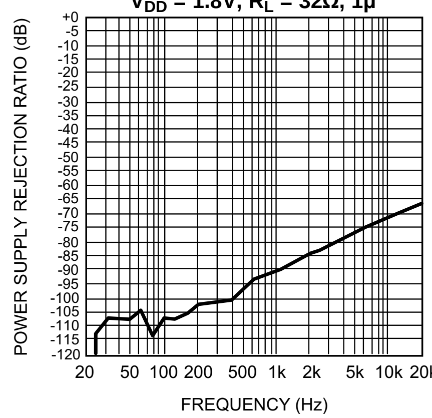

Figure 19.

PSRR vs Frequency
V_{DD} = 2.4V, R_L = 32Ω, 1µ

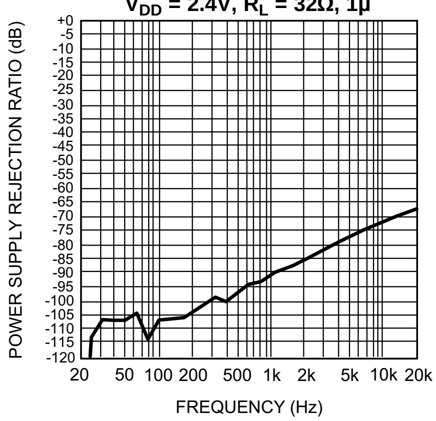

Figure 20.

PSRR vs Frequency
V_{DD} = 3V, R_L = 32Ω, 1µ

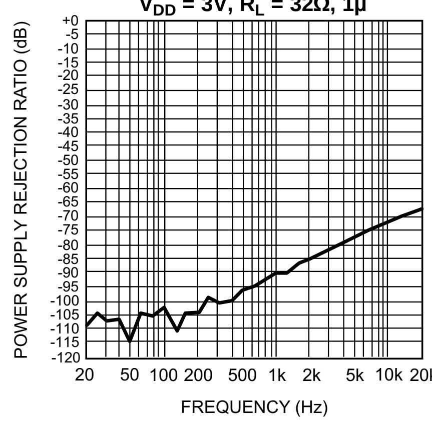

Figure 21.

Typical Performance Characteristics (T_A = 25°C) (continued)

Crosstalk vs Frequency
V_{DD} = 1.8V, R_L = 32Ω, P_{OUT} = 9mW
Channel A Driven, Channel B Measured

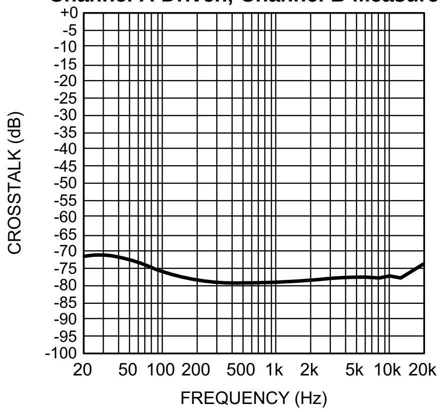

Figure 22.

Crosstalk vs Frequency
V_{DD} = 1.8V, R_L = 32Ω,P_{OUT} = 9mW
Channel B Driven, Channel A Measured

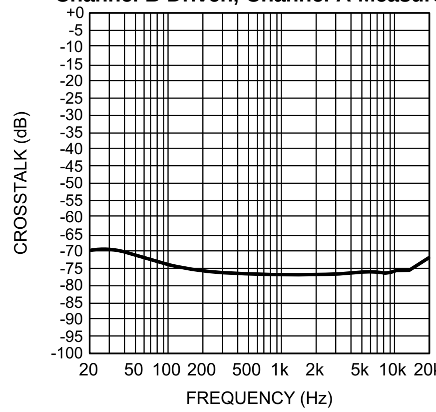

Figure 23.

Crosstalk vs Frequency
V_{DD} = 2.4V, R_L = 32Ω, P_{OUT} = 17mW
Channel A Driven, Channel B Measured

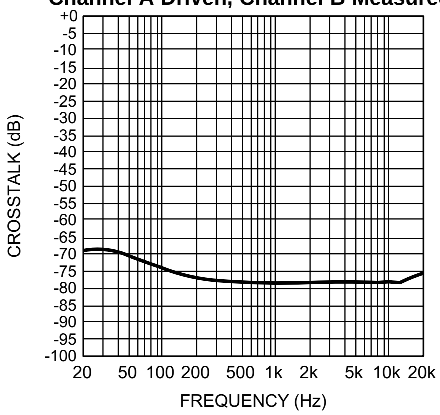

Figure 24.

Crosstalk vs Frequency
V_{DD} = 2.4V, R_L = 32Ω, P_{OUT} = 17mW
Channel B Driven, Channel A Measured

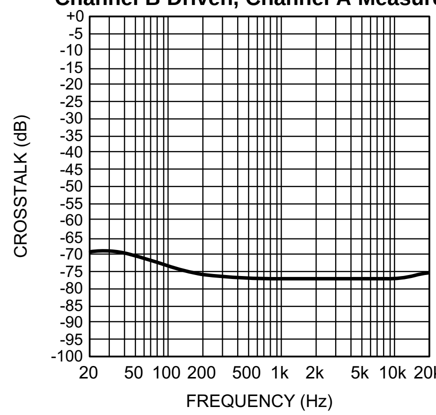

Figure 25.

Crosstalk vs Frequency
V_{DD} = 3V, R_L = 32Ω, P_{OUT} = 27mW
Channel A Driven, Channel B Measured

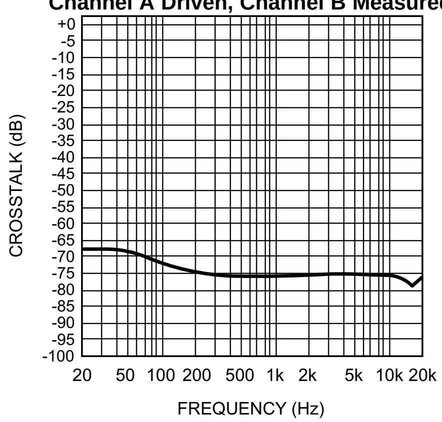

Figure 26.

Crosstalk vs Frequency
V_{DD} = 3V, R_L = 32Ω, P_{OUT} = 27mW
Channel B Driven, Channel A Measured

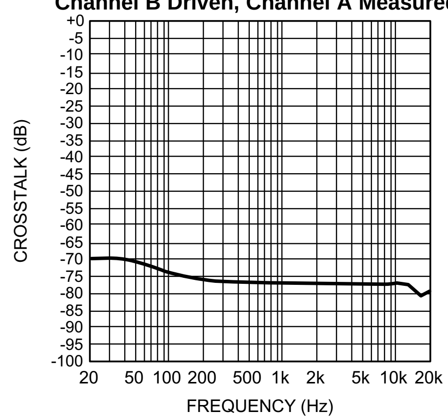

Figure 27.

Typical Performance Characteristics (T_A = 25°C) (continued)

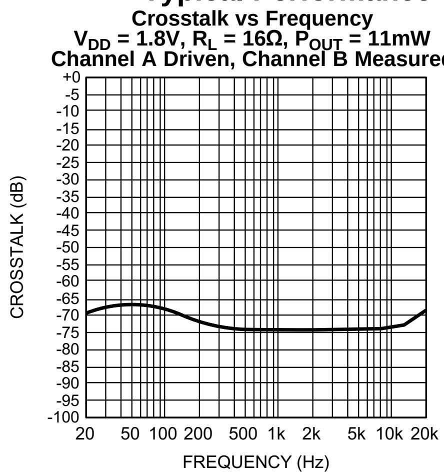

Figure 28.

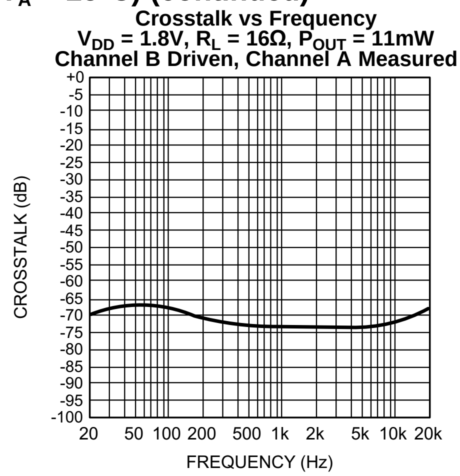

Figure 29.

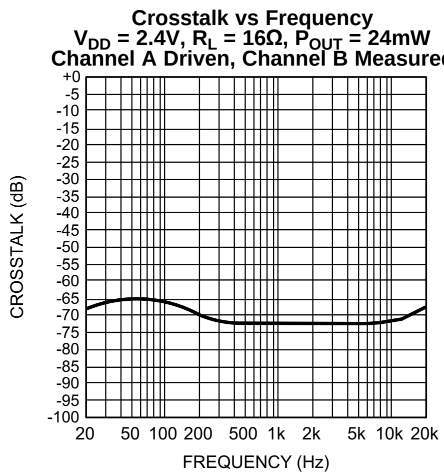

Figure 30.

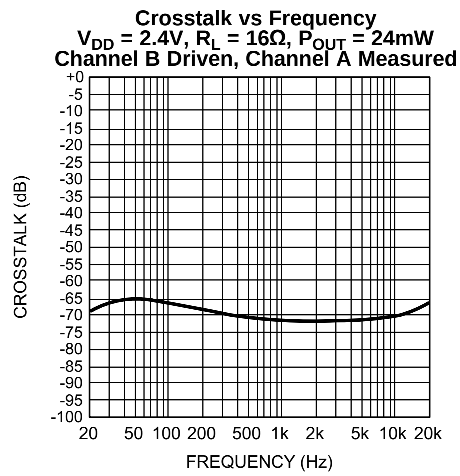

Figure 31.

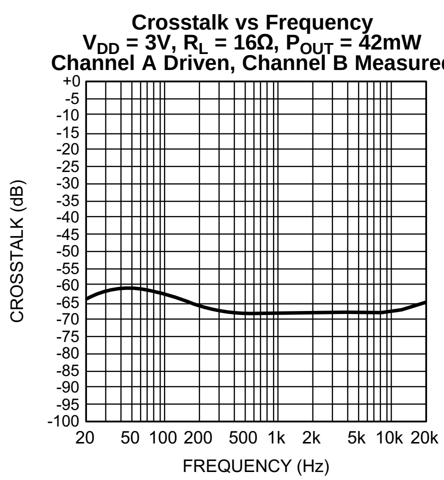

Figure 32.

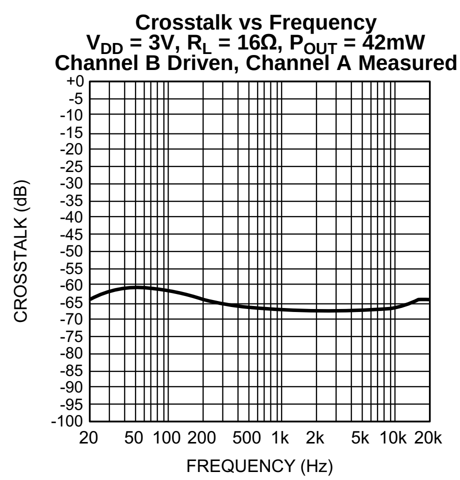

Figure 33.

Typical Performance Characteristics (T_A = 25°C) (continued)

Output Power vs Supply Voltage
R_L = 32Ω

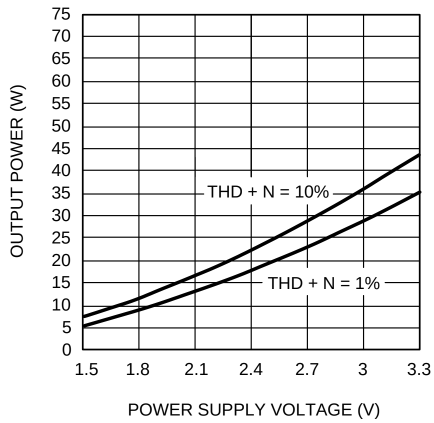

Figure 34.

Output Power vs Supply Voltage
R_L = 16Ω

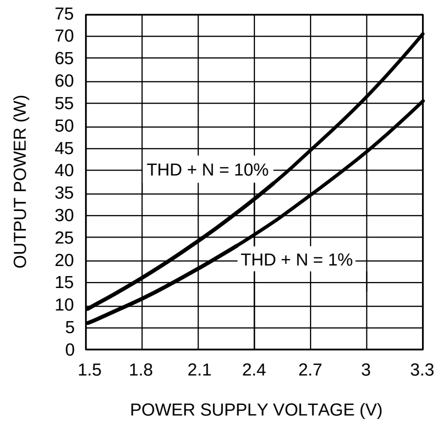

Figure 35.

Output Power vs Load Resistance
V_{DD} = 1.8V

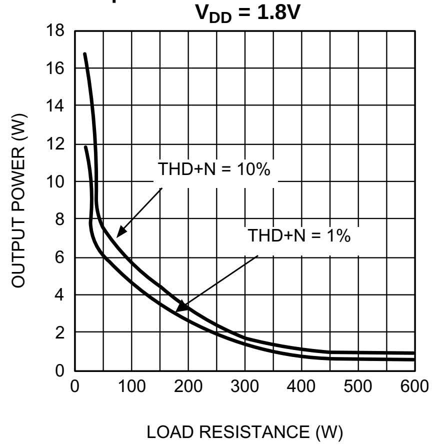

Figure 36.

Output Power vs Load Resistance
V_{DD} = 2.4V

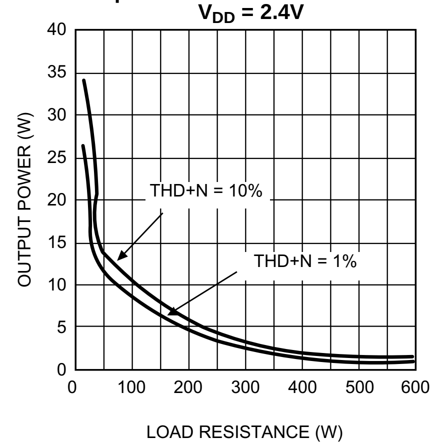

Figure 37.

Output Power vs Load Resistance
V_{DD} = 3.0V

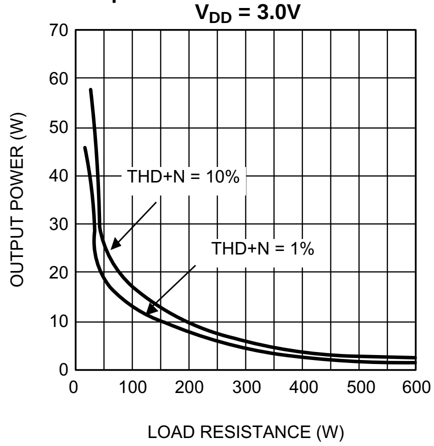

Figure 38.

Load Dissipation vs Amplifier Dissipation
V_{DD} = 1.8V

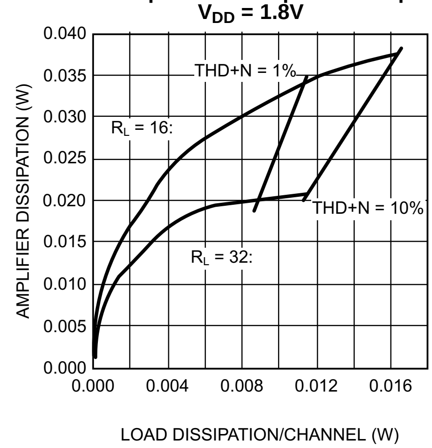

Figure 39.

Typical Performance Characteristics (T_A = 25°C) (continued)

Amplifier Dissipation vs Load Dissipation
V_{DD} = 2.4V

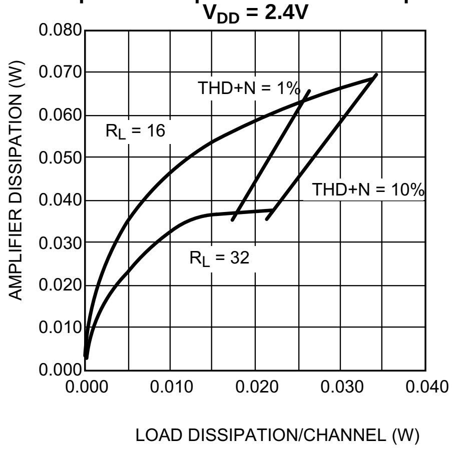

Figure 40.

Amplifier Dissipation vs Load Dissipation
V_{DD} = 3.0V

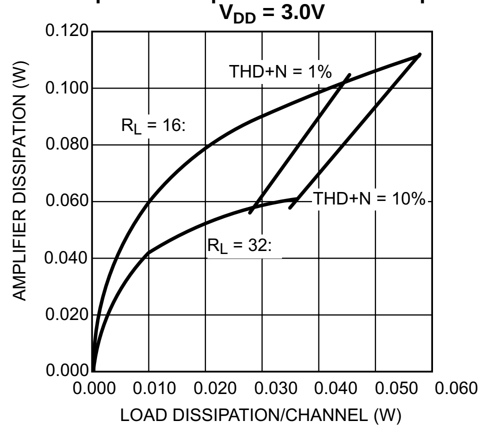

Figure 41.

Power Supply Current vs Power Supply Voltage
V_{IN} = 0V

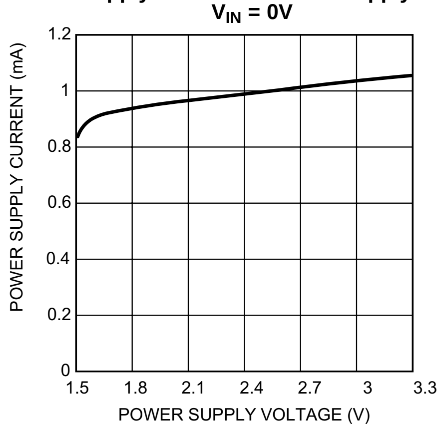

Figure 42.

APPLICATION INFORMATION

AMPLIFIER CONFIGURATION

As shown in Figure 1, the LM4980 consists of a stereo pair of audio amplifiers. These amplifiers operate on a single supply and have single-ended inputs and outputs. The quiescent operating point of each amplifier input and output is equal to the voltage applied to the V_{MID} pin (usually $V_{DD}/2$).

C_{MIDCAP} VALUE SELECTION

Careful consideration should be paid to value of C_{MIDCAP}, the capacitor connected between the MIDCAP pin and ground. The value of C_{MIDCAP} determines how fast the LM4980 settles to quiescent operation and determines the amount of output transient suppression. Choosing C_{MIDCAP} equal to 4.7µF along with a small value of C_{IN} (in the range of 0.1µF to 1.0µF), produces shutdown function that is essentially output-transient free. Choosing C_{IN} no larger than necessary for the desired bandwidth helps minimize clicks and pops. This ensures that output transients are minimized when power is first applied or the LM4980 resumes operation after shutdown. The MIDCAP offers the following benefits: better linearity for reduced THD+N, reduced channel-to-channel crosstalk, and less susceptibility to ground noise. For the ultimate suppression of output transient when power is applied or removed, ensure that the voltage applied to the $\overline{SHDN}$ pin is a logic low. This will activate the micro-power shutdown.

OPTIMIZING OUTPUT-GROUND NOISE REDUCTION

In addition to the output-ground noise reduction afforded by C_{MIDCAP}, further reduction can be achieved by the inclusion of a ferrite bead. The ferrite bead (FB) is placed between ground and common connection between the C_{MIDCAP} and the headphone ground connection. This is shown in Figure 43. The ferrite bead is beneficial in environments where the headphone and C_{MIDCAP} ground connection is shared with circuitry (such as video) that may inject noise on a common ground.

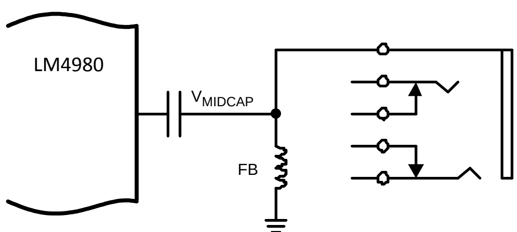

Figure 43. Adding a ferrite bead improves ground-noise suppression

OPTIMIZING OUTPUT TRANSIENT SUPPRESSION

The LM4980 contains circuitry that eliminates turn-on and shutdown output transients ("clicks and pops"). For this discussion, turn-on refers to either applying the power supply voltage or when the micro-power shutdown mode is deactivated. The turn-on time delay is the time duration that occurs between the application of the power supply voltage or deactivating shutdown and when the applied input signal appears at the amplifier outputs.

C_{MIDCAP}'s value plays a significant role in the suppression of output transients. The amount of suppression increases as C_{MIDCAP}'s value increases. However, changing the value of C_{MIDCAP} alters the LM4980's turn-on time. There is a linear relationship between the value of C_{MIDCAP} and the turn-on time. Here are some typical turn-on times for various values of C_{MIDCAP}.

Table 1. Typical turn-on time versus C_{MIDCAP} value

C_{MIDCAP} VALUE (µF)	Turn-On Time (ms)
4.7	250
6.8	360
10.0	530

STAND-ALONE V_{MID} VOLTAGE GENERATION

The LM4980 is designed to take advantage of audio DACs (digital-to-analog converters) and other signal sources that, in addition to generating an analog signal, also create an AC ground potential. This AC ground potential is typically $V_{DD}/2$. This $V_{DD}/2$ is applied to the LM4980's V_{MID} pin (pin 4).

Using two external resistors allows the LM4980 to be easily used in applications where the V_{MID} voltage is not internally generated and supplied to the LM4980 by other circuits. Figure 44 shows this configuration.

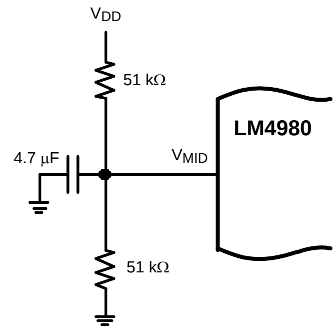

Figure 44. Simple circuit generates LM4980's V_{MID} voltage

SELECTING THE OUTPUT COUPLING CAPACITOR VALUE

To ensure that no performance degrading DC current flows through the load (something with which speakers would just as soon not have to tolerate), coupling capacitors are necessary between the amplifier output pins and the load. Besides blocking DC current, the output coupling capacitor value, together with the load resistance, produces a low frequency amplitude rolloff, whose cutoff frequency is found using Equation 1.

$$f_{-3\ dB} = \frac{1}{2\pi R_{LOAD} C_{COUPLING}} \quad (1)$$

When driving 32Ω headphones, the 220µF $C_{COUPLING}$ capacitors shown in Figure 3 produce a cutoff frequency equal to 23Hz.

The output coupling capacitors also influence the output transient behavior at power-up and when activating or deactivating shutdown. As $C_{COUPLING}$'s value increases, output transient magnitude can also increase. This increase can be mitigated by a corresponding increase in C_{MIDCAP}'s value. A minimum starting point when selecting C_{MIDCAP}'s value is 6.8µF when using 220µF output coupling capacitors.

SELECTING THE INPUT CAPACITOR VALUE

Amplifiying the lowest audio frequencies requires a relatively high value input coupling capacitor, (C_{IN} in Figure 3). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the headphones used in portable systems have limited ability to reproduce signals below 60Hz. Applications using headphones with this limited frequency response reap little improvement by using a high value input capacitor. A small value of Ci (in the range of 0.1µF to 1.0µF), is recommended.

DRIVING POWERED SPEAKERS

Though the LM4980 is design primarily to drive headphones, in many cases, it may be called on to act as a line level driver when powered speakers or other devices may be connected to the amplifier outputs. For powered speakers or other devices with typical input resistances (10kΩ) that are significantly higher than the typical headphone resistance (32Ω), the output transients may not sufficiently suppressed when using the Figure 3 circuit. If this is anticipated, a minor modification of an additional resistor (a nominal value of 1kΩ) between each output and ground in the Figure 3 circuit is needed to ensure that the output transient suppression is not compromised. This reduces both the load resistance seen by the LM4980 and the magnitude of power-on and shutdown output transients.

POWER DISSIPATION

Power dissipation has to be evaluated and considered when designing a successful amplifier. A direct consequence of the power delivered to a load an amplifier is internal power dissipation. The maximum per-amplifier power dissipation for a given application can be derived from the power dissipation graphs or from Equation 2.

$$PDMAX = V_{DD}^2 / 2\pi R_{LOAD} \tag{2}$$

It is critical that the maximum junction temperature T_{JMAX} of 150°C is not exceeded. Since the typical application is for headphone operation (16Ω impedance) using a 3.0V supply the maximum power dissipation is less than 29mW. Therefore, in the case of this headphone amplifier, the power dissipation is not a major concern.

POWER SUPPLY BYPASSING

As with any amplifier, proper supply bypassing is important for low noise performance and high power supply rejection. The capacitor location on the power supply pins should be as close to the device as possible. Typical applications employ a 3.0V regulator with 10µF tantalum or electrolytic capacitor and a ceramic bypass capacitor which aid in supply stability. This does not eliminate the need for local power supply bypassing connected as close as possible to the LM4980's supply pin. A power supply bypass capacitor value in the range of 1.0µF to 10µF is recommended.

MICRO POWER SHUTDOWN

The voltage applied to the shutdown ($\overline{SHDN}$) pin controls the LM4980's shutdown function. Activate micro-power shutdown by applying a logic-low voltage to the $\overline{SHDN}$ pin. When active, the LM4980's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The trigger point is 0.4V (max) for a logic-low level, and 1.4V (min) for a logic-high level. The low 0.1µA (typ) shutdown current is achieved by applying a voltage that is as near as ground as possible to the $\overline{SHDN}$ pin. A voltage that is higher than ground may increase the shutdown current.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100kΩ pull-up resistor between the $\overline{SHDN}$ pin and GND. Connect the switch between the $\overline{SHDN}$ pin and V_{DD}. Select normal amplifier operation by closing the switch. Opening the switch connects the $\overline{SHDN}$ pin to ground, activating micro-power shutdown. The switch and resistor ensure that the $\overline{SHDN}$ pin will not float. This prevents unwanted state changes. In a system with a microprocessor or microcontroller, use a digital output to apply the control voltage to the $\overline{SHDN}$ pin. Driving the $\overline{SHDN}$ pin with active circuitry eliminates the pull-up resistor.

SUGGESTED PCB SCHEMATIC

Figure 45 is the schematic for the suggested PCB Layout. This schematic and its associated PCB provide both a lean tested layout and platform that can be used to verify the LM4980's outstanding audio performance.

Suggested PCB Design and Layout

Figure 46 through Figure 49 show a suggested PCB layout for a headphone amplifier circuit using the LM4980 .

PCB Layout Guidelines

This section provides practical guidelines for mixed signal PCB layout that involves various digital/analog power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results will depend heavily on the final layout.

MINIMIZING THD+N

PCB trace impedance on the power, ground, and all output traces should be minimized to achieve optimal THD performance. Therefore, use PCB traces that are as wide as possible for these connections. As the gain of the amplifier is increased, the trace impedance will have an ever increasing adverse affect on THD performance. At unity-gain (0dB) the parasitic trace impedance effect on THD performance is reduced but still a negative factor in the THD performance of the LM4980 in a given application.

GENERAL MIXED SIGNAL LAYOUT RECOMMENDATION

Power and Ground Circuits

For two layer mixed signal design, it is important to isolate the digital power and ground trace paths from the analog power and ground trace paths. Star trace routing techniques (bringing individual traces back to a central point rather than daisy chaining traces together in a serial manner) can greatly enhance low level signal performance. Star trace routing refers to using individual traces to feed power and ground to each circuit or even device. This technique will require a greater amount of design time but will not increase the final price of the board. The only extra parts required may be some jumpers.

Single-Point Power and Ground Connections

The analog power traces should be connected to the digital traces through a single point (link). A "PI-filter" can be helpful in minimizing high frequency noise coupling between the analog and digital sections. Further, place digital and analog power traces over the corresponding digital and analog ground traces to minimize noise coupling.

Placement of Digital and Analog Components

All digital components and high-speed digital signal traces should be located as far away as possible from analog components and circuit traces.

Avoiding Typical Design / Layout Problems

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other do it at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and cross talk.

Schematic for the LM4980 Suggested PCB Layout

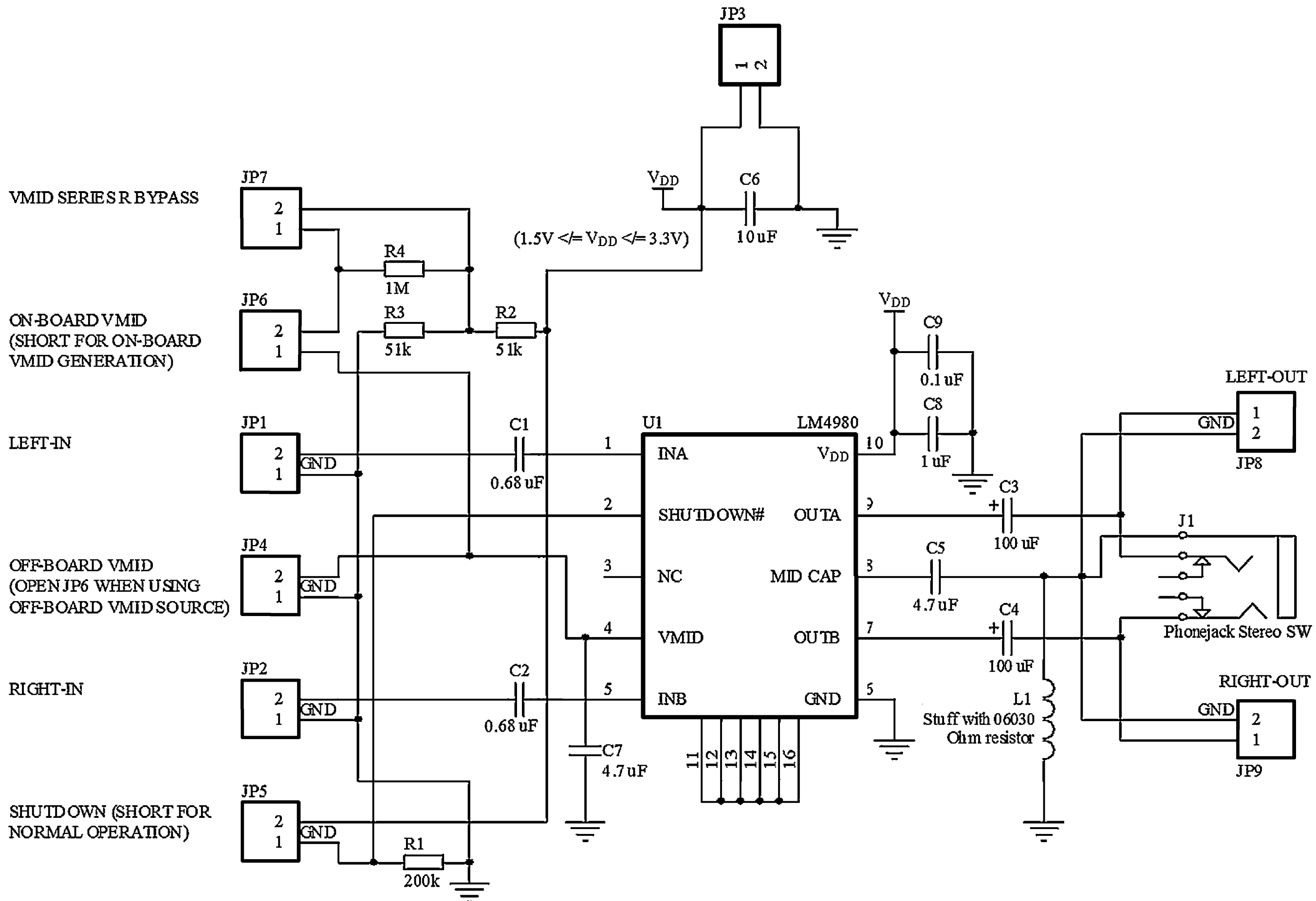

Figure 45.

Suggested PCB Layout

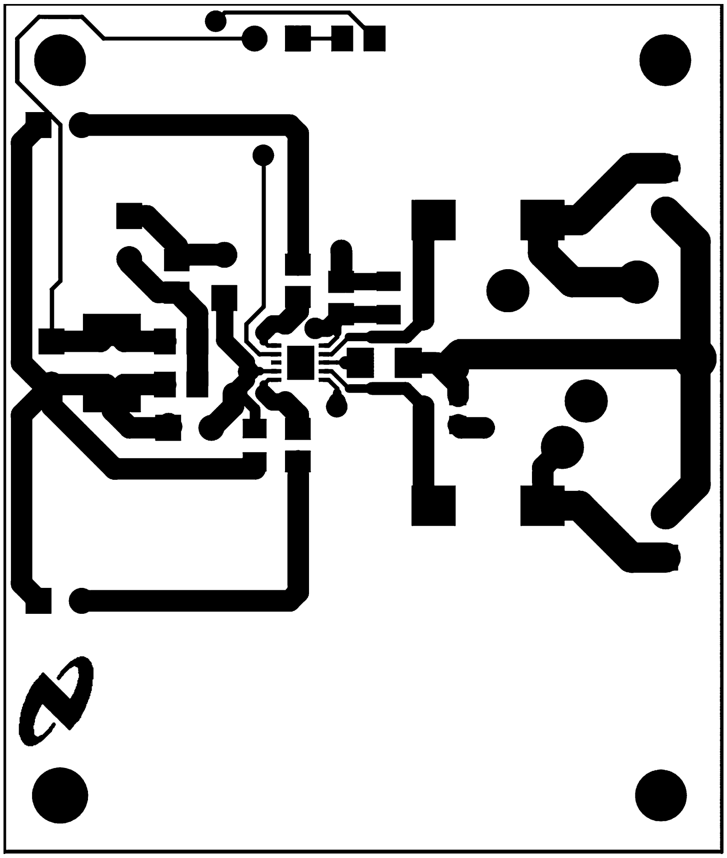

Figure 46. Top Layer

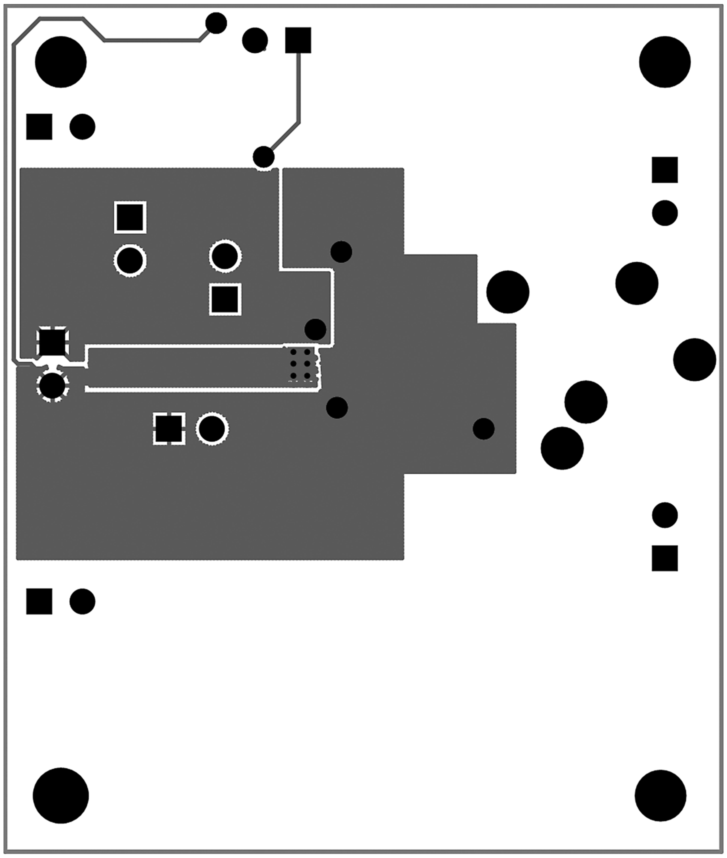

Figure 47. Bottom Layer

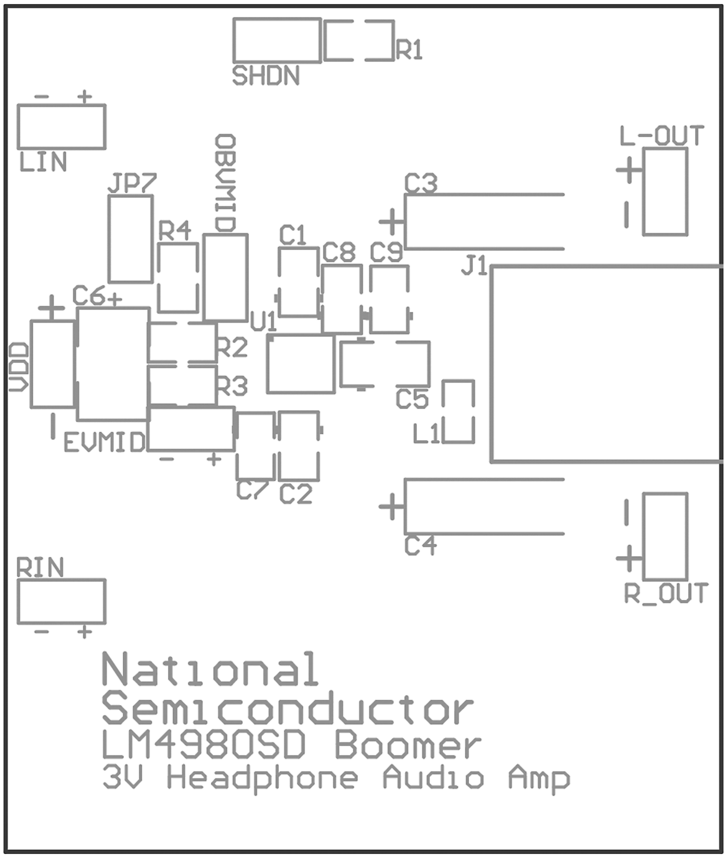

Figure 48. Silkscreen Layer

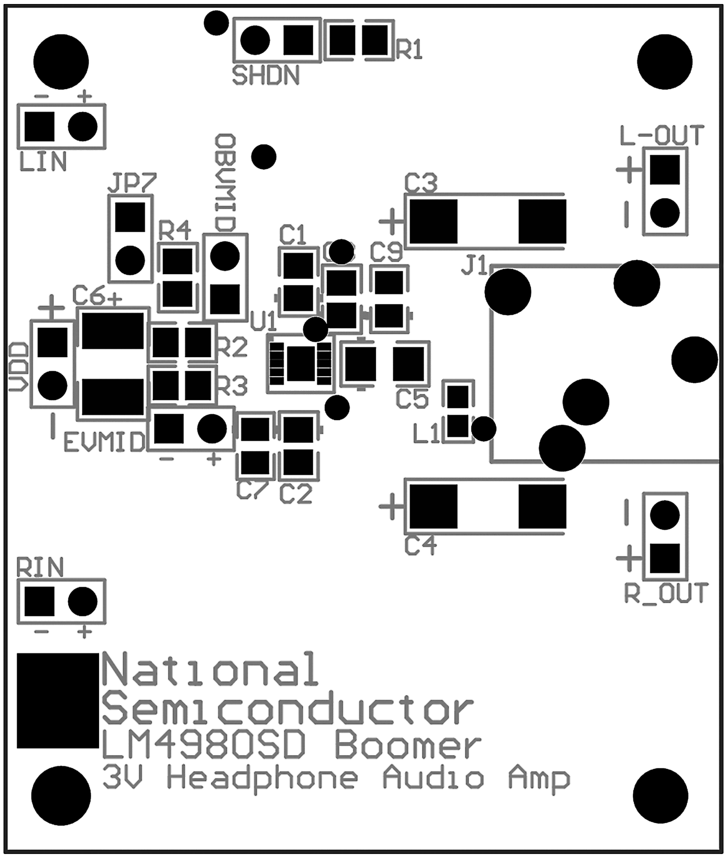

Figure 49. Top Layer Pads

REVISION HISTORY

Rev	Date	Description
1.0	6/08/05	Initial release.
1.1	6/29/05	Correct typographical and schematic errors. Re-released D/S to the WEB.
1.2	7/18/05	Replaced curves 20142971 and 72 with 20142990 and 91 respectively, then re-released D/S to the WEB.

Changes from Revision B (April 2013) to Revision C **Page**

- Changed layout of National Data Sheet to TI format 21

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM4980SD/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L4980	Samples
LM4980SDX/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L4980	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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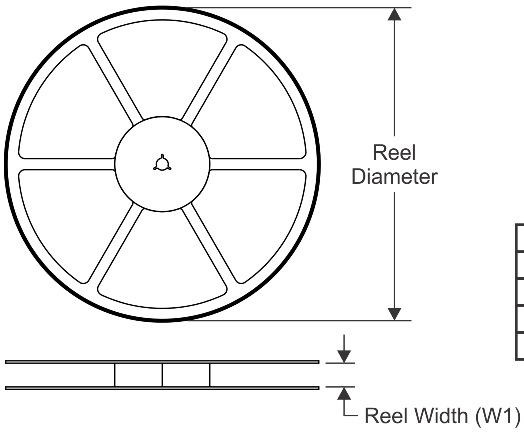
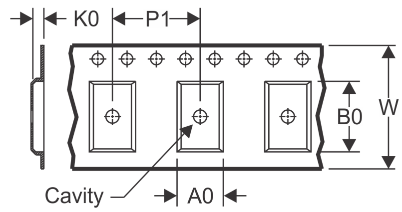
TAPE AND REEL INFORMATION

REEL DIMENSIONS

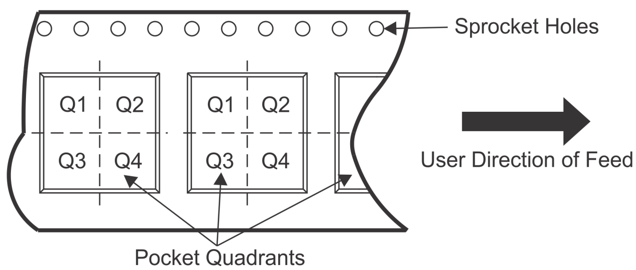


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

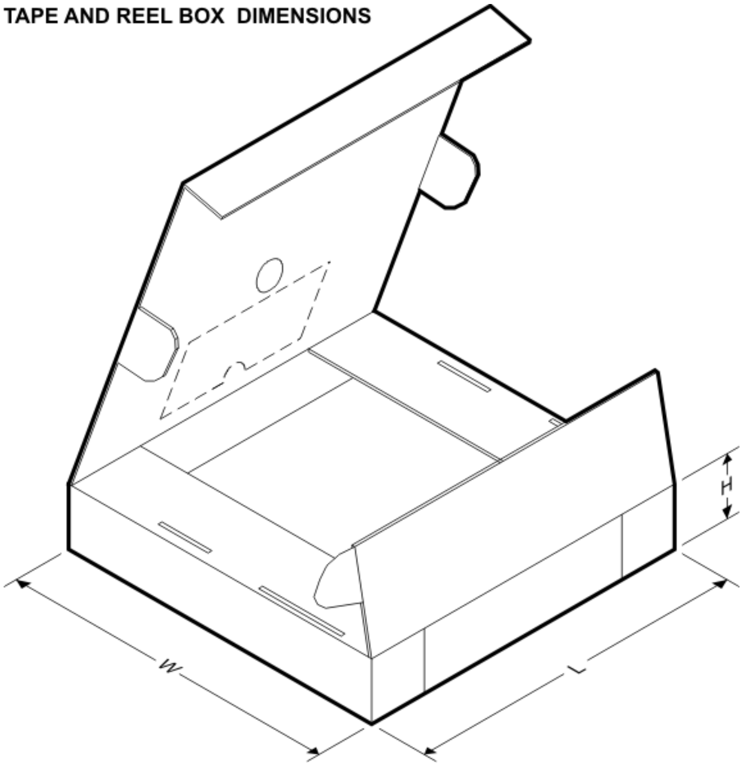
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4980SD/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM4980SDX/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

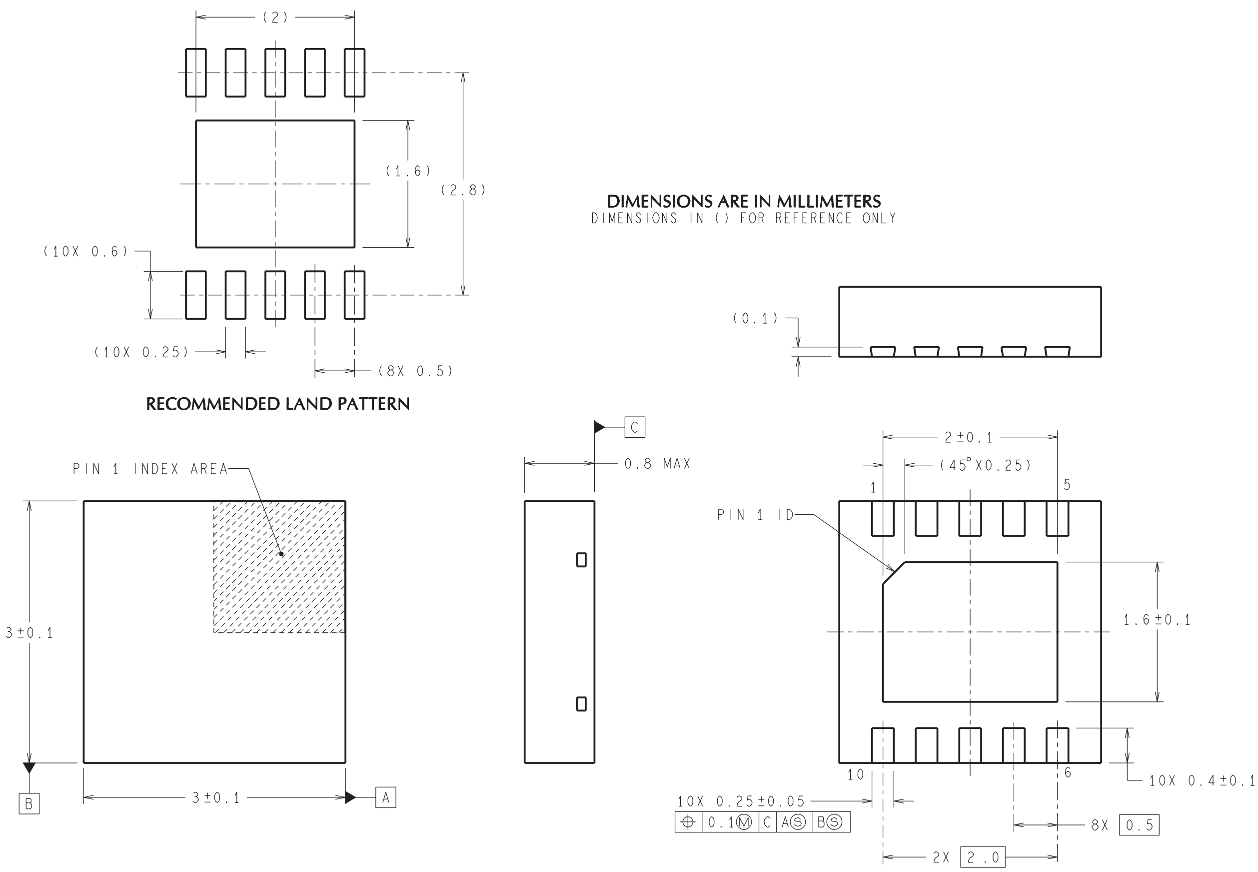
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4980SD/NOPB	WSON	DSC	10	1000	203.0	190.0	41.0
LM4980SDX/NOPB	WSON	DSC	10	4500	367.0	367.0	35.0

DSC0010A



SDA10A (Rev A)