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Digital Input Class-D Amplifier with IV Feedback and Brownout Protection

MAX98388/MAX98389

General Description

The MAX98388/MAX98389 is a small, cost-effective mono digital input amplifier with integrated IV feedback. The device operates over a wide supply voltage range from 2.3V to 10V. With this supply range, both versions support single-cell, two-cell, and externally regulated/boosted portable applications. MAX98388 is optimized for up to 5.5V applications (single-cell), while MAX98389 is optimized for 5V to 10V cases (two-cell).

The Class-D playback amplifier pairs Class-AB level audio performance with the efficiency needed to extend battery life in portable applications. Active emissions-limiting (AEL) and edge-rate limiting circuitry combined with a spread-spectrum modulation (SSM) scheme reduces EMI and eliminates the need for the output filtering required for traditional Class-D amplifiers.

The device provides a precision output current sense channel and an output voltage feedback channel. The data collected by these channels can be transmitted on the audio data output and enables algorithms such as audio enhancement, bass boosting, speaker protection, and haptic functions to be run on the host audio DSP.

The device includes a programmable threshold playback channel ALC that provides brownout protection for batteries in portable systems, and robust thermal and overcurrent protection to prevent device damage.

The device provides a PCM interface for audio playback and IV feedback data and pairs this with a standard I^2C interface for device control and status readback. The PCM interface supports common audio data formats such as I^2S, left justified, and TDM timing. A unique clocking structure eliminates the need for an external high-frequency reference clock. In addition to reducing device size and pin count, eliminating this clock saves interface power while reducing the risk of EMI from high-speed switching and potential board coupling issues.

The package connections are designed to only require edge routing, allowing the use of the cost-effective wafer-level package (WLP) with no requirement for expensive bump vias. The device is available in a 0.4mm pitch 16-bump WLP package and is specified over the extended -40°C to +85°C temperature range.

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Benefits and Features

- Wide Amplifier Supply Range (2.3V to 10V)
  - Supports Both Single-Cell and Two-Cell Cases
- High-Performance Class-D Amplifier
  - Up to 111dB Dynamic Range (A-Weighted)
  - 10µV_{RMS} Output Noise (Single-Cell Mode)
  - 14.5µV_{RMS} Output Noise (Two-Cell Mode)
- High Output Power (THD+N ≤ 1%)
  - 1.32W Output Power into 4Ω (V_{PVDD} = 3.7V)
  - 2.4W Output Power into 4Ω (V_{PVDD} = 5V)
  - 5.15W Output Power into 4Ω (V_{PVDD} = 7.4V)
  - 9.1W Output Power into 4Ω (V_{PVDD} = 10V)
- High Amplifier Efficiency (Playback Only Power)
  - 76% Efficiency at 0.1W into 4Ω (V_{PVDD} = 5V)
  - 85.5% Efficiency at 1W into 4Ω (V_{PVDD} = 5V)
  - 90% Efficiency at 1W into 8Ω (V_{PVDD} = 5V)
- Peak THD+N Better than -83dB at 1kHz
- Low Total Quiescent Power
  - 9.3mW (V_{PVDD} = 3.7V, IV Feedback Disabled)
  - 13.9mW (V_{PVDD} = 3.7V, IV Feedback Enabled)
  - 16.1mW (V_{PVDD} = 5V, IV Feedback Enabled)
  - 22.5mW (V_{PVDD} = 7.4V, IV Feedback Enabled)
- Low < 5µW Software Shutdown Power
- 1ms Turn-On Time (f_S = 48kHz, Ramp Disabled)
- Five Sample Playback Delay (f_S < 50kHz, f_{IN} = 1kHz)
- No External Reference Clock Required
- Playback Sample Rates from 8kHz to 96kHz
- Trimmed Class-D Switching Frequency for EMI Planning
- Extensive Click-and-Pop Reduction Circuitry
- Programmable ALC for Brownout Protection
- Robust Short-Circuit and Thermal Protection
- Available in Space-Saving Package:
  - 2.93mm^2, 16-pin WLP (0.4mm Pitch)

Applications

- AR/VR Wearables
- LRA Haptic Drive
- Smart Watches and IoT Devices
- Gaming Devices
- Notebooks and Tablets

***Ordering Information* appears at end of data sheet.**

19-101683; Rev 1; 9/23

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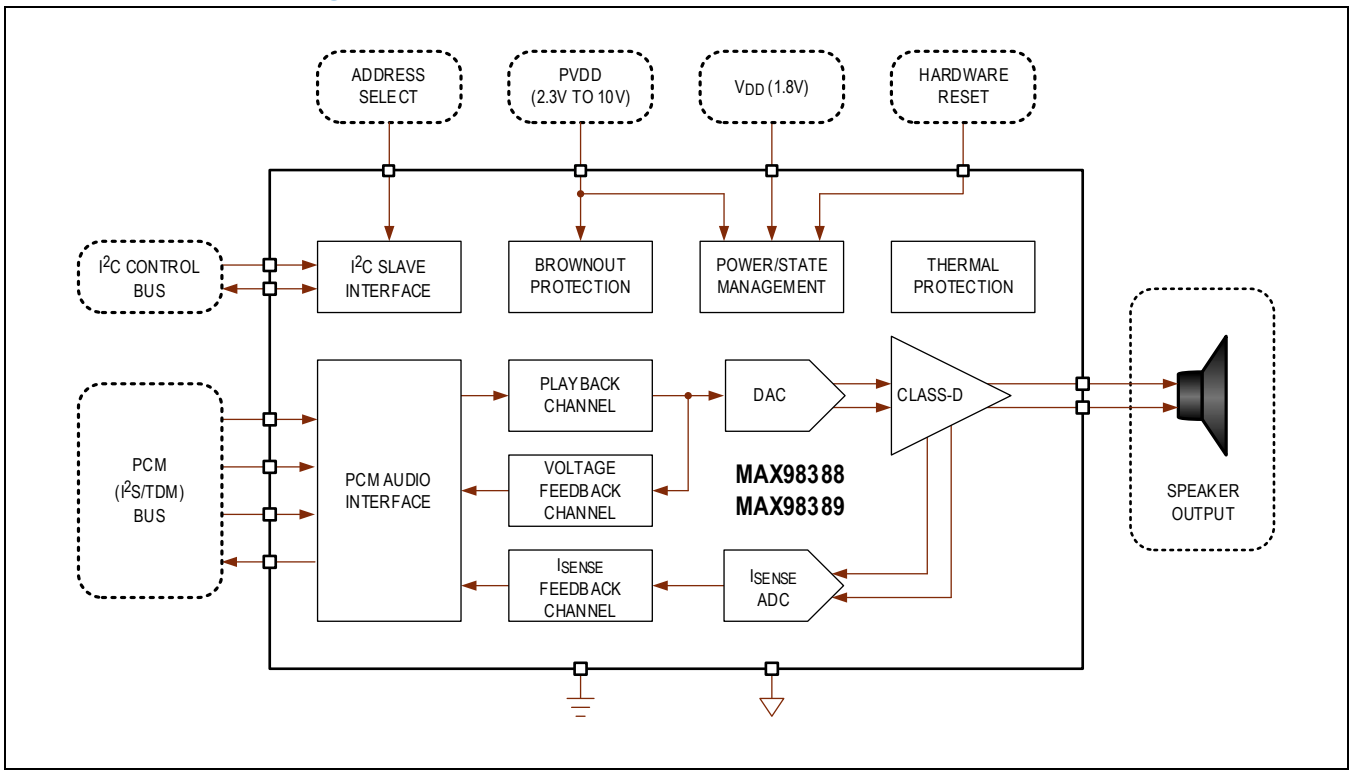
Simplified Block Diagram



Absolute Maximum Ratings

GND to PGND ..... -0.1V to +0.1V

V_{PVDD} to PGND ..... -0.3V to +12V

V_{DD} to GND ..... -0.3V to +2.2V

OUTP, OUTN to PGND ..... -0.3V to V_{PVDD} + 0.3V

BCLK, LRCLK, DIN, DOUT to GND ..... -0.3V to V_{DD} + 0.3V

ADDR, I.C. to GND ..... -0.3V to V_{DD} + 0.3V

All Other Pins to GND ..... -0.3V to +2.2V

Duration of short between OUTP and OUTN ..... Continuous

Duration of short circuit between OUTP or OUTN and PGND, PVDD, or V_{DD} ..... Continuous

Continuous power dissipation (T_A = +70°C, derate 13.7mW/°C above +70°C) 1.38W

Junction temperature ..... +150°C

Operating temperature range ..... -40°C to +85°C

Storage temperature range ..... -65°C to +150°C

Soldering temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W161P1Z+1
Outline Number	*21-100636*
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	57.93°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM-LEVEL							
PVDD Supply Voltage Range	V_{PVDD}	Guaranteed by PSRR test	Two-cell/ boosted mode	5		10	V
			Single-cell mode	3.0		5.5	
		Guaranteed by PSRR test, single-cell mode, the device is functional but parametric performance is not guaranteed		2.3			
V_{DD} Supply Voltage Range	V_{DD}	Guaranteed by PSRR test		1.71	1.8	1.89	V
PVDD Undervoltage Lockout	V_{UVLO_PVDD}	Single-cell mode	V_{PVDD} falling	1.9		2.2	V
		Two-cell mode	V_{PVDD} falling	4.4		4.7	
PVDD UVLO Hysteresis		Single-cell mode (Note 4)		150	200		mV
		Two-cell mode (Note 4)		120	150		
V_{DD} Undervoltage Lockout	V_{UVLO_VDD}	V_{DD} falling		1.3		1.6	V
V_{DD} UVLO Hysteresis		Note 4		20	40		mV
V_{DD} Supply Ramp Rate				0.1			V/ms
Thermal Shutdown Temperature		THERMSHDN_THRES = 0x2			155		°C
Thermal Shutdown Hysteresis					15		°C
Thermal Warning Temperature		THERMWARN_THRES = 0x2			115		°C
Thermal Warning Hysteresis					15		°C
POWER CONSUMPTION / QUIESCENT POWER CONSUMPTION							
Total Quiescent Power		Both supplies, IV feedback disabled	V_{PVDD} = 3.7V		9.3		mW
		Both supplies, IV feedback enabled	V_{PVDD} = 3.7V		13.9		
			V_{PVDD} = 5V		16.1		
			V_{PVDD} = 7.4V		22.5		
PVDD Quiescent Current		IV feedback disabled	V_{PVDD} = 3.7V		1.37		mA
V_{DD} Quiescent Current		IV feedback disabled			2.38		mA
PVDD Quiescent Current		IV feedback enabled	V_{PVDD} = 3.7V		1.42	2	mA
			V_{PVDD} = 5V		1.59	2.2	
			V_{PVDD} = 7.4V		1.86	2.5	
V_{DD} Quiescent Current		IV feedback enabled			4.83	6.8	mA
POWER CONSUMPTION / SOFTWARE SHUTDOWN POWER CONSUMPTION							
PVDD Software Shutdown Current	I_{PVDD_SWSD}	No toggling on PCM interface pins, T_A = +25°C	V_{PVDD} = 3.7V, single-cell mode		0.3	4	µA
			V_{PVDD} = 7.4V, two-cell mode		0.4	5	

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Software Shutdown Current	I_{VDD_SWSD}	No toggling on PCM interface pins, T_A = +25°C			1.5	6	µA
POWER CONSUMPTION / HARDWARE SHUTDOWN POWER CONSUMPTION							
PVDD Hardware Shutdown Current	I_{PVDD_HWSD}	T_A = +25°C	V_{PVDD} = 3.7V, single-cell mode		0.3	4	µA
			V_{PVDD} = 7.4V, two-cell mode		0.4	5	
V_{DD} Hardware Shutdown Current	I_{VDD_HWSD}	T_A = +25°C			0.2	1	µA
ENABLE / DISABLE TIMING							
Turn-On Time	t_{ON}	Software-shutdown state to active state (device ready to receive audio data)	Volume ramp disabled, f_S ≥ 44.1kHz		0.6	1	ms
			Volume ramp disabled, f_S < 44.1kHz (Note 4)		1.1	2.3	
			Volume ramp enabled, f_S ≥ 44.1kHz		2.3	2.7	
			Volume ramp enabled, f_S < 44.1kHz (Note 4)		2.9	4.2	
Turn-Off Time	t_{OFF}	From full-active state operation to software-shutdown state (power down done status)	Volume ramp disabled		70	100	µs
			Volume ramp enabled, f_S ≥ 44.1kHz		4.3	4.6	ms
			Volume ramp enabled, f_S < 44.1kHz		6.7	8	
Hardware Enable Time	t_{HW_EN}	Transition time from the hardware-shutdown state ($\overline{RESET}$ input set high) to the software-shutdown state (I^2C ready)				1.5	ms
Hardware Reset Time	t_{HW_RES}	Transition time from software reset (write 1 to the software reset bit) until the device is reset and returns to the software-shutdown state (I^2C ready)				0.4	ms
Hardware Disable Assert Time	t_{HW_DIS}	Minimum time $\overline{RESET}$ input must be asserted low to ensure the device transitions to the hardware-shutdown state			1		µs
SPEAKER DIGITAL AUDIO CHANNEL / DAC DIGITAL FILTER CHARACTERISTICS (f_{LRCLK} < 50kHz) (Note 2)							
Passband Cutoff Frequency	f_{PLP}	Ripple < δ_P		0.452 x f_S			Hz
		Droop < -3dB		0.457 x f_S			
Passband Ripple	δ_P	f_{IN} < f_{PLP}, referenced to signal level at 1kHz, digital filter response only		-0.1		+0.1	dB
Stopband Cutoff Frequency	f_{SLP}	Attenuation > δ_S				0.49 x f_S	Hz

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Stopband Attenuation	δ_S	$f_{IN} > f_{SLP}$		75			dB
Group Delay		f_{IN} = 1kHz			5		samples
SPEAKER DIGITAL AUDIO CHANNEL / DAC DIGITAL FILTER CHARACTERISTICS (f_{LRCLK} ≥ 50kHz) (Note 2)							
Passband Cutoff Frequency	f_{PLP}	Ripple < δ_P		0.227 x f_S			Hz
		Droop < -3dB		0.314 x f_S			
Passband Ripple	δ_P	$f_{IN} < f_{PLP}$, referenced to signal level at 1kHz, digital filter response only		-0.1		+0.1	dB
Stopband Cutoff Frequency	f_{SLP}	Attenuation < δ_S				0.49 x f_S	Hz
Stopband Attenuation	δ_S	$f_{IN} > f_{SLP}$		80			dB
Group Delay		f_{IN} = 1kHz			5.5		samples
SPEAKER DIGITAL AUDIO CHANNEL / DC BLOCKING DIGITAL FILTER CHARACTERISTICS (Note 2)							
DC Attenuation				80			dB
DC Blocking Filter -3dB Cutoff Frequency	f_C	f_S = 8kHz, 16kHz, 32kHz, 48kHz, and 96kHz			1.872		Hz
		f_S = 44.1kHz, 88.2kHz			1.72		
SPEAKER CLASS-D AMPLIFIER							
Output Offset Voltage	V_{OS}	T_A = +25°C		-3	±0.3	+3	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH	Amp output power down, single-cell mode		-77		dBV
			Amp output power down, two-cell mode		-71		
			Amp output power-up, single-cell mode		-76		
			Amp output power-up, two-cell mode		-70		
Output Noise	e_N	A-weighted, 24-bit, or 32-bit data	Single-cell mode, DAC low-power mode		10		μV_{RMS}
			Two-cell mode, DAC high-performance mode		14.5		
Dynamic Range	DR	A-weighted, 24-bit or 32-bit data, single-cell mode, DAC low power mode (Note 3)	Z_{SPK} = 4Ω + 33µH		110		dB
			Z_{SPK} = 8Ω + 33µH		110.5		
		A-weighted, 24-bit or 32-bit data, two-cell mode, V_{PVDD} = 7.4V, DAC high-performance mode (Note 3)	Z_{SPK} = 8Ω + 33µH		111		

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, T_A = +25°C, single-cell mode, V_{PVDD} = 5V	P_{OUT} = 1W, Z_{SPK} = 4Ω + 33µH		-87		dB
			P_{OUT} = 0.7W, Z_{SPK} = 8Ω + 33µH		-85	-73	
		f_{IN} = 1kHz, T_A = +25°C, two-cell mode, V_{PVDD} = 7.4V, POUT = 1.4W, Z_{SPK} = 8Ω + 33µH (Note 4)			-83	-74	
Full-Scale Output Voltage	FS	Single-cell mode, +12dB gain			12.4		dBV
		Two-cell mode, +18dB gain			18.4		
Efficiency	η	f_{IN} = 1kHz, Z_{SPK} = 8Ω + 33µH, V_{PVDD} = 5V	THD+N = 10%		92		%
			P_{OUT} = 1W		90		
			P_{OUT} = 0.1W		80		
			P_{OUT} = 0.05W		72		
		f_{IN} = 1kHz, Z_{SPK} = 4Ω + 33µH, V_{PVDD} = 5V	P_{OUT} = 1W		85.5		
			P_{OUT} = 0.1W		76		
			P_{OUT} = 0.05W		69		
Output Power	P_{OUT}	f_{IN} = 1kHz, THD+N ≤ 1%, Z_{SPK} = 4Ω + 33µH	V_{PVDD} = 3.7V, single-cell mode		1.32		W
			V_{PVDD} = 5V, single-cell mode		2.4		
			V_{PVDD} = 7.4V, two-cell mode		5.15		
			V_{PVDD} = 8.4V, two-cell mode		6.54		
		f_{IN} = 1kHz, THD+N ≤ 10%, Z_{SPK} = 4Ω + 33µH	V_{PVDD} = 3.7V, single-cell mode		1.65		
			V_{PVDD} = 5V, single-cell mode		3.0		
			V_{PVDD} = 7.4V, two-cell mode		6.35		
			V_{PVDD} = 8.4V, two-cell mode		8.02		
		f_{IN} = 1kHz, THD+N ≤ 1%, Z_{SPK} = 8Ω + 33µH	V_{PVDD} = 3.7V, single-cell mode		0.77		
			V_{PVDD} = 5V, single-cell mode		1.4		
			V_{PVDD} = 7.4V, two-cell mode		3.05		
			V_{PVDD} = 8.4V, two-cell mode		3.87		
		f_{IN} = 1kHz, THD+N ≤ 10%, Z_{SPK} = 8Ω + 33µH	V_{PVDD} = 3.7V, single-cell mode		0.95		
			V_{PVDD} = 5V, single-cell mode		1.72		
			V_{PVDD} = 7.4V, two-cell mode		3.75		

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
			V_{PVDD} = 8.4V, two-cell mode		4.84		
Class-D Switching Frequency	f_{SW}			285	300	315	kHz
Spread-Spectrum Bandwidth	f_{SSM}				±14		kHz
Intermodulation Distortion	IMD	ITU-R, 19kHz/ 20kHz, 1:1, V_{IN} = -3dBFS, Z_{SPK} = 8Ω + 33µH			-70		dB
Frequency Response		Full response from digital audio interface input to the amplifier output		-0.25		+0.25	dB
Output Stage On-Resistance	R_{ON}	PMOS + NMOS (Full H-Bridge), T_A = +25°C			0.38		Ω
Output Current Limit	I_{LIM}			3.5			A
Output Current Limit Auto-Restart Time					20		ms
Minimum Load Resistance	R_L	Nominal 4Ω load minus 25%			3		Ω
Maximum Device-to-Device Speaker Channel Phase Mismatch		Output phase shift between multiple devices from 20Hz to 20kHz across all sample rates and DAI operating modes			1.5		deg
Minimum Load Inductance		In series with a 4Ω load			0		µH
Maximum Load Inductance		In series with a 4Ω load			100		µH
SPEAKER CLASS-D AMPLIFIER / POWER-SUPPLY REJECTION							
PVDD DC Power Supply Rejection Ratio	PSRR	DC level, V_{PVDD} = 2.3V to 10V, T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞		70	85		dB
PVDD AC Power Supply Rejection Ratio	PSRR	V_{RIPPLE} = 200mV_{PP}, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH	f_{RIPPLE} = 217Hz		85		dB
			f_{RIPPLE} = 1kHz		85		
			f_{RIPPLE} = 10kHz		70		
V_{DD} DC Power Supply Rejection Ratio	PSRR	DC level, V_{DD} = 1.71V to 1.89V, T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞		70	85		dB
V_{DD} AC Power Supply Rejection Ratio	PSRR	V_{RIPPLE} = 100mV_{PP}, T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH	f_{RIPPLE} = 217Hz		90		dB
			f_{RIPPLE} = 1kHz		90		
			f_{RIPPLE} = 10kHz		80		
SPEAKER CLASS-D AMPLIFIER / POWER-SUPPLY INTERMODULATION							
Power-Supply Intermodulation			PVDD supply, f_{RIPPLE} = 217Hz,		-80		dB

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
		T_A = +25°C, f_{IN} = 1kHz, P_{OUT} = 400mW, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH	V_{RIPPLE} = 200mV_{PP}				
			V_{DD} supply, f_{RIPPLE} = 217Hz, V_{RIPPLE} = 100mV_{PP}		-80		
SPEAKER OUTPUT VOLTAGE FEEDBACK (Note 2)							
Resolution					16		Bits
Sample Rate	f_{S_VFB}			8		96	kHz
Voltage Range	V_{SPK}	Single-cell mode			±5.5		V
		Two-cell mode			±11		
Power Supply Feedthrough	PSF	No input signal, AC relative to PVDD or V_{DD}, f_{RIPPLE} = 1kHz, V_{RIPPLE} = 100mVP-P			-100		dB
Max Device to Device Voltage Feedback Channel Phase Mismatch		f_{IN} = 1kHz			0.05		Samples
SPEAKER OUTPUT VOLTAGE FEEDBACK / DIGITAL FILTER CHARACTERISTICS (f_S < 50kHz) (Note 2)							
Passband Ripple		f_{IN} < f_{PLP}, referenced to the signal level at 1kHz		-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	Ripple < δ_P		0.44 x f_S			Hz
		Droop < -3dB		0.45 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit				0.58 x f_S	Hz
Lowpass Filter Stopband Attenuation				40			dB
Group Delay		f_{IN} = 1kHz			8		Samples
SPEAKER OUTPUT VOLTAGE FEEDBACK / DIGITAL FILTER CHARACTERISTICS (f_S ≥ 50kHz) (Note 2)							
Passband Ripple		f_{IN} ≤ f_{PLP}, referenced to the signal level at 1kHz		-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz		0.235 x f_S			Hz
		Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz		0.29 x f_S			
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit				0.58 x f_S	Hz
Lowpass Filter Stopband Attenuation				40			dB
Group Delay		f_{IN} = 1kHz			9		Samples
SPEAKER OUTPUT CURRENT SENSE ADC (Note 2)							
Resolution					16		Bits
Sample Rate	f_{S_ISNS}			8		96	kHz
Current Range	I_{SPK}				±3		A

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dynamic Range	DNR	f_{IN} = 1kHz, unweighted			73		dB
Total Harmonic Distortion + Noise	THD+N	f_{IN} = 1kHz, Z_{LOAD} = 4Ω + 33µH	Single-cell mode, V_{PVDD} = 5V, I_{SPK} = 0.6A_{RMS}		-59		dB
			Two-cell mode, V_{PVDD} = 7.4V, I_{SPK} = 1A_{RMS}		-63		
		f_{IN} = 1kHz, Z_{LOAD} = 8Ω + 33µH	Single-cell mode, V_{PVDD} = 5V, I_{SPK} = 0.3A_{RMS}		-54		
			Two-cell mode, V_{PVDD} = 7.4V, I_{SPK} = 0.5A_{RMS}		-59		
Differential Mode Gain		Open loop current sense channel response		0.98		1.02	
Differential Mode Gain Variability		Across supply, T_A = -40°C to +85°C (Note 4)		-2.5		+2.5	%
Maximum Common Mode Gain					-60		dB
Highpass Cutoff Frequency		-3dB limit, across all sample rates				2	Hz
DC Offset Current		DC blocking filter enabled, T_A = +25°C		-0.12		+0.12	mA
		DC blocking filter disabled, T_A = +25°C	MAX98388, V_{PVDD} = 3.7V, single-cell mode	-2		+2	
		DC blocking filter disabled, T_A = +25 °C	MAX98389, V_{PVDD} = 7.4V, two-cell mode	-4		+4	
Voltage and Current Accuracy Drift Tracking		T_A = 0°C to +85°C, relative to +25°C			0.4		%
Speaker Amplifier Voltage to Current Sense Crosstalk		MAX98388, f_{IN} = 1kHz	Single-cell mode		-80		dB
		MAX98389, f_{IN} = 1kHz	Two-cell mode		-75		
Power Supply Feedthrough	PSF	No input signal, AC relative to V_{PVDD} or V_{DD}, f_{RIPPLE} = 1kHz, V_{RIPPLE} = 100mV_{P-P}			65		dB
Max Current Sense to Voltage Feedback Channel Phase Mismatch		f_{IN} = 1kHz			0.05		Samples
Max Device to Device Current Sense Channel Phase Mismatch		f_{IN} = 1kHz			0.05		Samples
SPEAKER OUTPUT CURRENT ADC / DIGITAL FILTER CHARACTERISTICS (f_S < 50 kHz) (Note 2)							
Passband Ripple		$f_{IN} \le f_{PLP}$		-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	-3dB limit		0.44 x f_S			Hz

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit				0.58 x f_S	Hz
Lowpass Filter Stopband Attenuation				40			dB
Max Group Delay		f_{IN} = 1kHz			8		Samples
SPEAKER OUTPUT CURRENT ADC / DIGITAL FILTER CHARACTERISTICS (f_S ≥ 50kHz) (Note 2)							
Passband Ripple		f_{IN} ≤ f_{PLP}		-0.225		+0.225	dB
Lowpass Filter Cutoff Frequency	f_{PLP}	Droop < -3dB, 88.2kHz ≤ f_S ≤ 96kHz		0.23 x f_S			Hz
Lowpass Filter Stopband Frequency	f_{SLP}	-40dB limit				0.58 x f_S	Hz
Lowpass Filter Stopband Attenuation				40			dB
Max Group Delay		f_{IN} = 1kHz			9		Samples
BROWNOUT PROTECTION ALC							
Brownout Response Time		From PVDD below voltage threshold event to audio attenuation			12		µs
Brownout Voltage Threshold Range		PVDD falling, single-cell mode	Minimum threshold setting		2.5		V
			Maximum threshold setting		3.625		
		PVDD falling, two-cell mode	Minimum threshold setting		5		
			Maximum threshold setting		7.25		
Brownout Voltage Threshold Hysteresis		Single-cell mode, MAX98388 (Note 4)		60	75		mV
		Two-cell mode, MAX98389 (Note 4)		120	150		
Brownout Voltage Threshold Accuracy		All brownout voltage threshold settings	Single-cell mode, MAX98388	-3		+3	%
			Two-cell mode, MAX98389	-3		+3	
DIGITAL I/O / INPUT—DIN, BCLK, LRCLK							
Input Voltage High	V_{IH}			0.7 x V_{DD}			V
Input Voltage Low	V_{IL}					0.3 x V_{DD}	V
Input Leakage Current				-1		+1	µA
Input Hysteresis	V_{HYS}	Note 4		75			mV
Maximum Input Capacitance	C_{IN}				10		pF
Internal Pull-Down Resistance	R_{PD}	BCLK, LRCLK, and DIN			3		MΩ
DIGITAL I/O / INPUT—$\overline{\text{RESET}}$							
Input Voltage High	V_{IH}			0.75 x V_{VDD}			V
Input Voltage Low	V_{IL}					0.25 x V_{VDD}	V

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current			-1		+1	µA
Input Hysteresis	V_{HYS}	Note 4	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
DIGITAL I/O / INPUT—SCL, SDA, ADDR						
Input Voltage High	V_{IH}		0.7 x V_{DD}			V
Input Voltage Low	V_{IL}				0.3 x V_{DD}	V
Input Leakage Current		T_A = +25 °C, input high	-1		+1	µA
Input Hysteresis	V_{HYS}	Note 4	75			mV
Maximum Input Capacitance	C_{IN}			10		pF
DIGITAL I/O / OPEN DRAIN OUTPUT—SDA						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Output High Leakage Current	I_{OH}	T_A = +25°C	-1		+1	µA
DIGITAL I/O / PUSH-PULL OUTPUT—DOUT						
Output Voltage High	V_{OH}	I_{OH} = 3mA	V_{DD} - 0.3			V
Output Voltage Low	V_{OL}	I_{OL} = 3mA			0.3	V
Output Current	I_{OH}	Maximum-drive mode		8		mA
		High-drive mode		6		
		Normal-drive mode		4		
		Reduced-drive mode		2		
PCM DIGITAL AUDIO INTERFACE / CLOCK CHARACTERISTICS						
LRCLK Frequency Range	f_{LRCLK}	All DAI operating modes	8		96	kHz
BCLK Frequency Range	f_{BCLK}	I^2S/left-justified modes	0.256		12.288	MHz
		TDM mode	0.256		24.576	
BCLK Duty Cycle	DC		45		55	%
BCLK Period	t_{BCLK}	I^2S/left-justified modes	81.3			ns
		TDM mode	40			
Maximum BCLK Input Low-Frequency Jitter		Maximum allowable jitter before a -20dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter ≤ 40kHz		0.2		ns
Maximum BCLK Input High-Frequency Jitter		Maximum allowable jitter before a -60dBFS, 20kHz input has a 1dB reduction in THD+N, RMS jitter > 40kHz		1		ns
PCM DIGITAL AUDIO INTERFACE / CLOCK AND DATA INPUT TIMING						
LRCLK to BCLK Active Edge Setup Time	$t_{SYNCSET}$		4			ns
LRCLK to BCLK Active Edge Hold Time	$t_{SYNCHOLD}$		4			ns

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 0V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Z_{SPK} = ∞ between OUTP and OUTN, Single-Cell Mode, AC Measurement Bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, Typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIN to BCLK Active Edge Setup Time	t_{SETUP}		4			ns
DIN to BCLK Active Edge Hold Time	t_{HOLD}		4			ns
DIN Frame Delay After LRCLK Edge		Measured in the number of BCLK cycles, set by selected TDM mode	0		2	cycles
PCM DIGITAL AUDIO INTERFACE / DATA OUTPUT TIMING						
BCLK Inactive Edge to DOUT Delay	t_{CLKTX}				14	ns
BCLK Active Edge to DOUT Hi-Z Delay	t_{HIZ}		4		18	ns
BCLK Inactive Edge to DOUT Active Delay	t_{ACTV}		0		14	ns
I^2C INTERFACE TIMING						
Serial Clock Frequency	f_{SCL}				1000	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition	$t_{HD,STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for a Repeated START Condition	$t_{SU,STA}$		0.26			µs
Data Hold Time	$t_{HD,DAT}$		0		450	ns
Data Setup Time	$t_{SU,DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_R	Note 4	20		120	ns
SDA and SCL Receiving Fall Time	t_F	Note 4	20 x V_{DD}/ 5.5V		120	ns
SDA Transmitting Fall Time	t_F		20 x V_{DD}/ 5.5V		120	ns
Setup Time for STOP Condition	$t_{SU,STO}$		0.26			µs
Bus Capacitance	C_B				550	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Digital filter performance is invariant over temperature and is production tested at T_A = +25°C.

Note 3: Measured using the EIAJ method with a -60dBFS output signal at 1kHz referenced to output power at 1% THD+N.

Note 4: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

Timing Diagrams

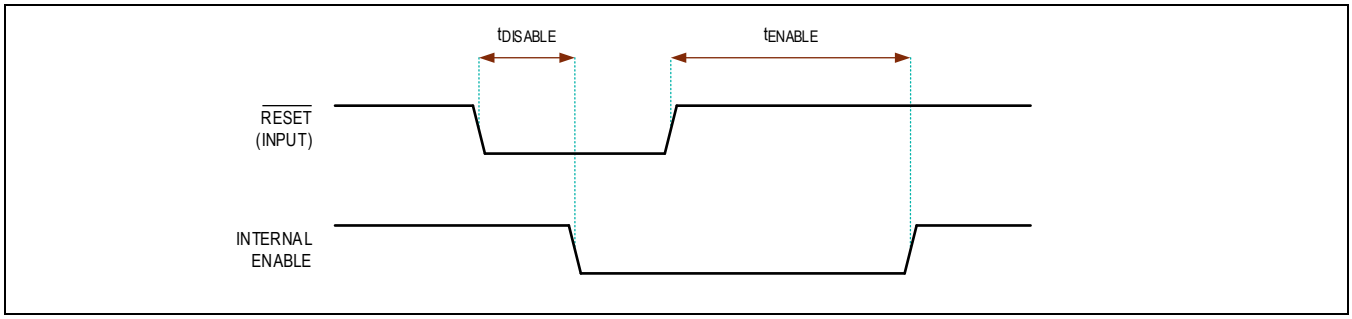


Figure 1. Hardware Enable and Disable Timing Diagram

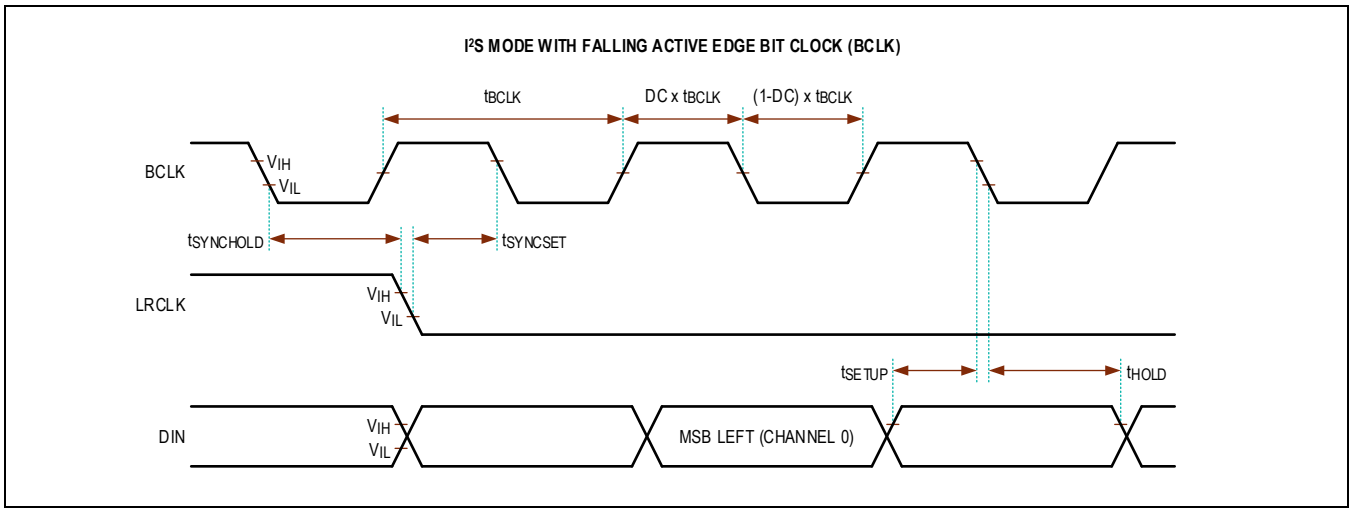


Figure 2. PCM Interface Timing Diagram for I^2S Mode

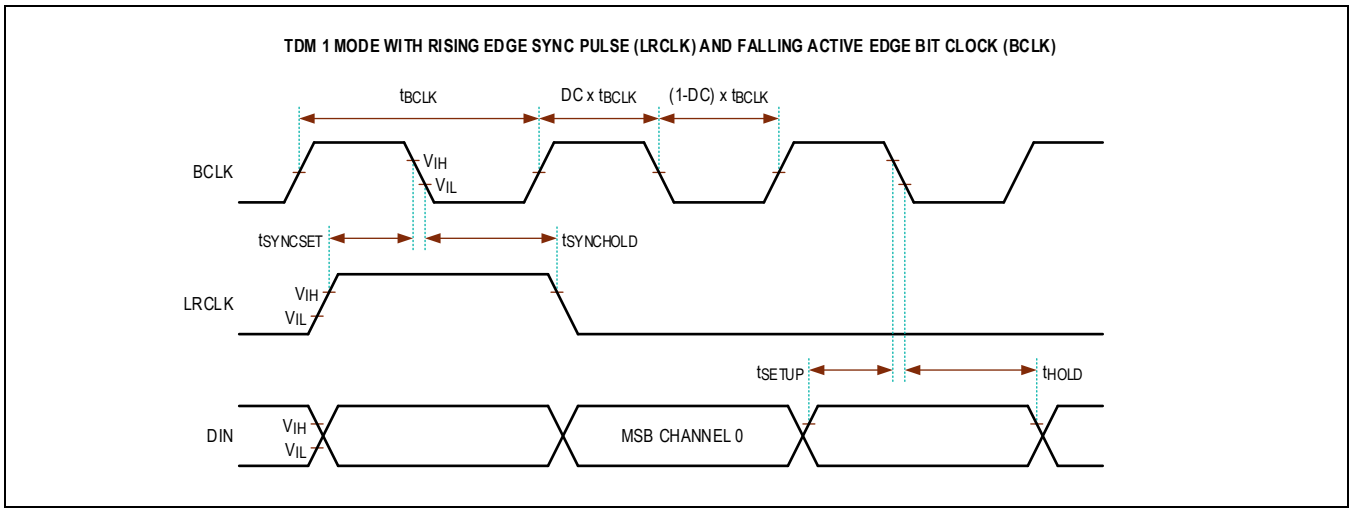


Figure 3. PCM Interface Timing Diagram for TDM 1 Mode

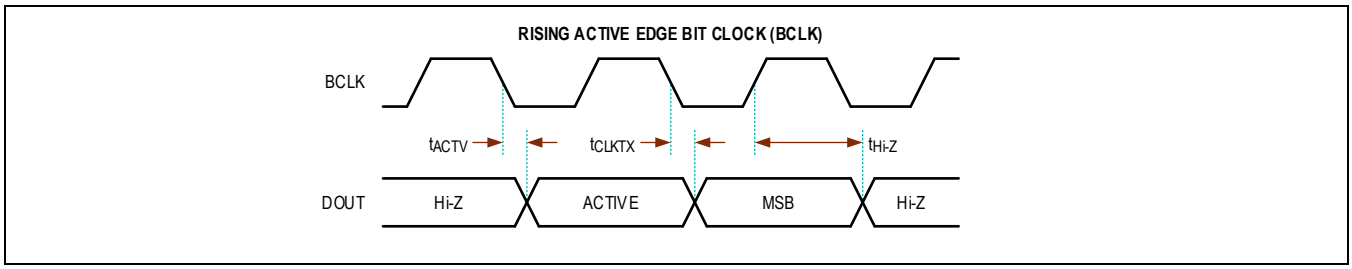


Figure 4. PCM Interface Data Output Timing Diagram

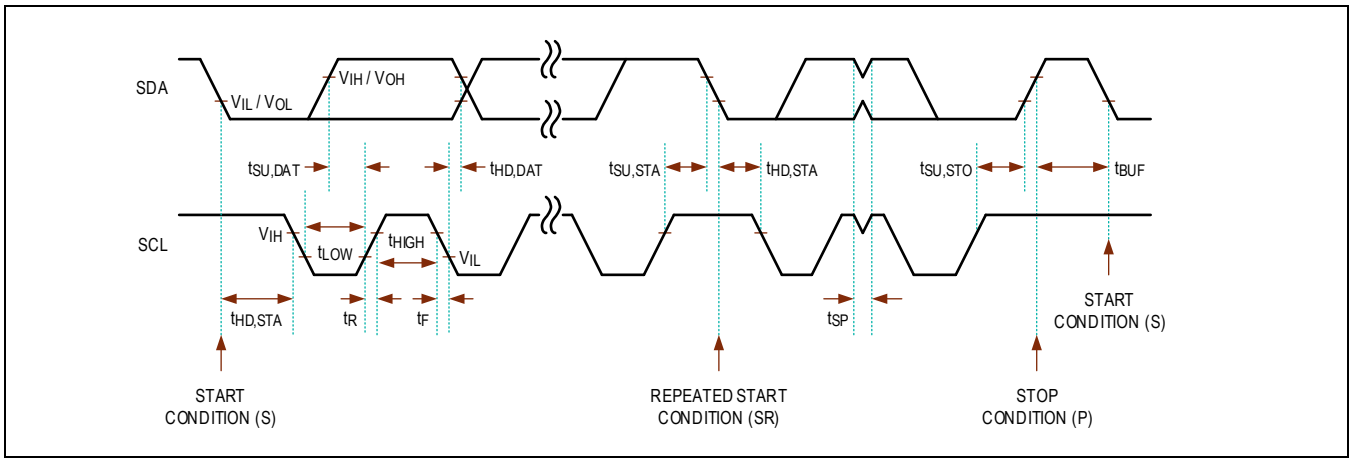
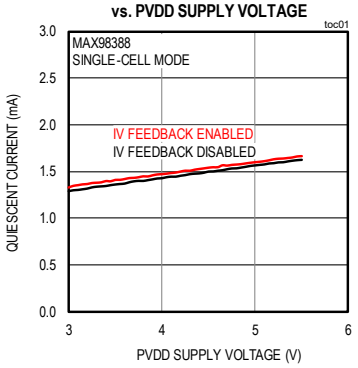


Figure 5. I^2C Peripheral Device Control Interface Timing Diagram

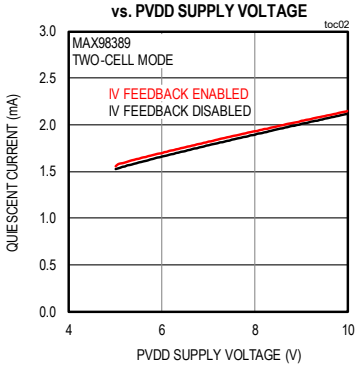
Typical Operating Characteristics

(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 1.8V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Playback Data Word Size ≥ 24-Bit, Z_{SPK} = Open between OUTP and OUTN, T_A = +25°C)

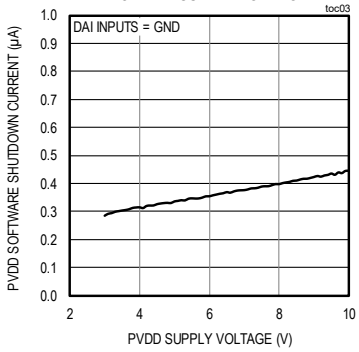
PVDD QUIESCENT CURRENT vs. PVDD SUPPLY VOLTAGE



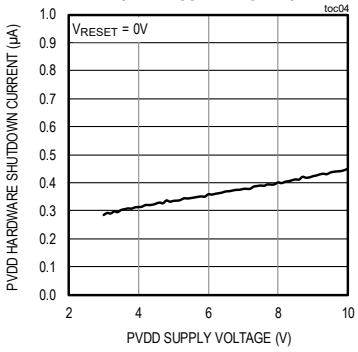
PVDD QUIESCENT CURRENT vs. PVDD SUPPLY VOLTAGE



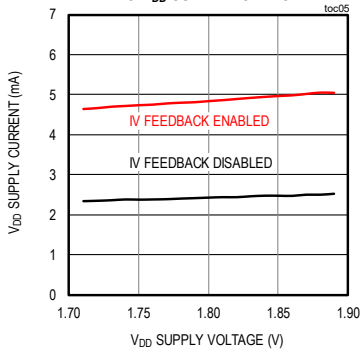
PVDD SOFTWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



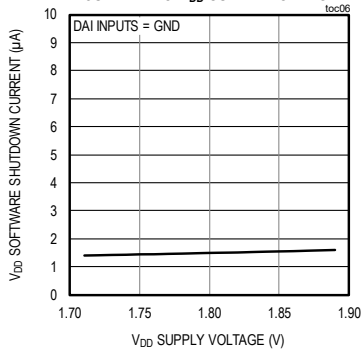
PVDD HARDWARE SHUTDOWN CURRENT vs. PVDD SUPPLY VOLTAGE



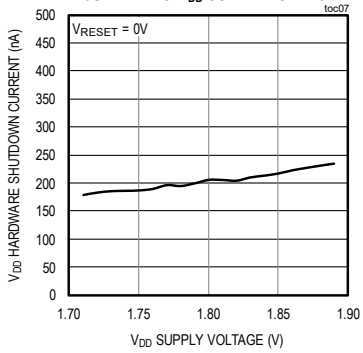
V_{DD} QUIESCENT CURRENT vs. V_{DD} SUPPLY VOLTAGE



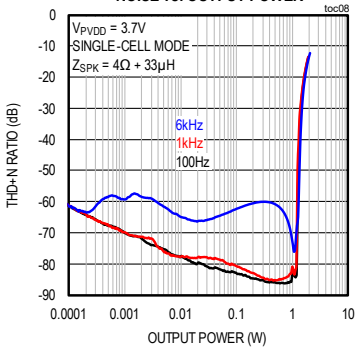
V_{DD} SOFTWARE SHUTDOWN CURRENT vs. V_{DD} SUPPLY VOLTAGE



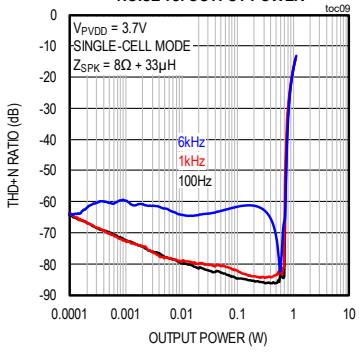
V_{DD} HARDWARE SHUTDOWN CURRENT vs. V_{DD} SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

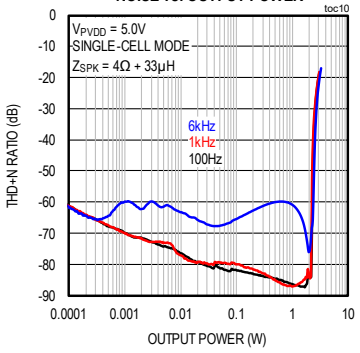


TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER

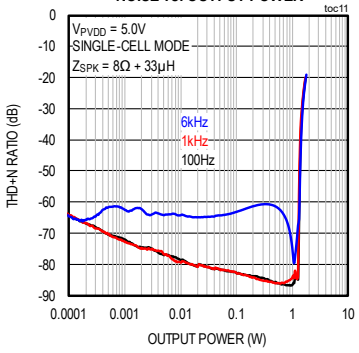


(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 1.8V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Playback Data Word Size ≥ 24-Bit, Z_{SPK} = Open between OUTP and OUTN, T_A = +25°C)

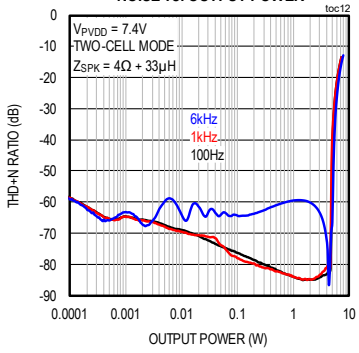
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



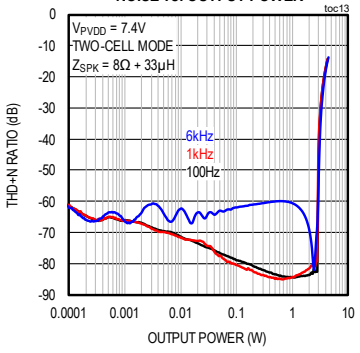
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



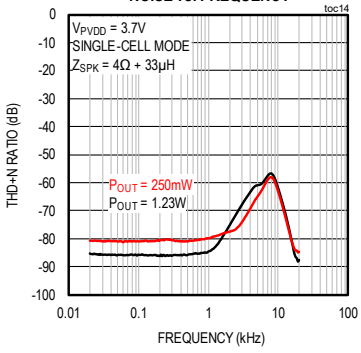
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



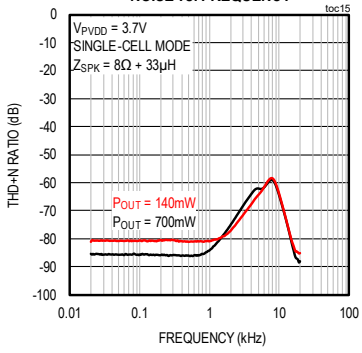
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



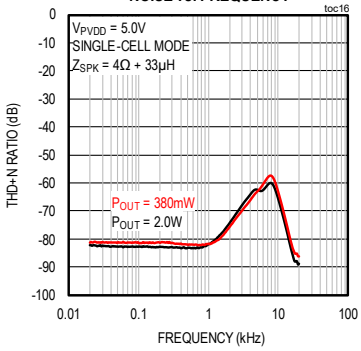
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



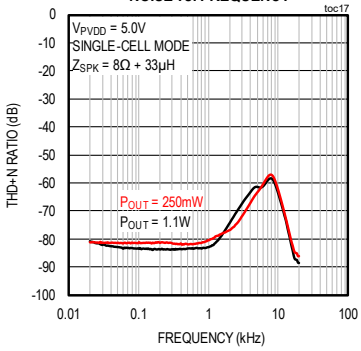
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



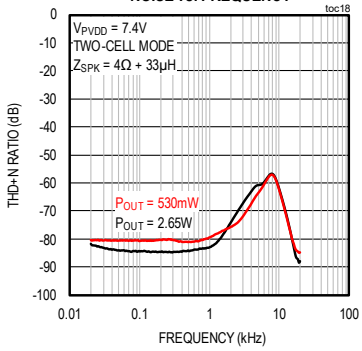
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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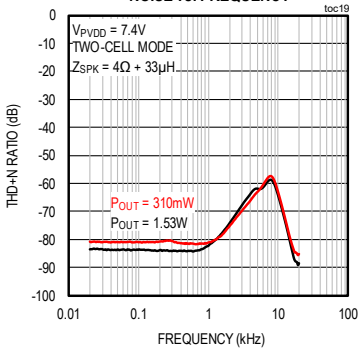
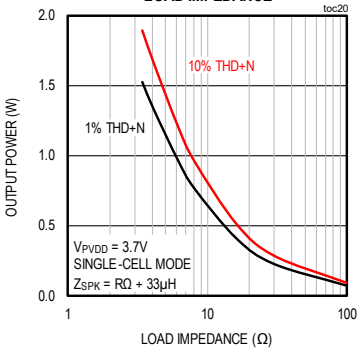
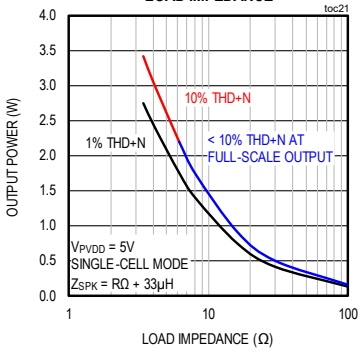
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



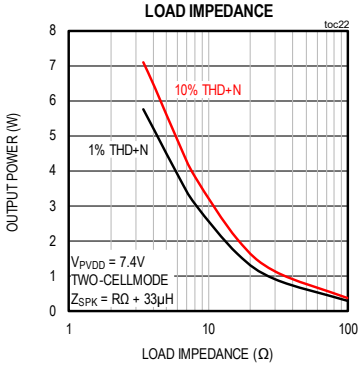
OUTPUT POWER vs. LOAD IMPEDANCE



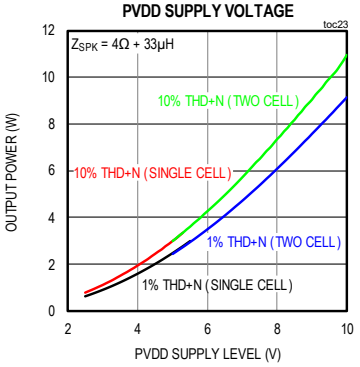
OUTPUT POWER vs. LOAD IMPEDANCE



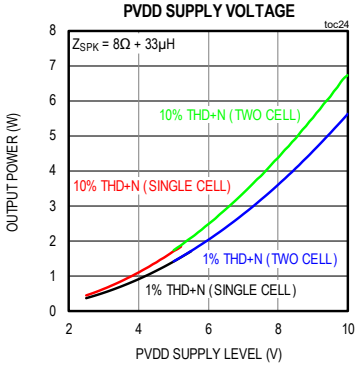
OUTPUT POWER vs. LOAD IMPEDANCE



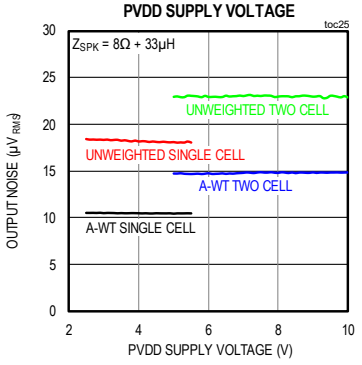
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



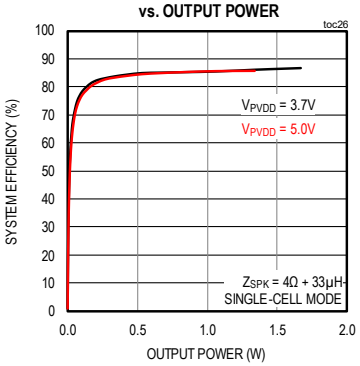
OUTPUT POWER vs. PVDD SUPPLY VOLTAGE



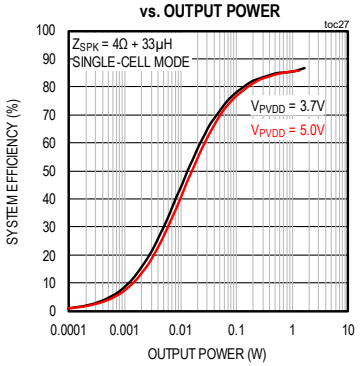
OUTPUT NOISE vs. PVDD SUPPLY VOLTAGE



SYSTEM EFFICIENCY vs. OUTPUT POWER



SYSTEM EFFICIENCY vs. OUTPUT POWER



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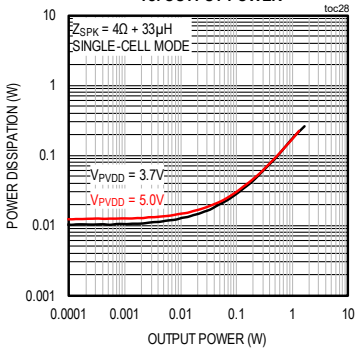
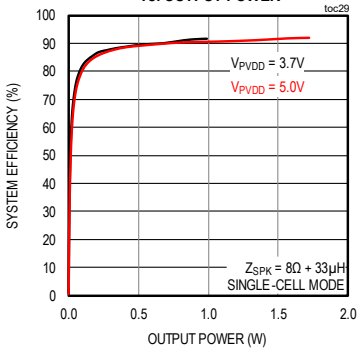
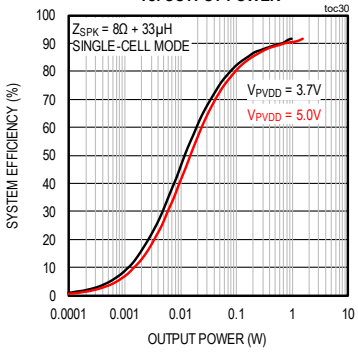
POWER DISSIPATION vs. OUTPUT POWER



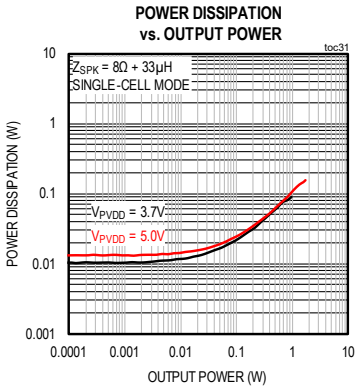
SYSTEM EFFICIENCY vs. OUTPUT POWER



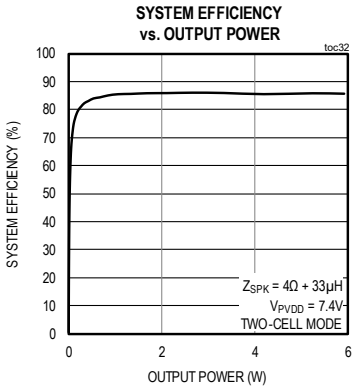
SYSTEM EFFICIENCY vs. OUTPUT POWER



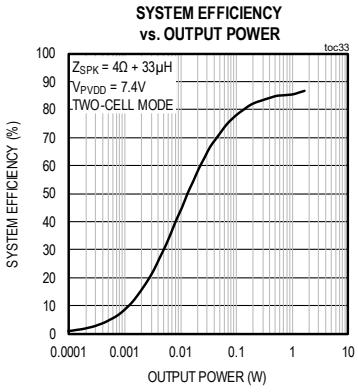
POWER DISSIPATION vs. OUTPUT POWER



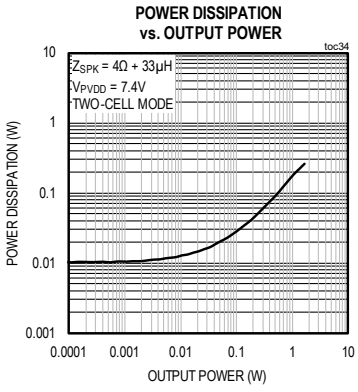
SYSTEM EFFICIENCY vs. OUTPUT POWER



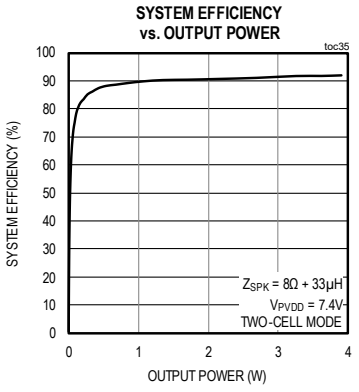
SYSTEM EFFICIENCY vs. OUTPUT POWER



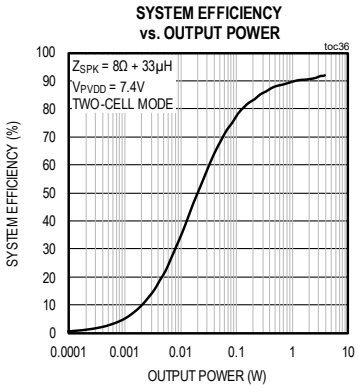
POWER DISSIPATION vs. OUTPUT POWER



SYSTEM EFFICIENCY vs. OUTPUT POWER



SYSTEM EFFICIENCY vs. OUTPUT POWER



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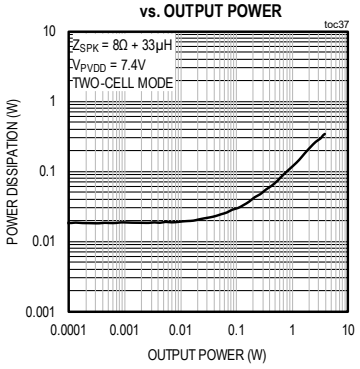
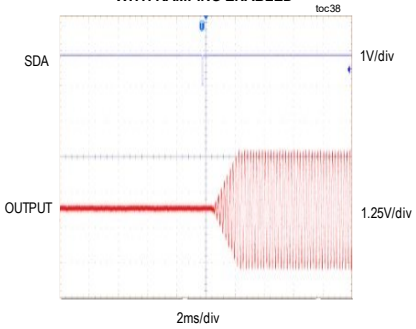
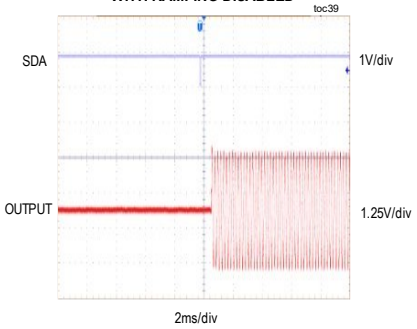
POWER DISSIPATION vs. OUTPUT POWER



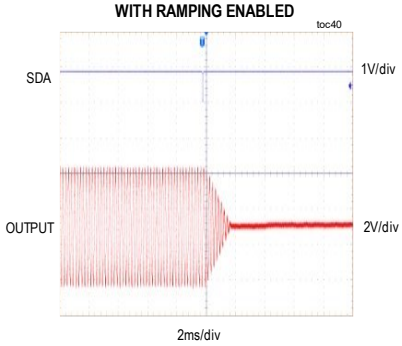
TURN-ON RESPONSE WITH RAMPING ENABLED



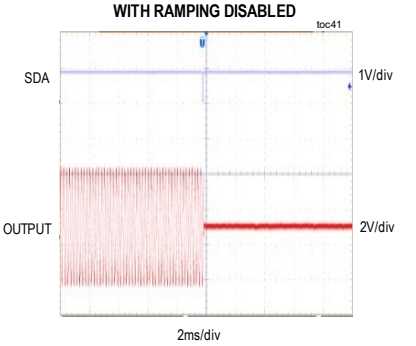
TURN-ON RESPONSE WITH RAMPING DISABLED



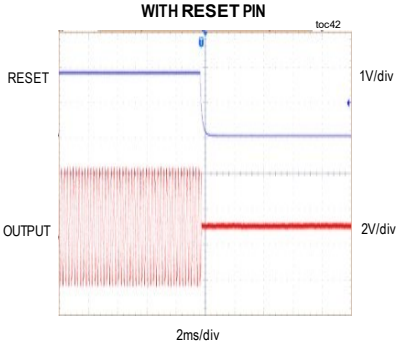
TURN-OFF RESPONSE WITH RAMPING ENABLED



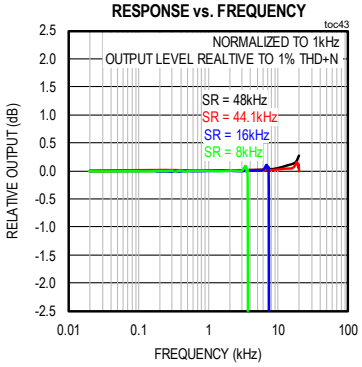
TURN-OFF RESPONSE WITH RAMPING DISABLED



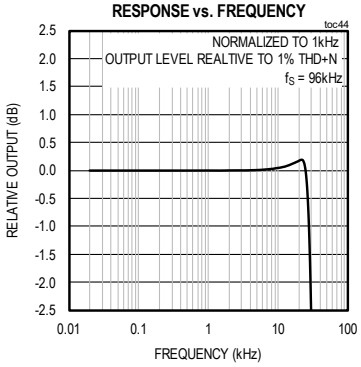
TURN-OFF RESPONSE WITH RESET PIN



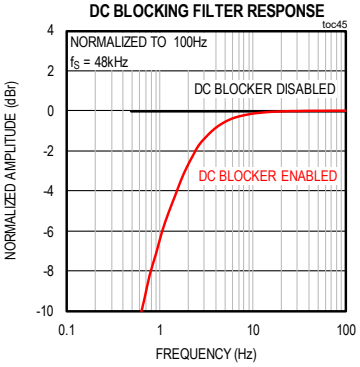
NORMALIZED PLAYBACK CHANNEL RESPONSE vs. FREQUENCY



NORMALIZED PLAYBACK CHANNEL RESPONSE vs. FREQUENCY



PLAYBACK CHANNEL DIGITAL DC BLOCKING FILTER RESPONSE



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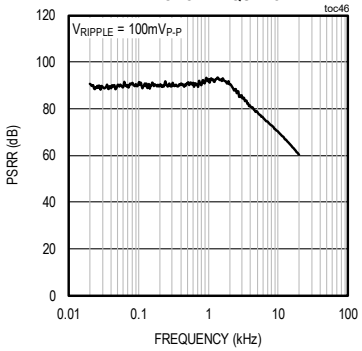
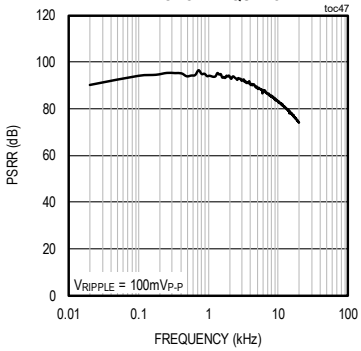
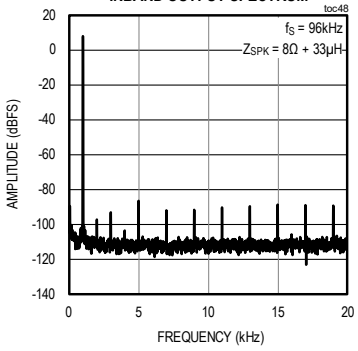
PLAYBACK OUTPUT CHANNEL PVDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



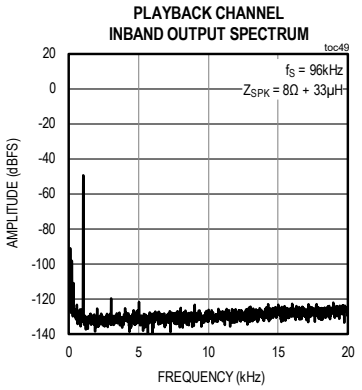
PLAYBACK OUTPUT CHANNEL VDD POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



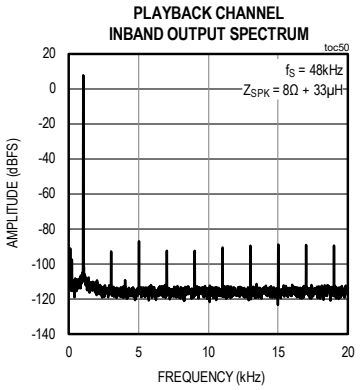
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



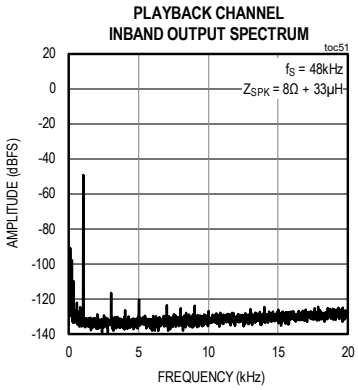
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



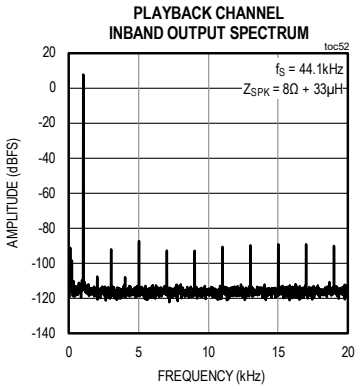
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



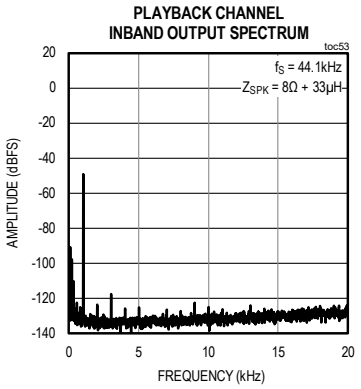
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



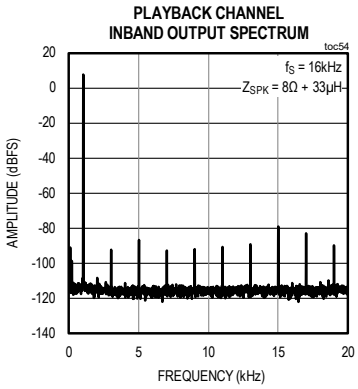
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



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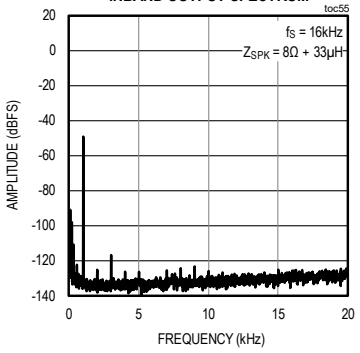
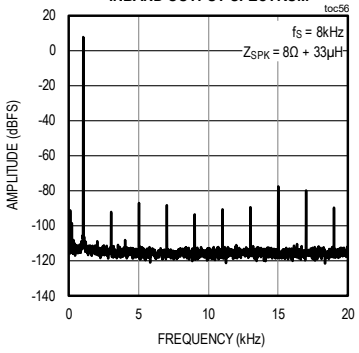
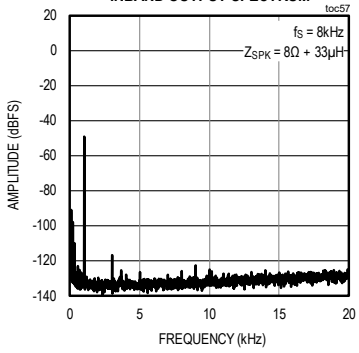
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



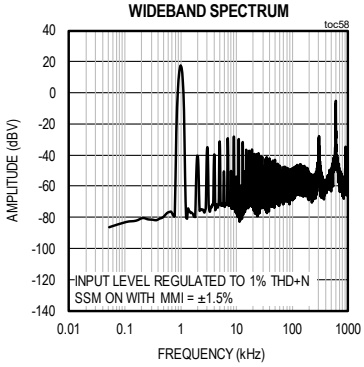
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



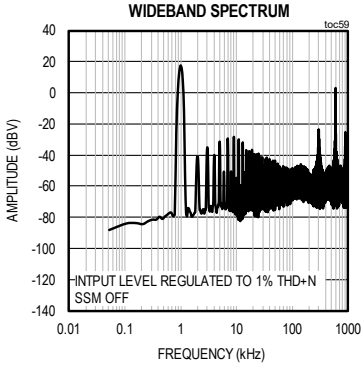
PLAYBACK CHANNEL INBAND OUTPUT SPECTRUM



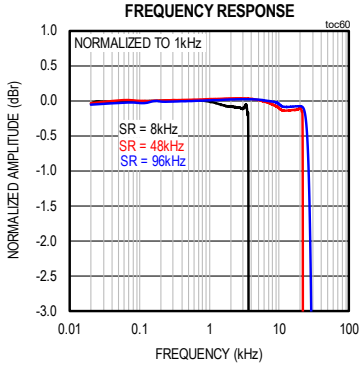
PLAYBACK CHANNEL WIDEBAND SPECTRUM



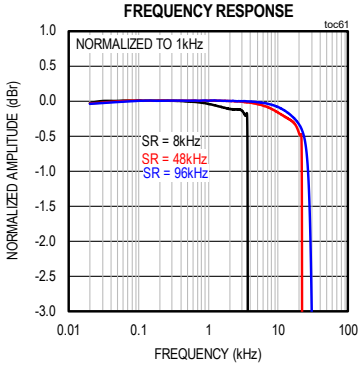
PLAYBACK CHANNEL WIDEBAND SPECTRUM



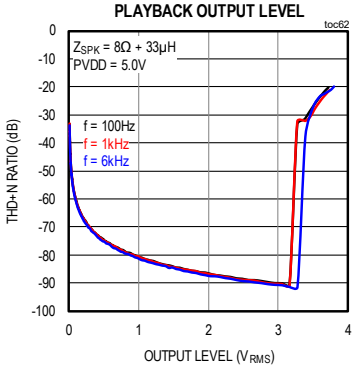
VOLTAGE FEEDBACK CHANNEL FREQUENCY RESPONSE



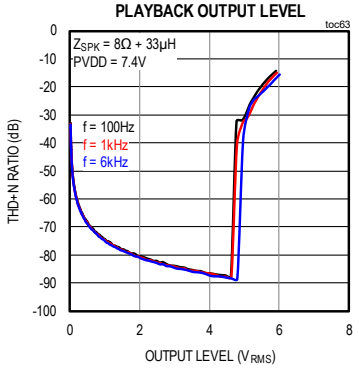
CURRENT SENSE CHANNEL FREQUENCY RESPONSE



VOLTAGE FEEDBACK THD+N vs. PLAYBACK OUTPUT LEVEL



VOLTAGE FEEDBACK THD+N vs. PLAYBACK OUTPUT LEVEL



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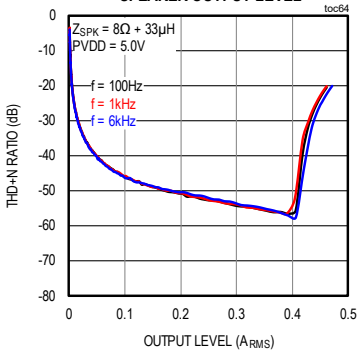
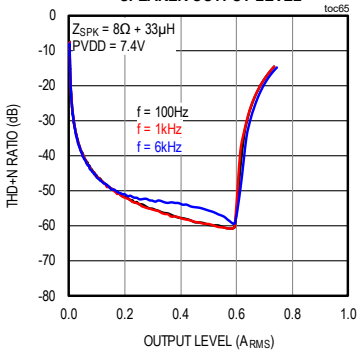
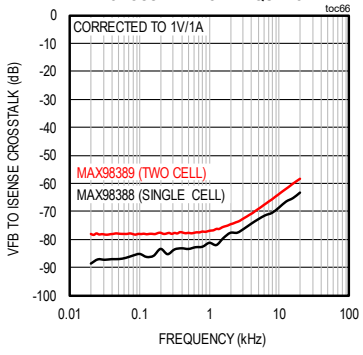
CURRENT SENSE THD+N vs. SPEAKER OUTPUT LEVEL



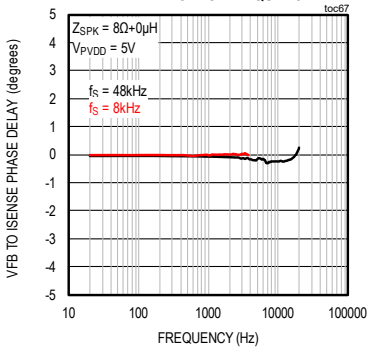
CURRENT SENSE THD+N vs. SPEAKER OUTPUT LEVEL



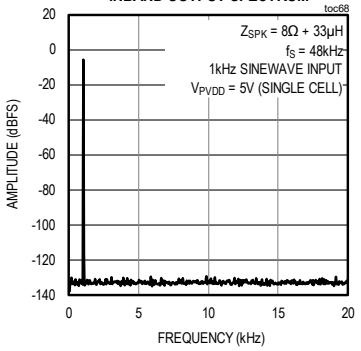
VOLTAGE FEEDBACK TO CURRENT SENSE CHANNEL CROSSTALK vs. FREQUENCY



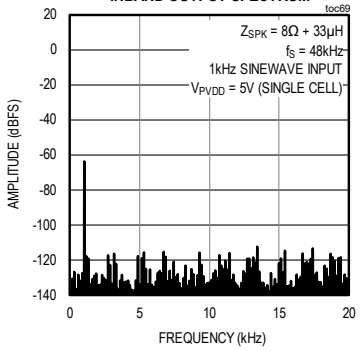
VOLTAGE FEEDBACK TO CURRENT SENSE PHASE DIFFERENCE vs. FREQUENCY



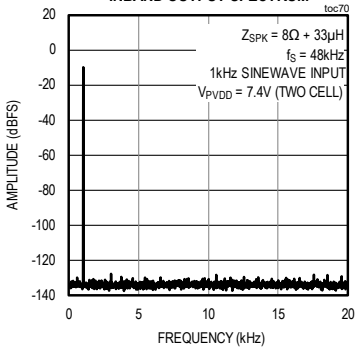
VOLTAGE FEEDBACK CHANNEL INBAND OUTPUT SPECTRUM



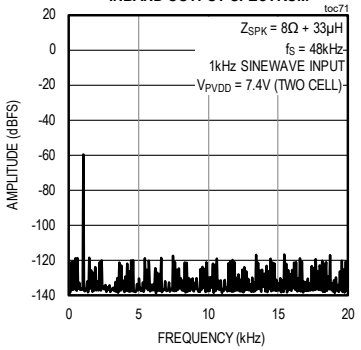
VOLTAGE FEEDBACK CHANNEL INBAND OUTPUT SPECTRUM



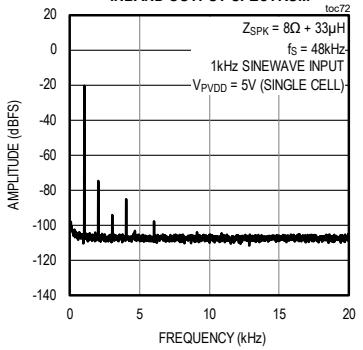
VOLTAGE FEEDBACK CHANNEL INBAND OUTPUT SPECTRUM



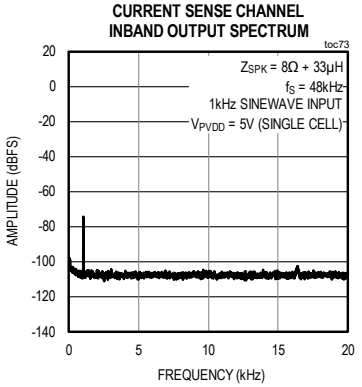
VOLTAGE FEEDBACK CHANNEL INBAND OUTPUT SPECTRUM

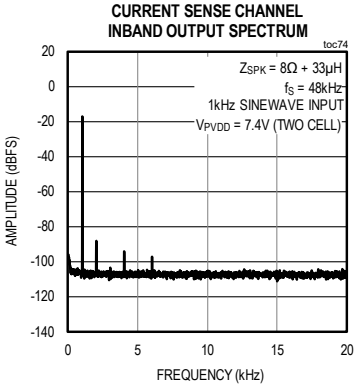


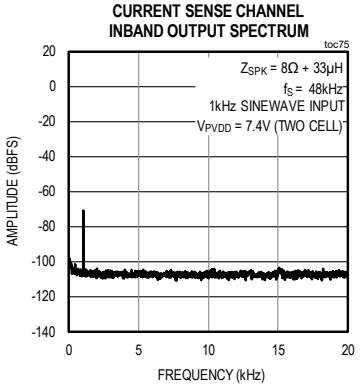
CURRENT SENSE CHANNEL INBAND OUTPUT SPECTRUM

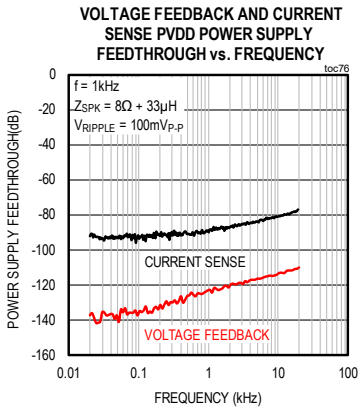


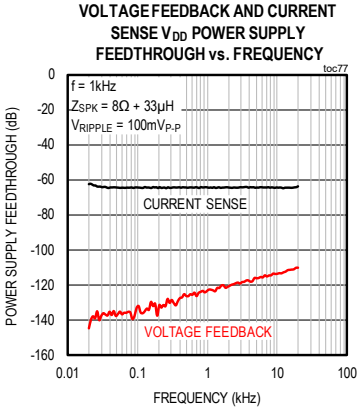
(V_{PVDD} = 5V (Single-Cell Mode) or 7.4V (Two-Cell Mode), V_{DD} = 1.8V, V_{GND} = V_{PGND} = 1.8V, C_{PVDD} = 10µF + 0.1µF, C_{VDD} = 1µF, f_{BCLK} = 3.072MHz, f_{LRCLK} = 48kHz, Playback Data Word Size ≥ 24-Bit, Z_{SPK} = Open between OUTP and OUTN, T_A = +25°C)



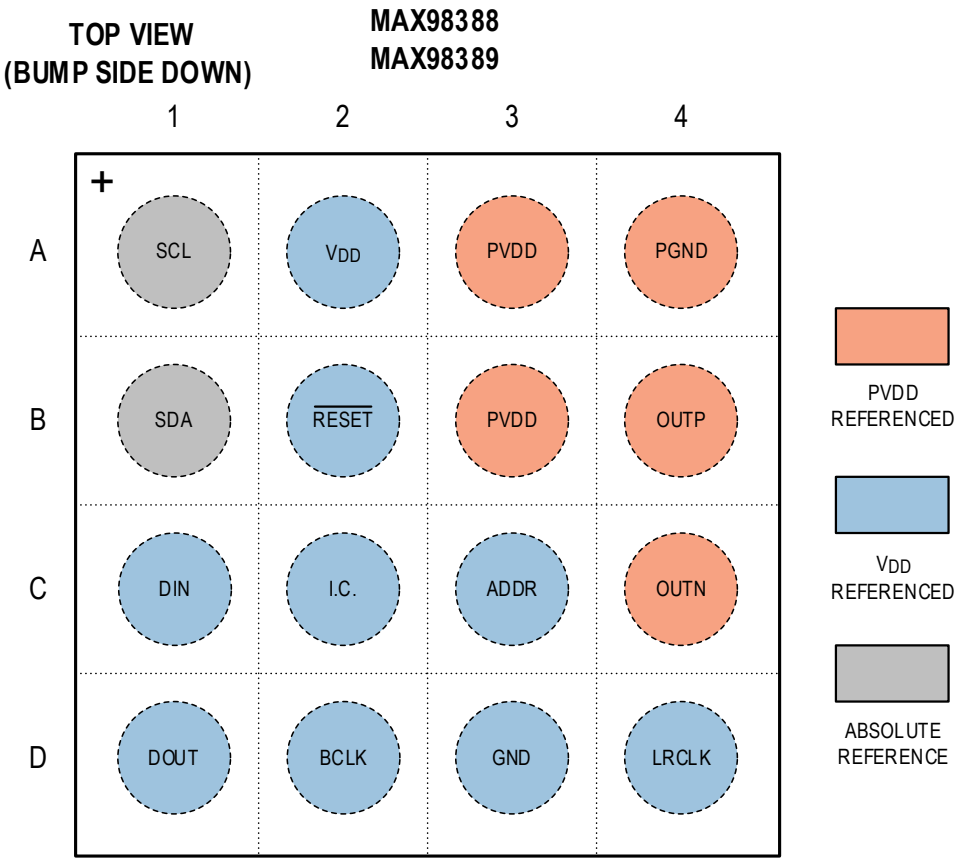








Pin Configurations



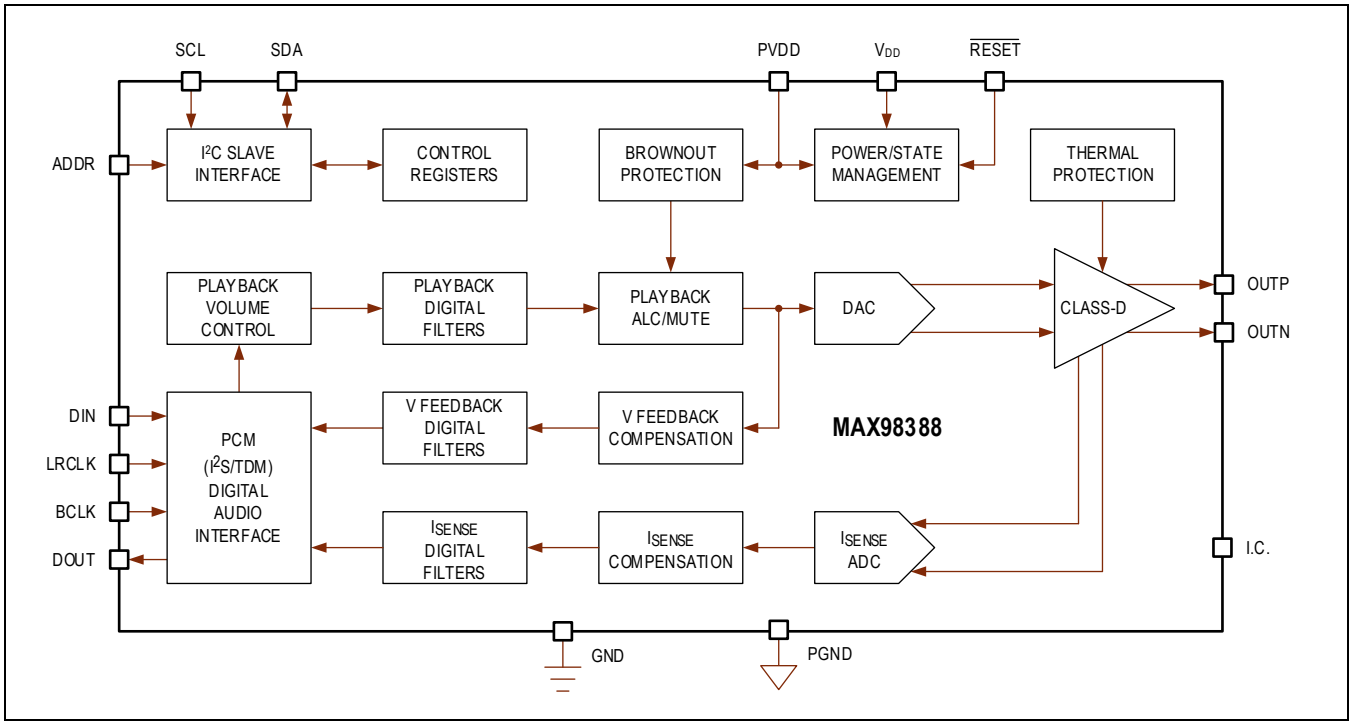
WLP
(1.638mm x 1.788mm x 0.64mm, 0.4mm PITCH)

Pin Descriptions

PIN	NAME	FUNCTION	REF SUPPLY	Type
A3, B3	PVDD	Speaker Amplifier Power Supply Input. Bypass to PGND with a 10µF capacitor and a 0.1µF capacitor both placed as close to the supply input as possible.	—	Supply
A4	PGND	Power Ground. Ground connection for the Class-D amplifier. Connect directly to the same ground plane as GND.	—	Supply
A2	V_{DD}	Internal Low Voltage Power Supply Input. Bypass to GND with a 1µF capacitor placed as close to the supply input as possible. For best performance, take care to minimize the return loop inductance in the PCB layout.	—	Supply
D3	GND	Ground. Ground connection for the internal low voltage analog and digital. Connect directly to the same ground plane as PGND.	—	Supply
B4	OUTP	Positive Class-D Amplifier Output	PVDD	Analog Output

C4	OUTN	Negative Class-D Amplifier Output	PVDD	Analog Output
C3	ADDR	I^2C Peripheral Device Address. Selects one of four I^2C addresses.	VDD	Digital Input
B1	SDA	I^2C-Compatible Serial-Data Input/Output. Connect a pullup resistor to V_{DD} for full output swing.	VDD	Digital Input/ Output
A1	SCL	I^2C-Compatible Serial-Clock Input. Connect a pullup resistor to V_{DD} for full output swing.	VDD	Digital Input
B2	$\overline{RESET}$	Hardware Reset Input. When held low, the device is reset and held in the hardware-shutdown state (resets all digital portions of the device and all registers to default PoR settings). When driven high (V_{DD}), the device can exit hardware shutdown if V_{DD} is above the UVLO threshold.	VDD	Digital Input
D2	BCLK	PCM Interface Bit Clock (BCLK) Input. Internally pulled down to GND through R_{PD}.	VDD	Digital Input
D4	LRCLK	PCM Interface Frame Clock Input (LRCLK). The frequency matches the playback sample rate. Internally pulled down to GND through R_{PD}.	VDD	Digital Input
C1	DIN	PCM Interface Data Input (DIN). Internally pulled down to GND through R_{PD}.	VDD	Digital Input
D1	DOUT	PCM Interface Data Output (DOUT).	VDD	Digital Output
C2	I.C.	Internally Connected. Not used for normal device operation. Leave open or connect to V_{DD} or GND externally. ADDR can be routed through this bump to connect to $\overline{RESET}$ and V_{DD}.	VDD	—

Functional Diagram



Detailed Description

Device State Control

The device has three distinct power states: the hardware-shutdown state, the software-shutdown state, and the active state. When transitioning normally between states, the device always moves from the hardware-shutdown state to the software-shutdown state to the active state (or the reverse) based on the state transition requirements. Normal transitions between the software-shutdown state and active state are reversible without waiting for an in-progress transition to be completed. State transitions due to fault conditions, supply removal, and reset conditions are not reversible and are always completed (once initiated) to protect the device. When powering up the device, there is no requirement for the sequence with which each supply is applied.

Hardware-Shutdown State

The hardware-shutdown state is the lowest power configuration. When in this state the device is globally held in a reset condition. As a result, the I^2C control interface is disabled, and all device registers are reset to their PoR states.

When the device is first powered up, it always initializes into the hardware-shutdown state. The device also transitions into the hardware-shutdown state after either a hardware ($\overline{RESET}$ input driven to logic low) or software (RST bit field) reset event, or anytime the V_{DD} supply drops below its UVLO threshold. Transitions into the hardware-shutdown state should only be initiated from the software-shutdown state and can cause audible glitches in the speaker output if initiated from the active state.

The device remains held in the hardware-shutdown state until the $\overline{RESET}$ input is asserted (driven to a logic high) and the V_{DD} supply rises above its UVLO threshold. Once both conditions are met, the device automatically exits the hardware-shutdown state, initializes, and then transitions into the software-shutdown state. During this transition (as part of initialization), the OTP register trim settings are loaded.

Software-Shutdown State

The device first enters the software-shutdown state after it transitions out of the hardware-shutdown state. In the software-shutdown state, the I^2C interface is active. All device registers can be programmed without restriction and all programmed register states are retained. All other blocks (regardless of block enable settings) are automatically disabled in the software-shutdown state.

The global enable bit (EN) is used to transition the device between the software-shutdown state and the active state. When global enable (EN) is set high, the device powers up and transitions to the active state. When the device is in the active state and global enable (EN) is set low, the device powers down and transitions back to the software-shutdown state. Additionally, anytime the software reset bit (RST) is written with a 1, the device is first reset (transitions to the hardware-shutdown state) and then transitions back into the software shutdown state.

If the V_{DD} supply drops below its UVLO threshold, or the hardware reset input ($\overline{RESET}$) is pulled low, the device transitions from the software-shutdown state to the hardware-shutdown state.

Active State

The device always enters the active state through a transition from the software-shutdown state. In the active state, all enabled device blocks are active and speaker amplifier playback is possible. In the active state, only dynamic register settings (or those restricted to disabled blocks) can be programmed safely.

The only non-fault state transition from the active state is initiated through the global enable bit (EN). All other transitions from the active state are the result of either PVDD dropping below its UVLO threshold or a fault event, and these can result in audible glitches if they occur during active playback.

Power Supply Sequencing

There is no requirement for the sequence with which each supply must be applied. However, certain state transitions cannot be completed when a supply is below its UVLO threshold. The V_{DD} supply must be above its UVLO threshold to transition from the hardware-shutdown state to the software-shutdown state. The PVDD supply must be above its UVLO threshold to transition from the software-shutdown state to the active state.

Device Sequencing

Example device enable and disable sequences are provided. In the tables, steps with the same number followed by a letter can be performed in any order (i.e., Steps nA, nB, and nC are non-sequential sub-steps of Step n).

Example Device Enable Sequencing

The following recommended device enable sequencing example applies to audio playback with current sense and voltage feedback enabled or disabled.

Table 1. Recommended Power-Up Sequence for Audio Playback

STEP	ACTION (STATE)	DETAILED DESCRIPTION
0	None (Hardware-Shutdown State)	This is the lowest power state. The device and registers are held in reset, and no control or audio interface interactions are possible.
1A	Power-Up V_{DD} Supply (Hardware Shutdown State)	Power the V_{DD} supply to above the UVLO threshold. The PVDD supply is not monitored in this state, and the level may be above or below the UVLO threshold. No supply sequencing (V_{DD} and PVDD) is required.
1B	Release Hardware Reset (Hardware-Shutdown State)	Drive the not hardware reset input ($\overline{RESET}$) high or always connect (pull up) to the V_{DD} supply input.
2	Transition to the Software-Shutdown State (State Transition)	Once conditions are met (Steps 1A and 1B), the device automatically transitions to the software-shutdown state. The transition is complete after the hardware enable time (t_{HW_EN}) has elapsed (if no error status is reported). Do not attempt to program or read back the device registers during this transition.
3	None (Software-Shutdown State)	This is the lowest power state where the I^2C interface is active and register settings can be programmed and retained. Can be used for a system idle/standby case or when the host system is active, but no playback use case is active.
4A	Program Device Registers (Software-Shutdown State)	The system software should fully configure the device registers (except EN—the global enable bit) for the desired audio use case. This includes clock/interface settings, amplifier mode, playback channel settings, and current sense/voltage feedback channel settings (if enabled).
4B	Power-Up PVDD Supply (Software-Shutdown State)	Power the PVDD supply to above the UVLO threshold (if not done previously) before attempting to transition to the active state.
4C	Enable the External Clocks (Software-Shutdown State)	Start the PCM interface clocks (bit clock and frame clock) before attempting to transition to the active state.
5	Set Global Enable Bit (Software-Shutdown State)	Set the global enable bit high (EN) to allow the device to transition to the active state (if all other conditions are met). To avoid potentially audible glitches, the input PCM playback data (DIN) should be silent before and during the transition to the active state.
6	Transition to the Active State (State Transition)	The state transition is complete after the turn-on time (t_{ON}) has elapsed. Note that the duration of the turn-on time (t_{ON}) varies depending on whether volume ramp-up is enabled or bypassed. When the transition has been completed, the power-up done status state bit is set. If the transition fails, one or more fault status state bits can be set.
7	Audio Playback (Active State)	The device is in the active state with playback active or ready. To avoid errors and audible glitches during any device programming in the active state, all register bit field restrictions must be observed.

Example Device Disable Sequencing

The following recommended device disable sequencing example applies to the audio playback with current sense and voltage feedback enabled or disabled.

Table 2. Recommended Power-Down Sequence for Audio Playback

STEP	ACTION (STATE)	DETAILED DESCRIPTION
0	Audio Playback (Active State)	The device is in the active state with playback active or ready.
1	Clear Global Enable Bit (Active State)	Before power-down, the host should first ramp down and disable (silence) the audio input data (DIN). Next, set the global enable bit (EN) low to transition the device to the software-shutdown state.
2	Transition to the Software-Shutdown State (State Transition)	The transition is complete after the audio turn-off time (t_{OFF}) has elapsed. Note that the duration of the turn-off time (t_{OFF}) varies depending on whether volume ramp down is enabled or bypassed. When the transition has been completed, the power-down done status state bit is set.
3	Idle/Reprogram Device (Software-Shutdown State)	The device can idle in the software-shutdown state. The PVDD supply can be powered down, and the external clocks can be disabled to save power. The device can be freely reconfigured in this state. To return to the active state, start from Step 3 in the example device enable sequencing, and follow the power-up sequence from there.
4	Transition to the Hardware-Shutdown State (State Transition)	Before transitioning to the hardware-shutdown state, first ensure that the external clocks are disabled. Then, either assert the not hardware reset input ($\overline{RESET}$) to a valid logic low level for longer than the hardware disable time (t_{HW_DIS}) or power down the V_{DD} supply to below the UVLO threshold.
5	None (Hardware-Shutdown State)	This is the lowest power state. All supplies can be disabled as desired. The device, all interfaces, and all registers are fully reset in this state.

Device Status Event Reporting

The device provides a set of status bits that inform the host about events that have occurred on-chip. For each status event source, both a RAW and STATE bit is provided with the following functions:

Raw Status (RAW)

Each status event source has a read-only bit to indicate the real-time raw status of the interrupt source. Some RAW status bits are asserted allowing for live readback of the current event source status. Other RAW status bits are pulsed only on event occurrence, in which case the STATE bit should be read to determine if an event has occurred since the last readback.

State Status (STATE)

Each status event source has a clear-on-read (read-only) state bit that is set whenever a rising edge occurs on the associated RAW status bit.

Device Status Event Sources

The complete list of status event sources is described in *Table 3*.

Table 3. Device Status Event Sources 1

REGISTER ADDRESS	BIT	EVENT SOURCE	BIT NAME	RAW STATUS	DESCRIPTION
RAW 0x2001 STATE 0x2004	7	Thermal Shutdown	THERMSHDN_*	Asserted Level	Indicates that the die temperature is greater than the configured thermal-shutdown threshold.
	6	Thermal Warning Begin	THERMWARN_BGN_*	Asserted Level	Indicates that the die temperature has exceeded the configured thermal-warning threshold.
	5	Thermal Warning End	THERMWARN_END_*	Asserted Level	Indicates that the die temperature has dropped below the configured thermal-warning threshold (after exceeding it).
	4	Speaker Output Monitor	SPKMON_ERR_*	Pulsed-On Event	Indicates that the speaker output monitor has detected a fault event. Events are only generated when the global enable bit (EN) is set high.
	3	Clock Monitor	CLK_ERR_*	Asserted in Auto Mode/ Pulsed in Manual Mode	Indicates the clock monitor has detected a clock error event. Events are only generated when the global enable bit (EN) is set high.
	2	Power-Down Done	PWRDN_DONE_*	Pulsed-On Event	Indicates the device completed power down into the software-shutdown state from the active state.
	1	Power-Up Done	PWRUP_DONE_*	Pulsed-On Event	Indicates the device has both transitioned out of the software-shutdown state, and that the playback channel is enabled and ready to receive audio data.
	0	OTP Fail	OTP_FAIL_*	Asserted Level	Indicates that the OTP load routine that runs when initializing the device has failed to complete successfully.

Table 4. Device Status Event Sources 2

REGISTER ADDRESS	BIT	EVENT SOURCE	BIT NAME	RAW STATUS	DESCRIPTION
RAW 0x2002 STATE 0x2005	7	—	—	—	—
	6	—	—	—	—
	5	Brownout Protection ALC Mute	BR_ALC_MUTE_*	Asserted Level	Indicates that the Brownout Protection ALC is muting the speaker channel.
	4	Brownout Protection ALC Active	BR_ALC_ACTIVE_*	Asserted Level	Indicates that the Brownout Protection ALC is attenuating the speaker channel.
	3	Brownout Protection ALC Thresh	BR_ALC_THRES_*	Asserted Level	Indicates that the PVDD level is below the Brownout Protection ALC threshold.
	2	PVDD UVLO Shutdown	PVDD_UVLO_SHDN_*	Asserted in Auto Mode/ Pulsed in Manual Mode	Indicates that the PVDD level dropped below the UVLO threshold during operation in the audio-active state.
	1	Speaker Amplifier Overcurrent	SPK_OVC_*	Asserted Level	Indicates that the amplifier output current exceeded the overcurrent threshold.
	0	Speaker Amplifier Clipping	SPK_CLIP_*	Asserted Level	Indicates that an amplifier output clipping event was detected.

PCM Interface

The flexible PCM interface supports common audio playback sample rates from 8kHz to 96kHz and I/V feedback sample rates from 8kHz to 96kHz. The PCM interface also supports standard I²S, left-justified, and TDM data formats. The PCM interface is disabled and powered down when both the PCM data input (DIN) and PCM data output (DOUT) are disabled.

PCM Clock Configuration

The device PCM interface functions as a peripheral, and as such, requires the host (also called the manager or controller) to supply both an external bit clock (BCLK) and frame clock (LRCLK). To configure the PCM interface clock inputs, the host must program both the PCM interface and playback channel sample rate (PCM_SR) and the bit clock (BCLK) to frame clock (LRCLK) ratio (PCM_BSEL). The PCM interface sample rate and the speaker playback channel sample rate always match and must be configured (PCM_SR) to match the frequency of the frame clock (LRCLK).

The current sense ADC and voltage feedback channel sample rate (IV_SR) can be set to the same sample rate as the PCM interface and speaker channel, or to any supported lower sample rate according to the restrictions in *Table 5*. When the current sense ADC channel is set to a lower rate than the speaker amplifier channel, the output data contains repeated samples.

Table 5. Supported PCM Interface to IV Feedback Channel Sample Rate Ratios

N/A = NOT AVAILABLE N/S = NOT SUPPORTED		ISENSE ADC/V FEEDBACK DATA SAMPLE RATE (kHz)										
		96	**88.2**	**48**	**44.1**	**32**	**24**	**22.05**	**16**	**12**	**11.025**	**8**
PCM INTERFACE AND SPEAKER CHANNEL SAMPLE RATE (kHz)	96	1	N/S	2	N/S	3	4	N/S	6	8	N/S	12
	88.2	N/A	1	N/S	2	N/S	N/S	4	N/S	N/S	8	N/S
	48	N/A	N/A	1	N/S	N/S	2	N/S	3	4	N/S	6
	44.1	N/A	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4	N/S
	32	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	N/S	4
	24	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S	3
	22.05	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2	N/S
	16	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S	2
	12	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S	N/S
	11.025	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1	N/S
	8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

The device supports a range of bit-clock-to-frame clock ratios (PCM_BSEL) ranging from 32 to 512. However, based on the selected PCM interface sample rate (LRCLK frequency), the configured clock ratio cannot result in a BLCK frequency that exceeds 24.576MHz.

PCM Data Format Configuration

The device supports the standard I²S, left-justified, and TDM data formats. The operating mode is configured using the PCM_FORMAT bit field.

I²S/Left-Justified Mode

I²S and left-justified formats support two channels that can be 16-, 24-, or 32-bits in length. The BCLK to LRCLK ratio (PCM_BSEL) must be configured to be twice the desired channel length. The audio data word size is configurable to 16-, 24-, or 32-bits in length (PCM_CHANSZ) and must be programmed to be less than or equal to the channel length. If the resulting channel length exceeds the configured data word size, then the data input LSBs are truncated and the data output LSBs are padded with either zero or Hi-Z data based on the PCM_TX_EXTRA_HIZ register bit setting.

Table 6. Supported I²S/Left-Justified Mode Configurations

CHANNELS	CHANNEL LENGTH	BCLK TO LRCLK RATIO (PCM_BSEL)	SUPPORTED DATA WORD SIZES (PCM_CHANSZ)
2	16	32	16
	24	48	16, 24
	32	64	16, 24, 32

With the default PCM settings, falling LRCLK indicates the left channel data (Channel 0) and the start of a new frame, while rising LRCLK indicates the right channel data (Channel 1). In I²S mode, the MSB of the audio word is latched on the second active BCLK edge after an LRCLK transition. In left-justified mode, the MSB of the audio word is latched on the first active BCLK edge after an LRCLK transition.

The PCM_BCLKEDGE register bit selects either the rising or falling edge of BCLK as the active edge that is used for data capture (DIN) and data output (DOUT). The PCM_CHANSEL bit configures which LRCLK edge indicates the start of a new frame (Channel 0), and LRCLK transitions always align with the inactive BCLK edge. The data output is valid on the same active BCLK edge as the data input. The data output also transitions on the same edge as the data input.

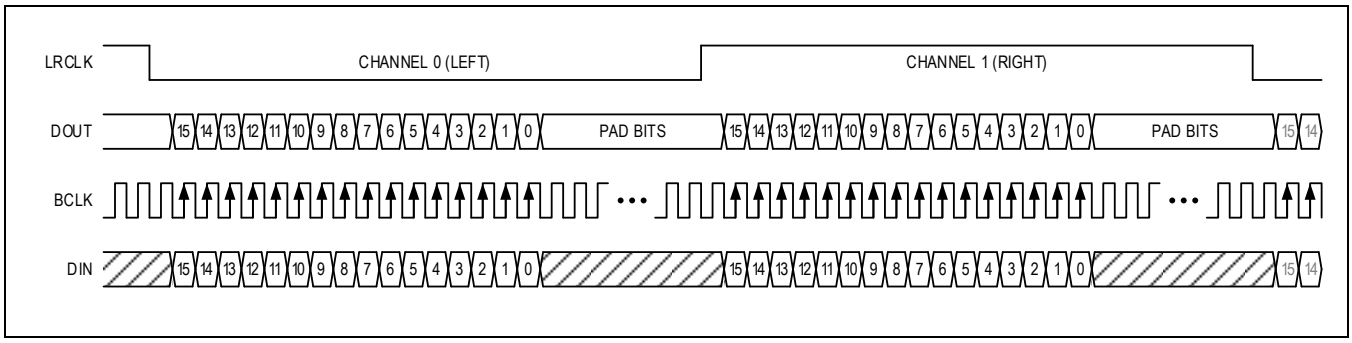


Figure 6. Standard I²S Mode Example

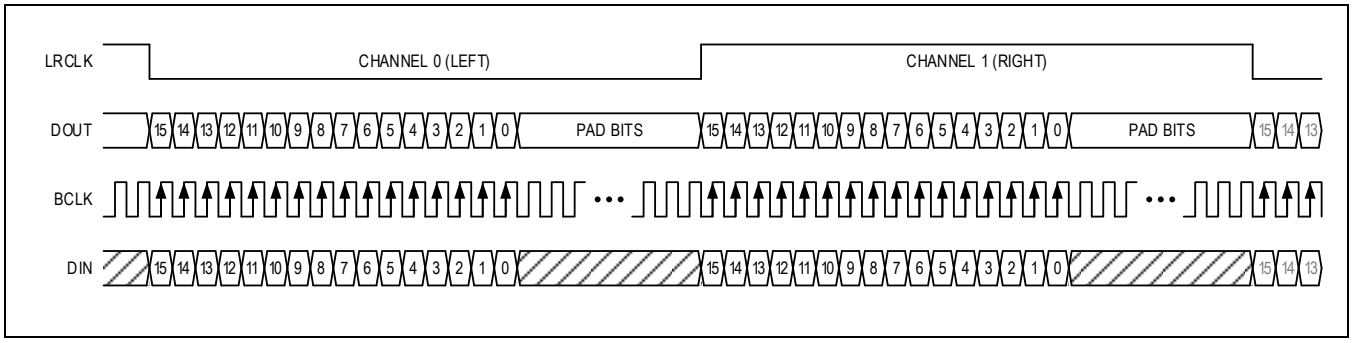


Figure 7. Baseline Left-Justified Mode Example

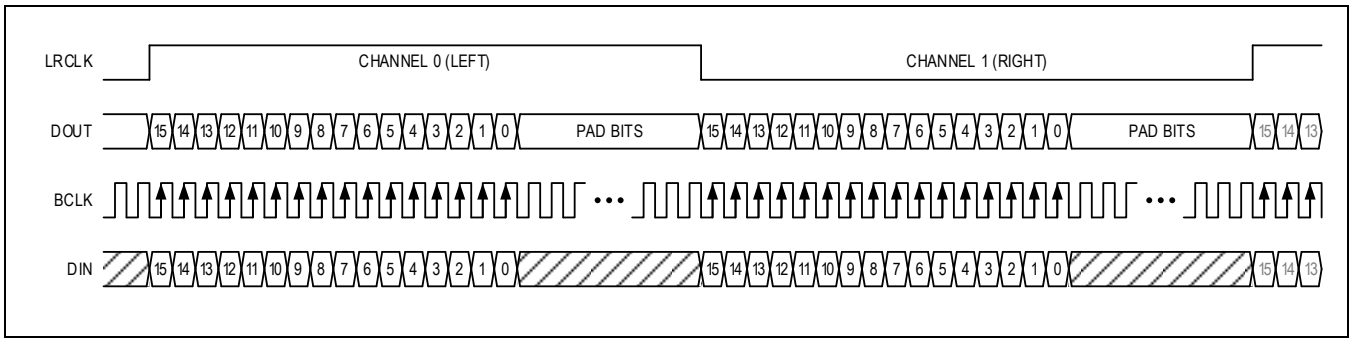


Figure 8. Left-Justified Mode (Frame Clock Inverted)

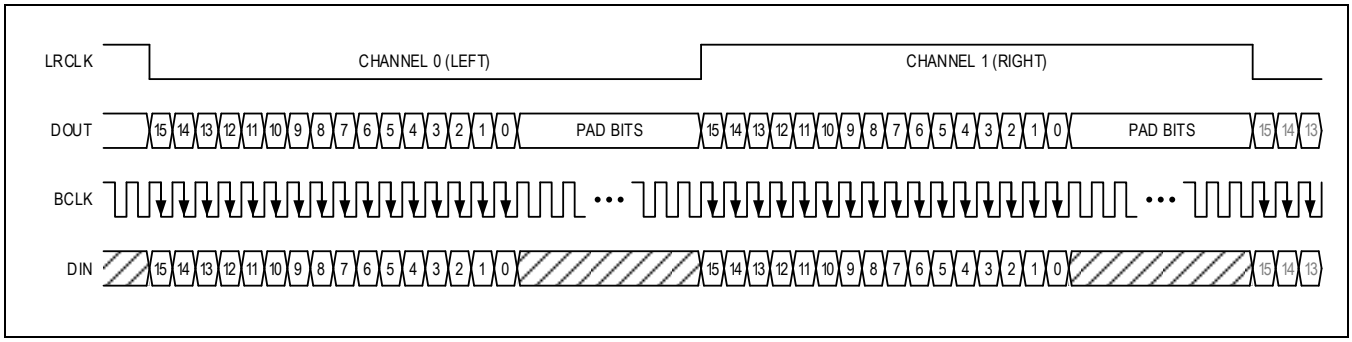


Figure 9. Left-Justified Mode (Bit Clock Inverted)

TDM Modes

The provided TDM modes support timing for up to 16 digital audio input channels (DIN), each containing 16-, 24-, or 32-bits of data. The digital audio output (DOUT) is structured into 8-bit slots, and the timing can support up to a maximum of 128 data output slots. The number of TDM input channels and output slots is determined by both the selected bit clock (BCLK) to frame clock (LRCLK) ratio (PCM_BSEL) and the selected data word and channel length (PCM_CHANSZ).

For a given valid configuration, the number of available data input channels per frame is calculated as follows:

Number of Available Data Input Channels = BCLK to LRCLK Ratio/Channel Length

For a given valid configuration, the number of available 8-bit data output slots per frame is calculated as follows:

Number of Available Data Output Slots = BCLK to LRCLK Ratio/8

Table 7 shows the supported TDM mode configurations for each combination of input data channels and output data slots. In some configurations, the maximum PCM interface and speaker amplifier playback sample rate is limited to less than 96kHz to avoid violating the nominal bit clock (BCLK) frequency limit of 24.576MHz.

Table 7. Supported TDM Mode Configurations

INPUT DATA CHANNELS	OUTPUT DATA SLOTS	DATA WORD SIZES (PCM_CHANSZ)	BCLK TO LRCLK RATIO (PCM_BSEL)	MAXIMUM PLAYBACK SAMPLE RATE (f_{LRCLK})
2	4	16	32	96kHz
	6	24	48	
	8	32	64	
3	15	32	125	
4	8	16	64	
	12	24	96	
	16	32	128	
5	15	24	125	
7	15	16	125	
	31	32	250	
8	16	16	128	
	24	24	192	
	32	32	256	
10	31	24	250	
15	31	16	250	
16	32	16	256	
7	31	32	250	48kHz
10	31	24	250	
10	40	32	320*	
15	31	16	250	
16	48	24	384	
	64	32	512	

Note: *A BCLK to LRCLK ratio of 320 can only be used with sample rate settings of 44.1kHz and 48kHz.*

With the default PCM interface settings in TDM mode, a rising frame clock (LRCLK) edge acts as the frame sync pulse and indicates the start of a new frame. The frame sync pulse width must be equal to at least one bit clock period. However, the falling edge can occur at any time as long as it does not violate the setup time of the next frame sync pulse rising edge. The PCM_CHANSEL bit is used to invert the frame clock (LRCLK) edges (sync pulse) that start a TDM frame.

In TDM mode, the MSB of the first audio word can be latched on the first (TDM Mode 0), second (TDM Mode 1), or third (TDM Mode 2) active bit clock edge after the sync pulse and is programmed by the PCM_FORMAT bits. Additionally, the PCM_BCLKEDGE register bit allows the active bit clock edge (for data capture and data output) to be programmed.

The data output is valid on and transitions on the same active bit clock (BCLK) edge as the data input.

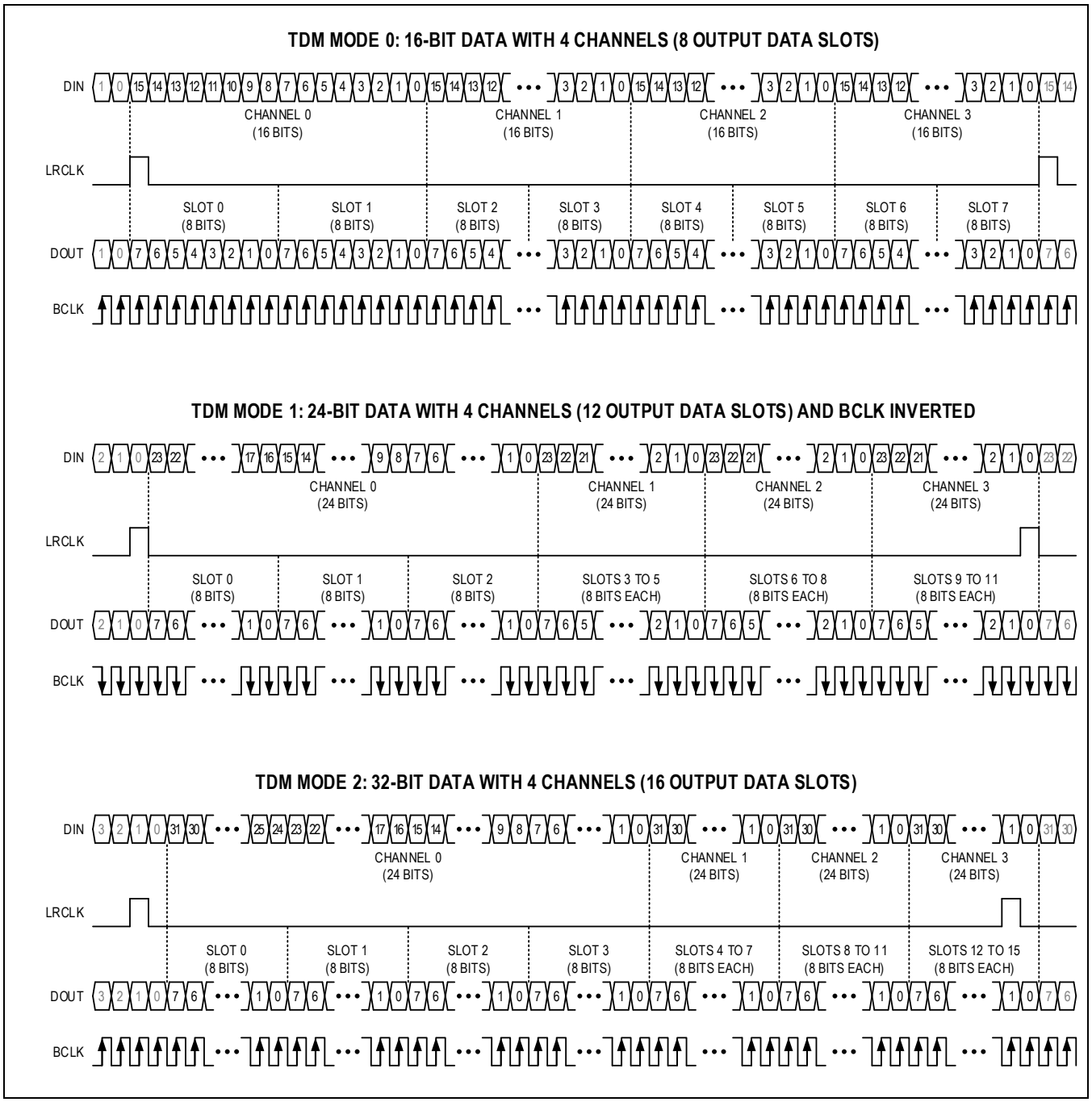


Figure 10. TDM Mode Examples

PCM Data Channel Configuration

The PCM interface data input (DIN) receives the source data for the speaker amplifier channel while the data output (DOUT) transmits the data from the current sense ADC and voltage feedback channels.

PCM Data Input

The PCM playback channel is enabled with the PCM_RX_EN bit and can accept data from any valid input data channel. The device provides an input digital mono mixer that can route a single channel or can mix two PCM input channels to create a mono input to the speaker playback channel. The PCM_DMMIX_CFG bit is used to configure the mixer, while the PCM_DMMIX_CH0_SOURCE and PCM_DMMIX_CH1_SOURCE bits select which of the potential 16 PCM input channels are used as the input to the mono mixer. In I²S and left-justified modes, only the two lowest input channels (PCM input channels 0 and 1) are available. In TDM mode, the number of available PCM input channels depends on the interface configuration and ranges from a minimum of 2 channels up to the maximum of 16 channels. If the PCM playback channel is disabled (PCM_RX_EN = 0), a zero code value is driven into the speaker amplifier channel.

PCM Data Output

The PCM interface data output (DOUT) is enabled by the PCM_TX_EN bit field and can transmit voltage and current data onto any valid output channel or slot. In I²S and left-justified mode, only two data output channels are available in each output transmit frame (Channel 0 and 1). In TDM mode, each output transmit frame can contain up to 64 sequential 8-bit data output slots, each of which is numbered from 0 up to a maximum of 63.

In I²S and left-justified modes, the speaker amplifier output voltage feedback and output current sense data are available for data output transmission in either output channel. The voltage and current output data only contain 16-bits of valid data, and if the PCM interface data word size (PCM_CHANSZ) exceeds this, the remaining bits are zero-padded (out to 24- or 32-bits). Furthermore, if the channel length (set by the bit clock to frame clock ratio with PCM_BSEL) exceeds the PCM interface data word size, additional trailing bits can be either Hi-Z or zeros (based on the PCM_TX_EXTRA_HIZ setting). The output data can also be assigned to share the same channel or to be frame interleaved in the same channel.

In TDM mode, the voltage and current data are individually assigned to data output slots. The output data is always a 16-bit word size that fits into two consecutive data output transit slots. *Table 8* shows the output data format and parameters.

Table 8. Supported PCM Data Output Types

OUTPUT DATA TYPE	SYMBOL	DATA WORD SIZE (BITS)	NUMBER OF TDM SLOTS	ENABLE/SLOT ASSIGNMENT
Speaker Amplifier Output Voltage Feedback	VFB	16	2	PCM_VFB_EN/ PCM_VFB_SLOT
Speaker Amplifier Output Current Sense	IMON	16	2	PCM_IMON_EN/ PCM_IMON_SLOT

An individual enable and slot assignment bit field is provided for both the voltage and current output data. In I²S and left-justified modes, use output Slot 0 to assign data to Channel 0 and output Slot 1 to assign data to Channel 1. In TDM mode, the slot assignment selects the slot where the output data type transmission begins for the required two data output transmit slots (e.g., voltage output data assigned to Slot 6 would occupy Slots 6 and 7).

In TDM mode, voltage and current data can be assigned to any valid data output slot with some restrictions. First, it is invalid for data to be assigned such that the data word extends beyond the end of the data output frame. For example, since the data requires two slots to transmit, it cannot be assigned to the last slot of the frame. Next, it is also invalid to assign output data to any slot that overlaps with the slot assignment of other output data (this also applies to channels in I²S and left-justified modes unless channel sharing or interleaving is used). Finally, it is invalid to assign data to any slots that do not exist in the frame structure of the current PCM interface configuration.

Any data output (DOUT) slots that exist in the current frame structure but have no output data assigned to them are either Hi-Z or driven with a 0 code (as set by the PCM_TX_SLOT_HIZ bit field). If a data output is disabled, then the assigned data output slots are either Hi-Z or driven with 0 code (set by the PCM_TX_SLOT_HIZ bit field).

Data Output Channel-Interleaved I/V Data

In I²S and left-justified use cases, the PCM interface limits the number of available data output channels to two making it impossible to fit amplifier output current sense and voltage feedback data from stereo devices on a single shared data output (DOUT) line. For these cases, the data output can be configured to allow the current sense and voltage feedback data types from a single device to share a single data output channel. To enable channel-interleaved mode, set the PCM_TX_INTERLEAVE bit high. Then assign the current sense and voltage feedback data types to the same valid data channel (using PCM_VFB_SLOT and PCM_IMON_SLOT).

In this configuration, the current and voltage data types are frame interleaved on the assigned data output channel. The current and voltage data words are both 16-bits in length, and as a result, if the channel length is longer than 16-bits, the trailing padding bits are set to either Hi-Z or zero code depending on the state of the PCM_TX_EXTRA_HIZ bit field.

To identify the data type in channel-interleaved mode, the LSB of the 16-bit data word is dropped (truncated). The data word is then right-shifted by a single bit, and the now vacant MSB is replaced with either a 0 to indicate voltage feedback data or a 1 to indicate current sense data. For phase alignment, the voltage data for a single sampling instant is always transmitted in the assigned channel on the first frame, followed by the current data on the second frame. The MSB value and the transmission order allow the host to identify and phase-align the output data across frames.

Since the I/V data is frame interleaved, the sample rate for the PCM interface must be greater than that of the I/V channels by an integer ratio of 2. *Figure 11* shows a basic case where the sample rate of the PCM interface is twice that of the I/V channels.

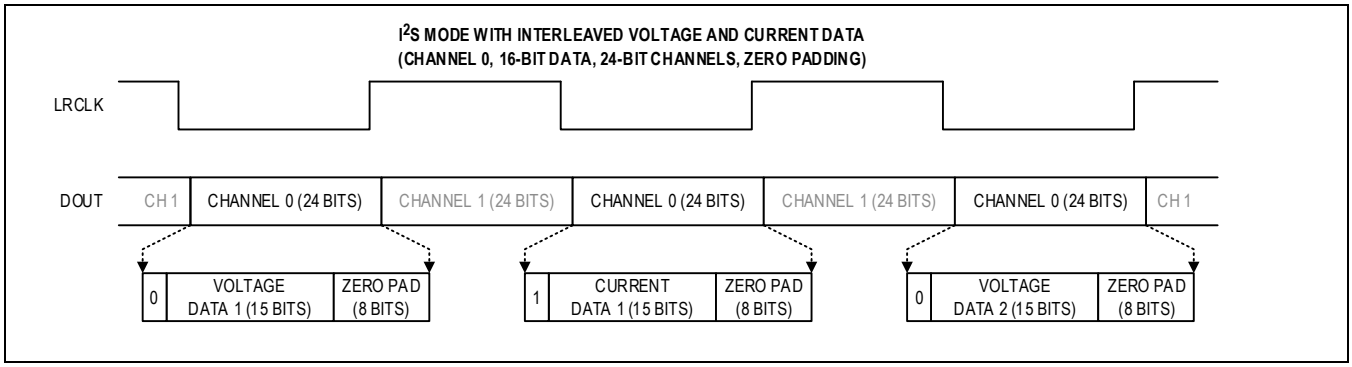


Figure 11. I/V Feedback Channel Data Interleaved on Data Output Channel 0

Data Output Shared Channel I/V Data

In I²S and left-justified use cases, the PCM interface limits the number of available data output channels to two. This makes it impossible to fit amplifier output current sense and voltage feedback data from a stereo pair of devices onto a single shared data output (DOUT) line (would require four channels). For these cases, the data output can be configured to allow the current and voltage data types from a single device to share a single data output channel.

To enable channel-shared mode, assign the current and voltage data types to the same valid data channel (using PCM_VFB_SLOT = PCM_IMON_SLOT). The voltage data is always transmitted first followed by the current data in the same assigned channel. In this configuration, the bit clock (BCLK) to frame clock (LRCLK) ratio should be configured for 64 (allowing for 32-bit channels) as the current and voltage data words are both 16-bits in length. If the clock ratio is less than 64, the current and voltage data do not decode properly.

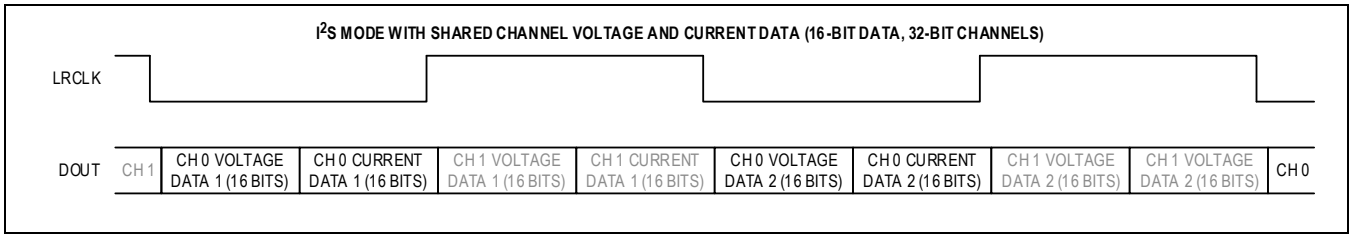


Figure 12. I/V Feedback Shared Channel Data Example

I²C Peripheral Serial Control Interface

The device features an I²C/SMBus™-compatible, 2-wire serial interface that is used to program the control registers. The interface comprises a serial data line (SDA) and a serial clock line (SCL) that facilitate communication between this peripheral device and the upstream I²C manager (also referred to as the I²C controller in some documentation). The device's I²C interface supports FM+ clock rates up to 1MHz. The I²C control interface is activated when the device is not in the hardware-shutdown state, and when a valid I²C start condition is detected at the SCL and SDA pins.

I²C Interface Address

The peripheral device address is defined as the seven most significant bits (MSBs) followed by the read/write bit. The seven most significant bits are programmable through the ADDR input connection (as shown in *Table 9*). The device does not communicate if the ADDR input is open or unconnected. Setting the read/write bit to 1 configures the device for read mode. Setting the read/write bit to 0 configures the device for write mode. The address is the first byte of information transmitted by the I²C manager to the peripheral device after the START condition.

Table 9. I²C Peripheral Device Address

ADDR INPUT CONNECTION	DEVICE I²C ADDRESS (BINARY)	I²C WRITE (BINARY)	I²C READ (BINARY)
Connected to V_{DD}	0111000x	01110000	01110001
Connected to GND	0111001x	01110010	01110011
Connected to SDA	0111010x	01110100	01110101
Connected to SCL	0111011x	01110110	01110111

I²C Interface Bit Transfer Protocol

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA, while SCL is high, are control signals (START and STOP conditions).

I²C Interface START and STOP Conditions

SDA and SCL idle high when the bus is not in use. An I²C manager initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. A START condition from the manager signals the beginning of a transmission to the peripheral device. The manager terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

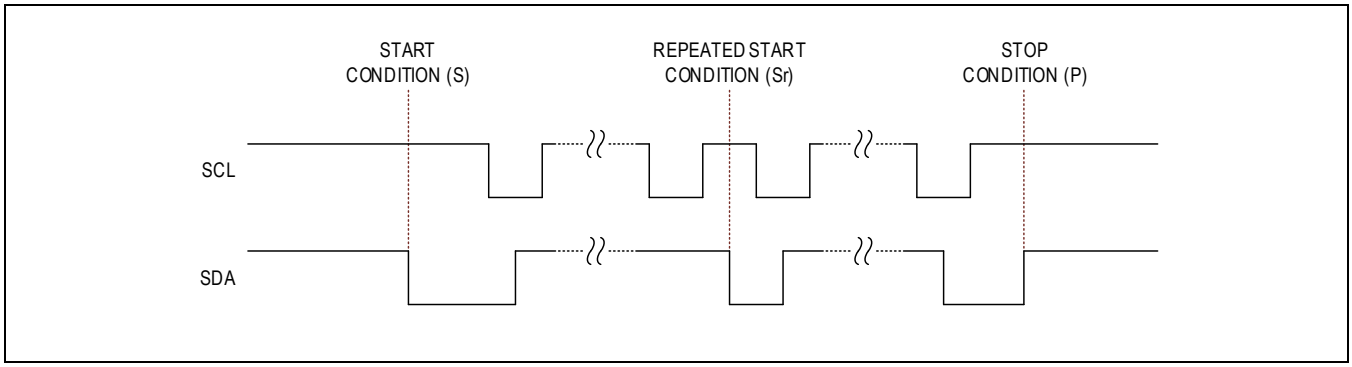


Figure 13. I²C Peripheral Device Interface START and STOP Condition Example

I²C Interface Early STOP Condition

The device recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

I²C Interface Acknowledge Bit

The acknowledge bit (ACK) is a clocked ninth bit that the peripheral device uses to handshake receipt of each byte of data when in write mode (*Figure 14*). The peripheral device pulls down SDA during the entire manager-generated ninth clock pulse if the previous byte is successfully received. Monitoring ACK allows for the detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus manager may retry communication.

The I²C manager pulls down SDA during the ninth clock cycle to acknowledge receipt of data when the peripheral device is in read mode. An acknowledge is sent by the manager after each read byte to allow data transfer to continue. A not-acknowledge (NACK) is sent when the manager reads the final byte of data and is followed by a STOP condition.

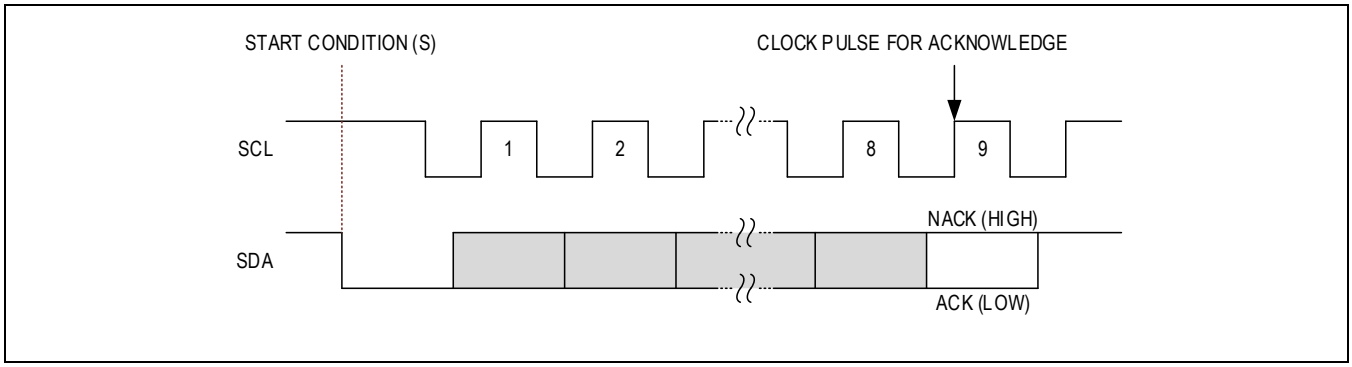


Figure 14. I²C Peripheral Device Interface Acknowledge Bit Example

I²C Interface Write Data Format

A write to the device through the I²C peripheral device interface includes the transmission of a START condition, the device address with the READ-$\overline{\text{WRITE}}$ bit set to 0, two bytes of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

Transmission of the device address with the READ-$\overline{\text{WRITE}}$ bit set to 0 indicates that the I²C manager intends to write data to the device. The device acknowledges receipt of the address byte during the ninth SCL pulse.

The second and third bytes transmitted from the manager configure the device's internal register address pointer. The pointer tells the device where to write the next byte of data. An acknowledge pulse is sent by the device upon receipt of each byte of the register address data.

The fourth byte sent to the device contains the data to be written to the chosen register address. An acknowledge pulse from the device signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows the manager to write to sequential registers within one continuous frame. The manager signals the end of transmission by issuing a STOP condition.

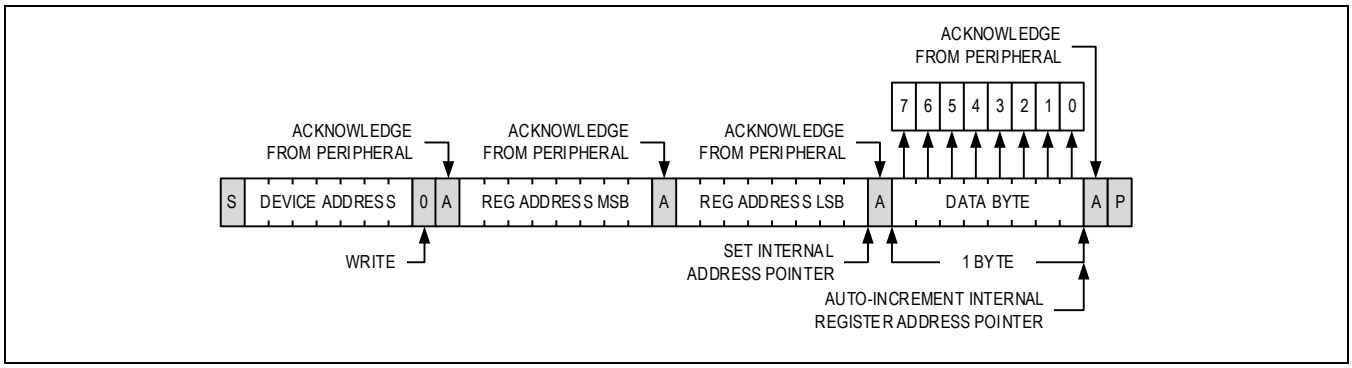


Figure 15. I²C Manager Writing One Byte of Data to the Peripheral Device

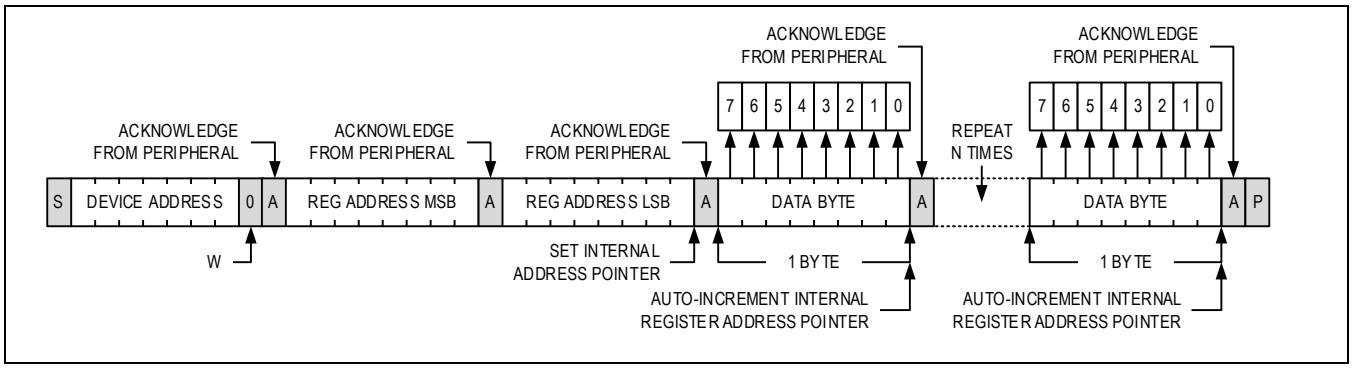


Figure 16. I²C Manager Writing n-Bytes of Data to the Peripheral Device

I²C Interface Read Data Format

The I²C register address pointer must be preset to a target register before a read command is issued. The manager presets the peripheral device register address pointer by first sending the device's address with the READ-$\overline{\text{WRITE}}$ bit set to 0 (write command) followed by two commands containing the target register address for the address pointer.

A REPEATED START condition is then sent followed by the read command (device address with the READ-$\overline{\text{WRITE}}$ bit set to 1). This begins a read command with the internal register address pointer set to the target register address. The first byte transmitted from the device contains the contents of the register that the address pointer is set to. Transmitted data is valid on the rising edge of SCL. The manager acknowledges (ACK) receipt of each read byte during the acknowledge clock pulse. The address pointer then auto-increments after each acknowledged read data byte. This auto-increment feature allows multiple device registers to be read sequentially within one continuous frame.

The manager must issue an acknowledge (ACK) for all correctly received bytes except the last byte. To terminate the read operation, the final byte must be followed by a not acknowledge (NACK) from the manager and then a STOP condition. A not-acknowledge (NACK) followed by a STOP condition can be issued after any number of read data bytes.

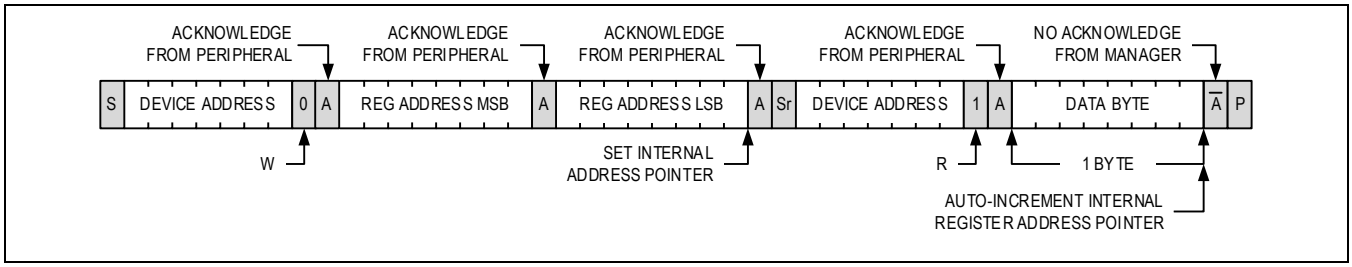


Figure 17. I²C Manager Reading One Byte of Data from the Peripheral Device

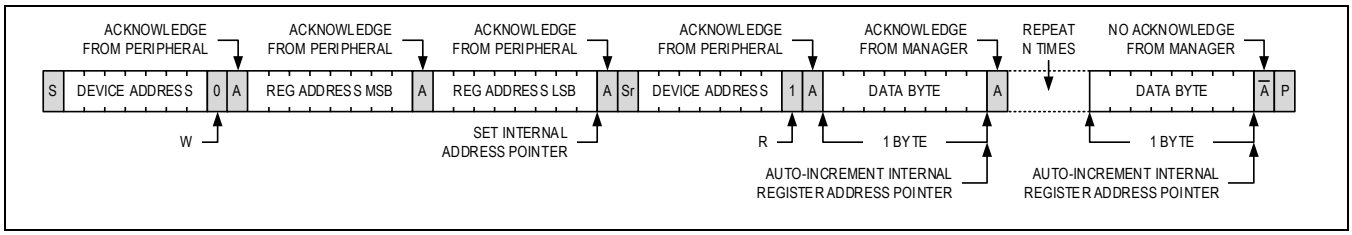


Figure 18. I²C Manager Reading n-Bytes of Data from the Peripheral Device

Speaker Playback Channel

The input data to the speaker amplifier channel is accepted from the PCM digital audio interface data input (DIN) through the mono mixer stage. The data is then routed through the digital filters, signal processing, and volume control blocks in the speaker playback channel before reaching the DAC and Class-D speaker amplifier. The digital playback channel data is also tapped just before the DAC and is routed to the input of the voltage feedback channel.

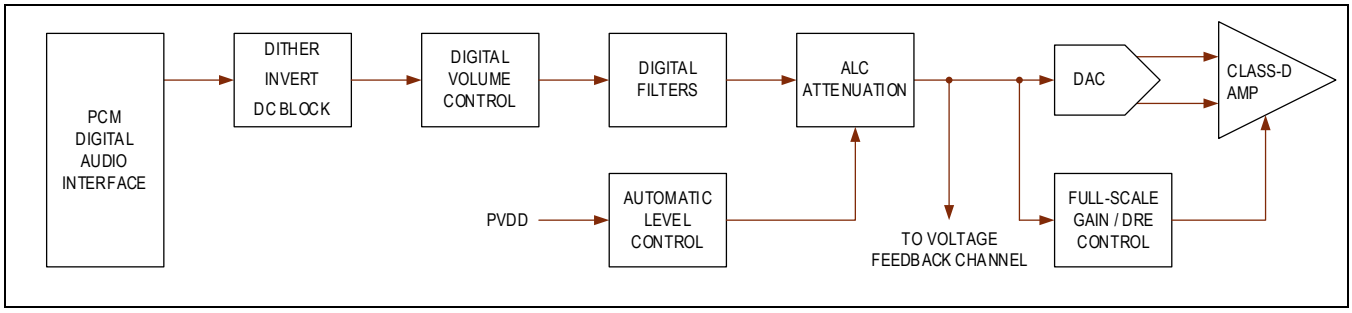


Figure 19. Speaker Playback Channel Detailed Block Diagram

Speaker Channel Dither

The input data to the speaker channel can optionally have dither (±1LSB peak-to-peak) applied if SPK_DITH_EN is set to 1. No dither is applied when SPK_DITH_EN is set to 0.

Speaker Channel Data Inversion

The input data to the speaker channel can optionally be inverted by setting the SPK_INVERT bit to 1.

Speaker Channel DC Blocking Filter

A DC blocking filter can be enabled for the speaker channel by setting the SPK_DCBLK_EN bit to 1.

Speaker Channel DAC Digital Filters

The speaker channel DAC features a digital lowpass filter that is automatically configured based on the selected playback sample rate (PCM_SR). This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. See the *DAC Digital Filters* section in the *Electrical Characteristics* table.

Speaker Channel Maximum Peak Output Voltage Scaling

The full-scale output of the speaker path DAC is 0.5dBV (typical). The speaker path no-load maximum peak output voltage level is then programmable relative to this baseline level. The peak output scaling range is set with the SPK_GAIN bit field, and the available range is determined by whether the device is operating in single-cell or two-cell/boosted mode (as set by the SPK_AMP_MODE bit). The range of peak output settings is as follows:

Table 10. Speaker Channel Peak Output Settings

MAXIMUM PEAK OUTPUT VOLTAGE LEVEL SELECTED	SINGLE-CELL MODE (SPK_AMP_MODE = 0)	TWO-CELL/BOOSTED MODE (SPK_AMP_MODE = 1)
SPK_GAIN = 0x0	$0.75V_{RMS}$ (-3dB)	$1.50V_{RMS}$ (+3dB)
SPK_GAIN = 0x1	$1.06V_{RMS}$ (0dB)	$2.11V_{RMS}$ (+6dB)
SPK_GAIN = 0x2	$1.50V_{RMS}$ (+3dB)	$2.99V_{RMS}$ (+9dB)
SPK_GAIN = 0x3	$2.11V_{RMS}$ (+6dB)	$4.22V_{RMS}$ (+12dB)
SPK_GAIN = 0x4	$2.99V_{RMS}$ (+9dB)	$5.96V_{RMS}$ (+15dB)
SPK_GAIN = 0x5	$4.22V_{RMS}$ (+12dB)	$8.41V_{RMS}$ (+18dB)

The speaker output signal level for a given digital input signal level is calculated as follows:

Output Signal Level (dBV) = Input Signal Level (dBFS) + Digital Volume (dBFS) + 0.5 (dBV) + SPK_GAIN (dB) (0dBFS is referenced to 0dBV or $1V_{RMS}$)

Speaker Channel Digital Volume Control

The device provides dynamically programmable speaker channel digital volume control. The digital volume control provides an attenuation range of 0dB to -63dB in 0.5dB steps that are configured with the SPK_VOL bit field. A digital mute is also provided and is enabled when SPK_VOL is set to 0x7F.

Digital volume level changes (from one volume level to another during active playback) are always ramped. However, digital volume ramping during start-up, shutdown, and mute/unmute is disabled by default. Volume ramp-up and ramp-down for these functions are individually enabled or disabled with the SPK_VOL_RMPUP_BYPASS and SPK_VOL_RMPDN_BYPASS bit fields respectively. When volume ramping is enabled (not bypassed), the device turn-on and turn-off times are longer. If volume ramping is disabled (bypassed), then the audio level should instead be ramped in the host and should already be silent during startup, shutdown, and mute/unmute to avoid potentially audible artifacts.

Speaker Amplifier

The filterless Class-D amplifier offers much higher efficiency than Class-AB amplifiers. The high efficiency of a Class-D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class-D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Speaker Amplifier Output Short-Circuit Protection

If the output current limit of the Class-D amplifier (I_{LIM}) is exceeded (see the *Electrical Characteristics* table), the speaker output is disabled. When configured for manual mode (OVC_RETRY_EN = 0), after an overcurrent event occurs, the speaker amplifier output is disabled and the device is placed into the software-shutdown state (EN is set to 0). The device remains in this state until re-enabled by the system software.

When configured for automatic mode (OVC_RETRY_EN = 1), the speaker output is disabled for approximately 20ms. At the end of the 20ms, the speaker output is re-enabled. If the fault condition still exists, the speaker output continues to disable and reenable until the fault condition is removed.

Speaker Amplifier Click-and-Pop Suppression

The speaker amplifier features comprehensive click-and-pop suppression. During turn-on, the click-and-pop suppression circuitry reduces audible transient sources internal to the device. When powering down to software or hardware shutdown, the differential speaker outputs simultaneously go to Hi-Z.

The comprehensive click-and-pop suppression of the device is unaffected by power-up or power-down sequencing. Disabling the device through software and applying or removing the clocks before or after the transition of the $\overline{RESET}$ input all yield the same click-and-pop performance. However, when volume ramping is enabled, for the best click-and-pop performance, the clocks and supplies must remain valid for 13ms after the software sets the global enable bit high or low (EN) to allow for volume ramping to complete.

Speaker Amplifier Ultra-Low EMI Filterless Output

Traditional Class-D amplifiers require the use of external LC filters or shielding to meet the EN55022B electromagnetic interference (EMI) regulation standards. Analog Devices' active emissions-limiting, edge-rate control circuitry, and spread-spectrum modulation reduce EMI emissions while maintaining high efficiency.

The optional spread-spectrum modulation (SSM) mode is enabled with the SPK_AMP_SSM_EN bit. When active, the spread-spectrum modulator randomly varies the Class-D switching frequency around the center frequency (f_{SW}) within the bounds set by the configured SSM ratio (SPK_AMP_SSM_MOD bit field). SSM mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

The device also provides an integrated pink noise generator that is primarily used for EMI measurements. This mode must be enabled or disabled (with the SPK_PINK_NOISE_EN bit) while the device is in the software-shutdown state (before setting global enable and powering the device up). When enabled, the device requires external clock input (valid bit clock and frame clock) to power up to the active state. Once in the active state, the clocks can be stopped, and the pink noise generator continues to operate. In this state, the pink noise generator provides the input data to the speaker playback channel (replacing the data input DIN as the playback data source). The pink noise data is affected by the speaker playback channel gain, and with 0dB of gain the signal level is around -55dBV at 1kHz before reducing down to just above -70dBFS at 20kHz.

Speaker Current Sense and Voltage Feedback Channels

The device provides both a speaker output current sense ADC channel and a speaker output voltage feedback channel (also referred to as the IV Feedback channels). The current sense channel features a 16-bit ADC that is used to internally measure the speaker amplifier output current. The voltage feedback channel taps the digital signal in the speaker playback channel (just before the DAC) and then routes the signal through compensation filters to accurately model the Class-D speaker amplifier output voltage.

The current and voltage feedback channels are independently enabled with the IVFB_I_EN and IVFB_V_EN bits, respectively. To ensure phase alignment, the channels should both be enabled either with a single write to the register containing the IVFB_I_EN and IVFB_V_EN bits (if enabled when the global enable EN = 1), or by setting both bits high before exiting software shutdown.

Both channels can optionally have dither applied (±1 LSB peak-to-peak) by setting the IVFB_DITH_EN bit field to 1. Each channel also provides a separate, optional DC blocking filter (first-order high-pass). The current and voltage channel filters are enabled by setting the IVFB_I_DCBLK_EN and IVFB_V_DCBLK_EN bit fields to 1, respectively.

Speaker Current Sense and Voltage Feedback Channel Data Format

The output current and voltage data are routed to the host through the PCM interface data output (DOUT). See the *PCM Interface* section for details on configuring the current sense and voltage feedback data on the PCM interface data output channels/slots. Both the current sense and voltage feedback data use a 2's complement data format.

The current sense ADC channel has a 16-bit resolution and a range of ±3A, and the LSB size is calculated as 3A / (2^{15}). A current sense reading of 0x7FFF translates to a positive full-scale output current of +3A − 1 LSB, and a reading of 0x8000 translates to a negative full-scale output current of -3A.

The voltage feedback channel supports 16-bit resolutions and a range of ±5.5V in single-cell mode and ±11V in two-cell (or external boost) mode. The LSB size is calculated as 5.5V / (2^{15}) in single-cell mode and as 11V / (2^{15}) in two-cell mode. A voltage feedback code of 0x7FFF translates to a positive full-scale output voltage of +5.5V − 1 LSB in single-cell mode or +11V – 1 LSB in two-cell mode. Likewise, a code of 0x8000 is a negative full-scale output voltage of -5.5V in single-cell mode or -11V in two-cell mode.

When the speaker amplifier output clips, the voltage feedback channel data cannot accurately model the voltage at the speaker output. In this case, once the speaker amplifier clipping detection status is asserted (SPK_CLIP), the voltage feedback channel output data is held at the clipped level. This (and the status bits) indicate to the host that the speaker amplifier output is clipping and that the output voltage level cannot be tracked. Once the speaker amplifier output is no longer clipping, the status is de-asserted and the voltage feedback channel resumes tracking the speaker amplifier output voltage.

Clock and Speaker Output Monitors

The device provides both an optional clock monitor and an optional speaker output monitor. The clock monitor is enabled by setting the CMON_EN bit to 1 while the speaker output monitor is enabled by setting the SPKMON_EN bit to 1. The clock monitor is enabled by default, while the speaker output monitor must be enabled by the system software drivers.

Clock Monitor

The clock monitor is enabled by default and is provided to both inform the host of the device status and prevent invalid signals from reaching the speaker channel output during a clock fault condition. When enabled (CMON_EN to 1), the block monitors both the bit clock (BCLK) and the frame clock (LRCLK) inputs and automatically disables the speaker amplifier output if a clock error is detected. If the clock monitor is disabled (CMON_EN to 0) and either clock fails during active playback (bit clock or frame clock), it may be possible for invalid signals (including DC) to reach the speaker amplifier output.

For clock stop errors, the clock monitor detects and reports a clock source error if either the bit clock (BCLK) or frame clock (LRCLK) sources stop high or low for more than 60µs. The clock stop timeout is determined by an internal oscillator, which has a variability of ±10% over the device operating temperature range. In addition, the clock monitor also detects gross bit clock frequency errors (a completely invalid BCLK that results in an FLL unlock event) and internal clock generation errors (such as the DAC or ADC clocks failing).

The clock monitor can be programmed to respond to clock errors in two ways. When the CLOCK_AUTORESTART_EN bit is set to 0, the clock monitor is in manual mode. In manual mode, when a clock error is detected, the clock monitor

reports the clock error status (CLK_ERR) and places the device into software shutdown by setting EN to 0. The device remains in software shutdown until the host software sets EN to 1.

When the CLOCK_AUTORESTART_EN bit is set to 1, the clock monitor is in automatic mode. In automatic mode, when a clock error is detected, the clock monitor still reports the clock error status (CLK_ERR), however, the clock monitor does not reset the EN bit field and instead directly holds the device in software shutdown. Once valid clocking is reapplied and detected, the device automatically exits the software-shutdown state and returns to the active state. The value of the global enable bit field (EN) is not changed in auto-restart mode and remains 1 throughout the process.

Speaker Output Monitor

When enabled (SPKMON_EN to 1), the block monitors the speaker output level for signals in excess of the configured speaker output error threshold. The speaker output monitor error threshold is selected with the SPKMON_THRESH bit field. The threshold calculation differs depending on whether or not the current sense channel is active.

If the current sense channel is active, then the speaker output monitor threshold is directly selected as follows (and is compared to the measured output level):

Threshold (V) = SPKMON_THRESH x 0.03375V

The nominal speaker load resistance used by the speaker output monitor is selected with the SPKMON_LOAD bit field. The measured output current and this selected load resistance value are used to calculate the output voltage level used by the output monitor (relative to the selected voltage threshold). This has no effect if the current sense channel is disabled.

When the current sense channel is disabled, the threshold is calculated as a percentage of the output full-scale voltage:

Threshold (V) = (SPKMON_THRESH / 256) x PVDD Voltage

However, in this mode, the full-scale level varies as PVDD voltage changes, and therefore threshold should be selected based on the worst-case PVDD condition (typically the maximum possible PVDD in a given system).

The speaker output monitor error duration is configured with the SPKMON_DURATION bit field. If the monitored speaker output level exceeds the configured output error threshold for longer than the selected error duration, then a speaker output error is detected. The duration of a speaker output monitor error is determined by an internal oscillator, which has a typical variability of ±10% over the device operating temperature range. The speaker output error threshold and duration should be configured with careful consideration given to both the desired maximum sustained speaker output levels and the operation of any host-side audio software algorithms.

When a speaker output error is detected, the monitor reports the error status (SPKMON_ERR) and places the device into software shutdown by setting EN to 0. The device remains in software shutdown until the host software sets EN to 1.

Brownout Protection Automatic Level Control (ALC)

The brownout protection automatic level control (ALC) can reduce the speaker channel volume and/or mute the channel when the PVDD voltage drops below a programmable brownout threshold. The ALC compares the PVDD level to the threshold (set by ALC_TH) and activates when PVDD drops below the programmed level. The available threshold settings scale based on the speaker amplifier operating mode (single-cell mode or two-cell/boosted mode as selected with the SPK_AMP_MODE bit).

Brownout Protection ALC Ballistics

When PVDD drops below the brownout threshold, the ALC activates and starts to reduce speaker channel volume at a programmable attack rate (set by ALC_ATK_RATE). The maximum ALC attenuation is programmable from 0dB to -15dB in 1dB steps (set by ALC_MAX_ATTEN).

If at any time either during or after the ALC volume attenuation completes, the PVDD supply recovers and rises above the brownout threshold, and the release debounce timer starts (set by ALC_RLS_DBT). The speaker channel volume reduction continues (if still in progress—up to the maximum attenuation) while the debounce timer runs, and release does not start until PVDD remains above the threshold for longer than the selected debounce time. The rate at which the volume attenuation releases is set by the ALC_RLS_RATE bit field. *Figure 20* illustrates this behavior in a typical situation.

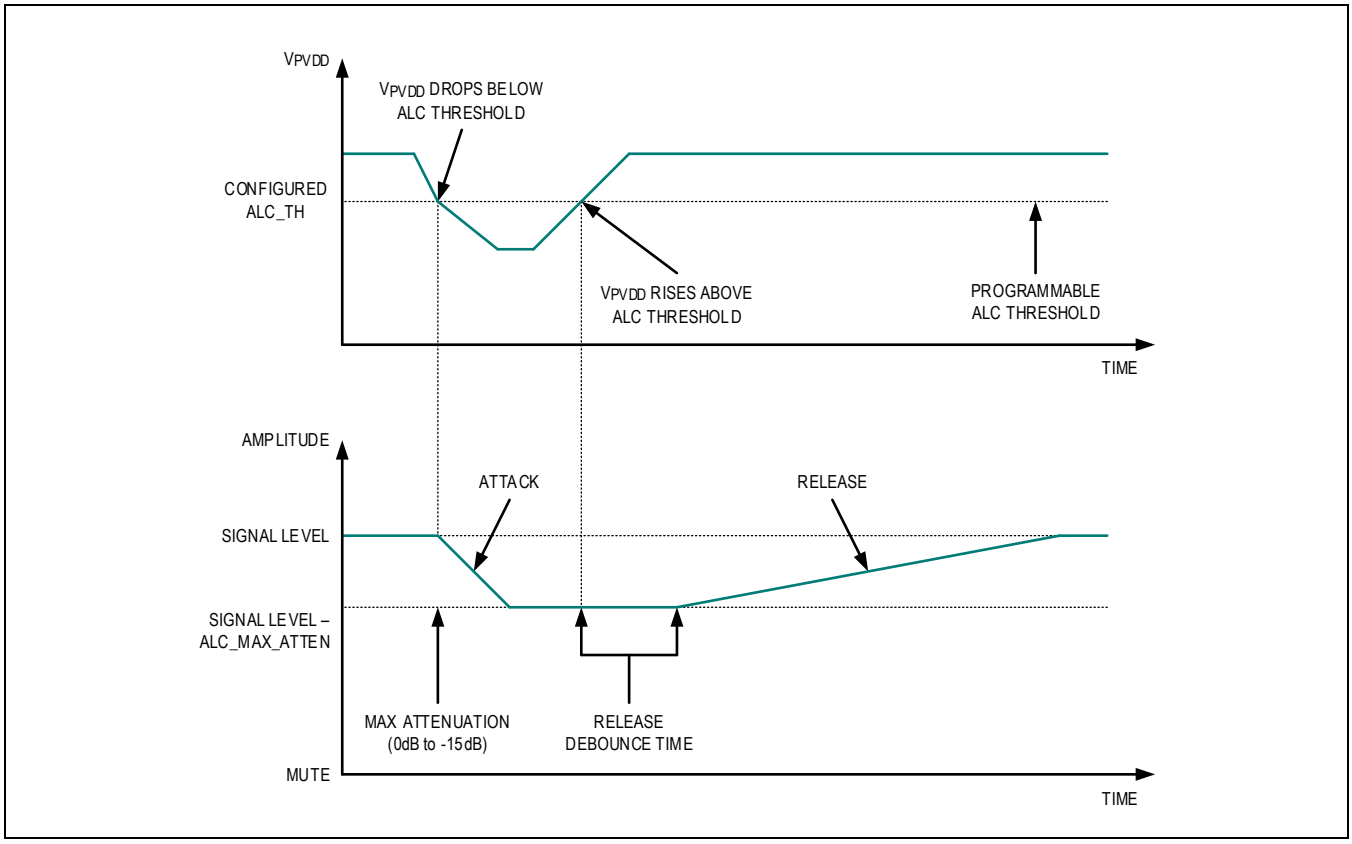


Figure 20. Brownout Protection ALC Volume Attenuation Behavior

When the ALC mute function is enabled (ALC_MUTE_EN), the ALC can also completely mute the speaker playback channel. The ALC mute and unmute functions can be independently configured to apply either instantly, or with a volume ramp (as selected with ALC_MUTE_RAMP_EN and ALC_UNMUTE_RAMP_EN). When ramping is enabled, the mute and unmute are applied at a rate of 20µs/dB.

When ALC mute is enabled and PVDD drops below the brownout threshold, attack starts normally and proceeds until the configured maximum attenuation (ALC_MAX_ATTEN) is applied. If PVDD remains below the threshold for longer than the ALC mute delay time (set by ALC_MUTE_DLY), then mute is applied (either instantly or ramped as selected). Once PVDD recovers and exceeds the brownout threshold for longer than the selected release debounce time, ALC unmute begins (again either instantly or ramped).

When the ALC mute ramp is enabled, if PVDD exceeds the brownout threshold while the mute ramp down is still in progress, then the mute ramp continues until the release debounce time has expired (similarly to volume attenuation attack and release). If the debounce time expires before the mute ramp is completed, then unmute begins from the current volume level. *Figure 21* demonstrates the behavior with the mute ramp disabled, while *Figure 22* is with the mute ramp enabled.

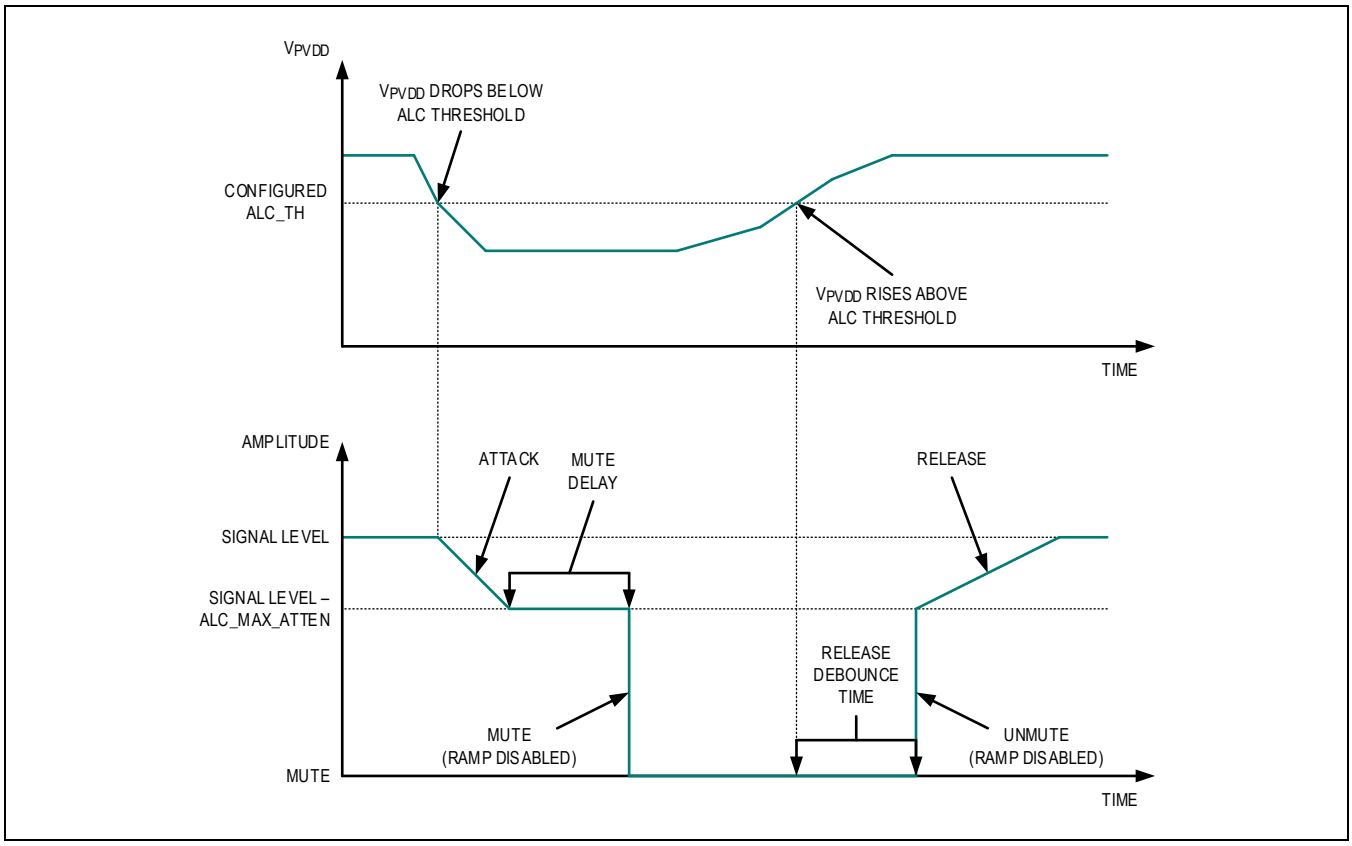


Figure 21. Brownout Protection ALC with Mute Enabled with No Ramp

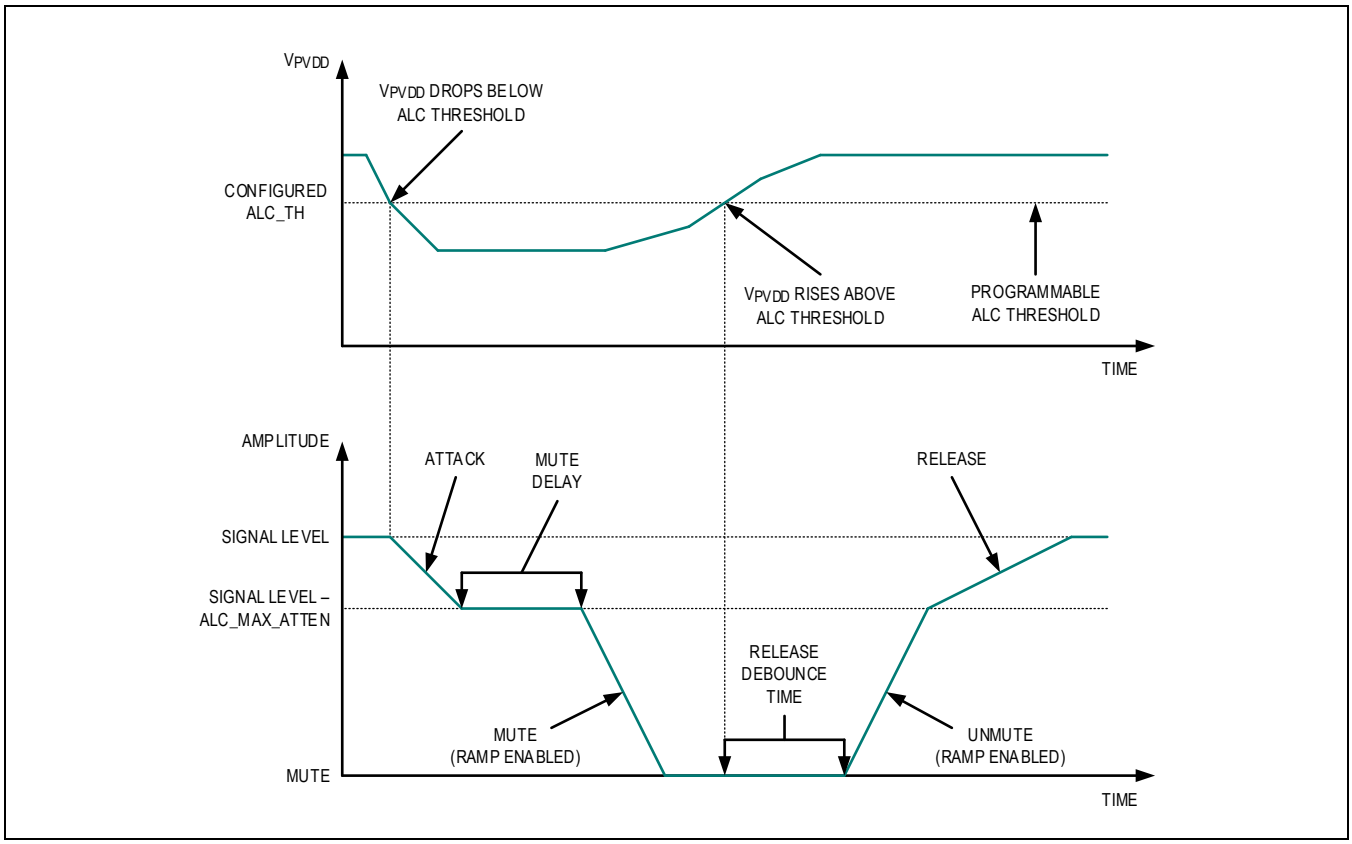


Figure 22. Brownout Protection ALC with Mute Enabled with Ramp

If the brownout ALC is used for battery protection only, and no volume attenuation is required before muting, then the ALC maximum attenuation should be set to 0dB (ALC_MAX_ATTEN). In this scenario, once PVDD drops below the brownout threshold no attenuation is applied and instead, the mute delay time begins. Once the mute delay time elapses, the ALC mute begins. This behavior is illustrated for a case with maximum attenuation set to 0dB with mute ramp enabled in *Figure 23*.

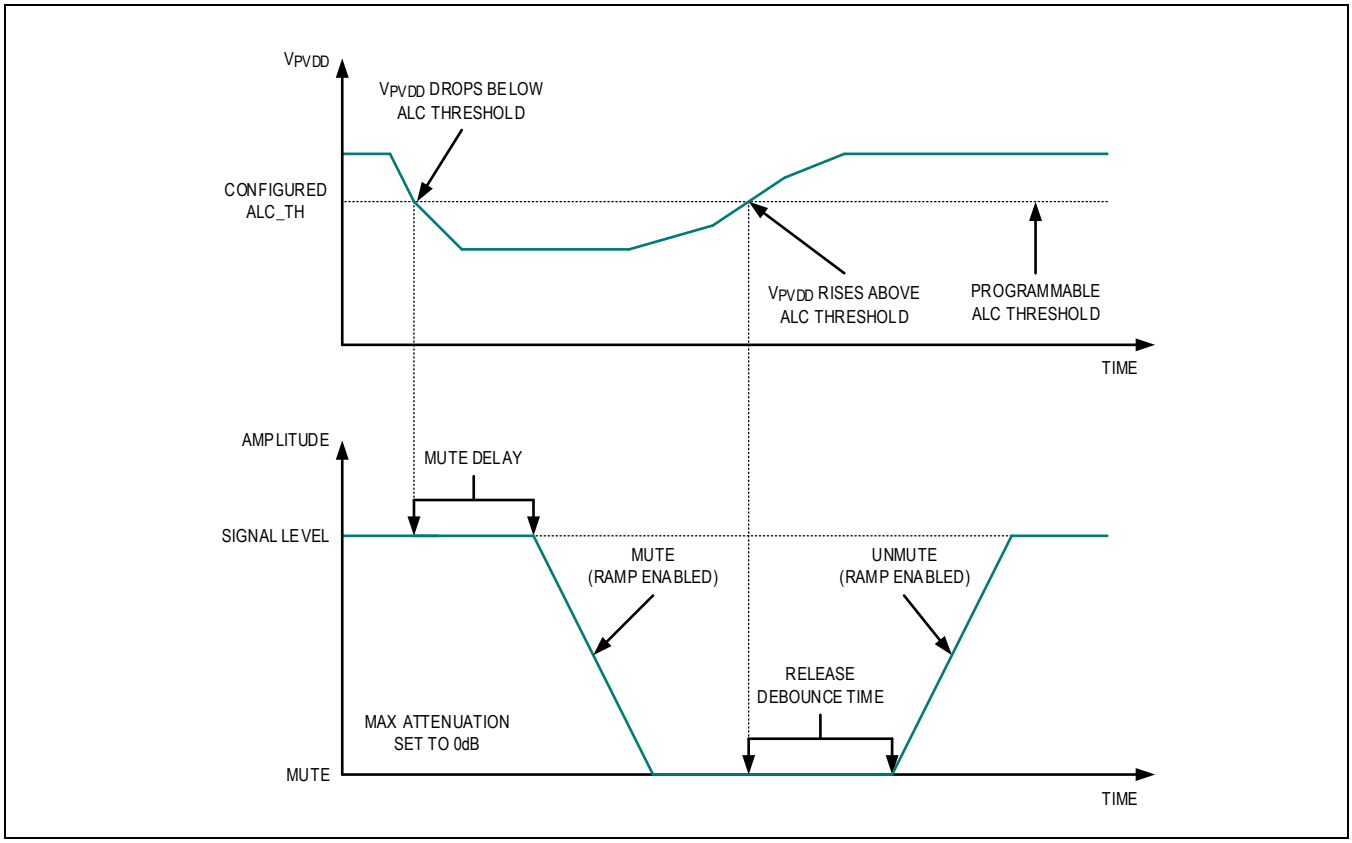


Figure 23. Brownout Protection ALC with Maximum Attenuation set to 0dB and Mute Enabled with Ramp

If the ALC release debounce time (ALC_RLS_DBT) is set to infinite hold, then once applied the configured volume attenuation and/or mute is not automatically released even after the PVDD voltage rises above the brownout threshold. The volume attenuation and mute remain applied until the host system software manually triggers the ALC release with the ALS_RLS_TGR bit. Attempting to release infinite hold while PVDD is still below the ALC threshold has no effect. An example of ALC infinite hold with a triggered release from attenuation (including an ineffective release attempt) is shown in *Figure 24*. A second example with a triggered release from mute is shown in *Figure 25*.

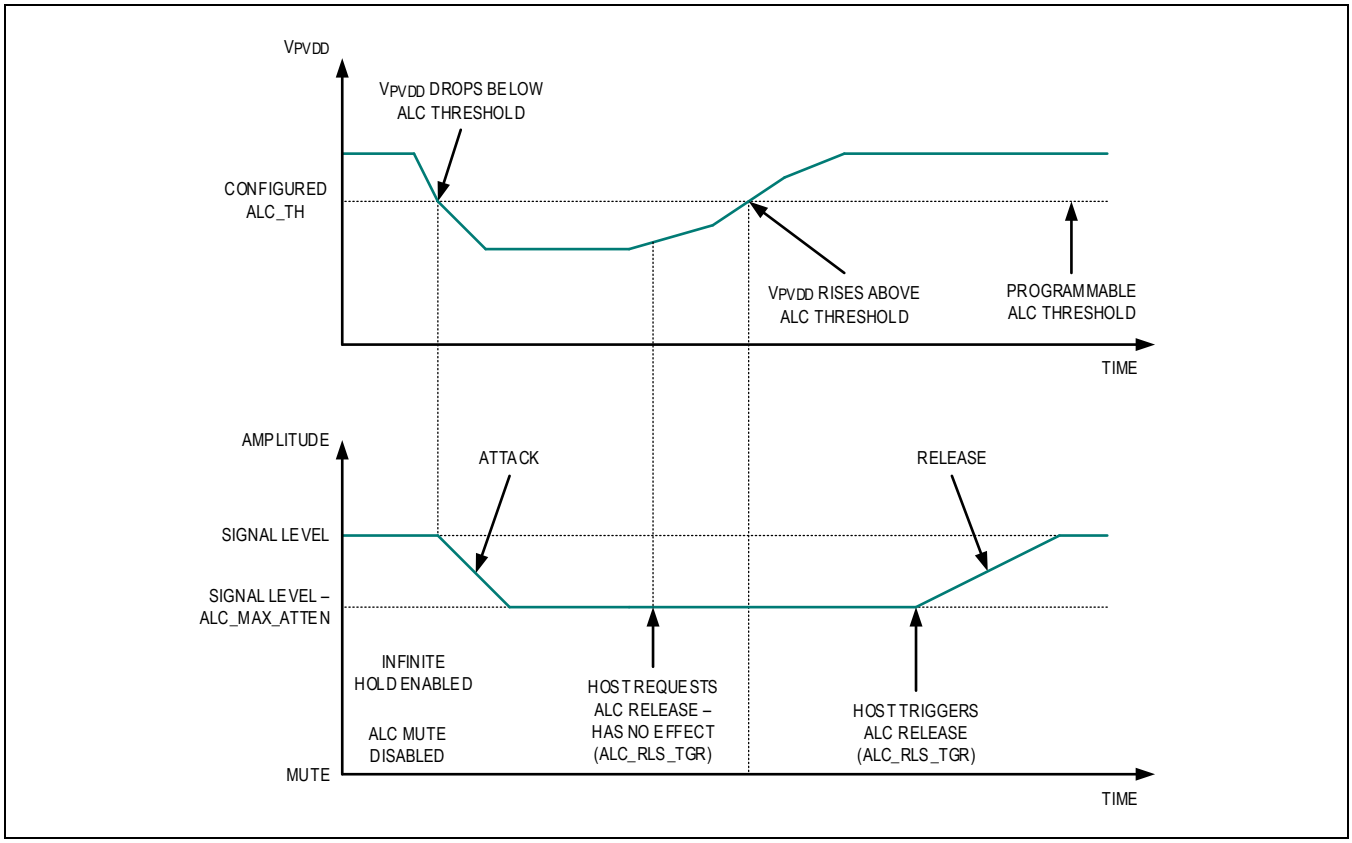


Figure 24. Brownout Protection ALC with Infinite Hold Enabled and Mute Disabled

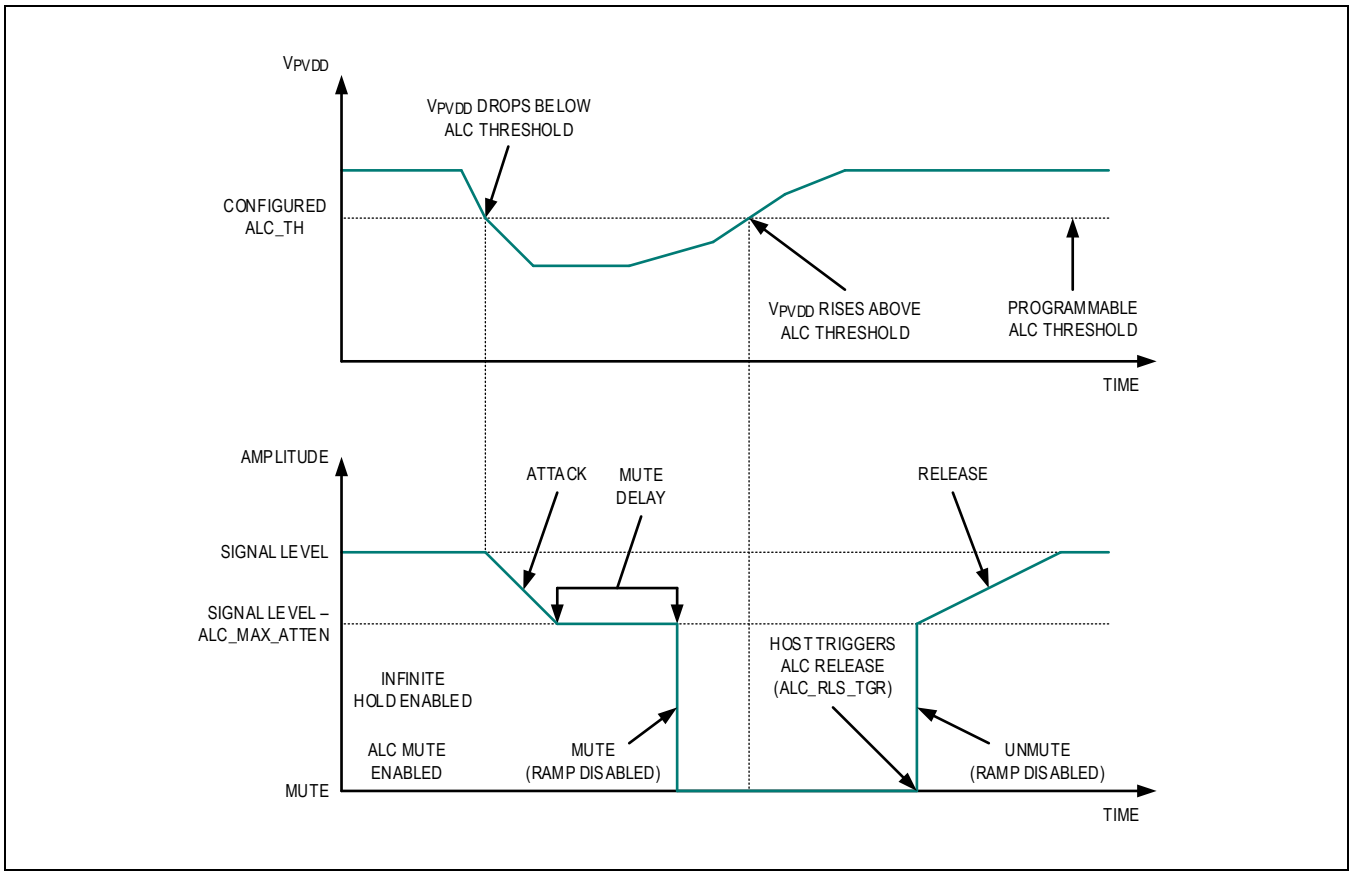


Figure 25. Brownout Protection ALC with Infinite Hold Enabled and Mute Enabled with No Ramp

Brownout Protection ALC Status Reporting

The device provides three status signals (threshold, active, and mute) to allow the host to monitor the brownout protection ALC operating state. The raw status bits for each of these three status signals directly report the current ALC operating state, and the rising edges of each raw status are captured by the state status bits (and are cleared on readback only).

The brownout ALC active status (BR_ALC_ACTIVE) reports whether the ALC is currently active. The raw ALC active status signal is low anytime PVDD is above the configured ALC threshold and the ALC attenuation/mute is fully released. The raw ALC active status goes high as soon as the PVDD voltage drops below the configured ALC threshold and attenuation begins (this includes the case where max attenuation is set to 0dB, and the ALC is waiting for the mute delay time). It remains high until PVDD has risen above the ALC threshold, and the ALC attenuation/mute has fully released.

The brownout ALC threshold status (BR_ALC_THRESH) notifies the host when the PVDD level has recovered to above the brownout threshold. Once PVDD drops below the currently configured brownout threshold, the ALC is activated, and the raw brownout ALC threshold status goes low. Then, once the PVDD level rises above the configured ALC threshold, the raw brownout ALC threshold status goes high (and is latched into the state bit) to indicate PVDD has recovered. The ALC is still active at this point, and release would proceed from here if PVDD remains above the brownout threshold.

The brownout ALC mute status (BR_ALC_MUTE) reports whether the ALC mute is currently fully applied. The raw ALC mute status signal is low anytime the ALC mute is not active and fully applied (this includes during the mute and unmute ramps). The raw ALC active status goes high once the ALC mute is fully applied (either instantly, or when the mute ramp is completed), and it remains high until the ALC mute release starts (either instantly, or when the unmute ramp begins).

The behavior of the brownout protection ALC raw status bits relative to the ALC operation state is shown in *Figure 26* for a normal case and in *Figure 27* for a case with infinite hold enabled.

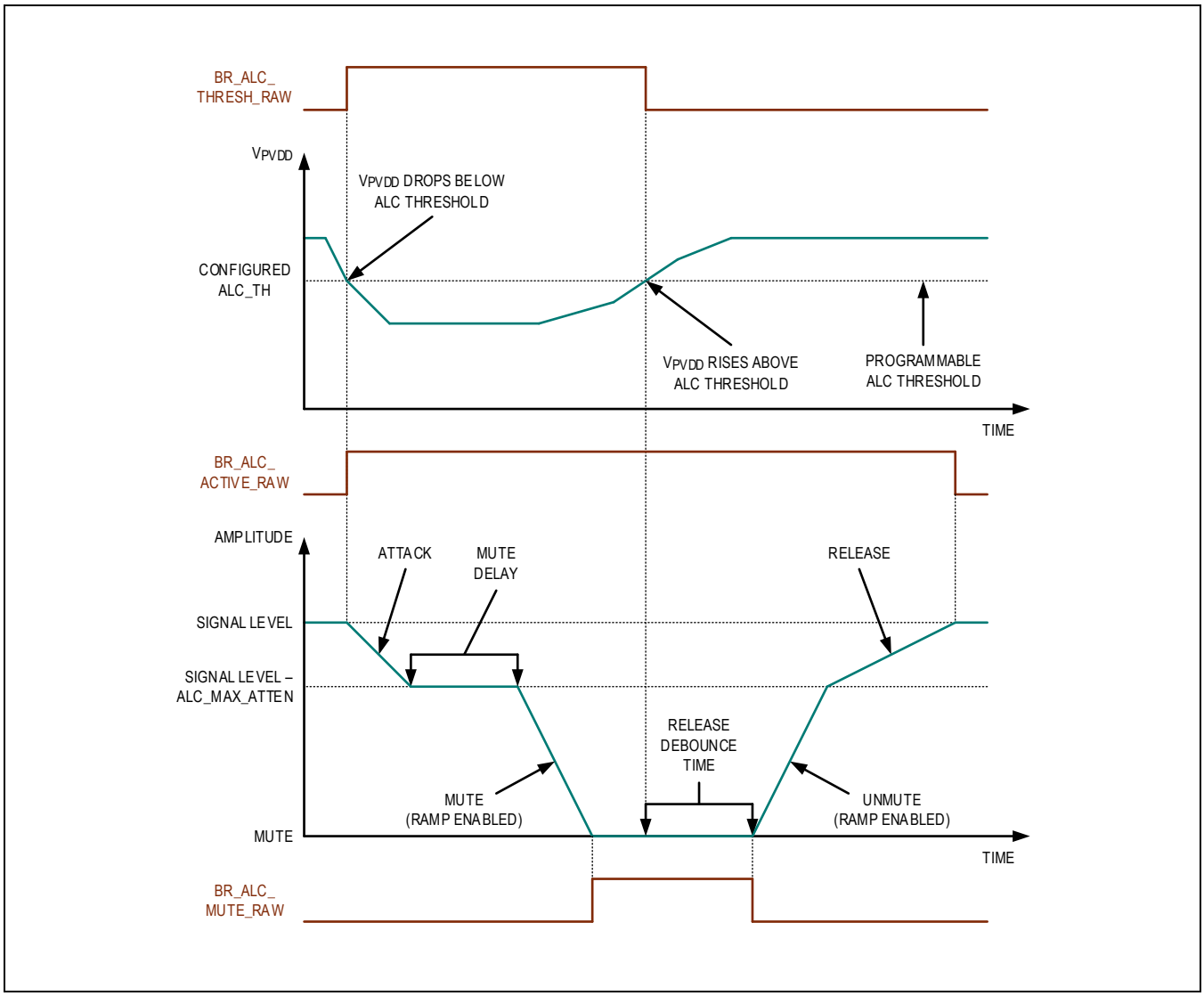


Figure 26. Brownout Protection ALC Status Signals for a Case with Mute Enabled with Ramp

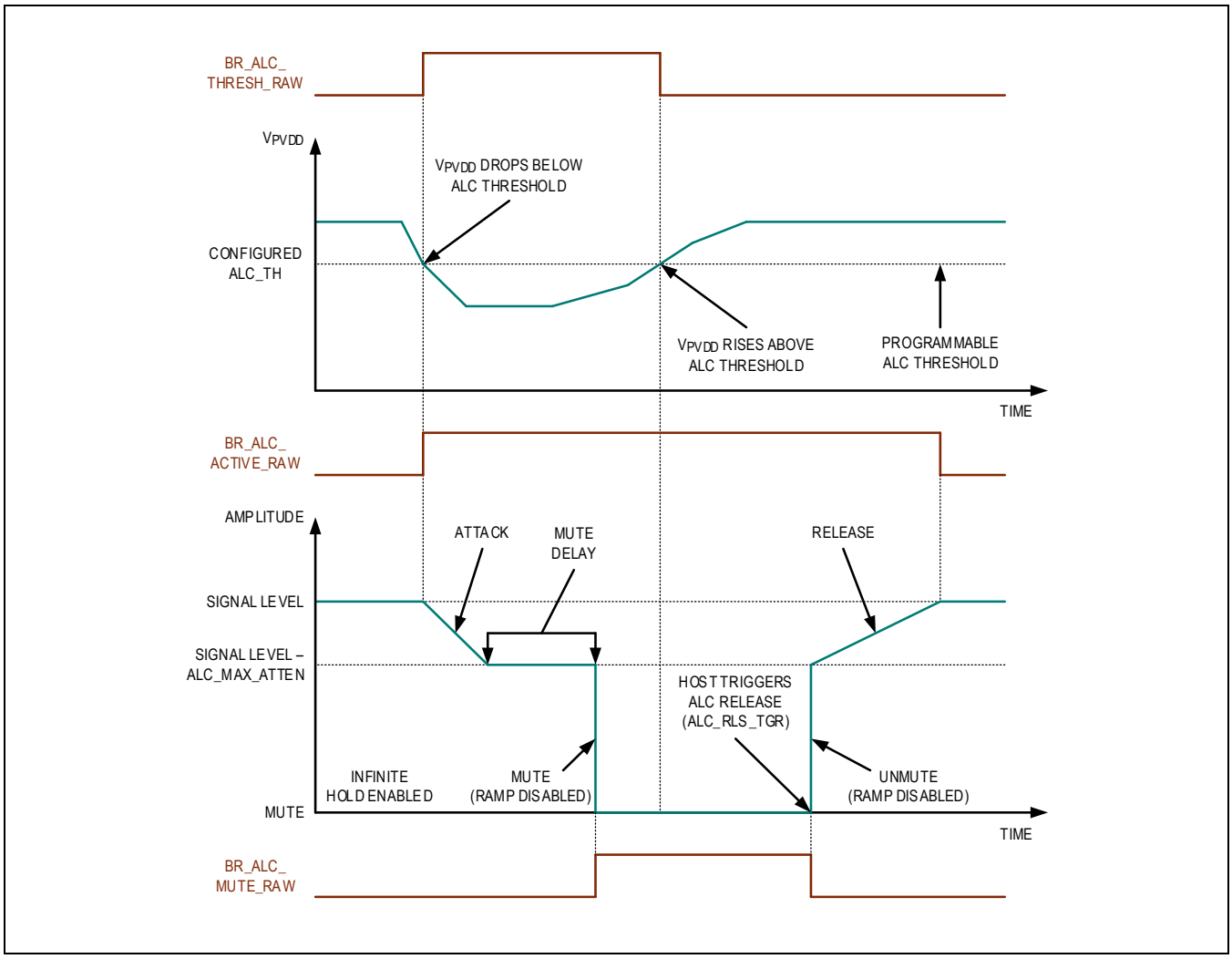


Figure 27. Brownout Protection ALC Status Signals for an Infinite Hold Case with Mute Ramp Disabled

Thermal Protection

When the device is active, to prevent damage the die temperature is automatically monitored to ensure that it does not exceed the thermal thresholds. The thermal-warning threshold is configured by the THERMWARN_THRESH[1:0] bit field and the thermal-shutdown threshold is configured by the THERMSHDN_THRESH[1:0] bit field, and each threshold has 15ºC (TYP) hysteresis.

If the die temperature exceeds the thermal-warning threshold, a status indicator (thermal warning begin) is set to warn the system. The thermal-shutdown recovery behavior is determined by the state of the THERM_AUTORESTART_EN bit.

When the THERM_AUTORESTART_EN bit is set to 0, the thermal-shutdown recovery is in manual mode. In manual mode, when the die temperature exceeds the thermal-shutdown threshold a status indicator is set (thermal shutdown) and the amplifier output is automatically disabled. Once the die temperature drops below the thermal warning threshold (minus hysteresis), a status indicator is set (thermal waning end), and the device is placed into software shutdown (EN = 0). The device remains in that state until the host manually re-enables it (with the global enable EN).

When the THERM_AUTORESTART_EN bit is set to 1, the thermal-shutdown recovery is in automatic mode. In automatic mode, when the die temperature exceeds the thermal-shutdown threshold a status indicator is set (thermal shutdown) and the amplifier output is automatically disabled. Once the die temperature drops below the thermal-warning threshold (minus hysteresis), a status indicator is set (thermal warning end), and the amplifier is automatically re-enabled. The global enable (EN = 1) is never changed during thermal shutdown and recovery in automatic mode.

Device Register Map Description

The device control bits fall into one of three basic types: read (R), write (W), or read and write (RW).

Read-only bit fields (R) are used to indicate an internal device state and cannot be changed directly by the host. Writing to these registers has no effect.

Write-only bit fields (W) are single-bit push-button controls. Writing a 1 to these bit fields performs an action (i.e., software reset, interrupt clear, etc.). Writing a 0 has no effect, and a readback always returns a 0.

Read/Write bit fields (RW) can be both read and written by the host, and the last written value is the value returned on readback.

Reserved bit fields are not used to program or control the device. When writing a register that contains reserved bit fields, always write a 0 to the reserved bit field segments.

Register Default Setting Differences Between MAX98388 and MAX98389

The register map shows the default power-on reset (PoR) settings for the MAX98388. Only one register default setting is different for MAX98389. In register 0x2092, the SPK_AMP_MODE bit defaults to single-cell mode (low) for MAX98388 and to two-cell mode (high) for MAX98389. Reading this register on power-up or after reset can be used to determine which version of the device is installed in the system.

Control Bit Write Access Restrictions

There are no direct read restrictions, and any bit field can be read back anytime the I^2C control interface is active. There are however write restrictions, and every write-enabled bit field falls into one of two write access subtypes.

The first write access subtype is dynamic. Dynamic bit fields effectively have no write access restrictions and can be safely changed (written) in any device state where the I^2C control interface is active. The second-bit field access subtype is restricted. Restricted bit fields should only be changed (written) when the related functional block is powered down. If the write access is restricted to the global enable (restriction EN), then the restricted bit field should only be changed (written) when the device is in software shutdown.

The bit field type and write access subtype are provided for every bit field in the detailed register description tables. For all bit fields with the restricted subtype, the dependency is also denoted in the "RES" column.

A detailed description of all device register types, access subtypes, and restriction dependencies that are used by this device is provided. The write access restrictions describe the specific device condition(s) that should be met (and the corresponding bit field settings) before the system attempts to change (write to) bit fields with that restriction type.

Table 11. Control Bit Types and Write Access Restrictions

REGISTER TYPE	WRITE ACCESS	WRITE ACCESS RESTRICTIONS		"RES" SYMBOL
		DESCRIPTION	CONDITION	
Read	Read-Only	None	—	—
Write or Write/Read	Dynamic	None	—	—
	Restricted	Device Held in Software Shutdown	EN = 0	EN
		Write Access Locked by the Hardware Unless Device is in Software Shutdown	EN = 0	ENL
		PCM Interface Disabled	PCM_TX_EN = 0 and PCM_RX_EN = 0	PCM
		Speaker Channel Disabled	SPK_EN = 0	SPK
		I/V Feedback Channels Disabled	IVFB_I_EN = 0 and IVFB_V_EN	IVFB
		Brownout Protection ALC Disabled	ALC_EN = 0	ALC

Register Map

Register Map

ADDRESS	NAME	MSB							LSB
Reset									
0x2000	Software Reset[7:0]	–	–	–	–	–	–	–	RST
Device Status Registers									
0x2001	Device Status Raw 1[7:0]	THERMSHDN_RAW	THERMWARN_BGN_RAW	THERMWARN_END_RAW	SPKMON_ERR_RAW	CLK_ERR_RAW	PWRDN_DONE_RAW	PWRUP_DONE_RAW	OTP_FAIL_RAW
0x2002	Device Status Raw 2[7:0]	–	–	BR_ALC_MUTE_RAW	BR_ALC_ACTIVE_RAW	BR_ALC_THRESH_RAW	PVDD_UVLO_SHDN_RAW	SPK_OVC_RAW	SPK_CLIP_RAW
0x2004	Device Status State 1[7:0]	THERMSHDN_STATE	THERMWARN_BGN_STATE	THERMWARN_END_STATE	SPKMON_ERR_STATE	CLK_ERR_STATE	PWRDN_DONE_STATE	PWRUP_DONE_STATE	OTP_FAIL_STATE
0x2005	Device Status State 2[7:0]	–	–	BR_ALC_MUTE_STATE	BR_ALC_ACTIVE_STATE	BR_ALC_THRESH_STATE	PVDD_UVLO_SHDN_STATE	SPK_OVC_STATE	SPK_CLIP_STATE
Thermal Protection									
0x2020	Thermal Warning Threshhold[7:0]	–	–	–	–	THERMWARN_THRESH[1:0]		THERMSHDN_THRESH[1:0]	
Error Monitor									
0x2031	Speaker Mon Threshold[7:0]	SPKMON_THRESH[7:0]							
0x2032	Speaker Mon Load	–	SPKMON_LOAD[6:0]						

ADDRESS	NAME	MSB							LSB
	Select[7:0]								
0x2033	Speaker Mon Duration[7:0]	–	–	–	–	SPKMON_DURATION[3:0]			
0x2037	Error Monitor Control[7:0]	–	–	–	–	–	–	SPKMON_EN	CMON_EN
PCM Registers									
0x2040	PCM Mode Config[7:0]	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			PCM_TX_INTERLEAVE	PCM_CHANSEL	PCM_TX_EXTRA_HIZ
0x2041	PCM Clock Setup[7:0]	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
0x2042	PCM Sample Rate Setup[7:0]	IV_SR[3:0]				PCM_SR[3:0]			
0x2044	PCM Tx Control 1[7:0]	–	–	PCM_VMON_SLOT[5:0]					
0x2045	PCM Tx Control 2[7:0]	–	–	PCM_IMON_SLOT[5:0]					
0x2050	PCM Tx HiZ Control 1[7:0]	PCM_TX_SLOT_HIZ[63:56]							
0x2051	PCM Tx HiZ Control 2[7:0]	PCM_TX_SLOT_HIZ[55:48]							

ADDRESS	NAME	MSB							LSB
0x2052	PCM Tx HiZ Control 3[7:0]	PCM_TX_SLOT_HIZ[47:40]							
0x2053	PCM Tx HiZ Control 4[7:0]	PCM_TX_SLOT_HIZ[39:32]							
0x2054	PCM Tx HiZ Control 5[7:0]	PCM_TX_SLOT_HIZ[31:24]							
0x2055	PCM Tx HiZ Control 6[7:0]	PCM_TX_SLOT_HIZ[23:16]							
0x2056	PCM Tx HiZ Control 7[7:0]	PCM_TX_SLOT_HIZ[15:8]							
0x2057	PCM Tx HiZ Control 8[7:0]	PCM_TX_SLOT_HIZ[7:0]							
0x2058	PCM RX Source 1[7:0]	–	–	–	–	–	–	PCM_DMMIX_CFG[1:0]	
0x2059	PCM RX Source 2[7:0]	PCM_DMMIX_CH1_SOURCE[3:0]				PCM_DMMIX_CH0_SOURCE[3:0]			
0x205C	PCM Tx Drive Strength[7:0]	–	–	–	–	–	–	PCM_DOUT_DRV[1:0]	
0x205D	PCM Tx Source Enables [7:0]	–	–	–	–	–	–	PCM_IMON_EN	PCM_VMON_EN

ADDRESS	NAME	MSB							LSB
0x205E	PCM Rx Enable[7:0]	–	–	–	–	–	–	–	PCM_RX_EN
0x205F	PCM Tx Enable[7:0]	–	–	–	–	–	–	–	PCM_TX_EN
Speaker Channel Control									
0x2090	Speaker Channel Volume Control[7:0]	–	SPK_VOL[6:0]						
0x2091	Speaker Channel Configuration[7:0]	–	–	–	SPK_VOL_RMPDN_BYPASS	SPK_VOL_RMPUP_BYPASS	SPK_INVERT	SPK_DITH_EN	SPK_DCBLK_EN
0x2092	Speaker Amplifier Output Configuration[7:0]	–	–	–	SPK_DAC_MODE	SPK_AMP_MODE	SPK_GAIN[2:0]		
0x2093	Speaker Amplifier SSM Configuration[7:0]	–	–	–	–	–	SPK_AMP_SSM_MOD[1:0]		SPK_AMP_SSM_EN
0x2094	Speaker Amplifier Edge Rate Control[7:0]	–	–	–	–	SPK_AMP_FALL_SR[1:0]		SPK_AMP_RISE_SR[1:0]	
0x209E	Speaker Channel Pink Noise Enable[7:0]	–	–	–	–	–	–	–	SPK_PINK_NOISE_EN

ADDRESS	NAME	MSB							LSB
0x209F	Speaker Channel and Amp Enable[7:0]	–	–	–	–	–	–	–	SPK_EN
IV Data Channel Control									
0x20A0	IV Data DSP Control[7:0]	–	–	–	IVFB_DITH_EN	IVFB_I_INVERT_EN	IVFB_V_INVERT_EN	IVFB_I_DCBLK_EN	IVFB_V_DCBLK_EN
0x20A7	IV Data Enables [7:0]	–	–	–	–	–	–	IVFB_I_EN	IVFB_V_EN
Brownout Protection ALC									
0x20E0	Brownout Protection ALC Threshold[7:0]	–	–	–	–	ALC_TH[3:0]			
0x20E1	Brownout Protection ALC Rates[7:0]	ALC_ATK_RATE[3:0]				ALC_RLS_RATE[3:0]			
0x20E2	Brownout Protection ALC Attenuation[7:0]	–	–	–	–	ALC_MAX_ATTEN[3:0]			
0x20E3	Brownout Protection ALC Release [7:0]	–	–	–	–	–	ALC_RLS_DBT[2:0]		
0x20E4	Brownout	–	–	ALC_UNMUTE_RAMP_EN	ALC_MUTE_RAMP_EN	ALC_MUTE_DELAY[2:0]			ALC_MUTE_EN

ADDRESS	NAME	MSB							LSB
	Protection ALC Mute[7:0]								
0x20EE	Brownout Protection ALC Infinite Hold Release [7:0]	–	–	–	–	–	–	–	ALC_RLS_TGR
0x20EF	Brownout Protection ALC Enable[7:0]	–	–	–	–	–	–	–	ALC_EN
System Configuration									
0x210E	Auto-Restart Behavior[7:0]	–	–	–	–	CLOCK_AUTORESTART_EN	OVC_RETRY_EN	THERM_AUTORESTART_EN	PVDD_UVLO_AUTORESTART_EN
0x210F	Global Enable[7:0]	–	–	–	–	–	–	–	EN
Device and Revision ID									
0x22FF	Revision ID[7:0]	REV_ID[7:0]							

Register Details

Software Reset (0x2000)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	RST
Reset	–	–	–	–	–	–	–	0b0

Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
RST	0	–	This bit field is used to trigger a software reset event. Writing a 1 resets the device and return the control registers to their power-on reset states. Writing a 0 has no effect, and readback always returns 0.	0: No action 1: Triggers a software reset event

Device Status Raw 1 (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_RAW	THERMWARN_BGN_RAW	THERMWARN_END_RAW	SPKMON_ERR_RAW	CLK_ERR_RAW	PWRDN_DONE_RAW	PWRUP_DONE_RAW	OTP_FAIL_RAW
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMSHDN_RAW	7	–	Thermal shutdown raw status bit.	0x0: Die temperature is lower than the configured thermal-shutdown threshold. 0x1: Die temperature is greater than the configured thermal-shutdown threshold.
THERMWARN_BGN_RAW	6	–	Thermal warning raw status bit.	0x0: Die temperature is lower than the configured thermal-warning threshold. 0x1: Die temperature is greater than the configured thermal-warning threshold.
THERMWARN_END_RAW	5	–	Thermal warning end raw status bit.	0x0: Die temperature has not dropped below the configured thermal-warning threshold (after exceeding it). 0x1: Die temperature has dropped below the configured thermal-warning threshold (after exceeding it).
SPKMON_ERR_RAW	4	–	Speaker amplifier output DC level monitor raw bit.	0x0: DC level exceeding the configured threshold was not detected at the speaker amplifier output since the last state clear. 0x1: DC level exceeding the configured threshold was detected at the speaker amplifier output since the last state clear.
CLK_ERR_RAW	3	–	Clock monitor error raw bit.	0x0: BCLK was present during active-mode operation since the last state clear. 0x1: BCLK stopped during active-mode operation.
PWRDN_DONE_RAW	2	–	Power-down transition done statrus raw bit.	0x0: Power-down transition from active state to software-shutdown state is not done (no transition or transition is in progress). 0x1: Power-down transition from active state to software-shutdown state done (transition completed).

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRUP_DONE_RAW	1	–	Power-up done transition status raw bit.	0x0: Power-up transition from software shutdown state to active state is not done (no transition or transition is in progress). 0x1: Power-up transition from software shutdown state to active state done (transition completed).
OTP_FAIL_RAW	0	–	OTP load fail status raw bit.	0x0: OTP settings successfully loaded during initialization. 0x1: OTP settings failed to load during initialization.

Device Status Raw 2 (0x2002)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BR_ALC_MUTE_RAW	BR_ALC_ACTIVE_RAW	BR_ALC_THRESH_RAW	PVDD_UVLO_SHDN_RAW	SPK_OVC_RAW	SPK_CLIP_RAW
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BR_ALC_MUTE_RAW	5	–	Brownout protection ALC mute raw status bit. Asserts high when the ALC mute is applied, and deasserts when the ALC mute is disabled.	0x0: Brownout protection ALC is not muting the speaker channel (ALC mute is not active or ramp is not complete). 0x1: Brownout protection ALC is muting the speaker channel (ALC mute is active and ramp down is complete).
BR_ALC_ACTIVE_RAW	4	–	Brownout protection ALC active raw status bit. Asserts high when PVDD drops below the configured ALC threshold and the ALC activates. Deasserts after both the PVDD voltage level recovers (rises above threshold) and any applied ALC attenuation has completely released.	0x0: Brownout protection ALC is not actively attenuating or muting the speaker channel (ALC is inactive or release is complete). 0x1: Brownout protection ALC is actively attenuating or muting the speaker channel (ALC is active or release is not complete).
BR_ALC_THRESH_RAW	3	–	Brownout protection ALC PVDD voltage threshold raw status bit. Asserts high when PVDD drops below the configured ALC threshold, and deasserts when the PVDD voltage level recovers (rises above threshold).	0x0: PVDD voltage level is currently above the configured brownout ALC threshold. 0x1: PVDD voltage level is currently below the configured brownout ALC threshold.
PVDD_UVLO_SHDN_RAW	2	–	PVDD undervoltage lockout error raw status bit.	0x0: PVDD UVLO has not triggered during active-state operation. 0x1: PVDD UVLO has triggered during active-state operation.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_OVC_RAW	1	–	Speaker amplifier output overcurrent monitor raw bit.	0x0: Speaker amplifier output overcurrent event is not detected. 0x1: Speaker amplifier output overcurrent event detected.
SPK_CLIP_RAW	0	–	Speaker amplifier output clipping monitor raw bit.	0x0: Speaker amplifier output clipping event is not detected. 0x1: Speaker amplifier output clipping event is detected.

Device Status State 1 (0x2004)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_STATE	THERMWARN_BGN_STATE	THERMWARN_END_STATE	SPKMON_ERR_STATE	CLK_ERR_STATE	PWRDN_DONE_STATE	PWRUP_DONE_STATE	OTP_FAIL_STATE
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMSHDN_STATE	7	–	Thermal shutdown status state bit.	0x0: Die temperature has not exceeded the configured thermal-shutdown threshold since the last state clear. 0x1: Die temperature has exceeded the configured thermal-shutdown threshold since the last state clear.
THERMWARN_BGN_STATE	6	–	Thermal warning status state bit.	0x0: Die temperature has not exceeded the configured thermal-warning threshold since the last state clear. 0x1: Die temperature has exceeded the configured thermal-warning threshold since the last state clear.
THERMWARN_END_STATE	5	–	Thermal warning end status state bit.	0x0: Die temperature has either not exceeded or remains above the configured thermal-warning threshold since the last state clear. 0x1: Die temperature has dropped back below the configured thermal-warning threshold (after previously exceeding it) since the last state clear.
SPKMON_ERR_STATE	4	–	Speaker amplifier output DC level monitor state bit.	0x0: DC level exceeding the configured threshold was detected at the speaker amplifier output. 0x1: DC level exceeding the configured threshold detected at the speaker amplifier output.
CLK_ERR_STATE	3	–	Clock monitor error state bit.	0x0: BCLK was present during active-mode operation since the last state clear. 0x1: BCLK was stopped during active-mode operation since the last state clear.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PWRDN_DONE_STATE	2	–	Power-down transition done state bit.	0x0: Power-down transition from active state to software-shutdown state was not completed (no transition or transition is in progress) since the last state clear. 0x1: Power-down transition from active state to software-shutdown state was completed since the last state clear.
PWRUP_DONE_STATE	1	–	Power-up transition done state bit.	0x0: Power-up transition from software-shutdown state to active state was not completed (no transition or transition is in progress) since the last state clear. 0x1: Power-up transition from software-shutdown state to active state was completed since the last state clear.
OTP_FAIL_STATE	0	–	OTP load fail status state bit.	0x0: OTP settings were successfully loaded during initializations since the last state clear. 0x1: OTP settings failed to load during an initialization since the last state clear.

Device Status State 2 (0x2005)

BIT	7	6	5	4	3	2	1	0
Field	–	–	BR_ALC_MUTE_STATE	BR_ALC_ACTIVE_STATE	BR_ALC_THRESH_STATE	PVDD_UVLO_SHDN_STATE	SPK_OVC_STATE	SPK_CLIP_STATE
Reset	–	–	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	–	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext

BITFIELD	BITS	RES	DESCRIPTION	DECODE
BR_ALC_MUTE_STATE	5	–	PVDD brownout protection ALC mute status state bit.	0x0: Brownout protection ALC did not fully mute the speaker channel since the last state clear. 0x1: Brownout protection ALC did fully mute the speaker channel since the last state clear.
BR_ALC_ACTIVE_STATE	4	–	PVDD brownout protection ALC active status state bit.	0x0: Brownout protection ALC did not actively attenuate the speaker channel since the last state clear. 0x1: Brownout protection ALC did actively attenuate the speaker channel since the last state clear.
BR_ALC_THRESH_STATE	3	–	PVDD brownout protection ALC threshold status state bit.	0x0: PVDD voltage did not rise above the configured brownout ALC threshold since the last state clear. 0x1: PVDD voltage did rise above the configured brownout ALC threshold since the last state clear.
PVDD_UVLO_SHDN_STATE	2	–	PVDD UVLO error state bit.	0x0: PVDD UVLO was not triggered during normal operation since the last state clear. 0x1: PVDD UVLO was triggered during normal operation since the last state clear.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_OVC_STATE	1	–	Speaker amplifier output overcurrent monitor state bit.	0x0: Speaker amplifier output overcurrent event was not detected since the last state clear. 0x1: Speaker amplifier output overcurrent event detected since the last state clear.
SPK_CLIP_STATE	0	–	Speaker amplifier output clipping monitor state bit.	0x0: Speaker amplifier output clipping event not detected since the last state clear. 0x1: Speaker amplifier output clipping event detected since the last state clear.

Thermal Warning Threshhold (0x2020)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	THERMWARN_THRESH[1:0]		THERMSHDN_THRESH[1:0]	
Reset	–	–	–	–	0b10		0b10	
Access Type	–	–	–	–	Write, Read		Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
THERMWARN_THRESH	3:2	EN	Sets the initial thermal-warning threshold temperature.	0x00: 95°C 0x01: 105°C 0x02: 115°C 0x03: 125°C
THERMSHDN_THRESH	1:0	EN	Sets the final thermal-shutdown threshold temperature.	0x00: 135°C 0x01: 145°C 0x02: 155°C 0x03: 165°C

Speaker Mon Threshold (0x2031)

BIT	7	6	5	4	3	2	1	0
Field	SPKMON_THRESH[7:0]							
Reset	0x58							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION
SPKMON_THRESH	7:0	EN	Sets the speaker output monitor voltage threshold. The threshold calculation differs depending on whether or not the current sense channel is active. If the current sense channel is active, then the speaker output monitor threshold is directly selected as follows (and is compared to the measured output level): **Threshold (voltage) = SPKMON_THRESH x 0.03375V** If the current sense channel is disabled, the threshold is calculated as % of

BITFIELD	BITS	RES	DESCRIPTION
			output full-scale voltage. However, in this mode the full-scale level varies as PVDD voltage changes, and therefore threshold should be selected based on the worst case PVDD condition (typically maximum possible PVDD in a given system). **Threshold (voltage) = (SPKMON_THRESH/256) x PVDD Voltage**

Speaker Mon Load Select (0x2032)

BIT	7	6	5	4	3	2	1	0
Field	–	SPKMON_LOAD[6:0]						
Reset	–	0b0001000						
Access Type	–	Write, Read						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPKMON_LOAD	6:0	EN	Selects the nominal speaker load resistance used by the speaker output monitor when the current sense channel is enabled. The measured output current and the selected load resistance value are used to calculate the output voltage level used by the output monitor (relative to the selected voltage threshold). This has no effect if the current sense channel is disabled.	0x0: 2.00Ω 0x1: 2.25Ω 0x2 to 0x5: ... (0.25Ω Steps) 0x6: 3.50Ω 0x7: 3.75Ω 0x8: 4.00Ω (Default) 0x9: 4.25Ω 0xA: 4.50Ω 0xB to 0x15: ... (0.25Ω Steps) 0x16: 7.50Ω 0x17: 7.75Ω 0x18: 8.00Ω 0x19: 8.25Ω 0x1A: 8.50Ω 0x1B to 0x7C: ... (0.25Ω Steps) 0x7D: 33.25Ω 0x7E: 33.50Ω 0x7F: 33.75Ω

Speaker Mon Duration (0x2033)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_DURATION[3:0]			
Reset	–	–	–	–	0x2			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPKMON_DURATION	3:0	EN	Sets the time duration over which the speaker output monitor must consecutively	0x0: 10ms 0x1: 25ms 0x2: 50ms 0x3: 75ms

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			detect an output level above the selected threshold before asserting a speaker output monitor error.	0x4: 100ms 0x5: 200ms 0x6: 300ms 0x7: 400ms 0x8: 500ms 0x9: 600ms 0xA: 700ms 0xB: 800ms 0xC: 900ms 0xD: 1000ms 0xE: 1100ms 0xF: 1200ms

Error Monitor Control (0x2037)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	SPKMON_EN	CMON_EN
Reset	–	–	–	–	–	–	0b0	0b1
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPKMON_EN	1	ENL	Enables the internal speaker output protection monitor.	0x0: Disable internal speaker output monitor. 0x1: Enable internal speaker output monitor.
CMON_EN	0	ENL	Enables the clock monitor. When enabled, the bit clock input (BCLK), frame clock input (LRCLK), and some internal clock busses are all monitored for clock activity.	0x0: Disable the clock monitor. 0x1: Enable the clock monitor.

PCM Mode Config (0x2040)

BIT	7	6	5	4	3	2	1	0
Field	PCM_CHANSZ[1:0]		PCM_FORMAT[2:0]			PCM_TX_INTERLEAVE	PCM_CHANSEL	PCM_TX_EXTRA_HIZ
Reset	0b11		0b000			0b0	0b0	0b0
Access Type	Write, Read		Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_CHANSZ	7:6	ENL	Configures the PCM data word size for each channel.	00: Reserved 01: 16-bit 10: 24-bit 11: 32-bit
PCM_FORMAT	5:3	ENL	Selects the PCM data format.	0x0: I^2S Mode 0x1: Left-justified 0x2: Reserved

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x3: TDM Mode 0 (0 BCLK delay from LRCLK) 0x4: TDM Mode 1 (1 BCLK delay from LRCLK) 0x5: TDM Mode 2 (2 BCLK delay from LRCLK) 0x6 to 0x7: Reserved
PCM_TX_INTERLEAVE	2	ENL	Controls whether or not I/V data assigned to the same channel is frame interleaved on the PCM data output (DOUT).	0x0: Disable Interleave mode. 0x1: Enable Interleave mode.
PCM_CHANSEL	1	ENL	Selects which LRCK edge starts a new frame (channel 0 or slot 0).	0: I^2S and LJ mode: Falling LRCLK edge starts a new frame. In TDM modes: Rising LRCLK edge starts a new frame. 1: In I^2S and LJ mode: Rising LRCLK edge starts a new frame. In TDM modes: Falling LRCLK edge starts a new frame.
PCM_TX_EXTRA_HIZ	0	ENL	Select whether DOUT is driven to zero or Hi-Z during extra BCLK cycles.	0x0: Transmit zero on DOUT during extra BCLK cycles. 0x1: Transmit Hi-Z on DOUT during extra BCLK cycles.

PCM Clock Setup (0x2041)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	PCM_BCLKEDGE	PCM_BSEL[3:0]			
Reset	–	–	–	0b0	0x4			
Access Type	–	–	–	Write, Read	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_BCLKEDGE	4	ENL	Selects the active BCLK edge.	0: Input data captured and output data valid on rising edge of BCLK. 1: Input data captured and output data valid on falling edge of BCLK.
PCM_BSEL	3:0	ENL	Selects the number of BCLKs per LRCLK expected by the PCM Interface.	0x0 to 0x1: Reserved 0x2: 32 0x3: 48 0x4: 64 0x5: 96 0x6: 128 0x7: 192 0x8: 256 0x9: 384 0xA: 512 0xB: 320 0xC to 0xF: Reserved

PCM Sample Rate Setup (0x2042)

BIT	7	6	5	4	3	2	1	0
Field	IV_SR[3:0]				PCM_SR[3:0]			
Reset	0x8				0x8			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IV_SR	7:4	ENL	Sets the sample rate of the I/V data output channels.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB to 0xF: Reserved
PCM_SR	3:0	ENL	Sets the sample rate of the PCM interface and the speaker playback channel. This corresponds to the expected LRCLK frequency.	0x0: 8kHz 0x1: 11.025kHz 0x2: 12kHz 0x3: 16kHz 0x4: 22.05kHz 0x5: 24kHz 0x6: 32kHz 0x7: 44.1kHz 0x8: 48kHz 0x9: 88.2kHz 0xA: 96kHz 0xB to 0xF: Reserved

PCM Tx Control 1 (0x2044)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_VMON_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_VMON_SLOT	5:0	PCM	Selects the data output (DOUT) slots for the voltage feedback channel output data. In non-TDM mode, only slot 0 and slot 1 are valid.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM Tx Control 2 (0x2045)

BIT	7	6	5	4	3	2	1	0
Field	–	–	PCM_IMON_SLOT[5:0]					
Reset	–	–	0b000000					
Access Type	–	–	Write, Read					

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_IMON_SLOT	5:0	PCM	Selects the data output (DOUT) slots for the current sense ADC channel output data. In non-TDM mode, only slot 0 and slot 1 are valid.	0x0: Slot 00/01 0x1: Slot 01/02 0x2: Slot 02/03 0x22 to 0x3D: ... 0x3E: Slot 62/63 0x3F: Reserved

PCM Tx HiZ Control 1 (0x2050)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[63:56]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 2 (0x2051)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[55:48]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 3 (0x2052)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[47:40]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 4 (0x2053)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[39:32]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 5 (0x2054)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[31:24]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 6 (0x2055)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[23:16]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 7 (0x2056)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[15:8]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM Tx HiZ Control 8 (0x2057)

BIT	7	6	5	4	3	2	1	0
Field	PCM_TX_SLOT_HIZ[7:0]							
Reset	0xFF							
Access Type	Write, Read							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_SLOT_HIZ	7:0	PCM	Configures the unused PCM transmitter data output slots to transmit either Hi-Z or 0. This setting only applies if the output data slot is unused, and is disregarded if an output data source is assigned to the slot and the output data source is enabled.	0: Output zero (logic-low) on the output slot if unused. 1: Output high impedance (Hi-Z) on the output slot if unused.

PCM RX Source 1 (0x2058)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_DMMIX_CFG[1:0]	
Reset	–	–	–	–	–	–	0b00	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DMMIX_CFG	1:0	PCM	Determines the behavior of the mono mixer circuit.	0x0: Output of mono mixer is Channel 0. 0x1: Output of mono mixer is Channel 1. 0x2: Output of mono mixer is (Channel 0 +Channel1)/2. 0x3: Reserved

PCM RX Source 2 (0x2059)

BIT	7	6	5	4	3	2	1	0

Field	PCM_DMMIX_CH1_SOURCE[3:0]	PCM_DMMIX_CH0_SOURCE[3:0]
Reset	0x0	0x0
Access Type	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DMMIX_CH1_SOURCE	7:4	PCM	Selects the PCM data input channel that is routed to channel 1 of the digital mono mixer.	0x0: PCM Input Channel 0 0x1: PCM Input Channel 1 0x2: PCM Input Channel 2 ...: ... 0xE: PCM Input Channel 14 0xF: PCM Input Channel 15
PCM_DMMIX_CH0_SOURCE	3:0	PCM	Selects the PCM data input channel that is routed to channel 0 of the digital mono mixer.	0x0: PCM Input Channel 0 0x1: PCM Input Channel 1 0x2: PCM Input Channel 2 ...: ... 0xE: PCM Input Channel 14 0xF: PCM Input Channel 15

PCM Tx Drive Strength (0x205C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_DOUT_DRV[1:0]	
Reset	–	–	–	–	–	–	0b01	
Access Type	–	–	–	–	–	–	Write, Read	

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_DOUT_DRV	1:0	PCM	Configures the output drive strength of DOUT pin.	0x0: Reduced drive strength. 0x1: Normal drive strength. 0x2: High drive strength. 0x3: Maximum drive strength.

PCM Tx Source Enables (0x205D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	PCM_IMON_EN	PCM_VMON_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_IMON_EN	1	TXEN	Enables transmit of the current sense ADC channel output data on the assigned data output (DOUT) slot.	0x0: Disable current sense ADC data transmit. 0x1: Enable current sense ADC data transmit.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_VMON_EN	0	TXEN	Enables transmit of the voltage feedback channel output data on the assigned data output (DOUT) slot.	0x0: Disable voltage feedback data transmit. 0x1: Disable voltage feedback data transmit.

PCM Rx Enable (0x205E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PCM_RX_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_RX_EN	0	–	Enables the speaker playback channel data input.	0: PCM data input disabled. 1: PCM data input enabled.

PCM Tx Enable (0x205F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	PCM_TX_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
PCM_TX_EN	0	–	Enables the data output (DOUT) of the PCM interface.	0x0: PCM T_X disabled. 0x1: PCM T_X enabled.

Speaker Channel Volume Control (0x2090)

BIT	7	6	5	4	3	2	1	0
Field	–	SPK_VOL[6:0]						
Reset	–	0b0000000						
Access Type	–	Write, Read						

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_VOL	6:0	–	Sets the digital volume level of the speaker amplifier channel.	0x00: 0dB 0x01: -0.5dB 0x02: -1.0dB ...: (-0.5dB steps) 0x7C: -62.0dB 0x7D: -62.5dB 0x7E: -63dB 0x7F: Mute

Speaker Channel Configuration (0x2091)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	SPK_VOL_RMPDN_BYPASS	SPK_VOL_RMPUP_BYPASS	SPK_INVERT	SPK_DITH_EN	SPK_DCBLK_EN
Reset	–	–	–	0b0	0b0	0b0	0b1	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_VOL_RMPDN_BYPASS	4	SPK	Controls whether the speaker amplifier channel volume is internally ramped-down both during shutdown and when muting the channel.	0: Volume ramp enabled 1: Volume ramp bypassed
SPK_VOL_RMPUP_BYPASS	3	SPK	Controls whether the speaker amplifier channel volume is internally ramped-up both during startup and when unmuting the channel.	0: Volume ramp enabled 1: Volume ramp bypassed
SPK_INVERT	2	SPK	Inverts the speaker amplifier channel output.	0: Output is normal. 1: Output is inverted.
SPK_DITH_EN	1	SPK	Selects whether or not dither is applied to the data in the speaker amplifier channel.	0: Dither disabled. 1: Dither enabled.
SPK_DCBLK_EN	0	SPK	Enables the DC blocking filter in the speaker amplifier channel.	0: DC blocking filter disabled. 1: DC blocking filter enabled.

Speaker Amplifier Output Configuration (0x2092)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	SPK_DAC_MODE	SPK_AMP_MODE	SPK_GAIN[2:0]		
Reset	–	–	–	0b0	0b0	0b011		
Access Type	–	–	–	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_DAC_MODE	4	–	Sets the speaker amplifier channel DAC to operate in low-power mode or high-performance mode.	0x0: DAC operates in low-power mode. 0x1: DAC operates in high-performance mode.
SPK_AMP_MODE	3	SPK	Selects whether the speaker amplifier is operating in single-cell mode or in two-cell/boosted mode. The expected PVDD supply range is different based on the selected speaker amplifier operating mode. The MAX98388 defaults to single-cell mode (shown as the default value here), while the MAX98389 defaults to two-cell mode.	0x0: Single-cell mode (default for MAX98388). 0x1: Two-cell/boosted mode (default for MAX98389).
SPK_GAIN	2:0	SPK	Sets the maximum peak output voltage level (V_{MPO}) in terms of RMS voltage for the speaker channel amplifier (no-load). The peak output voltage level for each setting depends on the selected speaker amplifier operating mode (SPK_AMP_MODE). Values in dB are gain relative to the baseline speaker path DAC full-scale output level of 0.5dBV.	0x00: Single-cell mode: 0.75V_{RMS} (-3dB) Two-cell mode: 1.50V_{RMS} (+3dB) 0x01: Single-cell mode: 1.06V_{RMS} (0dB) Two-cell mode: 2.11V_{RMS} (+6dB) 0x02: Single-cell Mode: 1.50V_{RMS} (+3dB) Two-cell mode: 2.99V_{RMS} (+9dB) 0x03: Single-cell Mode: 2.11V_{RMS} (+6dB) Two-cell mode: 4.22V_{RMS} (+12dB) 0x04: Single-cell Mode: 2.99V_{RMS} (+9dB) Two-cell mode: 5.96V_{RMS} (+15dB) 0x05: Single-cell Mode: 4.22V_{RMS} (+12dB) Two-cell mode: 8.41V_{RMS} (+18dB) 0x06-0x07: Reserved

Speaker Amplifier SSM Configuration (0x2093)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SPK_AMP_SSM_MOD[1:0]		SPK_AMP_SSM_EN
Reset	–	–	–	–	–	0b00		0b1
Access Type	–	–	–	–	–	Write, Read		Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_AMP_SSM_MOD	2:1	SPK	Selects the speaker amplifier spread-spectrum modulation ratio.	0x0: ±1.5% 0x1: ±3.0% 0x2: ±4.5% 0x3: ±6.0%
SPK_AMP_SSM_EN	0	SPK	Speaker amplifier spread-spectrum modulation enable.	0x0: SSM disabled. 0x1: SSM enabled.

Speaker Amplifier Edge Rate Control (0x2094)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPK_AMP_FALL_SR[1:0]		SPK_AMP_RISE_SR[1:0]	
Reset	–	–	–	–	0x3		0x3	

Access Type	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_AMP_FALL_SR	3:2	SPK	Speaker amplifier falling edge slew-rate control.	0x0: Normal slew rate. 0x1: Reduced slew rate. 0x2: Maximum slew rate. 0x3: Increased slew rate.
SPK_AMP_RISE_SR	1:0	SPK	Speaker amplifier rising edge slew rate control.	0x0: Normal slew rate. 0x1: Reduced slew rate. 0x2: Maximum slew rate. 0x3: Increased slew rate.

Speaker Channel Pink Noise Enable (0x209E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SPK_PINK_NOISE_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_PINK_NOISE_EN	0	ENL	Reconfigures the speaker channel to output (when in the active state) internally generated pink noise (instead of input data from DIN). This mode must be enabled prior to exiting the software-shutdown state, and requires a valid bit clock (BCLK) and frame clock (LRCLK) during the power-up state transition. Once enabled in the active state, the clocks can be disabled and the amplifier continues to output pink noise.	0x0: Pink noise output mode disabled (normal operation). 0x1: Pink noise output mode enabled.

Speaker Channel and Amp Enable (0x209F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SPK_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
SPK_EN	0	–	Speaker Amplifier Channel Enable. If set high, then the speaker amplifier channel is enabled anytime global enable is also set.	0x0: Speaker amplifier channel disabled (Regardless of global enable setting). 0x1: Speaker amplifier channel enabled (When global enable is also set).

IV Data DSP Control (0x20A0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	IVFB_DITH_EN	IVFB_I_INVERT_EN	IVFB_V_INVERT_EN	IVFB_I_DCBLK_EN	IVFB_V_DCBLK_EN
Reset	–	–	–	0b1	0b0	0b0	0b0	0b0
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVFB_DITH_EN	4	IVFB	Select whether or not dither is applied to the I/V data channels.	0x0: Dither disabled. 0x1: Dither enabled.
IVFB_I_INVERT_EN	3	IVFB	Inverts the current feedback channel.	0x0: Channel is not inverted. 0x1: Channel is inverted.
IVFB_V_INVERT_EN	2	IVFB	Inverts the voltage feedback channel.	0x0: Channel is not inverted. 0x1: Channel is inverted.
IVFB_I_DCBLK_EN	1	IVFB	Enables the DC blocking filter in the current feedback channel.	0x0: DC blocker disabled. 0x1: DC blocker enabled.
IVFB_V_DCBLK_EN	0	IVFB	Enables the DC blocking filter in the voltage feedback channel.	0x0: DC blocker disabled. 0x1: DC blocker enabled.

IV Data Enables (0x20A7)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	IVFB_I_EN	IVFB_V_EN
Reset	–	–	–	–	–	–	0b0	0b0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVFB_I_EN	1	–	Enables the speaker current sense ADC channel. When this bit is set to 1, the current sense ADC channel is powered up when the device is in the active state (EN = 1).	0x0: Current sense ADC channel is disabled. 0x1: Current sense ADC channel is enabled.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
IVFB_V_EN	0	–	Enables the speaker voltage feedback channel. When this bit is set to 1, the voltage feedback channel is powered up when the device is in the active state (EN = 1).	0x0: Voltage feedback channel is disabled. 0x1: Voltage feedback channel is enabled.

Brownout Protection ALC Threshold (0x20E0)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALC_TH[3:0]			
Reset	–	–	–	–	0x4			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_TH	3:0	ALC	Selects the brownout ALC PVDD falling-voltage threshold (attack threshold). The threshold setting and step size changes depending on the selected speaker amplifier mode (SPK_AMP_MODE). The step size between threshold settings is 75mV in 1-cell mode, and 150mV in 2-cell or boosted mode. **Format:** 1-Cell mode threshold/2-Cell or boosted-mode threshold.	0x0: 3.625V / 7.25V 0x1: 3.550V / 7.10V 0x2: 3.475V / 6.95V 0x3: 3.400V / 6.80V 0x4: 3.325V / 6.65V 0x5: 3.250V / 6.50V 0x6: 3.175V / 6.35V 0x7: 3.100V / 6.20V 0x8: 3.025V / 6.05V 0x9: 2.950V / 5.90V 0xA: 2.875V / 5.75V 0xB: 2.800V / 5.60V 0xC: 2.725V / 5.45V 0xD: 2.650V / 5.30V 0xE: 2.575V / 5.15V 0xF: 2.500V / 5.00V

Brownout Protection ALC Rates (0x20E1)

BIT	7	6	5	4	3	2	1	0
Field	ALC_ATK_RATE[3:0]				ALC_RLS_RATE[3:0]			
Reset	0x2				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_ATK_RATE	7:4	ALC	Selects the ALC attack rate.	0x0: Instant 0x1: 10µs / dB 0x2: 20µs / dB 0x3: 40µs / dB 0x4: 80µs / dB 0x5: 160µs / dB 0x6: 320µs / dB 0x7: 640µs / dB 0x8: 1.28ms / dB

BITFIELD	BITS	RES	DESCRIPTION	DECODE
				0x9: 2.56ms / dB 0xA: 5.12ms / dB 0xB: 10.24ms / dB 0xC: 20.48ms / dB 0xD: 40.96ms / dB 0xE: 81.92ms / dB 0xF: 163.84ms / dB
ALC_RLS_RATE	3:0	ALC	Selects the ALC release rate.	0x0: 20µs / dB 0x1: 40µs / dB 0x2: 80µs / dB 0x3: 160µs / dB 0x4: 320µs / dB 0x5: 640µs / dB 0x6: 1.28ms / dB 0x7: 2.56ms / dB 0x8: 5.12ms / dB 0x9: 10.24ms / dB 0xA: 20.48ms / dB 0xB: 40.96ms / dB 0xC: 81.92ms / dB 0xD: 163.84ms / dB 0xE: 327.68ms / dB 0xF: 655.36ms / dB

Brownout Protection ALC Attenuation (0x20E2)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	ALC_MAX_ATTEN[3:0]			
Reset	–	–	–	–	0x6			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_MAX_ATTEN	3:0	ALC	Selects the ALC attack maximum attenuation.	0x0: 0dBFS 0x1: -1dBFS 0x2: -2dBFS 0x3: -3dBFS 0x4: -4dBFS 0x5: -5dBFS 0x6: -6dBFS 0x7: -7dBFS 0x8: -8dBFS 0x9: -9dBFS 0xA: -10dBFS 0xB: -11dBFS 0xC: -12dBFS 0xD: -13dBFS 0xE: -14dBFS 0xF: -15dBFS

Brownout Protection ALC Release (0x20E3)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	ALC_RLS_DBT[2:0]		

Reset	–	–	–	–	–	0b010
Access Type	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_RLS_DBT	2:0	ALC	Selects the ALC release debounce time.	0x0: 0.01ms 0x1: 0.1ms 0x2: 1ms 0x3: 10ms 0x4: 100ms 0x5: 250ms 0x6: 500ms 0x7: Infinite Hold

Brownout Protection ALC Mute (0x20E4)

BIT	7	6	5	4	3	2	1	0
Field	–	–	ALC_UNMUTE_RAMP_EN	ALC_MUTE_RAMP_EN	ALC_MUTE_DELAY[2:0]			ALC_MUTE_EN
Reset	–	–	0b1	0b1	0b001			0b1
Access Type	–	–	Write, Read	Write, Read	Write, Read			Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_UNMUTE_RAMP_EN	5	ALC	Enables volume ramping for ALC unmute transitions. When ALC unmute ramp is enabled, a release rate of 20µs/dB is used for the unmute ramp-up.	0x0: ALC does not ramp the volume level when unmuting. 0x1: ALC ramps the volume level when unmuting.
ALC_MUTE_RAMP_EN	4	ALC	Selects whether or not volume ramping is used for ALC mute transitions. When ALC mute ramp is enabled, an attack rate of 20µs/dB is used for the mute ramp-down.	0x0: ALC does not ramp the volume level when muting. 0x1: ALC ramps the volume level when muting.
ALC_MUTE_DELAY	3:1	ALC	Selects the delay before the onset of ALC mute (if enabled).	0x0: 0.01ms 0x1: 0.05ms 0x2: 0.1ms 0x3: 0.5ms 0x4: 1ms 0x5: 5ms 0x6: 25ms 0x7: 250ms
ALC_MUTE_EN	0	ALC	Selects whether or not the ALC can mute the speaker channel.	0x0: ALC cannot mute the speaker channel. 0x1: ALC can mute the speaker channel.

Brownout Protection ALC Infinite Hold Release (0x20EE)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ALC_RLS_TGR

Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write Only

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_RLS_TGR	0	–	Used to manually release brownout ALC volume attenuation and mute when infinite hold is enabled (ALC_RLS_DBT).	0x0: Self-clearing and always read back as '0'. 0x1: If infinite hold is enabled, write a '1' to begin the release phase. This has no effect if it is attempted while PVDD is still below the ALC threshold.

Brownout Protection ALC Enable (0x20EF)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ALC_EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
ALC_EN	0	EN	Select whether brownout protection ALC is enabled or disabled.	0: ALC is disabled. 1: ALC is enabled.

Auto-Restart Behavior (0x210E)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	CLOCK_AUTORESTART_EN	OVC_RETRY_EN	THERM_AUTORESTART_EN	PVDD_UVLO_AUTORESTART_EN
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	RES	DESCRIPTION	DECODE
CLOCK_AUTORESTART_EN	3	EN	Controls whether or not the device automatically resumes playback when the clocks become valid after the device is disabled due to a clock monitor error.	0x0: Device does not automatically restart after a valid bit clock (BCLK) is reapplied. 0x1: Device automatically restarts after a valid bit clock (BCLK) is reapplied.
OVC_RETRY_EN	2	EN	Controls whether or not the speaker amplifier is automatically reenabled after an OVC fault condition.	0x0: Overcurrent recovery is in manual retry mode. 0x1: Overcurrent recover is in automatic retry mode.
THERM_AUTORESTART_EN	1	EN	Control whether or not the device automatically returns to the active state	0x0: Thermal shutdown recovery is in manual mode.

BITFIELD	BITS	RES	DESCRIPTION	DECODE
			when the die temp recovers from thermal shutdown.	0x1: Thermal shutdown recovery is in auto mode.
PVDD_UVLO_AUTORESTART_EN	0	EN	Controls whether or not the device automatically returns to the active state when PVDD recovers from a UVLO event.	0: PVDD UVLO recovery is in manual mode. 1: PVDD UVLO recovery is in automatic mode.

Global Enable (0x210F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	EN
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

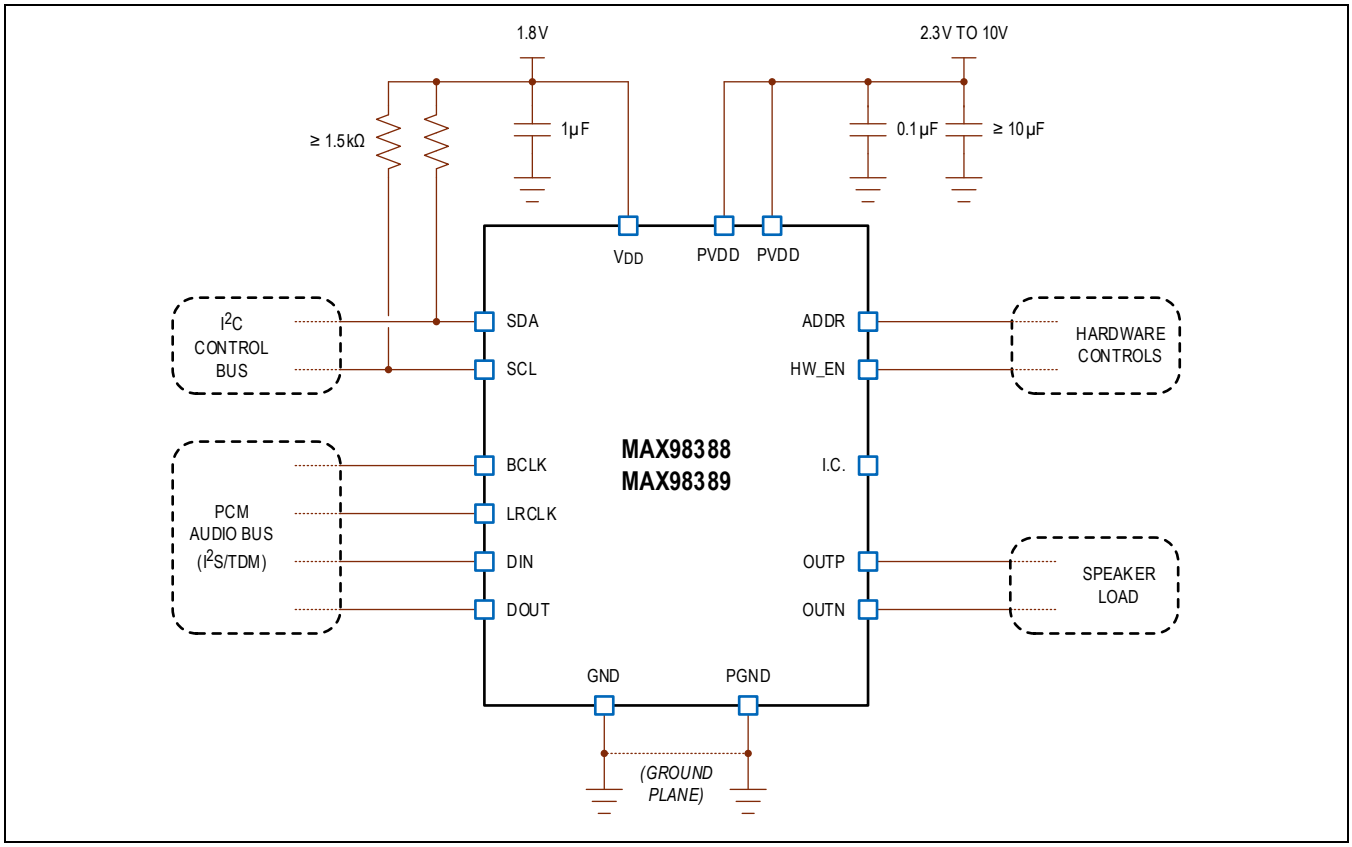
BITFIELD	BITS	RES	DESCRIPTION	DECODE
EN	0	–	Disable or enable all blocks and reset all logic except the I²C interface and control registers.	0: Device powered down. 1: Device enabled.

Revision ID (0x22FF)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x41							
Access Type	Read Only							

BITFIELD	BITS	RES	DESCRIPTION	DECODE
REV_ID	7:0	–	Revision of the device. Updated at every device hardware revision.	0x41: Device revision number.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX98388EWE+	-40°C to +85°C	16 WLP
MAX98388EWE+T	-40°C to +85°C	16 WLP
MAX98389EWE+	-40°C to +85°C	16 WLP
MAX98389EWE+T	-40°C to +85°C	16 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/23	Release for Market Intro	—
1	9/23	Corrected a typo in the speaker output monitor voltage threshold calculation	47, 67

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