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MAX98363

Tiny, Cost-Effective, SoundWire, Class D Amplifier

General Description

The MAX98363 is a tiny, low-cost, SoundWire® input Class D mono amplifier that provides industry-leading, Class AB audio performance with Class D efficiency. The device features an internal tone generator, interrupt control, and selectable slew-time settings for SoundWire data output PHY. A novel pinout allows customers to use the cost-effective wafer-level package (WLP) with no need for expensive in-pad vias.

The MAX98363 is a SoundWire peripheral device that supports MIPI SoundWire v1.2-compatible digital interface for audio and control data. The digital interface is highly flexible and supports a variety of input clock frequencies. Also, selectable slew-time controls on the SoundWire data output PHY help minimize EMI on a range of capacitive bus loads. The digital interface operates on 1.8V nominal voltage supply which can be either supplied externally, or generated by an internal LDO.

An internal tone generator, with a variety of frequency options, supports in-factory testing or system boot-up sounds during system power-up. An externally configurable address pin allows up to five unique SoundWire addresses for each device part number. The MAX98363A/B operate with DVDDIO supplied with internal LDO and can support up to 10 MAX98363 SoundWire peripheral devices on one data lane. The MAX98363C/D operate with externally supplied DVDDIO and support up to 10 MAX98363 SoundWire peripheral devices on one data lane.

Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution.

The device is specified over the -40°C to +85°C temperature range.

Applications

- Notebook Computers
- Tablets
- IoT Devices
- Gaming Devices (Audio and Haptics)
- Smart Speakers
- Smartphones
- Single Li-ion Cell/5V Devices

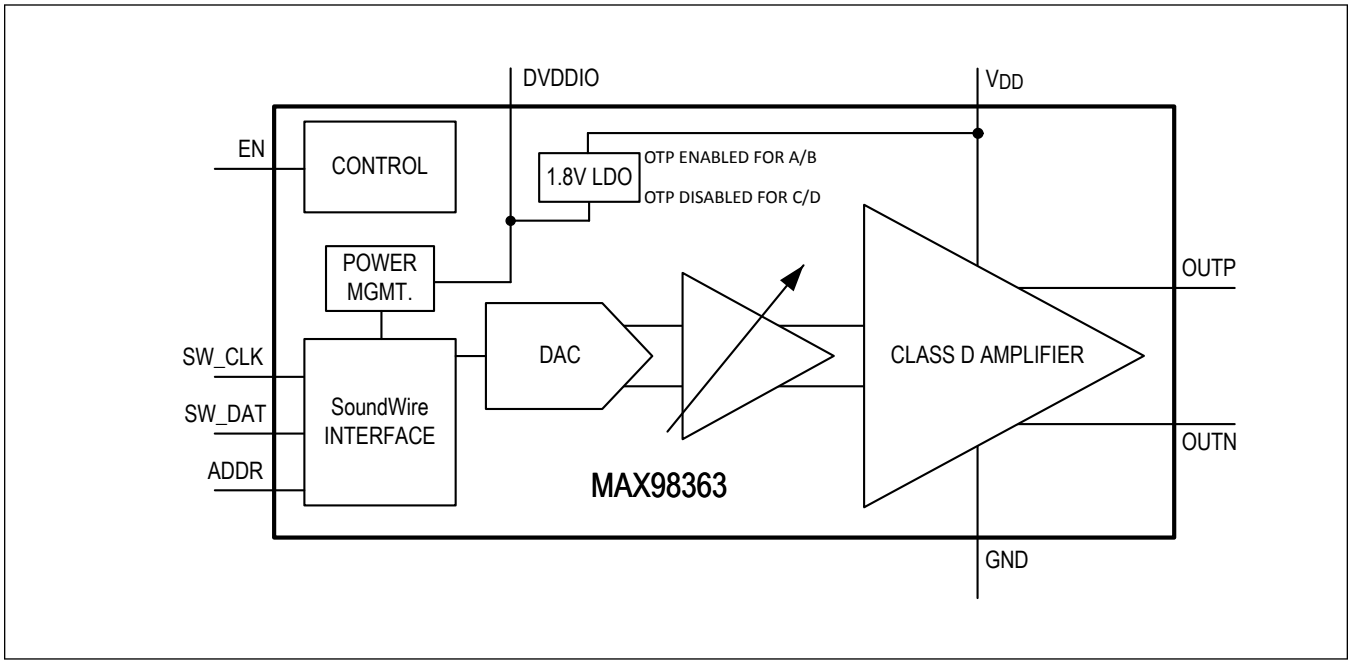
Benefits and Features

- Single-Supply Operation (2.5V to 5.5V) for the MAX98363A/B
- 3.2W Output Power into 4Ω at 5V, THD+N = 10%
- 12.3mW Quiescent Power with External DVDDIO
- MIPI SoundWire v1.2 Compliant
- Programmable Slew-Rate on SoundWire Data Output to Help Minimize EMI
- 92% Efficiency (R_L = 8Ω, THD+N = 10%)
- 12.8μV_{RMS} Output Noise
- 108.5dB Dynamic Range
- Low 0.014% THD+N at 1kHz
- Sophisticated Edge-Rate Control Enables Filterless Class D Outputs
- 82dB PSRR at 217Hz
- Low RF Susceptibility Rejects TDMA Noise from GSM Radios
- Class D Switching Frequency Trimmed to 5% for Better EMI Planning
- Extensive Click-and-Pop Reduction Circuitry
- Robust Short-Circuit and Thermal Protection
- Internal Tone Generator for In-Factory Testing
- Available in Space-Saving Package: 9-Bump WLP (1.528mm x 1.528mm, 0.4mm Pitch)

***Ordering Information** appears at end of data sheet.*

19-101593; Rev 0; 12/22

Simplified Block Diagram



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Absolute Maximum Ratings

V_{DD} to GND ..... -0.3V to +6V
DVDDIO to GND ..... -0.3V to 2.2V
SW_DAT, SW_CLK to GND .....-0.3V to V_{DVDDIO} + 0.3V
OUTP, OUTN, EN, ADDR to GND ..... -0.3V to V_{DD} + 0.3V
Duration of OUTP or OUTN Short Circuit to GND or V_{DD} ..... Continuous
Duration of OUTP Short to OUTN .....Continuous
Continuous Power Dissipation (T_A = +70°C) WLP (derate 13.7mW/°C above +70°C) 1096mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

9 WLP

Package Code	W91S1+1
Outline Number	*21-100615A*
Land Pattern Number	Refer to *Application Note 1891*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	49°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, f_S = 48kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
DVDDIO Power-Supply Voltage Range	V_{DVDDIO}	MAX98363C/D, guaranteed by PSRR test	1.7		1.9	V
V_{DD} Undervoltage Lockout	V_{DD_UVLO}		1.7	2.2	2.4	V
V_{DD} Power-Supply Voltage Range	V_{DD}	Guaranteed by PSRR test	2.5		5.5	V
DVDDIO Output Voltage	V_{DVDDIO_LDO}	MAX98363A/B, V_{DD} = 2.5V to 5.5V	1.76		1.87	V
POWER CONSUMPTION						
Total Quiescent Power Consumption	P_Q	T_A = +25°C, V_{DD} = 3.7V, V_{DVDDIO} = 1.8V, MAX98363C/D		9.3	11	mW
		T_A = +25°C, MAX98363C/D		12.3	14	
		T_A = +25°C, MAX98363A/B		18.4	21	
		T_A = +25°C, V_{DD} = 3.7V, MAX98363A/B		13	15	
V_{DD} Quiescent Current	I_{Q_VDD}	T_A = +25°C, MAX98363C/D		1.8	2	mA

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, f_S = 48kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DVDDIO Quiescent Current	I_{Q_DVDDIO}	T_A = +25°C, MAX98363C/D		1.9	2.2	mA
V_{DD} Software Shutdown Supply Current	$I_{VDD\_SHDN\_SW}$	EN = 1.8V, T_A = +25°C, SW_CLK toggling, MAX98363C/D		15	21	µA
DVDDIO Software Shutdown Current	$I_{DVDDIO\_SHDN\_SW}$	EN = 1.8V, DVDDIO = 1.8V, T_A = +25°C, SW_CLK toggling, MAX98363C/D		315	375	µA
V_{DD} Software Shutdown Supply Current	$I_{VDD\_SHDN\_SW}$	EN = 1.8V, T_A = +25°C, all SW pins at 0V, MAX98363A/B		220	260	µA
V_{DD} Hardware Shutdown Current	$I_{VDD\_SHDN\_HW}$	EN = 0V, T_A = +25°C		0.4	1	µA
DVDDIO Hardware Shutdown Current	$I_{DVDDIO\_SHDN\_HW}$	EN = 0V, T_A = +25°C, MAX98363C/D		0.014	1	µA
THERMAL PROTECTION						
Thermal Shutdown Temperature				150		°C
Thermal Shutdown Recovery Hysteresis				18		°C
TURN-ON/OFF TIME						
Turn-On Time	t_{ON}	Time from software shutdown to full-gain audio out, volume ramping disabled, f_S = 48kHz		1.5	1.7	ms
		Time from software shutdown to full-gain audio out, volume ramping enabled		5	6.2	
Turn-Off Time	t_{OFF}	Time from full-gain audio out to mute		0.1		ms
CLASS D AMPLIFIER						
Output Offset Voltage	V_{OS}	T_A = +25°C	-1	±0.1	+1	mV
Click-and-Pop Level	K_{CP}	Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, into software shutdown		-82		dBV
		Peak voltage, A-weighted, 32 samples per second, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, out of software shutdown		-71		

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, f_S = 48kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞, DC, V_{DD} = 2.5V to 5.5V	66	83		dB
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 217Hz, 200mV_{PP} ripple		82		
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 1kHz, 200mV_{PP} ripple		82		
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 10kHz, 200mV_{PP} ripple		65		
DVDDIO Power-Supply Rejection Ratio	PSRR	T_A = +25°C, digital silence used for input signal, Z_{SPK} = ∞, DC, V_{DVDDIO} = 1.7V to 1.9V, MAX98363C/D	95	100		dB
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 217Hz, 100mV_{PP} ripple, MAX98363C/D		100		
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 1kHz, 100mV_{PP} ripple, MAX98363C/D		100		
		T_A = +25°C, digital silence used for input signal, Z_{SPK} = 8Ω + 33µH or 4Ω + 33µH, f = 10kHz, 100mV_{PP} ripple, MAX98363C/D		99		
Output Power	P_{OUT}	THD+N ≤ 10%, Z_{SPK} = 4Ω + 33µH		3.2		W
		THD+N ≤ 10%, Z_{SPK} = 8Ω + 33µH		1.8		
		THD+N ≤ 10%, Z_{SPK} = 8Ω + 33µH, V_{DD} = 3.7V		0.93		
		THD+N ≤ 1%, Z_{SPK} = 4Ω + 33µH		2.5		
		THD+N ≤ 1%, Z_{SPK} = 8Ω + 33µH		1.4		
		THD+N ≤ 1%, Z_{SPK} = 8Ω + 33µH, V_{DD} = 3.7V		0.77		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 1W, T_A = +25°C, Z_{SPK} = 4Ω + 33µH		0.024		%
		f = 1kHz, P_{OUT} = 0.7W, T_A = +25°C, Z_{SPK} = 8Ω + 33µH		0.014	0.028	
Dynamic Range	DR	A-weighted, Z_{SPK} = 8Ω + 33µH, -60dB 1kHz output signal, normalized to full-scale (THD+N = 1%), 24- or 32-bit data		108.5		dB
Output Noise	e_{Nd}	A-weighted, 24-bit or 32-bit data		12.8		$µV_{RMS}$

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, f_S = 48kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain (Relative to a 0.49dBV Reference Level)	A_V	SPK_GAIN = 0x5 (+12dB)	11.4	12	12.6	dB
		SPK_GAIN = 0x4 (+9dB)	8.4	9	9.6	
		SPK_GAIN = 0x3 (+6dB)	5.4	6	6.6	
		SPK_GAIN = 0x2 (+3dB)	2.4	3	3.6	
		SPK_GAIN = 0x0 (-3dB)	-3.6	-3	-2.4	
Output Current Limit	I_{LIM}		2.15	2.6		A
Output Current Limit Autorestart Time				20		ms
Efficiency	η	Z_{SPK} = 8Ω + 33µH, THD+N = 10%, f = 1kHz		92		%
Frequency Response			-0.2		+0.3	dB
Class D Switching Frequency	f_{SW}		285	300	315	kHz
Spread-Spectrum Bandwidth	f_{SSM}	V_{DD} = 2.5V to 5.5V		±4		kHz
Output Stage On-Resistance	R_{ON}	PMOS + NMOS (Full H-Bridge), T_A = +25°C		345		mΩ
Maximum Device-to-Device Phase Error		Output phase shift between multiple devices from 20Hz to 20kHz across all sample rates		1.5		deg
Minimum Load Resistance	R_L			3.2		Ω
DAC DIGITAL FILTER (f_S < 50kHz)						
Passband	f_{PLP}	Ripple < δ_P	0.452 x f_S			Hz
		Droop < 3dB	0.457 x f_S			
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.1		+0.1	dB
Stopband	f_{SLP}	Attenuation > δ_S			0.49 x f_S	Hz
Stopband Attenuation	δ_S	f > f_{SLP}	75			dB
Group Delay		f = f_{PLP}		9.5		samples
DAC DIGITAL FILTERS/AUDIO MODE FOR LOWPASS FILTER (f_S > 50kHz)						
Passband	f_{PLP}	Ripple < δ_P, 88.2kHz ≤ f_S ≤ 96kHz	0.227 x f_S			Hz
		Droop < 3dB, 88.2kHz ≤ f_S ≤ 96kHz	0.314 x f_S			
	f_{PLP}	Ripple < δ_P, 176.4kHz ≤ f_S ≤ 192kHz	0.1135 x f_S			
		Droop < -3dB cutoff, 176.4kHz ≤ f_S ≤ 192kHz	0.232 x f_S			

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, f_S = 48kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Passband Ripple	δ_P	f < f_{PLP}, referenced to signal level at 1kHz	-0.25		+0.25	dB
Stopband	f_{SLP}	Attenuation > δ_S			0.495 x f_S	Hz
Stopband Attenuation	δ_S	f < f_{SLP}	75			dB
DAC DIGITAL FILTERS/DIGITAL DC BLOCKING FILTER						
DC Attenuation			80			dB
DC Blocking Filter -3dB Cutoff Frequency	f_C	For f_s = 8kHz, 16kHz, 32kHz, 48kHz, 96kHz and 192kHz		1.872		Hz
		For f_s = 44.1kHz, 88.2kHz		1.72		
EN PIN SPECIFICATIONS						
Input High Voltage	V_{IH}	EN	1.0			V
Input Low Voltage	V_{IL}	EN			0.24	V
Input Hysteresis	V_{HYS}	EN		34		mV
EN Leakage Current	I_{EN_LKG}		-1		+1	µA
ADDR PIN COMPARATOR TRIP POINTS						
Connect to GND	V_ADDR_TRIP2	Unique ID = 0x0 (MAX98363A/C), 0x5 (MAX98363B/D)	0		0.1 x VDD	V
Float	V_ADDR_TRIP1	Unique ID = 0x1 (MAX98363A/B), 0x6 (MAX98363C/D)	0.4 x VDD		0.6 x VDD	V
Connected to V_{DD}	V_ADDR_TRIP3	Unique ID = 0x2 (MAX98363A/B), 0x7 (MAX98363C/D)	0.9 x VDD		VDD	V
100kΩ to V_{DD}	V_ADDR_TRIP4	Unique ID = 0x3 (MAX98363A/B), 0x8 (MAX98363C/D)	0.65 x VDD		0.85 x VDD	V
100kΩ to GND	V_ADDR_TRIP5	Unique ID = 0x4 (MAX98363A/B), 0x9 (MAX98363C/D)	0.15 x VDD		0.35 x VDD	V
Input Leakage Current	IIH, IIL	V_{ADDR} = 0V, V_{DD} = 5.5V, T_A = +25C	-1		+1	µA
DIGITAL I/O CHARACTERISTICS / SoundWire INTERFACE (SW_CLK, SW_DAT)						
Clock Input Threshold for Rising (Positive) Edges	V_TP_Clock_1V8		0.5 x V_{DVDDIO}		0.65 x V_{DVDDIO}	V
Clock Input Threshold for Falling (Negative) Edges	V_TN_Clock_1V8		0.35 x V_{DVDDIO}		0.5 x V_{DVDDIO}	V
Clock Threshold Hysteresis	V_Hys_Clock_1V8	(Note 2)	0.10 x V_{DVDDIO}			V
Data Input—Voltage High	V_IHmin_Data_1V8		0.65 x V_{DVDDIO}			V
Data Input—Voltage Low	V_ILmax_Data_1V8				0.35 x V_{DVDDIO}	V

Electrical Characteristics (continued)

(V_{DD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, f_S = 48kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input—Hysteresis	V_Hys_Data_1V8	(Note 2)	0.10 x V_{DVDDIO}			V
Input Leakage Current			-3		+3	µA
Maximum Input Capacitance	C_{IN}			5		pF
Data Output—Voltage High	V_OH_Data_1V8		0.65 x V_{DVDDIO}			V
Data Output—Voltage Low	V_OL_Data_1V8				0.35 x V_{DVDDIO}	V
DIGITAL I/O CHARACTERISTICS / SoundWire INTERFACE TIMING CHARACTERISTICS						
SoundWire Clock Frequency	f_Clock				12.7	MHz
SoundWire Clock Input Duty Cycle	DC_In_Clock		45		55	%
Data Output Slew Time	t_Slew_Data_1V8	SlewTime_Ctrl = 0x00 & 0x01, t_R = 0.2 x V_{DVDDIO} to 0.8 x V_{DVDDIO}		3.3		ns
		SlewTime_Ctrl = 0x2, t_R = 0.2 x V_{DVDDIO} to 0.8 x V_{DVDDIO}		5.6		
		SlewTime_Ctrl = 0x3, t_R = 0.2 x V_{DVDDIO} to 0.8 x V_{DVDDIO}		10.3		
Minimum Data Input Setup Time	t_ISetup_min_Data_1V8				0	ns
Minimum Data Input Hold Time	t_IHold_min_Data_1V8				4	ns
Data Output Disable Time	t_DZ_Data_1V8				4	ns
Data Output Enable Time	t_ZD_Data		7.9			ns
Minimum Time for Data Output to Remain Stable	t_OH_Data		6.7			ns
Clock Edge to Valid Data Output	t_OV_Data	10pF ≤ C_{BUS_DATA} ≤ 60pF			27.6	ns
Clock Edge to Valid Data Output	t_OV_Data	10pF ≤ C_{BUS_DATA} ≤ 100pF			31.6	ns

Note 1: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 2: Minimum and/or maximum limit is guaranteed by design and by statistical analysis of device characterization data. The specification is not guaranteed by production testing.

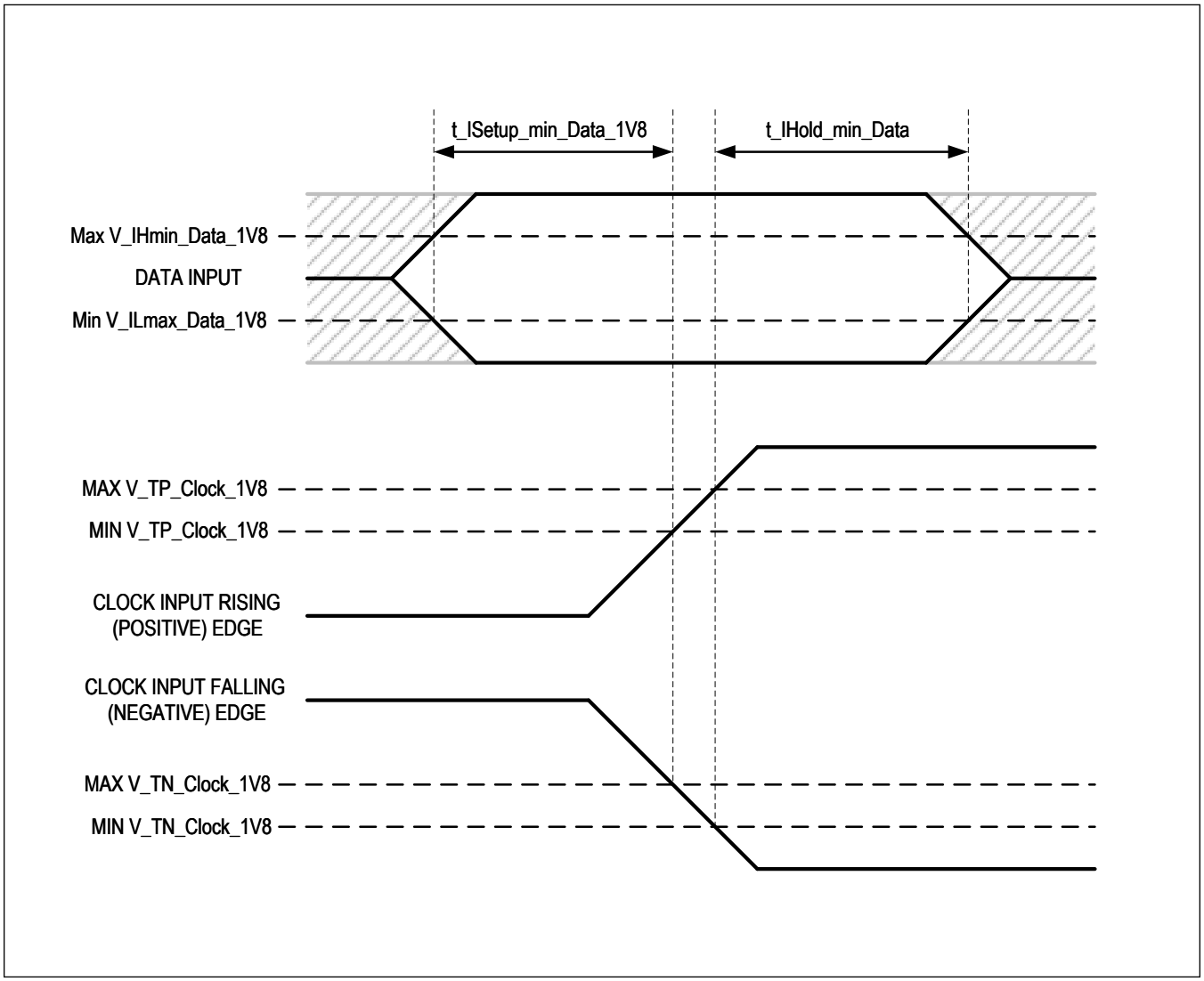


Figure 1. SoundWire Input Timing Diagram

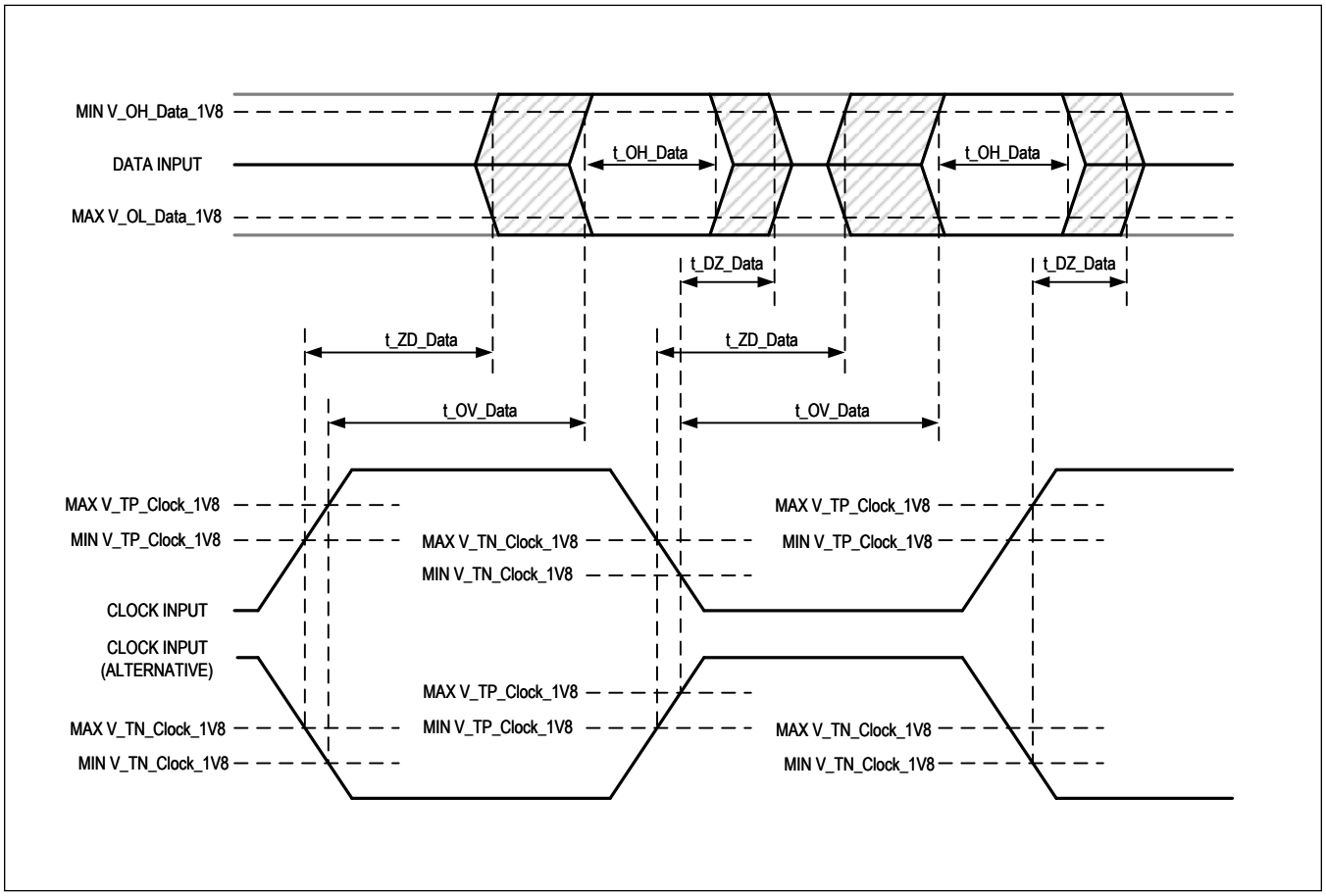
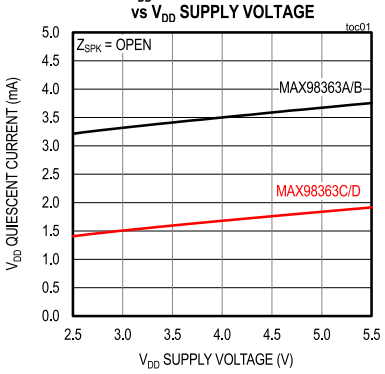


Figure 2. SoundWire Output Timing Diagram

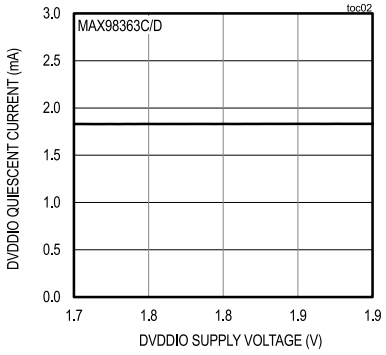
Typical Operating Characteristics

(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

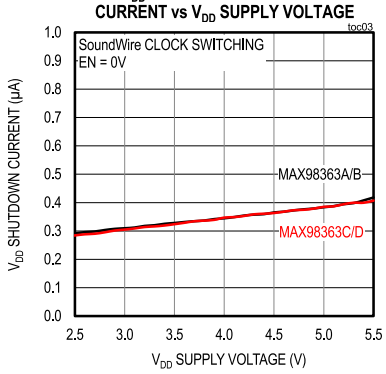
V_{DD} QUIESCENT CURRENT vs V_{DD} SUPPLY VOLTAGE



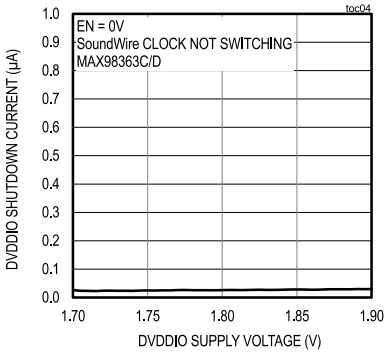
DVDDIO QUIESCENT CURRENT vs DVDDIO SUPPLY VOLTAGE



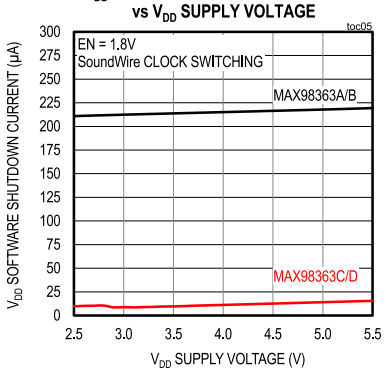
V_{DD} HARDWARE SHUTDOWN CURRENT vs V_{DD} SUPPLY VOLTAGE



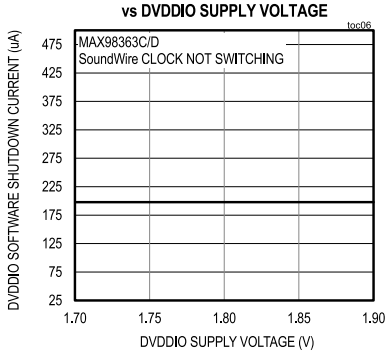
DVDDIO HARDWARE SHUTDOWN CURRENT vs DVDDIO SUPPLY VOLTAGE



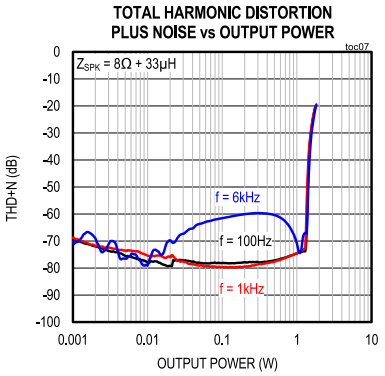
V_{DD} SOFTWARE SHUTDOWN CURRENT vs V_{DD} SUPPLY VOLTAGE



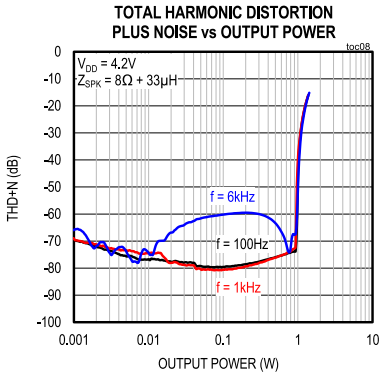
DVDDIO SOFTWARE SHUTDOWN CURRENT vs DVDDIO SUPPLY VOLTAGE



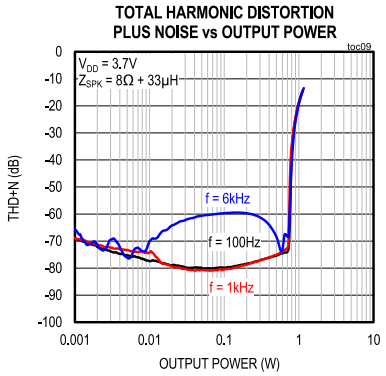
TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER



TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER



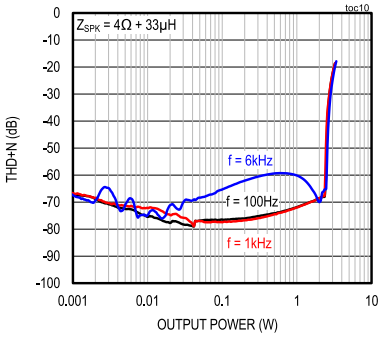
TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER



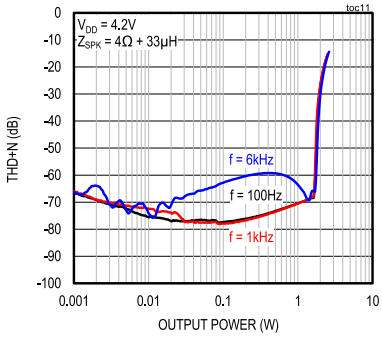
Typical Operating Characteristics (continued)

(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

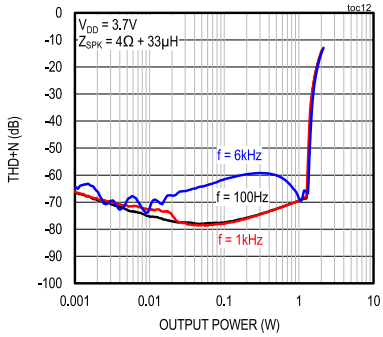
TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER



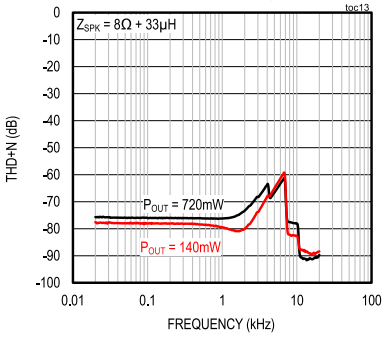
TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER



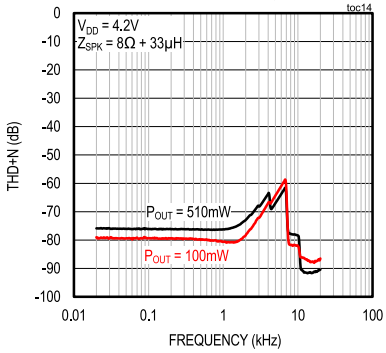
TOTAL HARMONIC DISTORTION PLUS NOISE vs OUTPUT POWER



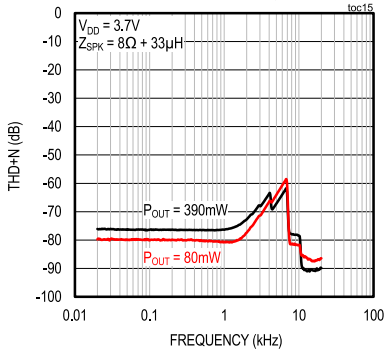
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



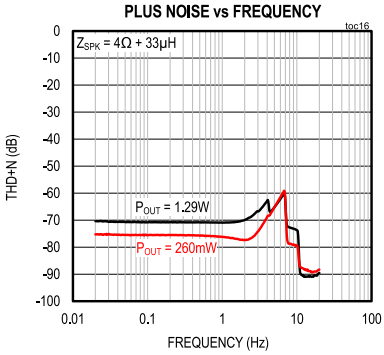
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



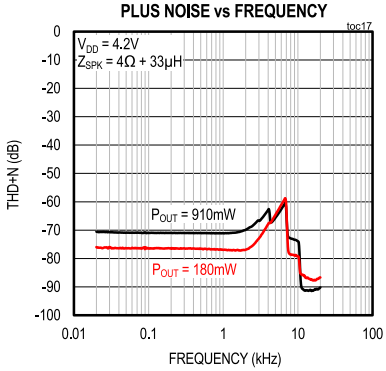
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



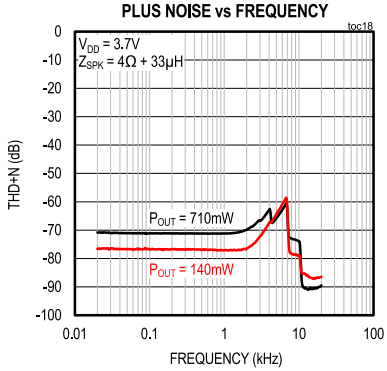
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY



TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

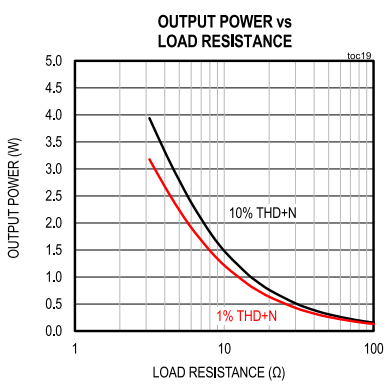


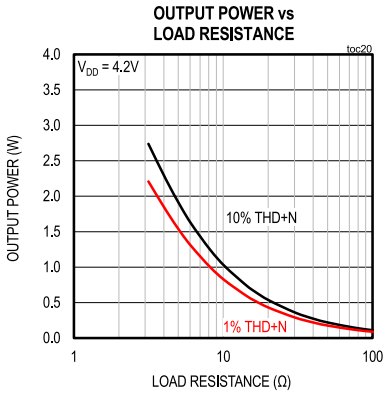
TOTAL HARMONIC DISTORTION PLUS NOISE vs FREQUENCY

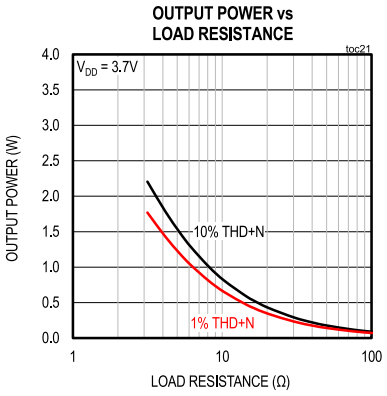


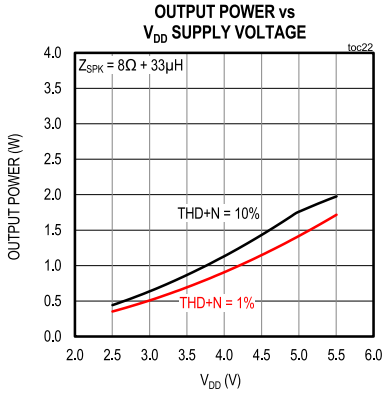
Typical Operating Characteristics (continued)

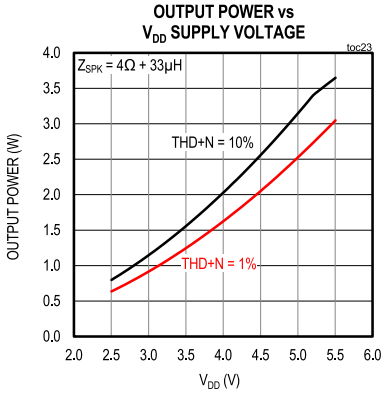
(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

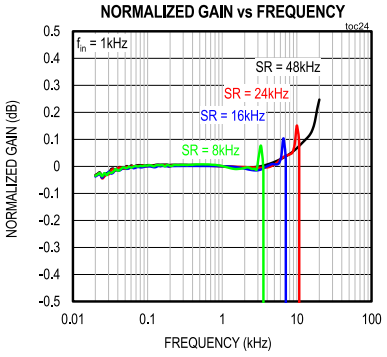


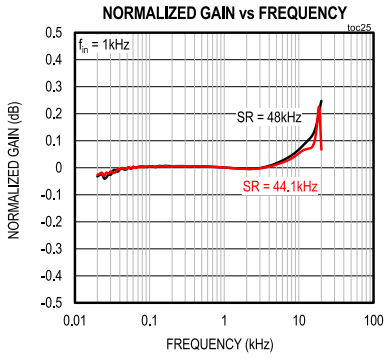


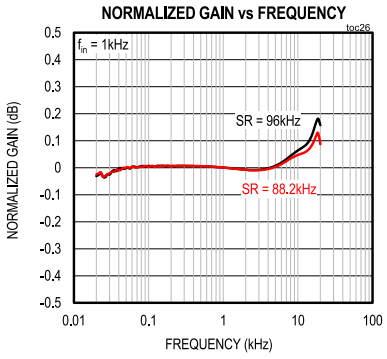


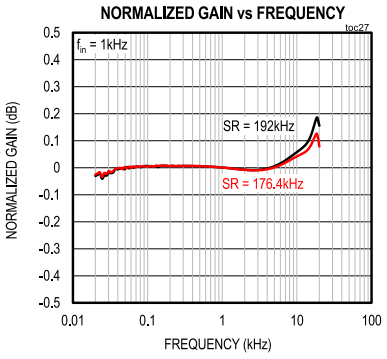






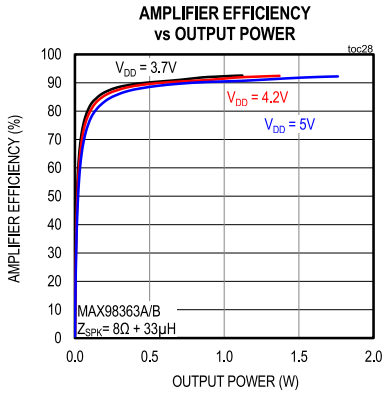


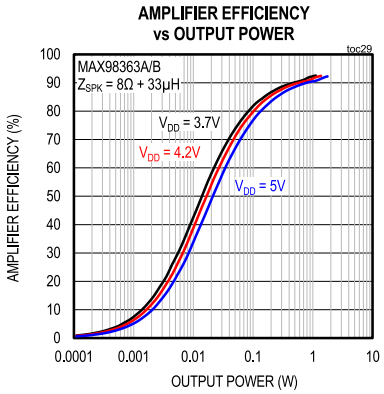


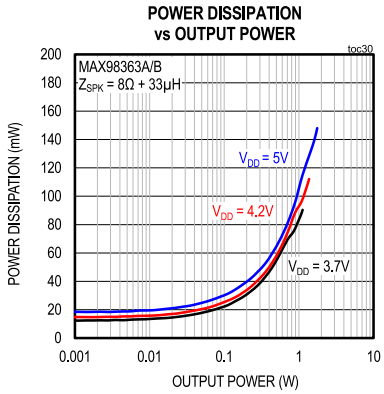


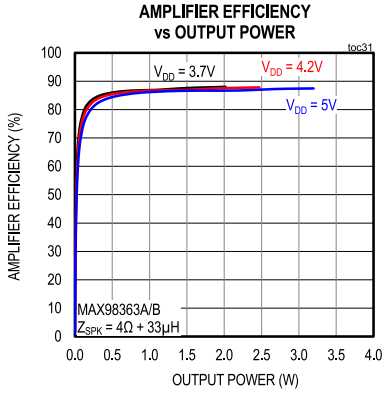
Typical Operating Characteristics (continued)

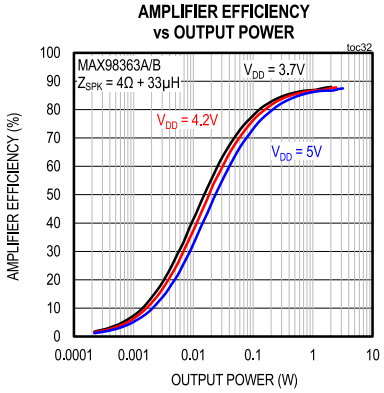
(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

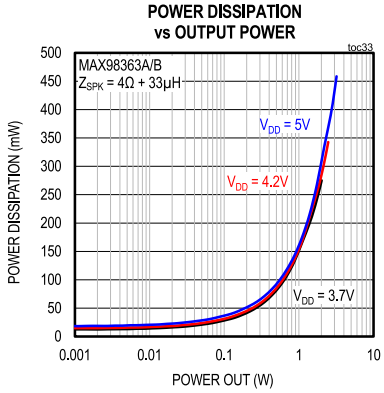


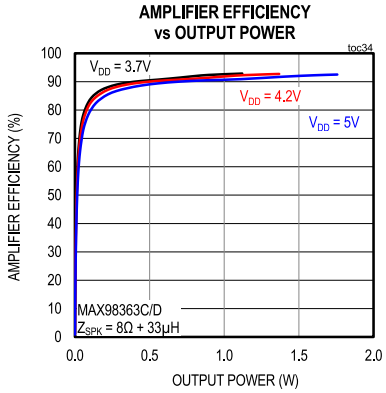


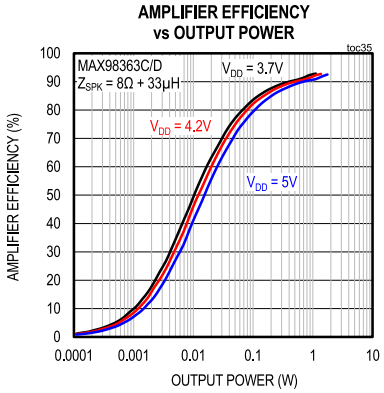


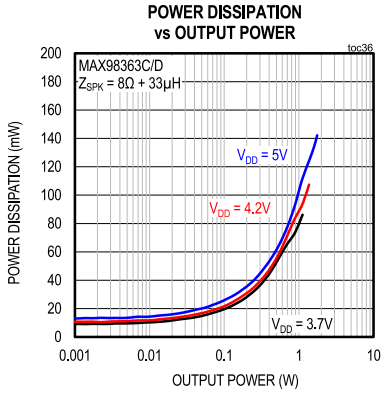








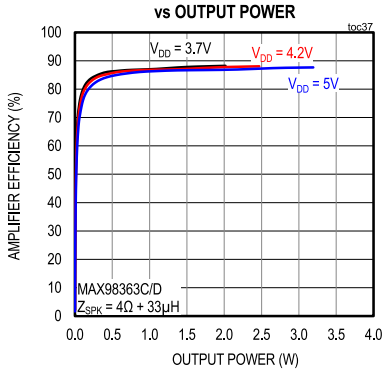




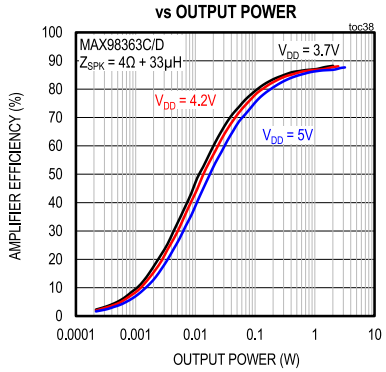
Typical Operating Characteristics (continued)

(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

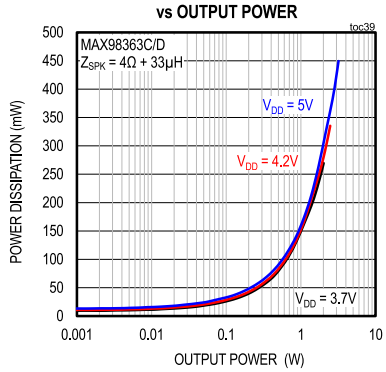
AMPLIFIER EFFICIENCY vs OUTPUT POWER



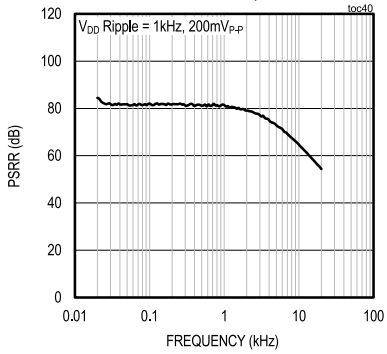
AMPLIFIER EFFICIENCY vs OUTPUT POWER



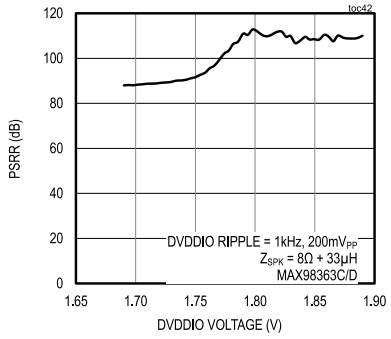
POWER DISSIPATION vs OUTPUT POWER



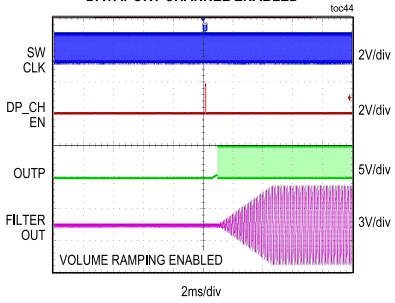
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



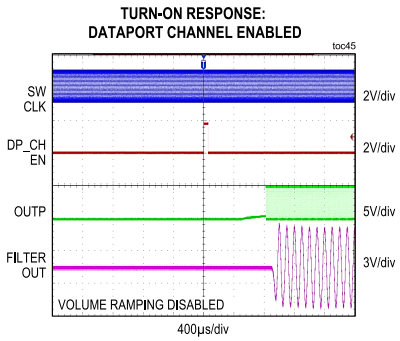
POWER SUPPLY REJECTION RATIO vs. DVDDIO VOLTAGE



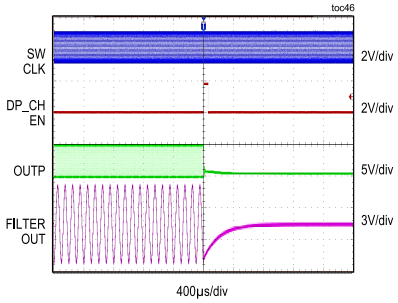
TURN-ON RESPONSE: DATAPORT CHANNEL ENABLED



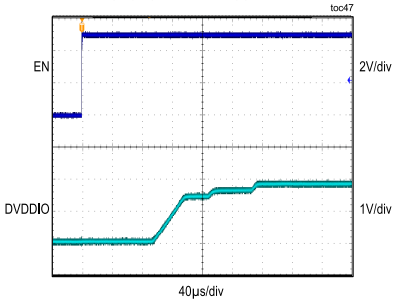
TURN-ON RESPONSE: DATAPORT CHANNEL ENABLED



TURN-OFF RESPONSE: DATAPORT CHANNEL DISABLED



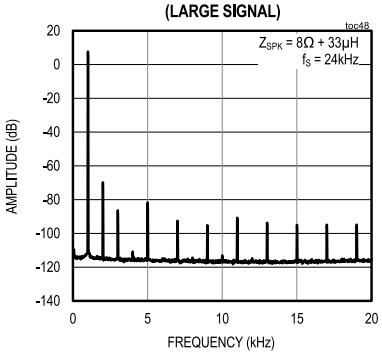
MAX98363A/B DVDDIO TURN ON RESPONSE: EN PIN ASSERTED



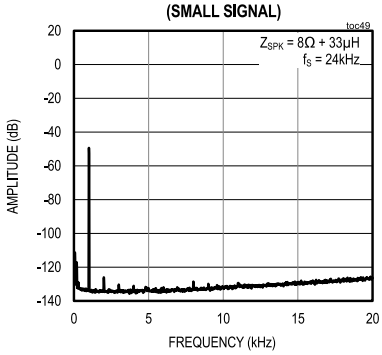
Typical Operating Characteristics (continued)

(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

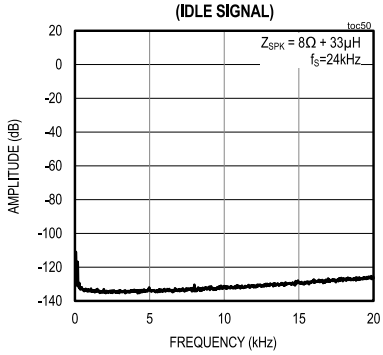
INBAND OUTPUT SPECTRUM (LARGE SIGNAL)



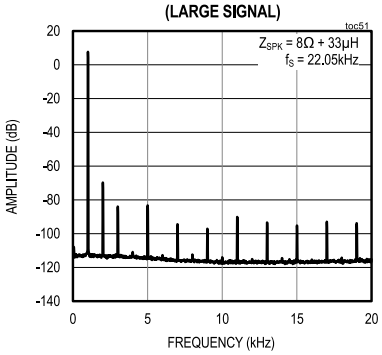
INBAND OUTPUT SPECTRUM (SMALL SIGNAL)



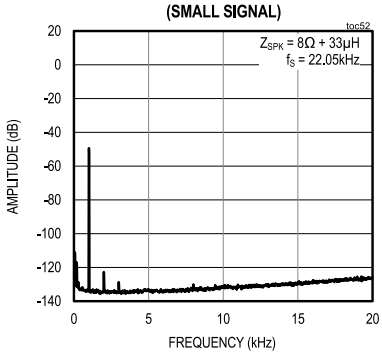
INBAND OUTPUT SPECTRUM (IDLE SIGNAL)



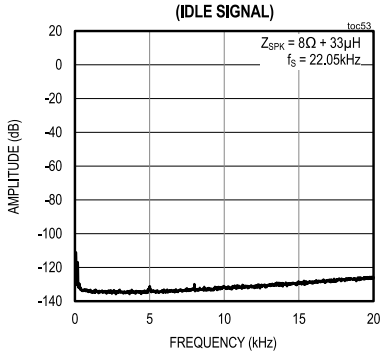
INBAND OUTPUT SPECTRUM (LARGE SIGNAL)



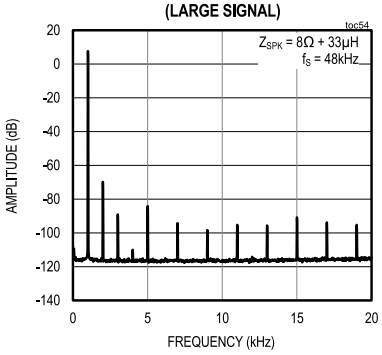
INBAND OUTPUT SPECTRUM (SMALL SIGNAL)



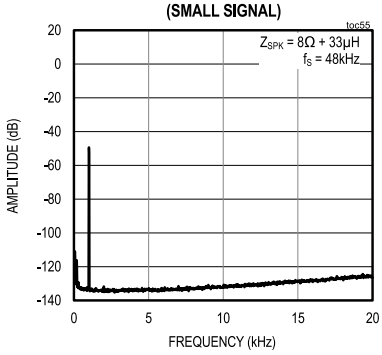
INBAND OUTPUT SPECTRUM (IDLE SIGNAL)



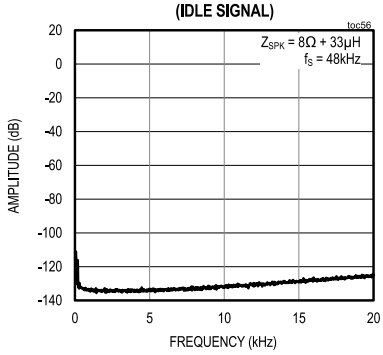
INBAND OUTPUT SPECTRUM (LARGE SIGNAL)



INBAND OUTPUT SPECTRUM (SMALL SIGNAL)



INBAND OUTPUT SPECTRUM (IDLE SIGNAL)



Typical Operating Characteristics (continued)

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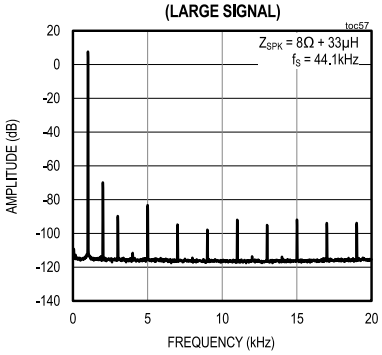
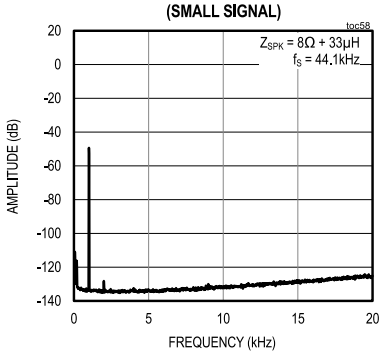
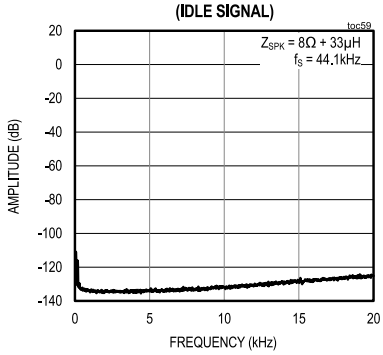
INBAND OUTPUT SPECTRUM (LARGE SIGNAL)



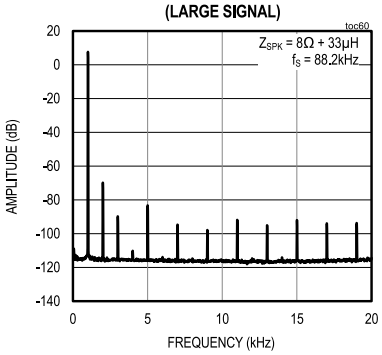
INBAND OUTPUT SPECTRUM (SMALL SIGNAL)



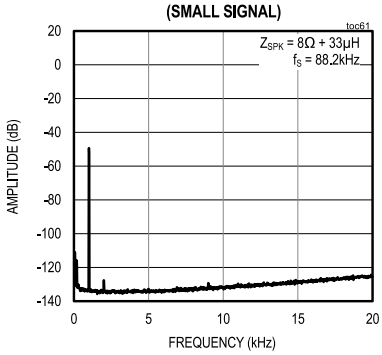
INBAND OUTPUT SPECTRUM (IDLE SIGNAL)



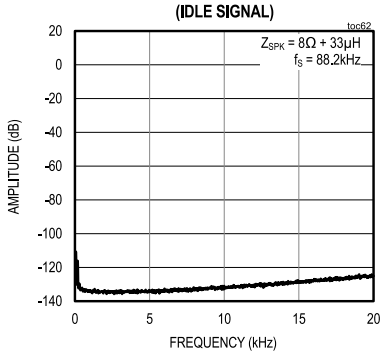
INBAND OUTPUT SPECTRUM (LARGE SIGNAL)



INBAND OUTPUT SPECTRUM (SMALL SIGNAL)



INBAND OUTPUT SPECTRUM (IDLE SIGNAL)



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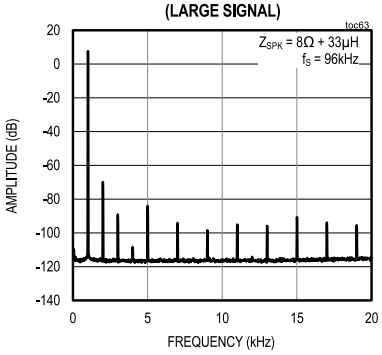

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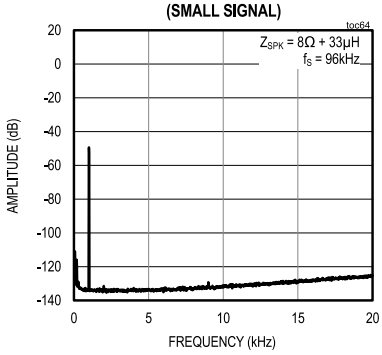

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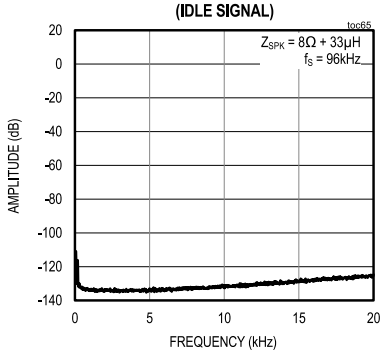
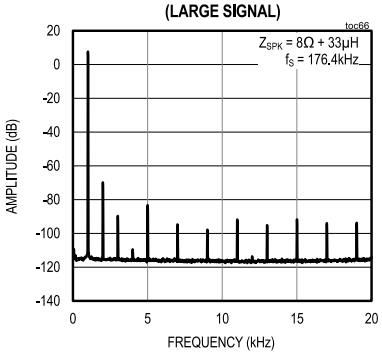


Typical Operating Characteristics (continued)

(V_{VDD} = 5V, V_{DVDDIO} = 1.8V (MAX98363C/D), V_{GND} = 0V, Z_{SPK} = ∞ between OUTP and OUTN, SPK_GAIN = +12dB, AC measurement bandwidth = 20Hz to 20kHz, T_A = T_{MIN} to T_{MAX}, f_S = 48kHz, 24-bit data. Typical values are at T_A = +25ºC)

INBAND OUTPUT SPECTRUM (LARGE SIGNAL)



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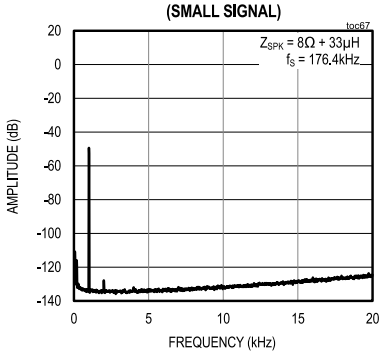

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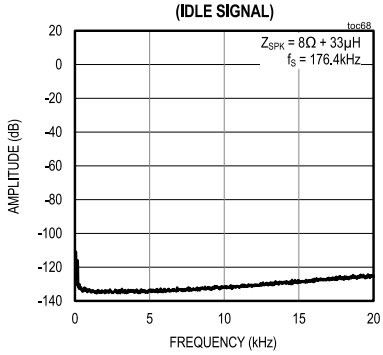

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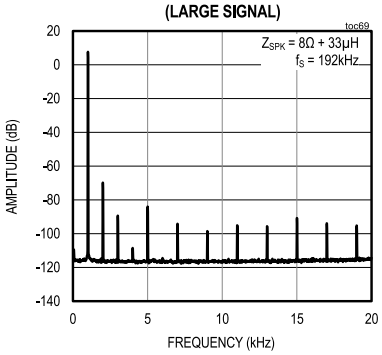

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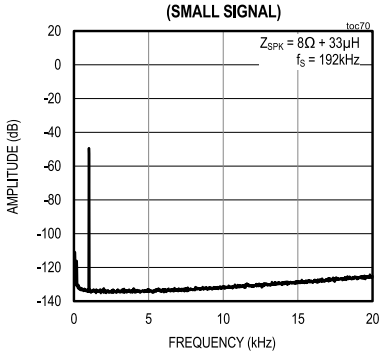

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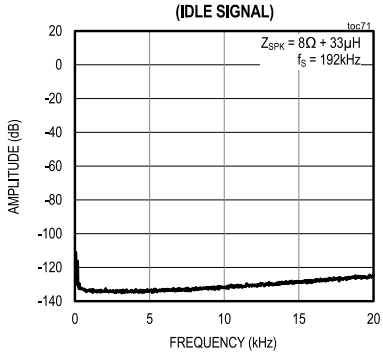

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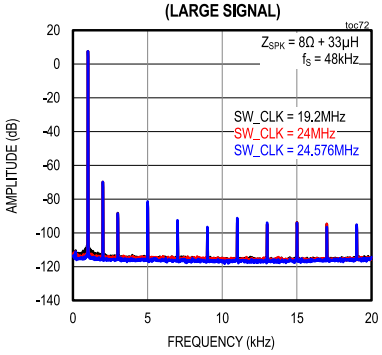
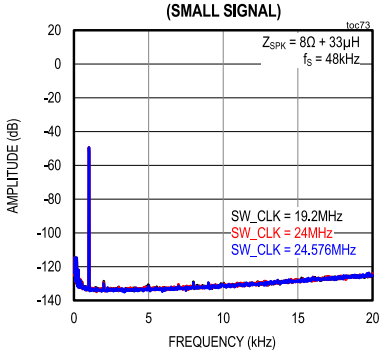


INBAND OUTPUT SPECTRUM (SMALL SIGNAL)



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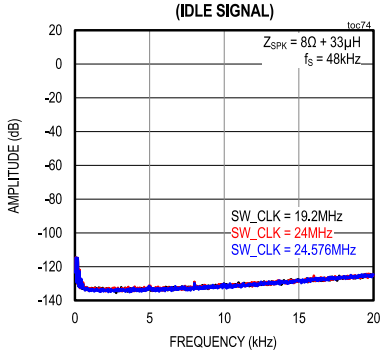

Typical Operating Characteristics (continued)

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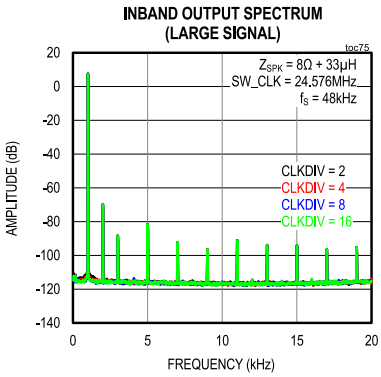
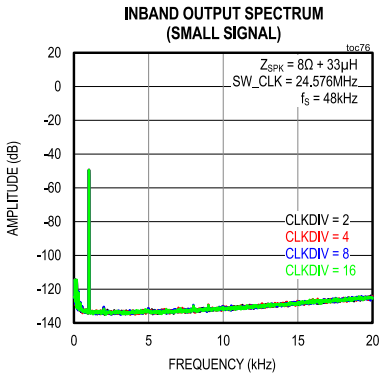
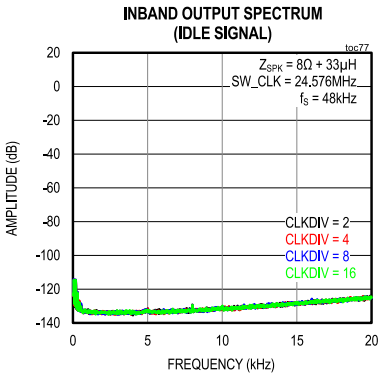
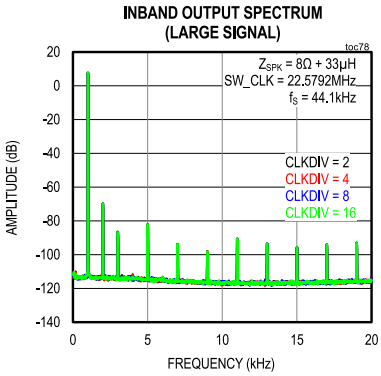
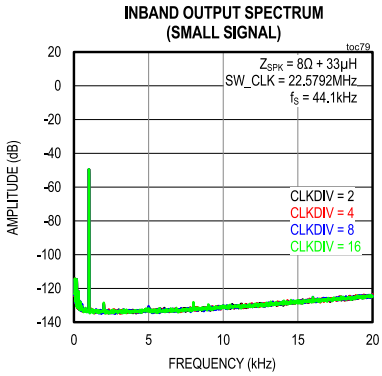
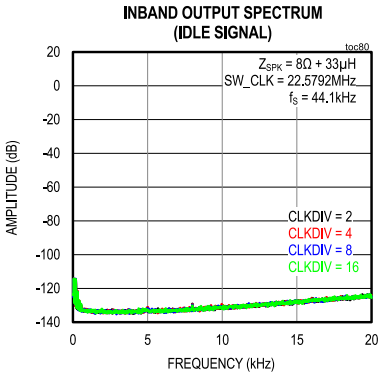






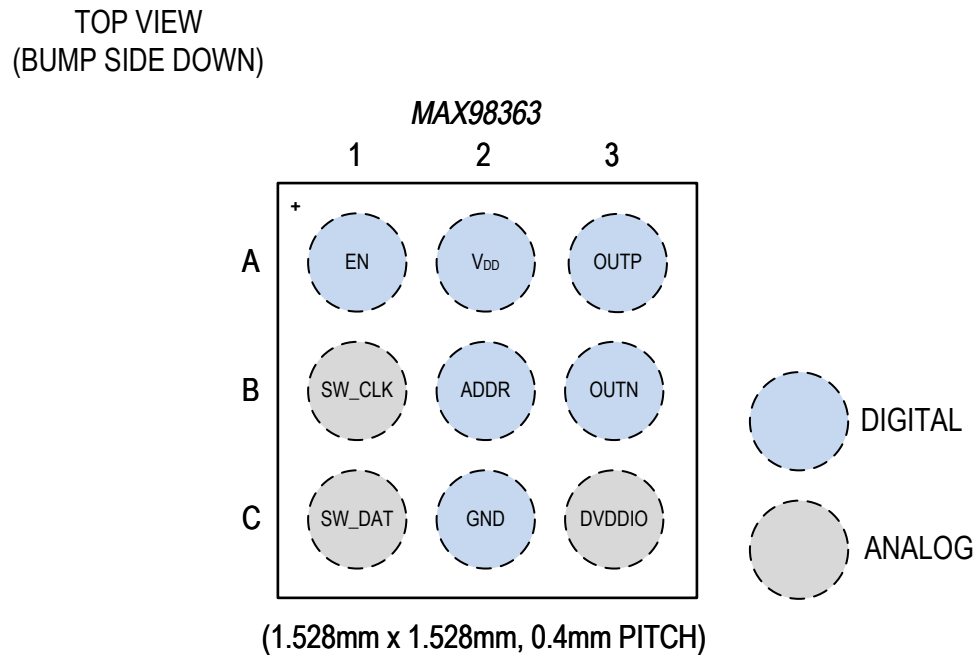






Pin Configuration

9 WLP



Pin Description

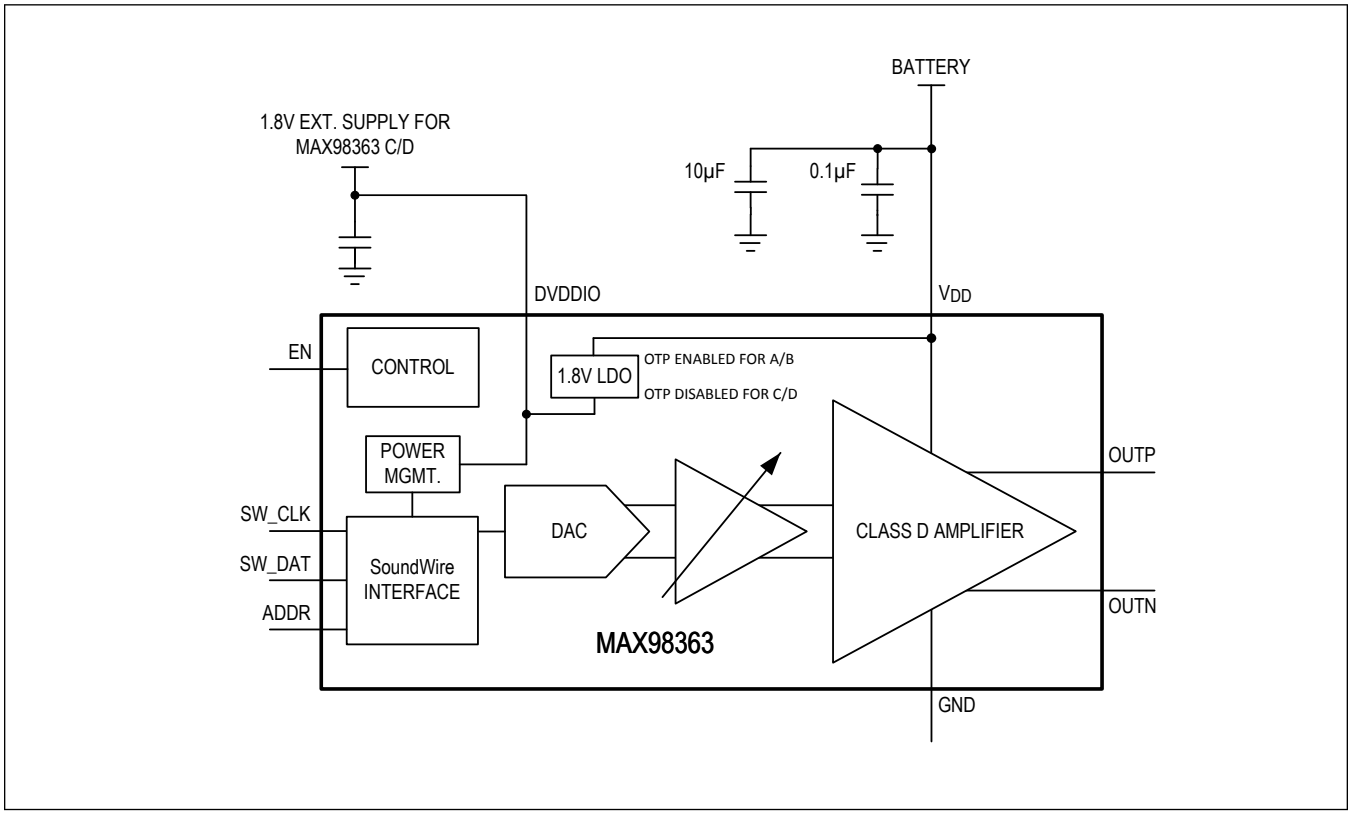
PIN	NAME	FUNCTION	REF SUPPLY	TYPE
A2	V_{DD}	Amplifier Power Supply Input. Bypass to GND with a 0.1µF and 10µF capacitor placed as close as possible.	—	Supply
C3	DVDDIO	MAX98363A/B: Internally Regulated LDO Output for Digital Interface Power-Supply. Bypass to GND with 2.2µF capacitor placed as close to the pin as possible. MAX98363C/D: Digital Interface Power-Supply Input. Bypass to GND with 0.1µF capacitor placed as close to the pin as possible.	V_{DD}	Supply
A1	EN	Hardware Enable Pin. Pull EN low to place the device in shutdown mode. The EN pin should not be left floating with V_{DD} present.	V_{DD}	Digital Input
A3	OUTP	Positive Class D Amplifier Output	V_{DD}	Analog Output
B1	SW_CLK	SoundWire Clock Input Pin. Internally pulled down to GND through a 3MΩ resistor.	DVDDIO	Digital Input
B2	ADDR	SoundWire Device Address Selection Pin. Along with the EN pin, ADDR selects one of five SoundWire device addresses for each part number.	V_{DD}	Digital Input

Pin Description (continued)

PIN	NAME	FUNCTION	REF SUPPLY	TYPE
B3	OUTN	Negative Class D Amplifier Output	V_{DD}	Analog Output
C1	SW_DAT	SoundWire Data Input Pin. Internally pulled down to GND through a 3MΩ resistor.	DVDDIO	Digital Input
C2	GND	Ground	—	Supply

Functional Diagrams

Detailed Block Diagram



Detailed Description

The MAX98363A/B/C/D are MIPI SoundWire v1.2 compatible Class D power amplifiers. The SoundWire interface on the MAX98363 supports both audio and control data transport over the shared 2-wire bus comprising a clock input (SW_CLK) and a bidirectional data input/output (SW_DATA). For device configuration, the SoundWire manager can access both the general control and SoundWire peripheral interface registers. Each SoundWire peripheral device is identified by the controller on the bus by a unique ID set on the device. On the MAX98363A/C, the ADDR pin connections set the unique IDs 0x0 to 0x4 whereas on the MAX98363B/D, the ADDR pin connections set the unique IDs 0x5 to 0x9. Overall, up to 10 MAX98363 devices can be connected on a single SoundWire data lane. Table 1 shows the different MAX98363 versions and their differences.

Table 1. MAX98363 Versions

VERSION	V_{DVDDIO}	UNIQUE ID RANGE (SET BY ADDR PIN)
MAX98363A	Supplied by internal 1.8V LDO	0x0 to 0x4
MAX98363B	Supplied by internal 1.8V LDO	0x5 to 0x9
MAX98363C	Requires external 1.8V	0x0 to 0x4
MAX98363D	Requires external 1.8V	0x5 to 0x9

Device State Control

The device features a combination of both hardware and software controls that can be used to place the device into a reduced power state and/or to return the device to the initial power-on reset (PoR) state.

Hardware Shutdown State

When the device is first powered up or after a hardware reset event, the device always initializes into the hardware shutdown state. In hardware shutdown, the device is configured to its lowest power state. Upon entering hardware shutdown, the device is globally placed into a reset condition. As a result, the SoundWire control interface is disabled and all device registers are returned to their PoR states. When exiting hardware shutdown, the device initializes and then transitions into the software shutdown state.

When the hardware enable input (EN) is asserted low, the device enters hardware shutdown. The device is also placed into hardware shutdown anytime the V_{DD} supply drops below its UVLO threshold.

The device only exits hardware shutdown when the V_{DD} supply is above its UVLO threshold, and the hardware enable input (EN) is asserted high. Once all of these conditions are met, the device automatically exits hardware shutdown, and transitions into software shutdown.

Software Shutdown State

The device enters the software shutdown state after it transitions out of the hardware shutdown state or after exiting the active state. In the software shutdown state, all device registers (SoundWire and general control) can be programmed without restriction and all programmed register states are retained.

The Enable Channel 1 bit in DP1_Channel_En register is used to transition the device into and out of active state to software shutdown state. When the EN pin is set high, the device transitions from hardware shutdown state to software shutdown state.

When the device is in the active state and the Channel Enable bit field is set to 0, the device transitions to the software shutdown state. Additionally, anytime a bus reset is issued, the device enters the hardware shutdown state but if the EN pin is set high, the device automatically enters the software shutdown state.

While in the software shutdown state, it is recommended to set the EN pin low, before the V_{DD} supply (and DVDDIO power supply if supplied externally) can be powered down safely. Regardless of the state of the Enable Channel 1 bit, the device cannot transition from the software shutdown state to the active state until V_{DD} is above its UVLO threshold.

Active State

The device enters the active state from the software shutdown state when valid clocks are applied to the device and

the Channel_Enable bit field in DP1 Channel Enable is set. In the active state, all enabled device blocks are active and speaker outputs are asserted. In the active state, only SPK_VOL can be programmed safely.

The only non-fault state transitions to or from the active state are those initiated through the Enable_Channel bit field. All other transitions to or from the active state are the result of fault events, and may result in audible glitches if they occur during active playback.

SoundWire Bus Reset

A SoundWire bus reset command, which is a sequence of 4096 successive bit slots of encoded logic 1s on the SoundWire bus, resets all device registers (including the SoundWire peripheral configuration registers) to the default PoR values.

SoundWire Register Reset

The SoundWire register bit field, ForceReset, in the SCP_Ctrl register is used to reset the MAX98363 SoundWire peripheral configuration registers to the default PoR values. The ForceReset bit field is write only, and a read of this register always returns zero. Writing a logic-low to the ForceReset bit field has no effect.

UVLO Mode

When EN = 1 and V_{DD} supply is below the UVLO threshold the device is in UVLO mode. There is a slightly higher power draw in this mode compared to shutdown mode to supply some internal power-up detection circuits. When V_{DD} supply recovers and rises above its UVLO threshold, the device transitions into software shutdown state.

SoundWire Peripheral Interface

The SoundWire peripheral interface supports both audio and control data transport over the shared 2-wire bus comprising a clock input (SW_CLK) and a bidirectional data input/output (SW_DATA). For device configuration, the SoundWire manager can access both the general control and SoundWire peripheral interface registers. The SoundWire peripheral interface receives and routes all enabled device status interrupts to the SoundWire manager for servicing.

SoundWire Peripheral-Device Identification

The SoundWire peripheral interface provides a 48-bit value (Device_Id[47:0] in the SCP_DevId_0 to SCP_DevId_5 registers) that is read by the SoundWire manager to identify the connected SoundWire peripheral device. The SoundWire peripheral-device identification bit field contains multiple segments each detailed in Table 2. All segments are fixed except the peripheral-device unique ID. The 4-bit SoundWire peripheral-device unique ID is pin configurable and has five possible combinations for a given part number. A combination of part number and pin configurability allows up to 10 possible combinations of unique IDs. To select a device-unique ID, connect the ADDR pin as shown in Table 3.

Table 2. SoundWire Peripheral-Device Identification

REGISTER	BIT FIELD SEGMENT	DESCRIPTION	VALUE
SCP_DevId_0	Device_Id[47:44]	SoundWire version number	0x3
	Device_Id[43:40]	Peripheral-device unique ID decoded from pin	0x0 to 0x9
SCP_DevId_1 and SCP_DevId_2	Device_Id[39:24]	MIPI assigned manufacturer ID	0x019F
SCP_DevId_3 and SCP_DevId_4	Device_Id[23:8]	Audio part number	0x8363
SCP_DevId_5	Device_Id[7:0]	Class–MIPI reserved	0x00

Table 3. SoundWire Peripheral-Device Unique ID Configuration

PART NUMBER	ADDR PIN	DEVICE UNIQUE ID
MAX98363A/C	GND	0x0
MAX98363A/C	Unconnected	0x1
MAX98363A/C	V_{DD}	0x2
MAX98363A/C	100kΩ pull-up to V_{DD}	0x3
MAX98363A/C	100kΩ pull-up to GND	0x4

Table 3. SoundWire Peripheral-Device Unique ID Configuration (continued)

MAX98363B/D	GND	0x5
MAX98363B/D	Unconnected	0x6
MAX98363B/D	V_{DD}	0x7
MAX98363B/D	100kΩ pull-up to V_{DD}	0x8
MAX98363B/D	100kΩ pull-up to GND	0x9

Soundwire Clock Configuration

The SoundWire peripheral interface operates and supports device programming with any valid input SoundWire clock frequency (as specified in v1.2 of the SoundWire specification). The external SoundWire clock is also the source clock for internal clock generation. Therefore, for the device audio and data paths to operate, the external SoundWire clock frequency must match one of the 19 supported frequencies given in Table 4. These rates are an integer multiple (2/4/8/16) of one of the five supported base rates. The table of supported external clock rates as a function of base clock frequencies is shown in Table 4.

Table 4. Supported SW_CLK Clock Frequencies for Audio

CLOCK SCALE	CLOCK BASE FREQUENCY RATES (MHz)				
	19.2	22.5792	24	24.576	32
1	—	—	—	—	—
2	9.6	11.2896	12	12.288	—
4	4.8	5.6448	6	6.144	8
8	2.4	2.8224	3	3.072	4
16	1.2	1.4112	1.5	1.536	2

SoundWire Peripheral Control Port Configuration

The device SCP supports the options shown in Table 5. The SCP configuration bit fields are in the SoundWire peripheral interface registers from address 0x0040 to address 0x0080. For detailed register and bit field descriptions, refer to the full MIPI SoundWire v1.2 specification.

Table 5. SoundWire Peripheral Control Port (SCP) Options

PERIPHERAL CONTROL PORT OPTION	IMPLEMENTATION
Implementation Defined Interrupt 1	Yes
Clock Stop Mode 1	Yes
Clock Stop Prepare State Machine	Simplified
Clock Stop Async Wake Up	No
Address Paging	No
Multi-Lane	No
Bridging	No
High PHY	No
Test Mode	No
Broadcast Read Response	Command_Ignored

SoundWire Device Data Port (DP) Configuration

The SoundWire peripheral interface provides one data port. The speaker path supports all data flow modes (Isochronous, Tx-Controlled, Rx-Controlled, Full-Asynchronous). Data port test modes (Normal, PRBS, Static-0, and Static-1) are provided.

When operating as a passive peripheral device (device is attached to the SoundWire bus but all data ports are deactivated), the interface is optimized to minimize power consumption and only the logic cells that need to be active are

switching. The SoundWire manager should only enable and disable the peripheral device's interface data ports while the device is in software shutdown.

The provided data ports support a subset of options as shown in Table 7. The data-port control bit fields are located in the SoundWire peripheral interface registers from address 0x0100 to address 0x01FF. For detailed register and bit field descriptions, refer to the full MIPI SoundWire v1.2 specification.

Table 6. SoundWire Peripheral Interface Data-Port Assignment

NUMBER	DIRECTION	TYPE	CHANNELS	MAX WORD LENGTH	PURPOSE
Data Port 1	Rx (Input)	Full	1	32 bits	Data input for the speaker path

Table 7. Data Port 1 Options

DATA-PORT OPTIONS	IMPLEMENTATION
Implementation Defined Interrupt 1	No
Implementation Defined Interrupt 2	No
Implementation Defined Interrupt 3	No
Flow Mode Support	Yes
Extended Buffer Operating Modes for Flow Control	No
Block Group Support	No
Prepare State Machine	Simplified

SoundWire Clock Stop

The MAX98363 supports Simplified Peripheral Clock Stop Prepare as defined in the MIPI SoundWire v1.2 specification. The ClockStop_Prepare bit field in the SoundWire register map is set to 1. As a result, the device automatically detaches from the bus after a successful host-initiated clock stop event, provided DP_EN = 1 prior to the clock stop event. If the SoundWire manager sets DP_EN = 0 prior to the clock stop event, the device retains SoundWire register and device values.

To prevent audible glitches at the speaker output due to a clock-stop event, it is recommended that the SoundWire manager places the device into a software shutdown (DP_EN = 0) prior to initializing a clock-stop event.

Interrupts

The device supports individually enabled status interrupts for sending feedback to the host about events that have occurred on-chip. When SoundWire implementation defined interrupt reporting is enabled in the SoundWire control registers, any individual enabled device interrupt triggers a request to the host to process the interrupt.

Interrupt Bit-Field Composition

Each implementation defined interrupt source has five individual bit-field components in the device register map. The function of each component is detailed below and the corresponding bit fields for each source can be identified by the appended suffix (shown in parentheses).

Raw Status (RAW)

Each interrupt source has a read-only bit to indicate the real-time raw status of the interrupt source.

State (STATE)

Each interrupt source has a read-only state bit that is set whenever a rising edge occurs on the associated raw status bit. The state bit is set regardless of the setting of the source enable bit.

Flag (FLAG)

Each interrupt source has a read-only flag bit. If the source-enable bit is set, the flag bit is set, and an interrupt can be generated whenever the source state bit is set.

Enable (EN)

Each interrupt source has a dynamic read/write enable bit. When the enable bit is set, the associated flag bit is set and

an interrupt can be generated whenever the source state bit is set.

Clear (CLR)

Each interrupt source has a dynamic write-only clear bit. Writing a 1 to a clear bit resets the associated state and flag bits to 0. Writing a 0 to a clear bit has no effect.

Interrupt Output Configuration

All device interrupt flag bits are OR'd to generate a signal that sets the data-port interrupt status bit in the SoundWire device register map (SCP_IntStat_1). When SCP_IntStat_1 is set, the SoundWire controller on the device alerts the SoundWire manager by sending a PREQ command. The host in turn issues a PING command to identify the peripheral device sending the interrupt-process request and processes the interrupt on the device.

Interrupt Sources

Table 8. Interrupt Sources

INTERRUPT SOURCES	BIT FIELD	DESCRIPTION
Thermal Shutdown Event	*THERMSHDN_**	Indicates when the thermal-shutdown threshold temperature has been exceeded.
OTP Load Fail Event	*OTP_FAIL_**	Indicates when the OTP load routine that runs when exiting hardware shutdown has failed to complete successfully. If the OTP load routine fails, the device is held in software shutdown.
Speaker Over Current Event	*SPK_OVC_**	Indicates that the speaker amplifier current limit has been exceeded.
Internal CLK Error	*CLK_ERR_**	Indicates a clock-stop error in the internal clocks of the device.
Speaker Amplifier Monitor Error	*SPKMON_ERR_**	Indicates an amplifier output stuck high or low error.
Power-Up Done Event	*PWRUP_DONE_**	Indicates when the device has entered the active state and the device is ready to play audio.
Power-Down Done Event	*PWRDN_DONE_**	Indicates when the device has entered the software-shutdown state from a successful power-up state.

Note: The bit fields are shown without the component suffixes. For example, OTP_FAIL_* refers to OTP_FAIL_RAW, OTP_FAIL_STATE, OTP_FAIL_FLAG, OTP_FAIL_EN, and OTP_FAIL_CLR. All Interrupt sources have these five component bit fields.

Gain Selection

The MAX98363 provides a programmable gain selection to allow the speaker output signal amplitude to be scaled according to the maximum desired output level. The selected gain is an analog gain that is applied to the output of the speaker path DAC. The full-scale output of the speaker path DAC is 3.58dBV$_{PK}$ (typical). The programmable gain steps are in +3dB increments from -3dB to +12dB. Table 9 shows the maximum peak output level for the selected SPK_GAIN setting.

Table 9. Maximum Peak Output Voltage per Gain Selection

SPK_GAIN SETTING	ANALOG GAIN (dB)	MAXIMUM PEAK OUTPUT VOLTAGE (V_{PK})
0x0	-3	1.07 (0.59dBV$_{PK}$)
0x1	0	1.51 (3.58dBV$_{PK}$)
0x2	+3	2.13 (6.57dBV$_{PK}$)
0x3	+6	3.01 (9.57dBV$_{PK}$)
0x4	+9	4.26 (12.59dBV$_{PK}$)
0x5	+12	6.01 (15.58dBV$_{PK}$)

DC Blocking Filter

The digital audio interface includes a DC blocking filter with a -3dB cutoff at f_C (see the *Electrical Characteristics* table).

DAC Digital Filters

The DAC features a digital lowpass filter that is automatically configured based on the sample rate that is used. This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. See the *DAC Digital Filters* section of the *Electrical Characteristics* table.

Tone Generator

The device includes a tone generator which when enabled (using the TONE_EN bit field) replaces the SoundWire interface audio input as the input source to the speaker playback path. The tone generator requires a valid SW_CLK rate for audio as indicated in the *SoundWire Clock Configuration* section.

The tone generator output is configured to generate sine wave tones or DC tones (using the TONE_CONFIG bit field).

The tone generator operates at a sample rate that is based on the base clock rate and can create sine wave tones that are an integer division of the 48kHz sample rate. The integer divider ranges from 4 to 192, producing a sinewave tone ranging from 12kHz to 250Hz for a 48kHz sample rate. The amplitude of the tone generator output sine wave tone is full-scale but the amplifier output can be adjusted using the speaker volume (*SPK_VOL*) and playback path gain control (*SPK_GAIN*).

The tone generator can output either a fixed or a programmable DC output level (as set by TONE_CONFIG). Fixed DC output levels of zero code, positive half-scale, and negative half-scale are provided for quick configuration.

Class D Amplifier

The filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Class D Output Short-Circuit Protection

If the output current limit of the Class D amplifier (I_{LIM}) is exceeded (see the *Electrical Characteristics* table), the outputs are disabled for approximately 20ms. At the end of the 20ms, the outputs are re-enabled. If the fault condition still exists, the outputs continue to disable and re-enable until the fault condition is removed.

Speaker Monitor

The MAX98363 features a speaker monitor that protects the speaker from potential damage due to DC at the output. The speaker monitor is enabled by default and can be disabled by setting the *SPKMON_EN* bit to zero. The circuit monitors the amplifier's PWM signal and shuts down the amplifier output when the signal goes above a programmed speaker monitor threshold (set by *SPKMON_THRESH*) for a programmed amount of time (set by *SPKMON_DURATION*). Additionally, the device also generates an *SPKMON_ERR* interrupt.

The speaker monitor circuit uses the PWM signals of the amplifier, and in the case of DC signals, the amplifier accurately detects signals above the threshold. However, for a sine wave with a DC offset, the average DC detected by the circuit is lower because of the zeroes presented from the sine signal. In this case, the speaker monitor threshold (set by *SPKMON_THRESH*) and/or the speaker monitor duration (set by *SPKMON_DURATION*) can be adjusted to protect the speaker against the DC present in the signal.

Clock Monitor

The MAX98363 features a clock monitor that detects any failures in the internal clocking of the device. These internal clocks are derived from the external SoundWire clock (SW_CLK). If a fault causes the clock signal on SW_CLK pin to stop without appropriate clock-stop procedure as described by the MIPI SoundWire v1.2 specification, the clock monitor automatically places the device into software shutdown (DP_EN_CH1 = 0) after 42µs (base rate = 19.2MHz/24.576MHz/16MHz) or 46µs (base rate = 22.5792MHz) and generates an internal clock error interrupt (CLK_ERR*). The clock monitor is enabled by the *CMON_EN* bit field and it operates when the device is in active state.

Turn-On and Turn-Off Volume Ramping

The MAX98363 features a volume ramp-up control to control speaker output amplitude ramping during speaker path start-up. The volume ramp-up can be bypassed with the *SPK_VOL_RMPUP_BYPASS* bit field for a faster turn-on time. The volume ramp-down is always enabled and ramps down the output during volume reduction or setting the output to mute. The volume ramp-down does not impact device turn-off time. See the *Electrical Characteristics* table for more information.

Click-and-Pop Suppression

The speaker amplifier features ADI's comprehensive click-and-pop suppression. During turn-on, the click-and-pop suppression circuitry reduces audible transient sources internal to the device. When entering shutdown or standby, the differential speaker outputs simultaneously go to high impedance.

SW_CLK and V_{DD} must remain valid for turn-off duration as mentioned in the *Electrical Characteristics* table after DP1_ChannelEN goes low for best click-and-pop performance.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters or shielding to meet EN55022B electromagnetic interference (EMI) regulation standards. Analog Devices' active emissions-limiting, edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions while maintaining high efficiency.

Analog Devices' spread-spectrum modulation mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The device's spread-spectrum modulator randomly varies the switching frequency by f_{SSM} around the center frequency (f_{SW}). Above 10MHz, the wideband spectrum looks like noise for EMI purposes.

Register Map

Register Map

ADDRESS	NAME	MSB							LSB
SoundWire Peripheral Control									
0x0040	SCP_IntStat_1[7:0]	–	–	–	–	–	IntStat ImpDef1	IntStat Bus Clash	IntStat Parity
0x0041	SCP_IntMask_1[7:0]	–	–	–	–	–	IntMask ImpDef1	IntMask Bus Clash	IntMask Parity
0x0044	SCP_Ctrl[7:0]	ForceReset	CurrentBank	–	–	–	–	ClockStop Now	ClockStop_NotFinished
0x0045	SCP_SystemCtrl[7:0]	–	–	–	–	–	–	–	ClockStop Prepare
0x0046	SCP_DevNumber[7:0]	–	–	Group_Id[1:0]		Device Number[3:0]			
0x004D	SCP BusClock Base[7:0]	–	–	–	–	–	Base Clock Freq[2:0]		
0x0050	SCP_DevId_0[7:0]	Device_ID[47:40]							
0x0051	SCP_DevId_1[7:0]	Device_ID[39:32]							
0x0052	SCP_DevId_2[7:0]	Device_ID[31:24]							
0x0053	SCP_DevId_3[7:0]	Device_ID[23:16]							
0x0054	SCP_DevId_4[7:0]	Device_ID[15:8]							
0x0055	SCP_DevId_5[7:0]	Device_ID[7:0]							
0x0060	SCP_FrameCtrl_Bank0[7:0]	RowControl_Bank0[4:0]					ColumnControl_Bank0[2:0]		
0x0062	Clock Scale Bank0[7:0]	–	–	–	–	Clock Scale[3:0]			
0x0070	SCP_FrameCtrl_Bank1[7:0]	RowControl_Bank1[4:0]					ColumnControl_Bank1[2:0]		
0x0072	Clock Scale Bank1[7:0]	–	–	–	–	Clock Scale[3:0]			
0x0080	SCP_PhyOutCtrl_0[7:0]	SlewTime_Ctrl_0[1:0]		–	–	–	–	–	–
Data Port 1 Registers									
0x0100	DP1_IntStat[7:0]	–	–	–	–	–	–	IntStat Port Ready	IntStat Test Fail
0x0101	DP1_IntMask[7:0]	–	–	–	–	–	–	IntMask Port Ready	IntMask Test Fail
0x0102	DP1_PortCtrl[7:0]	–	–	Port Direction	Next InvertBank	PortDataMode[1:0]		PortFlowMode[1:0]	
0x0103	DP1_BlockCtrl[7:0]	–	–	–	WordLength[4:0]				
0x0104	DP1_PrepareStatus[7:0]	–	–	–	–	–	–	–	N-Finished Channel 1

ADDRESS	NAME	MSB							LSB
0x0105	DP1_PrepareCtrl[7:0]	–	–	–	–	–	–	–	Prepare Channel 1
Data Port 1- Bank 0 Registers									
0x0120	DP1_ChannelEn[7:0]	–	–	–	–	–	–	–	Enable Channel 1
0x0122	DP1_SampleCtrl1[7:0]	SampleIntervalLow[7:0]							
0x0123	DP1_SampleCtrl2[7:0]	SampleIntervalHigh[7:0]							
0x0124	DP1_OffsetCtrl1[7:0]	Offset1[7:0]							
0x0125	DP1_OffsetCtrl2[7:0]	Offset2[7:0]							
0x0126	DP1_HCtrl[7:0]	HStart[3:0]				HStop[3:0]			
0x0127	DP1_BlockCtrl3[7:0]	–	–	–	–	–	–	–	BlockPacking Mode
Data Port 1- Bank 1 Registers									
0x0130	DP1_ChannelEn[7:0]	–	–	–	–	–	–	–	Enable Channel 1
0x0132	DP1_SampleCtrl1[7:0]	SampleIntervalLow[7:0]							
0x0133	DP1_SampleCtrl2[7:0]	SampleIntervalHigh[7:0]							
0x0134	DP1_OffsetCtrl1[7:0]	Offset1[7:0]							
0x0135	DP1_OffsetCtrl2[7:0]	Offset2[7:0]							
0x0136	DP1_HCtrl[7:0]	HStart[3:0]				HStop[3:0]			
0x0137	DP1_BlockCtrl3[7:0]	–	–	–	–	–	–	–	BlockPacking Mode
Interrupt Registers									
0x2001	Interrupt Raw[7:0]	THERM SHDN_RAW	PWRDN_DONE_RAW	PWRUP_DONE_RAW	–	CLK_ERR_RAW	SPKMON_ERR_RAW	SPK_OVC_RAW	OTP_FAIL_RAW
0x2003	Interrupt State[7:0]	THERM SHDN_STATE	PWRDN_DONE_STATE	PWRUP_DONE_STATE	–	CLK_ERR_STATE	SPKMON_ERR_STATE	SPK_OVC_STATE	OTP_FAIL_STATE
0x2005	Interrupt Flag[7:0]	THERM SHDN_FLAG	PWRDN_DONE_FLAG	PWRUP_DONE_FLAG	–	CLK_ERR_FLAG	SPKMON_ERR_FLAG	SPK_OVC_FLAG	OTP_FAIL_FLAG
0x2007	Interrupt Enable[7:0]	THERM SHDN_EN	PWRDN_DONE_EN	PWRUP_DONE_EN	–	CLK_ERR_EN	SPKMON_ERR_EN	SPK_OVC_EN	OTP_FAIL_EN
0x2009	Interrupt Clear[7:0]	THERM SHDN_CLR	PWRDN_DONE_CLR	PWRUP_DONE_CLR	–	CLK_ERR_CLR	SPKMON_ERR_CLR	SPK_OVC_CLR	OTP_FAIL_CLR
Error Monitor									
0x2021	Error Monitor Control[7:0]	–	–	–	–	SPKMON_EN	–	–	CMON_EN
0x2022	Speaker Mon Threshold[7:0]	SPKMON_THRESH[7:0]							

ADDRESS	NAME	MSB							LSB
0x2023	Speaker Mon Duration[7:0]	–	–	–	–	SPKMON_DURATION[3:0]			
Tone Generator Control									
0x2030	Tone Generator and DC Config[7:0]	–	–	–	–	TONE_CONFIG[3:0]			
0x203F	Tone Generator Enable[7:0]	–	–	–	–	–	–	–	TONE_EN
Speaker Path Control									
0x2040	AMP volume control[7:0]	–	SPK_VOL[6:0]						
0x2041	AMP Path Gain[7:0]	–	–	–	–	–	SPK_GAIN[2:0]		
0x2042	AMP DSP Config[7:0]	–	–	–	RSVD	SPK_VOL_RMPUP_BYPASS	RSVD	RSVD	RSVD
Device and Revision ID									
0x21FF	Revision ID[7:0]	REV_ID[7:0]							

Register Details

SCP_IntStat_1 (0x0040)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	IntStat ImpDef1	IntStat Bus Clash	IntStat Parity
Reset	–	–	–	–	–	0x0	0x0	0x0
Access Type	–	–	–	–	–	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IntStat ImpDef1	2	Refer to the MIPI SoundWire spec v1.2 documentation.
IntStat Bus Clash	1	Refer to the MIPI SoundWire spec v1.2 documentation.
IntStat Parity	0	Refer to the MIPI SoundWire spec v1.2 documentation

SCP_IntMask_1 (0x0041)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	IntMask ImpDef1	IntMask Bus Clash	IntMask Parity
Reset	–	–	–	–	–			
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
IntMask ImpDef1	2	Refer to the MIPI SoundWire spec v1.2 documentation.
IntMask Bus Clash	1	Refer to the MIPI SoundWire spec v1.2 documentation.
IntMask Parity	0	Refer MIPI Soundwire spec v1.2 documentation.

SCP_Ctrl (0x0044)

BIT	7	6	5	4	3	2	1	0
Field	ForceReset	CurrentBank	–	–	–	–	ClockStop Now	ClockStop_ NotFinished
Reset	0b0	0x0	–	–	–	–	0b0	0x0
Access Type	Write Only	Read Only	–	–	–	–	Write Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
ForceReset	7	This bit field is used to trigger a SoundWire reset event.	0: No action. 1: Triggers a software reset event.
CurrentBank	6	Refer to the MIPI SoundWire spec v1.2 documentation.	
ClockStop Now	1	Refer to the MIPI SoundWire spec v1.2 documentation.	0: No action. 1: Triggers a software reset event.
ClockStop_NotFinished	0	Refer to the MIPI SoundWire spec v1.2 documentation.	

SCP_SystemCtrl (0x0045)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	ClockStop Prepare
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
ClockStop Prepare	0	Refer to the MIPI SoundWire spec v1.2 documentation.

SCP_DevNumber (0x0046)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Group_Id[1:0]		Device Number[3:0]			
Reset	–	–	0x0		0x0			
Access Type	–	–	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Group_Id	5:4		00: No group membership, device responds to programmed device numbers from 1 to 11, or device address 15 (all devices on the bus. 01: Device responds to programmed device number (from 1 to 11), group 12 i.e., all peripherals with device address 12, or device address 15 (all devices on the bus). 10: Device responds to programmed device number (from 1 to 11), group 13 i.e., all peripherals with device address 13, or device address 15 (all devices on the bus). 11: Reserved.

BITFIELD	BITS	DESCRIPTION	DECODE
Device Number	3:0	Refer to the MIPI SoundWire spec v1.2 documentation.	

SCP BusClock Base (0x004D)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	Base Clock Freq[2:0]		
Reset	–	–	–	–	–	0x0		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
Base Clock Freq	2:0		0x0: Unknown, manager is explicitly not informing the peripheral of the bus clock frequency. 0x1: Base clock frequency = 19.2MHz, relates to 48kHz sample frequencies. 0x2: Base clock frequency = 24MHz, relates to 48kHz sample frequencies. 0x3: Base clock frequency = 24.576MHz, relates to 48kHz sample frequencies. 0x4: Base clock frequency = 22.5792MHz, relates to 44.1kHz sample frequencies. 0x5: Base clock frequency = 32MHz, relates to Bluetooth® frequencies. 0x6: Reserved. 0x7: Implementation-defined frequency. Not supported frequency listed in DisCo data for the device.

SCP_DevId_0 (0x0050)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[47:40]							
Reset	0x30							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		0x30: Unique ID set for the MAX98363A/C with ADDR = GND. 0x31: Unique ID set for the MAX98363A/C with ADDR = Float. 0x32: Unique ID set for the MAX98363A/C with ADDR = V_{DD}. 0x33: Unique ID set for the MAX98363A/C with ADDR = 100kΩ pull-up to V_{DD}. 0x34: Unique ID set for the MAX98363A/C with ADDR = 100kΩ pull-up to GND. 0x35: Unique ID set for the MAX98363B/D with ADDR = GND. 0x36: Unique ID set for the MAX98363B/D with ADDR = Float. 0x37: Unique ID set for the MAX98363B/D with ADDR = V_{DD}. 0x38: Unique ID set for the MAX98363B/D with ADDR = 100kΩ pull-up to V_{DD}. 0x39: Unique ID set for the MAX98363B/D with ADDR = 100kΩ pull-up to GND.

SCP_DevId_1 (0x0051)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[39:32]							
Reset	0x01							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		0x01: MIPI assigned manufacturer ID MSB.

SCP_DevId_2 (0x0052)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[31:24]							
Reset	0x9F							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		0x9F: MIPI assigned manufacturer ID LSB.

SCP_DevId_3 (0x0053)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[23:16]							
Reset	0x83							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		0x83: Manufacturer part number (MSB).

SCP_DevId_4 (0x0054)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[15:8]							
Reset	0x63							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		0x63: Manufacturer part number (LSB).

SCP_DevId_5 (0x0055)

BIT	7	6	5	4	3	2	1	0
Field	Device_ID[7:0]							
Reset	0x0							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
Device_ID	7:0		0x0: Class MIPI reserved.

SCP_FrameCtrl_Bank0 (0x0060)

BIT	7	6	5	4	3	2	1	0
Field	RowControl_Bank0[4:0]					ColumnControl_Bank0[2:0]		
Reset	0x0					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION
RowControl_Bank0	7:3	Refer to the MIPI SoundWire spec v1.2 documentation.
ColumnControl_Bank0	2:0	Refer to the MIPI SoundWire spec v1.2 documentation.

Clock Scale Bank0 (0x0062)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Clock Scale[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Clock Scale	3:0		0x0: Reserved. 0x1: Reserved. 0x2: Scaling factor = 2. 0x3: Scaling factor = 4. 0x4: Scaling factor = 8. 0x5: Scaling factor = 16. 0x6: Scaling factor = 32. 0x7-0xF: Reserved.

SCP_FrameCtrl_Bank1 (0x0070)

BIT	7	6	5	4	3	2	1	0
Field	RowControl_Bank1[4:0]					ColumnControl_Bank1[2:0]		
Reset	0x0					0x0		
Access Type	Write, Read					Write, Read		

BITFIELD	BITS	DESCRIPTION
RowControl_Bank1	7:3	Refer to the MIPI SoundWire spec v1.2 documentation.
ColumnControl_Bank1	2:0	Refer to the MIPI SoundWire spec v1.2 documentation.

Clock Scale Bank1 (0x0072)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	Clock Scale[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
Clock Scale	3:0		0x0: Reserved. 0x1: Reserved. 0x2: Scaling Factor = 2. 0x3: Scaling Factor = 4. 0x4: Scaling Factor = 8. 0x5: Scaling Factor = 16. 0x6: Scaling Factor = 32. 0x7-0xF: Reserved.

SCP_PhyOutCtrl_0 (0x0080)

BIT	7	6	5	4	3	2	1	0
Field	SlewTime_Ctrl_0[1:0]		–	–	–	–	–	–
Reset	0x0		–	–	–	–	–	–
Access Type	Write Only		–	–	–	–	–	–

BITFIELD	BITS	DESCRIPTION	DECODE
SlewTime_Ctrl_0	7:6	SW_DAT output driver slew-rate control register.	0x0: Slew time controlled indirectly by selecting output drive strength. 0x1: Short slew time/fast edge. 0x2: Medium slew time. 0x3: Long slew time/slow edge.

DP1_IntStat (0x0100)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	IntStat Port Ready	IntStat Test Fail
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IntStat Port Ready	1	Refer to the MIPI SoundWire spec v1.2 documentation.
IntStat Test Fail	0	Refer to the MIPI Soundwire spec v1.2 documentation.

DP1_IntMask (0x0101)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	IntMask Port Ready	IntMask Test Fail
Reset	–	–	–	–	–	–		
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
IntMask Port Ready	1	Refer to the MIPI SoundWire spec v1.2 documentation.
IntMask Test Fail	0	Refer to the MIPI Soundwire spec v1.2 documentation.

DP1_PortCtrl (0x0102)

BIT	7	6	5	4	3	2	1	0
Field	–	–	Port Direction	Next InvertBank	PortDataMode[1:0]		PortFlowMode[1:0]	
Reset	–	–	0x1	0x0	0x0		0x0	
Access Type	–	–	Read Only	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
Port Direction	5	Refer to the MIPI SoundWire spec v1.2 documentation.
Next InvertBank	4	Refer to the MIPI SoundWire spec v1.2 documentation.
PortDataMode	3:2	Refer to the MIPI SoundWire spec v1.2 documentation.
PortFlowMode	1:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_BlockCtrl (0x0103)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	WordLength[4:0]				
Reset	–	–	–	0x0				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
WordLength	4:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_PrepareStatus (0x0104)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	N-Finished Channel 1
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
N-Finished Channel 1	0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_PrepareCtrl (0x0105)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	Prepare Channel 1
Reset	–	–	–	–	–	–	–	0x1
Access Type	–	–	–	–	–	–	–	Read Only

BITFIELD	BITS	DESCRIPTION
Prepare Channel 1	0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_ChannelEn (0x0120)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	Enable Channel 1
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
Enable Channel 1	0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_SampleCtrl1 (0x0122)

BIT	7	6	5	4	3	2	1	0
Field	SampleIntervalLow[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SampleIntervalLow	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_SampleCtrl2 (0x0123)

BIT	7	6	5	4	3	2	1	0
Field	SampleIntervalHigh[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SampleIntervalHigh	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_OffsetCtrl1 (0x0124)

BIT	7	6	5	4	3	2	1	0
Field	Offset1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Offset1	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_OffsetCtrl2 (0x0125)

BIT	7	6	5	4	3	2	1	0
Field	Offset2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Offset2	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_HCtrl (0x0126)

BIT	7	6	5	4	3	2	1	0
Field	HStart[3:0]				HStop[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
HStart	7:4	Refer to the MIPI SoundWire spec v1.2 documentation.
HStop	3:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_BlockCtrl3 (0x0127)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BlockPacking Mode
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
BlockPacking Mode	0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_ChannelEn (0x0130)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	Enable Channel 1
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
Enable Channel 1	0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_SampleCtrl1 (0x0132)

BIT	7	6	5	4	3	2	1	0
Field	SampleIntervalLow[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SampleIntervalLow	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_SampleCtrl2 (0x0133)

BIT	7	6	5	4	3	2	1	0
Field	SampleIntervalHigh[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SampleIntervalHigh	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_OffsetCtrl1 (0x0134)

BIT	7	6	5	4	3	2	1	0
Field	Offset1[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Offset1	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_OffsetCtrl2 (0x0135)

BIT	7	6	5	4	3	2	1	0
Field	Offset2[7:0]							
Reset	0x0							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
Offset2	7:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_HCtrl (0x0136)

BIT	7	6	5	4	3	2	1	0
Field	HStart[3:0]				HStop[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
HStart	7:4	Refer to the MIPI SoundWire spec v1.2 documentation.
HStop	3:0	Refer to the MIPI SoundWire spec v1.2 documentation.

DP1_BlockCtrl3 (0x0137)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	BlockPacking Mode
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
BlockPacking Mode	0	Refer to the MIPI SoundWire spec v1.2 documentation.

Interrupt Raw (0x2001)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_RAW	PWRDN_DONE_RAW	PWRUP_DONE_RAW	–	CLK_ERR_RAW	SPKMON_ERR_RAW	SPK_OVC_RAW	OTP_FAIL_RAW
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	0x0
Access Type	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_RAW	7	Raw value indicating if the device is in thermal shutdown.	0x0: Die temperature is lower than thermal shutdown setting level. 0x1: Die temperature is greater than thermal shutdown setting level.
PWRDN_DONE_RAW	6	Raw value of power-down done.	0x0: Device is not reporting a power-down into software shutdown event. 0x1: Device is reporting a power-down into software shutdown event.
PWRUP_DONE_RAW	5	Raw value of power-up done.	0x0: Device is not reporting a power-up event. 0x1: Device is reporting a power-up into the active state.
CLK_ERR_RAW	3	Raw value of clock monitor error indicator.	0x0: No clock error is reported. 0x1: Clock error is reported.
SPKMON_ERR_RAW	2	Raw value of speaker monitor error indicating DC level detection at amplifier output.	0x0: DC level is not presented, or lower than the setting threshold level. 0x1: DC level is greater than the setting threshold level.
SPK_OVC_RAW	1	Raw value of speaker overcurrent limit.	0x0: Speaker overcurrent limit is not detected. 0x1: Speaker overcurrent limit is detected.
OTP_FAIL_RAW	0	OTP loading result.	0x0: OTP loading successful. 0x1: OTP loading failed CRC check.

Interrupt State (0x2003)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_STATE	PWRDN_DONE_STATE	PWRUP_DONE_STATE	–	CLK_ERR_STATE	SPKMON_ERR_STATE	SPK_OVC_STATE	OTP_FAIL_STATE
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	0x0
Access Type	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_STATE	7	Unmaskable interrupt state, cleared by THERMSHDN_CLR.	0x0: No rising edge of THERMSHDN_RAW. 0x1: Rising edge of THERMSHDN_RAW since last THERMSHDN_CLR.
PWRDN_DONE_STATE	6	Unmaskable interrupt state, cleared by PWRDN_DONE_CLR.	0x0: No rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR. 0x1: Rising edge of PWRDN_DONE_RAW detected since last PWRDN_DONE_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
PWRUP_DONE_STATE	5	Unmaskable interrupt state, cleared by PWRUP_DONE_CLR.	0x0: No rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR. 0x1: Rising edge of PWRUP_DONE_RAW detected since last PWRUP_DONE_CLR.
CLK_ERR_STATE	3	Unmaskable interrupt state, cleared by CLK_ERR_CLR.	0x0: No rising edge of CLK_ERR_RAW since last CLK_ERR_CLR. 0x1: Rising edge of CLK_ERR_RAW detected since last CLK_ERR_CLR.
SPKMON_ERR_STATE	2	Unmaskable interrupt state, cleared by SPKMON_ERR_CLR.	0x0: No rising edge of SPKMON_RAW since last SPKMON_CLR. 0x1: Rising edge of SPKMON_RAW detected since last SPKMON_CLR.
SPK_OVC_STATE	1	Unmaskable interrupt state, cleared by SPK_OVC_CLR.	0x0: No rising edge of SPK_OVC_RAW since last SPK_OVC_CLR. 0x1: Rising edge of SPK_OVC_RAW detected since last SPK_OVC_CLR.
OTP_FAIL_STATE	0	OTP loading result.	0x0: OTP loading successful. 0x1: OTP loading failed CRC check.

Interrupt Flag (0x2005)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_FLAG	PWRDN_DONE_FLAG	PWRUP_DONE_FLAG	–	CLK_ERR_FLAG	SPKMON_ERR_FLAG	SPK_OVC_FLAG	OTP_FAIL_FLAG
Reset	0x0	0x0	0x0	–	0x0	0x0	0b0	
Access Type	Read Only	Read Only	Read Only	–	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_FLAG	7	Thermal shutdown begin event maskable interrupt flag. Masked by THERMSHDN_EN and cleared by THERMSHDN_CLR. An interrupt is sent on SoundWire bus on flag bit rising edge.	0x0: No rising edge of THERMSHDN_RAW since last THERMSHDN_CLR or THERMSHDN_EN is low. 0x1: THERMSHDN_EN is high and rising edge of THERMSHDN_RAW since last THERMSHDN_CLR.
PWRDN_DONE_FLAG	6	Device power-down done event maskable interrupt flag. Masked by PWRDN_DONE_EN and cleared by PWRDN_DONE_CLR. An interrupt is generated on SoundWire bus on a flag bit rising edge.	0x0: No rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR or PWRDN_DONE_EN is low. 0x1: PWRDN_DONE_EN is high and rising edge of PWRDN_DONE_RAW since last PWRDN_DONE_CLR.
PWRUP_DONE_FLAG	5	Device power-up done event maskable interrupt flag. Masked by PWRUP_DONE_EN and cleared by PWRUP_DONE_CLR. An interrupt is generated on a flag bit rising edge.	0x0: No rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR or PWRUP_DONE_EN is low. 0x1: PWRUP_DONE_EN is high and rising edge of PWRUP_DONE_RAW since last PWRUP_DONE_CLR.
CLK_ERR_FLAG	3	SoundWire clock and internal clock error event maskable interrupt flag. Masked by CLK_ERR_EN and cleared by CLK_ERR_CLR. An interrupt is generated on a flag bit rising edge.	0x0: No rising edge of CLK_ERR_RAW since last CLK_ERR_CLR or CLK_ERR_EN is low. 0x1: CLK_ERR_EN high and rising edge of CLK_ERR_RAW since last CLK_ERR_CLR.

BITFIELD	BITS	DESCRIPTION	DECODE
SPKMON_ERR_FLAG	2	Internal speaker data monitor error event maskable interrupt flag. Masked by SPKMON_ERR_EN and cleared by SPKMON_ERR_CLR. An interrupt is generated on a flag bit rising edge.	0x0: No rising edge of SPKMON_ERR_RAW since last SPKMON_ERR_CLR or SPKMON_ERR_EN is low. 0x1: SPKMON_ERR_EN high and rising edge of SPKMON_ERR_RAW since last SPKMON_ERR_CLR.
SPK_OVC_FLAG	1	Speaker overcurrent event maskable interrupt flag. Masked by SPK_OVC_EN and cleared by SPK_OVC_CLR. An interrupt is generated on a flag bit rising edge.	0x0: No rising edge of SPK_OVC_RAW since last SPK_OVC_CLR or SPK_OVC_EN is low. 0x1: SPK_OVC_EN is high and rising edge of SPK_OVC_RAW since last SPK_OVC_CLR.
OTP_FAIL_FLAG	0	OTP load routine fail event maskable interrupt flag. Masked by OTP_FAIL_EN and cleared by OTP_FAIL_CLR. An interrupt is generated on a flag bit rising edge.	0x0: No rising edge of OTP_FAIL_RAW since last OTP_FAIL_CLR or OTP_FAIL_EN is low. 0x1: OTP_FAIL_EN is high and rising edge of OTP_FAIL_RAW since last OTP_FAIL_CLR.

Interrupt Enable (0x2007)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_EN	PWRDN_DONE_EN	PWRUP_DONE_EN	–	CLK_ERR_EN	SPKMON_ERR_EN	SPK_OVC_EN	OTP_FAIL_EN
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_EN	7	Enable (unmask) control for THERMSHDN_FLAG.	0x0: THERMSHDN_FLAG cannot go high. 0x1: THERMSHDN_FLAG goes high if there is a rising edge on THERMSHDN_RAW since last THERMSHDN_CLR.
PWRDN_DONE_EN	6	Enable (unmask) control for PWRDN_DONE_FLAG.	0: PWRDN_DONE_FLAG cannot go high. 1: PWRDN_DONE_FLAG goes high if there is a rising edge on PWRDN_DONE_RAW since last PWRDN_DONE_CLR.
PWRUP_DONE_EN	5	Enable (unmask) control for PWRUP_DONE_FLAG.	0: PWRUP_DONE_FLAG cannot go high. 1: PWRUP_DONE_FLAG goes high if there is a rising edge on PWRUP_DONE_RAW since last PWRUP_DONE_CLR.
CLK_ERR_EN	3	Enable (unmask) control for CLK_ERR_FLAG.	0x0: CLK_ERR_FLAG cannot be high. 0x1: CLK_ERR_FLAG goes high if there is a rising edge on CLK_ERR_RAW since last CLK_ERR_CLR.
SPKMON_ERR_EN	2	Enable (unmask) control for SPKMON_ERR_FLAG.	0x0: SPKMON_ERR_FLAG cannot go high. 0x1: SPKMON_ERR_FLAG goes high if there is a rising edge on SPKMON_ERR_RAW since last SPKMON_ERR_CLR.
SPK_OVC_EN	1	Enable (unmask) control for SPK_OVC_FLAG.	0x0: SPK_OVC_FLAG cannot go high. 0x1: SPK_OVC_FLAG goes high if there is a rising edge on SPK_OVC_RAW since last SPK_OVC_CLR.
OTP_FAIL_EN	0	Enable (unmask) control for OTP_FAIL_FLAG.	0: OTP_FAIL_FLAG cannot go high. 1: OTP_FAIL_FLAG goes high if there is a rising edge on OTP_FAIL_RAW since last OTP_FAIL_CLR.

Interrupt Clear (0x2009)

BIT	7	6	5	4	3	2	1	0
Field	THERMSHDN_CLR	PWRDN_DONE_CLR	PWRUP_DONE_CLR	–	CLK_ERR_CLR	SPKMON_ERR_CLR	SPK_OVC_CLR	OTP_FAIL_CLR
Reset	0b0	0b0	0b0	–	0b0	0b0	0b0	0x0
Access Type	Write Only	Write Only	Write Only	–	Write Only	Write Only	Write Only	Write Only

BITFIELD	BITS	DESCRIPTION	DECODE
THERMSHDN_CLR	7	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears THERMSHDN_STATE and THERMSHDN_FLAG interrupt bit.
PWRDN_DONE_CLR	6	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears PWRDN_DONE_STATE and PWRDN_DONE_FLAG interrupt bit.
PWRUP_DONE_CLR	5	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears PWRUP_DONE_STATE and PWRUP_DONE_FLAG interrupt bit.
CLK_ERR_CLR	3	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears CLK_ERR_STATE and CLK_ERR_FLAG interrupt bit.
SPKMON_ERR_CLR	2	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears SPKMON_ERR_STATE and SPKMON_ERR_FLAG interrupt bit.
SPK_OVC_CLR	1	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears SPK_OVC_STATE and SPK_OVC_FLAG interrupt bit.
OTP_FAIL_CLR	0	Clears associated STATE and FLAG bits.	0x0: Writing zero has no effect. 0x1: Clears OTP_FAIL_STATE and OTP_FAIL_FLAG interrupt bit.

Error Monitor Control (0x2021)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_EN	–	–	CMON_EN
Reset	–	–	–	–	0x0	–	–	0x1
Access Type	–	–	–	–	Write, Read	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPKMON_EN	3	Enables the internal speaker protection monitor.	0x0: Disable internal speaker data monitor. 0x1: Enable internal speaker data monitor.
CMON_EN	0	Enables the clock monitor to monitor internal clocks for clock errors.	0x0: Disable. 0x1: Enable.

Speaker Mon Threshold (0x2022)

BIT	7	6	5	4	3	2	1	0
Field	SPKMON_THRESH[7:0]							
Reset	0x58							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SPKMON_THRESH	7:0	Sets the speaker power threshold. If the signal power recovered by the circuit is above this threshold for longer than the DMON_DURATION, speaker monitor error is asserted. Threshold is calculated as % of full scale (FS). FS means the output voltage hit the rails. The voltage threshold can be calculated from the register setting using the following equation: Threshold (voltage) = (SPKMON_THRESH/128) x Class D Supply Voltage

Speaker Mon Duration (0x2023)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	SPKMON_DURATION[3:0]			
Reset	–	–	–	–	0x2			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPKMON_DURATION	3:0	Sets the time duration over which the speaker monitor must consecutively detect power above threshold before asserting a speaker monitor error.	**Value**: **Decode** 0x0: 8ms. 0x1: 20ms. 0x2: 40ms. 0x3: 60ms. 0x4: 80ms. 0x5: 160ms. 0x6: 240ms. 0x7: 320ms. 0x8: 400ms. 0x9: 480ms. 0xA: 560ms. 0xB: 640ms. 0xC: 720ms. 0xD: 800ms. 0xE: 880ms. 0xF: 960ms.

Tone Generator and DC Config (0x2030)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	TONE_CONFIG[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
TONE_CONFIG	3:0	Sets the type of output signal of the tone generator. Signal amplitude is set to full-scale.	0x00: Reserved. 0x01: DC = 0x0000 = 0. 0x02: DC = +full Scale/2. 0x03: DC = -fullScale/2. 0x04: 1kHz tone at 48kHz sample rate. 0x05: 12kHz tone at 48kHz sample rate. 0x06: 8kHz tone at 48kHz sample rate. 0x07: 6kHz tone at 48kHz sample rate. 0x08: 4kHz tone at 48kHz sample rate. 0x09: 3kHz tone at 48kHz sample rate. 0x0A: 2kHz tone at 48kHz sample rate. 0x0B: 1.5kHz tone at 48kHz sample rate. 0x0C: Reserved. 0x0D: 500Hz tone at 48kHz sample rate. 0x0E: 250Hz tone at 48kHz sample rate. 0x0E: Reserved.

Tone Generator Enable (0x203F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	TONE_EN
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION
TONE_EN	0	Enables the tone generator. When enabled, it replaces the SoundWire interface as the input to the speaker amplifier path.

AMP volume control (0x2040)

BIT	7	6	5	4	3	2	1	0
Field	–	SPK_VOL[6:0]						
Reset	–	0x0						
Access Type	–	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_VOL	6:0	Sets the digital volume level of the speaker amplifier path.	0x00: 0dB. 0x01: -0.5dB. 0x02: -1.0dB. ...: (-0.5dB steps). 0x7C: -62.0dB. 0x7D: -62.5dB. 0x7E: -63dB. 0x7F: Mute.

AMP Path Gain (0x2041)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	SPK_GAIN[2:0]		
Reset	–	–	–	–	–	0x5		
Access Type	–	–	–	–	–	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_GAIN	2:0	Sets the maximum peak output voltage level (V_{MPO}) for the speaker path (no-load). Values in dB are relative to the baseline speaker path DAC full-scale output level of 1.51Vp (3.68dBV).	0x00: 1.07V_P (-3dB). 0x01: 1.51V_P (0dB). 0x02: 2.13V_P (3dB). 0x03: 3.01V_P (6dB). 0x04: 4.26V_P (9dB). 0x05: 6.01V_P (12dB). 0x06-0x07: Reserved.

AMP DSP Config (0x2042)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	RSVD	SPK_VOL_RMPUP_BYPASS	RSVD	RSVD	RSVD
Reset	–	–	–	0b0	0b0	0b0	0b1	0b1
Access Type	–	–	–		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
SPK_VOL_RMPUP_BYPASS	3	Controls whether the speaker amplifier path volume is internally ramped up during start-up and during volume changes.	0: Volume ramp enabled. 1: Volume ramp bypassed.

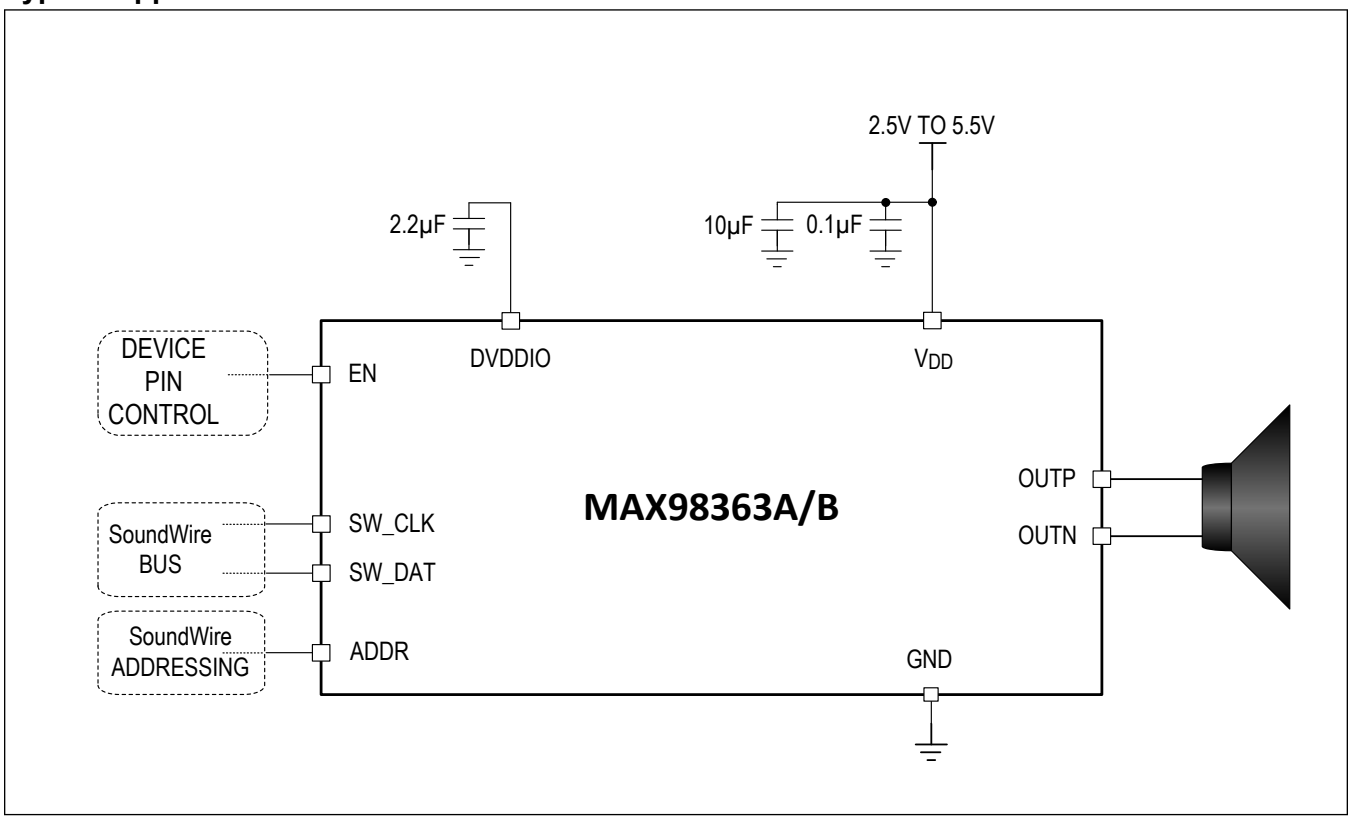
Revision ID (0x21FF)

BIT	7	6	5	4	3	2	1	0
Field	REV_ID[7:0]							
Reset	0x42							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
REV_ID	7:0	Revision of the device. Updated at every device revision.	0x42: Device revision.

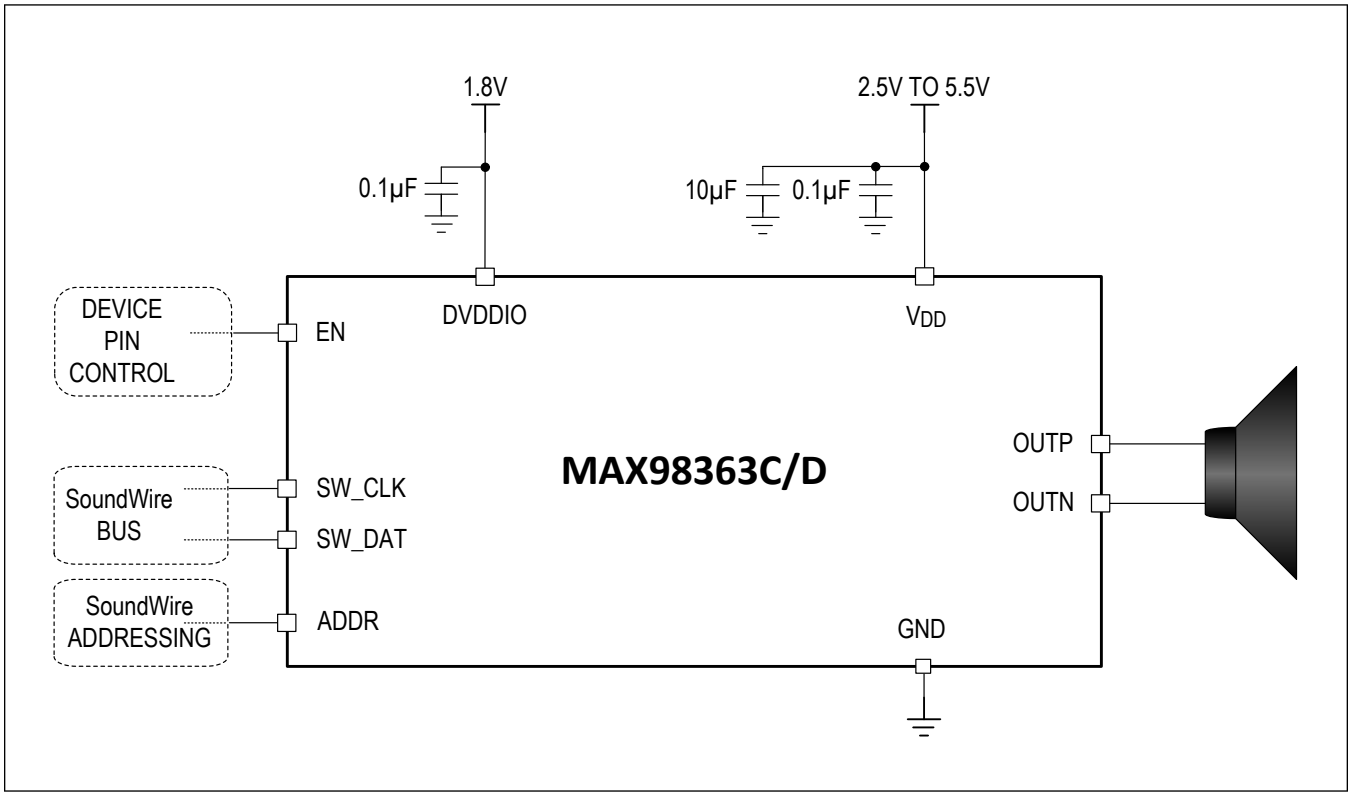
Typical Application Circuits

Typical Application Circuit with Internal DVDDIO LDO



Typical Application Circuits (continued)

Typical Application Circuit with External DVDDIO Power Supply



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	TOP MARKING
MAX98363AEWL+	-40°C to +85°C	9 WLP	ALX
MAX98363AEWL+T	-40°C to +85°C	9 WLP	ALX
MAX98363BEWL+	-40°C to +85°C	9 WLP	ALY
MAX98363BEWL+T	-40°C to +85°C	9 WLP	ALY
MAX98363CEWL+	-40°C to +85°C	9 WLP	AMF
MAX98363CEWL +T	-40°C to +85°C	9 WLP	AMF
MAX98363DEWL+	-40°C to +85°C	9 WLP	AME
MAX98363DEWL +T	-40°C to +85°C	9 WLP	AME

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/22	Initial release	—