



# Audio Subsystem with Class-D Speaker and Capless Headphone Driver

## SSM2804

### FEATURES

- 3 single-ended stereo audio inputs with optional differential mode
- Stereo, 1.4 W, filterless Class-D amplifiers with  $\Sigma$ - $\Delta$  modulation
- Integrated receiver path bypass switch
- Configurable, high performance capless headphone output with true ground Class-G technology
- Optional hardware-based headphone level limiter
- I<sup>2</sup>C control interface
  - Volume control
  - Flexible input/output mixing
  - Output mode control
  - EMI emissions control
  - Automatic level control (ALC)
  - Adjustable headphone level limiter
- Low shutdown current
- Short-circuit and thermal protection
- Pop-and-click suppression
- Available in a 30-ball, 2.5 mm × 3.0 mm WLCSP

### APPLICATIONS

- Mobile phones
- Portable multimedia devices

### GENERAL DESCRIPTION

The **SSM2804** is an audio subsystem designed specifically for mobile phones and portable multimedia devices. This highly flexible subsystem includes three input channels that can be configured as single-ended stereo or monaural differential for multimedia audio sources.

Each set of inputs is independently adjustable with the 2-wire I<sup>2</sup>C interface and features an adjustable gain over a 30 dB range in steps of 1 dB. Each set of input channels also offers the choice of variable input impedance PGA mode or fixed input impedance boost mode. The input signals are then mixed and routed to the desired set of outputs. This configuration is set using the 2-wire I<sup>2</sup>C control interface.

The **SSM2804** includes three selectable output modes.

The first output mode is a stereo Class-D speaker driver capable of delivering 2 × 1.4 W of continuous power to an 8  $\Omega$  bridge-tied load (BTL) with 1% THD + N when using a 5 V supply. This Class-D amplifier incorporates three-level  $\Sigma$ - $\Delta$  output modulation designed to increase battery life and improve EMI performance. The Class-D amplifier offers an I<sup>2</sup>C-adjustable volume control with a gain range from +12 dB to -63 dB in 31 steps.

The second output mode is a pair of high performance headphone drivers capable of delivering 20 mW per channel into stereo 32  $\Omega$  single-ended loads with 1% THD + N. The stereo headphone drivers use a highly efficient, true ground centered Class-G architecture. The headphone outputs incorporate I<sup>2</sup>C-adjustable volume control with a gain range from 0 dB to -75 dB in 32 steps.

The third output mode is an integrated receiver path bypass switch for passing voice signals from the audio baseband.

The **SSM2804** is specified over the industrial temperature range of -40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. The **SSM2804** is available in a 30-ball, 2.5 mm × 3.0 mm wafer level chip scale package (WLCSP).

#### Rev. 0

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## REVISION HISTORY

7/11—Revision 0: Initial Version

# FUNCTIONAL BLOCK DIAGRAM

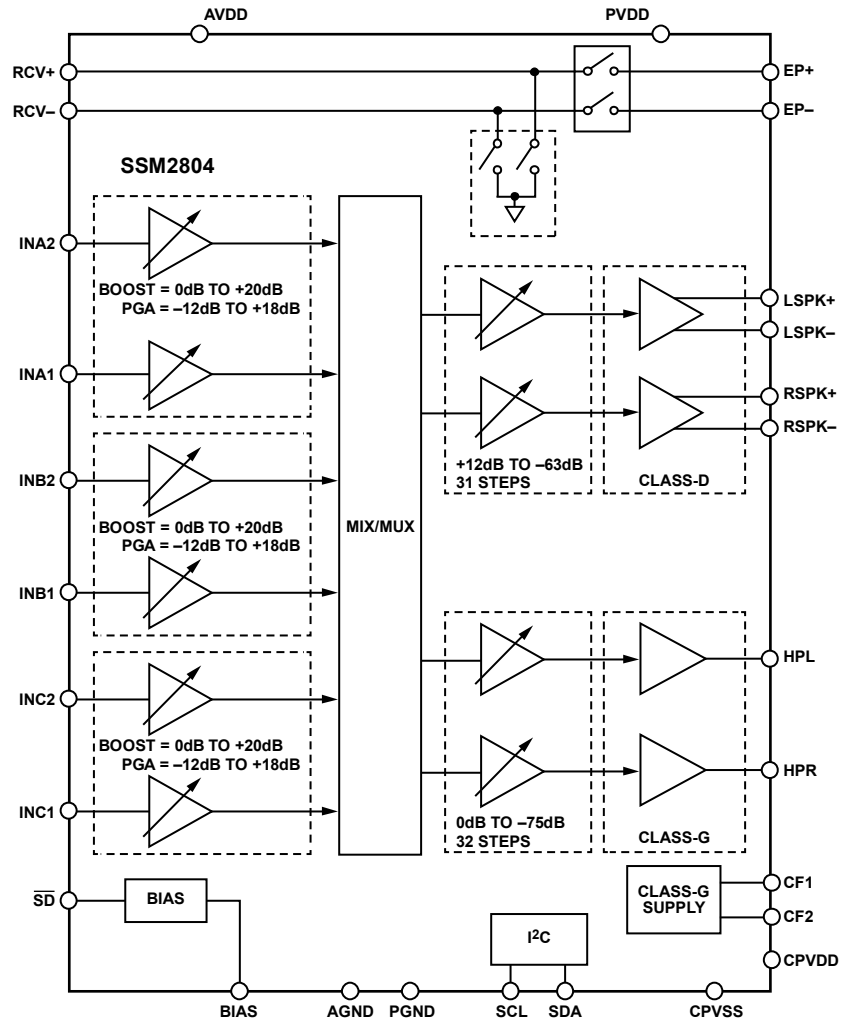


Figure 1.

099650-001

# SSM2804

## SPECIFICATIONS

T<sub>A</sub> = 25°C, AVDD = 3.3 V, PVDD = 3.6 V, gain = 0 dB, unless otherwise noted.

Table 1.

| Parameter                                      | Min | Typ  | Max | Unit | Test Conditions/Comments                                  |
|--|-----|------|-----|------|---|
| <b>POWER SUPPLY</b>                            |     |      |     |      |   |
| Analog Voltage Supply (AVDD)                   | 2.5 | 3.3  | 3.6 | V    |   |
| Speaker Voltage Supply (PVDD)                  | 2.7 | 3.6  | 5.5 | V    |   |
| Total Quiescent Current (I <sub>QD</sub> )     |     | 3.5  |     | mA   | HP mode only  |
|  |     | 6.0  |     | mA   | Stereo Class-D mode only                                  |
|  |     | 9.8  |     | mA   | HP and Class-D modes                                      |
|  |     | 400  |     | μA   | Receiver path mode  |
| Power-Down Current (I <sub>SD</sub> )          |     | 1    |     | μA   | $\overline{SD}$ pin low                                   |
| <b>INPUT CHARACTERISTICS</b>                   |     |      |     |      |   |
| Turn-On Time                                   |     | 10   |     | ms   | $\overline{SD}$ rising edge from AGND to AVDD             |
| <b>PGA Mode Operation</b>                      |     |      |     |      |   |
| Input Impedance                                | 38  | 54   |     | kΩ   | Minimum gain setting                                      |
|  | 4.5 | 6.5  |     | kΩ   | Maximum gain setting                                      |
| Gain Range                                     | -12 |      | +18 | dB   | INAx, INBx, INCx inputs, 31 steps                         |
| <b>Boost Mode Operation</b>                    |     |      |     |      |   |
| Input Impedance                                |     | 20   |     | kΩ   |   |
| Gain Range                                     | 0   |      | 20  | dB   | INAx, INBx, INCx inputs, 3 steps                          |
| <b>CLASS-D AMPLIFIER</b>                       |     |      |     |      |   |
| Output Offset Voltage (V <sub>OS</sub> )       |     | 2.3  |     | mV   | Output muted  |
|  |     | 12   |     | mV   | Output unmuted  |
| <b>Output Power (P<sub>OUT</sub>)</b>          |     |      |     |      |   |
|  |     | 310  |     | mW   | PVDD = 2.7 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 1%  |
|  |     | 700  |     | mW   | PVDD = 3.6 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 1%  |
|  |     | 1.0  |     | W    | PVDD = 4.2 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 1%  |
|  |     | 1.4  |     | W    | PVDD = 5.0 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 1%  |
|  |     | 700  |     | mW   | PVDD = 2.7 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 1%  |
|  |     | 1.5  |     | W    | PVDD = 3.6 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 1%  |
|  |     | 2.0  |     | W    | PVDD = 4.2 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 1%  |
|  |     | 2.9  |     | W    | PVDD = 5.0 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 1%  |
|  |     | 400  |     | mW   | PVDD = 2.7 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 10% |
|  |     | 860  |     | mW   | PVDD = 3.6 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 10% |
|  |     | 1.2  |     | W    | PVDD = 4.2 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 10% |
|  |     | 1.7  |     | W    | PVDD = 5.0 V, R <sub>L</sub> = 8 Ω + 33 μH, THD + N = 10% |
|  |     | 900  |     | mW   | PVDD = 2.7 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 10% |
|  |     | 1.8  |     | W    | PVDD = 3.6 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 10% |
|  |     | 2.5  |     | W    | PVDD = 4.2 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 10% |
|  |     | 3.6  |     | W    | PVDD = 5.0 V, R <sub>L</sub> = 4 Ω + 15 μH, THD + N = 10% |
| Total Harmonic Distortion Plus Noise (THD + N) |     | 0.01 |     | %    | R <sub>L</sub> = 8 Ω + 33 μH, P <sub>OUT</sub> = 250 mW   |
| Output Noise (V <sub>n</sub> )                 |     | 40   |     | μV   | 20 Hz to 20 kHz, A-weighted                               |
| Signal-to-Noise Ratio (SNR)                    |     | 94   |     | dB   | 2.0 V rms output, A-weighted, PVDD = 5 V                  |
| <b>Power Supply Rejection Ratio (PSRR)</b>     |     |      |     |      |   |
|  |     | 80   |     | dB   | 217 Hz, 200 mV p-p ripple                                 |
|  |     | 80   |     | dB   | 1 kHz, 200 mV p-p ripple                                  |
| <b>Common-Mode Rejection Ratio (CMRR)</b>      |     |      |     |      |   |
|  |     | 55   |     | dB   | Differential input mode, 1 kHz, 10 mV rms                 |
| Efficiency                                     |     | 89   |     | %    | P <sub>OUT</sub> = 700 mW                                 |
| Minimum Load Resistance (R <sub>LOAD</sub> )   | 4   |      |     | Ω    |   |
| Average Switching Frequency (f <sub>SW</sub> ) |     | 400  |     | kHz  |   |
| Volume Control Gain Range                      | -63 |      | +12 | dB   |   |

| Parameter   | Min | Typ     | Max    | Unit     | Test Conditions/Comments  |
|---|-----|---------|--------|----------|---|
| <b>HEADPHONE OUTPUT</b>   |     |         |        |          |   |
| Output Offset Voltage ( $V_{OS}$ )                              |     | 2       |        | mV       | Headphone only  |
|   |     | 8       |        | mV       | INAx, INBx, INCx inputs   |
| Output Power ( $P_{OUT}$ )                                      |     | 20      |        | mW       | $R_L = 32 \Omega$ , THD + N = 1%  |
|   |     | 40      |        | mW       | $R_L = 16 \Omega$ , THD + N = 1%, 1 $\mu$ F charge pump capacitor             |
| Total Harmonic Distortion Plus Noise (THD + N)                  |     | 0.012   |        | %        | $R_L = 32 \Omega$ , $P_{OUT} = 15$ mW   |
|   |     | 0.02    |        | %        | $R_L = 16 \Omega$ , $P_{OUT} = 10$ mW   |
| Output Noise ( $V_n$ )  |     | 16      |        | $\mu$ V  | 20 Hz to 20 kHz, A-weighted   |
| Signal-to-Noise Ratio (SNR)                                     |     | 96      |        | dB       | 800 mV rms output, A-weighted   |
| Power Supply Rejection Ratio (PSRR)                             |     | 95      |        | dB       | 217 Hz, 200 mV p-p ripple   |
|   |     | 85      |        | dB       | 1 kHz, 200 mV p-p ripple  |
| Crosstalk   |     | 90      |        | dB       | 1 kHz, $P_{OUT} = 12$ mW  |
| Minimum Load Resistance ( $R_{LOAD}$ )                          | 16  |         |        | $\Omega$ |   |
| Maximum Capacitive Load ( $C_{LOAD}$ )                          |     |         | 500    | pF       |   |
| Gain Range  | -75 |         | 0      | dB       |   |
| ESD Protection  |     | $\pm 8$ |        | kV       |   |
| <b>RECEIVER PATH (BYPASS SWITCH)</b>                            |     |         |        |          |   |
| Path Impedance ( $R_{ON}$ ), Receiver Inputs to Speaker Outputs |     | 1.5     |        | $\Omega$ | RCV+ to EP+ and RCV- to EP-   |
| Signal Path THD + N   |     | 0.1     |        | %        | $P_{OUT} = 70$ mW, $R_L = 32 \Omega$ or $P_{OUT} = 17.5$ mW, $R_L = 8 \Omega$ |
| Output Noise  |     | 10      |        | $\mu$ V  | 20 Hz to 20 kHz, A-weighted   |
| Off Channel Isolation   |     | 90      |        | dB       | 217 Hz, 200 mV p-p ripple   |
| Input Common Mode   |     |         | PVDD/2 | V        |   |

Table 2. Digital Logic Levels (CMOS Levels)

| Parameter                      | Min               | Typ | Max               | Unit |
|--------------------------------|-------------------|-----|-------------------|------|
| Input Low Level ( $V_{IL}$ )   |                   |     | 0.35              | V    |
| Input High Level ( $V_{IH}$ )  | 1.35              |     |                   | V    |
| Output Low Level ( $V_{OL}$ )  |                   |     | $0.1 \times AVDD$ | V    |
| Output High Level ( $V_{OH}$ ) | $0.9 \times AVDD$ |     |                   | V    |

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## I<sup>2</sup>C TIMING CHARACTERISTICS

Table 3.

| Parameter        | Limit            |                  | Unit | Description                |
|------------------|------------------|------------------|------|----------------------------|
|                  | t <sub>MIN</sub> | t <sub>MAX</sub> |      |                            |
| t <sub>SCS</sub> | 600              |                  | ns   | Start condition setup time |
| t <sub>SCH</sub> | 600              |                  | ns   | Start condition hold time  |
| t <sub>PH</sub>  | 600              |                  | ns   | SCL pulse width high       |
| t <sub>PL</sub>  | 1.3              |                  | μs   | SCL pulse width low        |
| f <sub>SCL</sub> | 0                | 526              | kHz  | SCL frequency              |
| t <sub>DS</sub>  | 100              |                  | ns   | Data setup time            |
| t <sub>DH</sub>  |                  | 900              | ns   | Data hold time             |
| t <sub>RT</sub>  |                  | 300              | ns   | SDA and SCL rise time      |
| t <sub>FT</sub>  |                  | 300              | ns   | SDA and SCL fall time      |
| t <sub>HCS</sub> | 600              |                  | ns   | Stop condition setup time  |

### Timing Diagram

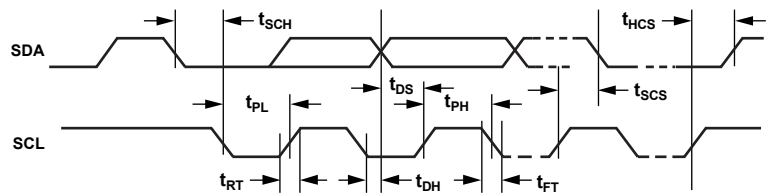


Figure 2. I<sup>2</sup>C Timing

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

| Parameter  | Rating                 |
|--|------------------------|
| Analog Supply Voltage (AVDD)                                   | -0.3 V to +3.6 V       |
| Speaker Supply Voltage (PVDD)                                  | -0.3 V to +3.6 V       |
| Input Voltage<br>$\overline{\text{SD}}$ , SCL, SDA, RCV+, RCV- | $V_{DD}$               |
| INA1, INA2, INB1, INB2, INC1, INC2                             | -0.3 V to AVDD + 0.3 V |
| ESD (HBM) on Headphone Output                                  | 8 kV                   |
| Storage Temperature Range                                      | -65°C to +150°C        |
| Operating Temperature Range                                    | -40°C to +85°C         |
| Junction Temperature Range                                     | -65°C to +165°C        |
| Lead Temperature (Soldering, 60 sec)                           | 300°C                  |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 5. Thermal Resistance**

| Package Type                   | PCB  | $\theta_{JA}$ | $\theta_{JB}$ | Unit |
|--------------------------------|------|---------------|---------------|------|
| 30-Ball, 2.5 mm × 3.0 mm WLCSP | 150P | 162           | 39            | °C/W |
|                                | 250P | 76            | 21            | °C/W |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

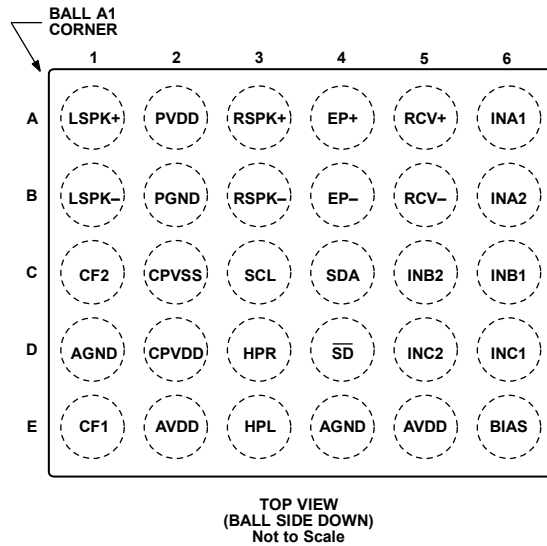


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

| Pin No. | Mnemonic | Description  |
|---------|----------|--|
| A1      | LSPK+    | Class-D Loudspeaker Output Left +  |
| B1      | LSPK-    | Class-D Loudspeaker Output Left -  |
| C1      | CF2      | Charge Pump Flyback Capacitor, Terminal 2                                      |
| D1      | AGND     | Analog Ground  |
| E1      | CF1      | Charge Pump Flyback Capacitor, Terminal 1                                      |
| A2      | PVDD     | Speaker Power Supply   |
| B2      | PGND     | Speaker Ground   |
| C2      | CPVSS    | Charge Pump Negative Supply for Class-G  |
| D2      | CPVDD    | Charge Pump Positive Supply for Class-G  |
| E2      | AVDD     | Analog Power Supply  |
| A3      | RSPK+    | Class-D Loudspeaker Output Right +   |
| B3      | RSPK-    | Class-D Loudspeaker Output Right -   |
| C3      | SCL      | 2-Wire I <sup>2</sup> C Control Interface Clock Input                          |
| D3      | HPR      | Class-G Headphone Output, Right Channel  |
| E3      | HPL      | Class-G Headphone Output, Left Channel   |
| A4      | EP+      | Integrated Switch Output +   |
| B4      | EP-      | Integrated Switch Output -   |
| C4      | SDA      | 2-Wire I <sup>2</sup> C Control Interface Data Input/Output                    |
| D4      | SD       | Shutdown Control, Active Low (Optional Limiter Threshold Voltage)              |
| E4      | AGND     | Analog Ground  |
| A5      | RCV+     | Baseband Receiver (Voice) Input +  |
| B5      | RCV-     | Baseband Receiver (Voice) Input -  |
| C5      | INB2     | Configurable Input B2 (Single-Ended Input B- or Stereo Input B, Left Channel)  |
| D5      | INC2     | Configurable Input C2 (Single-Ended Input C- or Stereo Input C, Left Channel)  |
| E5      | AVDD     | Analog Power Supply  |
| A6      | INA1     | Configurable Input A1 (Single-Ended Input A+ or Stereo Input A, Right Channel) |
| B6      | INA2     | Configurable Input A2 (Single-Ended Input A- or Stereo Input A, Left Channel)  |
| C6      | INB1     | Configurable Input B1 (Single-Ended Input B+ or Stereo Input B, Right Channel) |
| D6      | INC1     | Configurable Input C1 (Single-Ended Input C+ or Stereo Input C, Right Channel) |
| E6      | BIAS     | Device Bias Pin  |



# TYPICAL PERFORMANCE CHARACTERISTICS

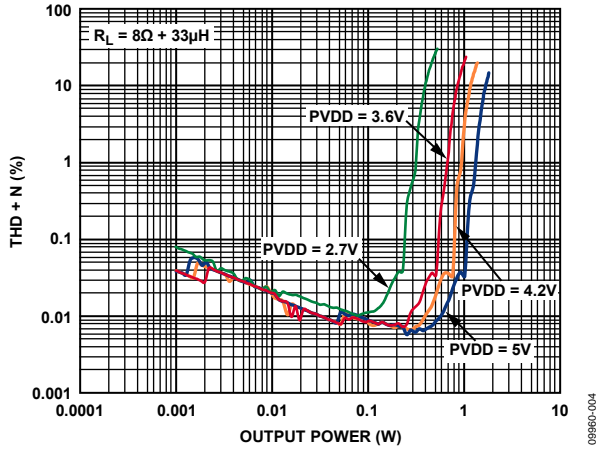


Figure 4. THD + N vs. Output Power into 8 Ω, Class-D Amplifier, Mono Operation

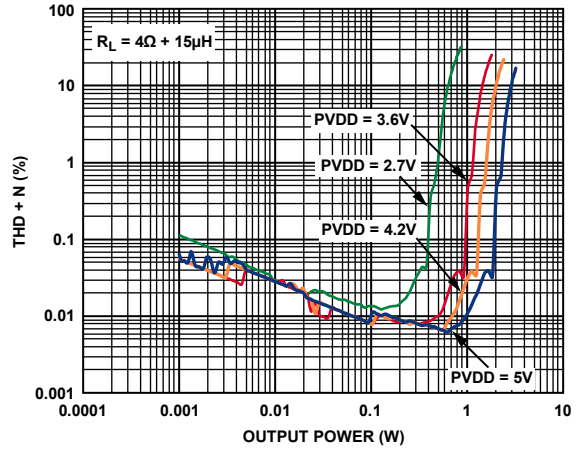


Figure 7. THD + N vs. Output Power into 4 Ω, Class-D Amplifier, Mono Operation

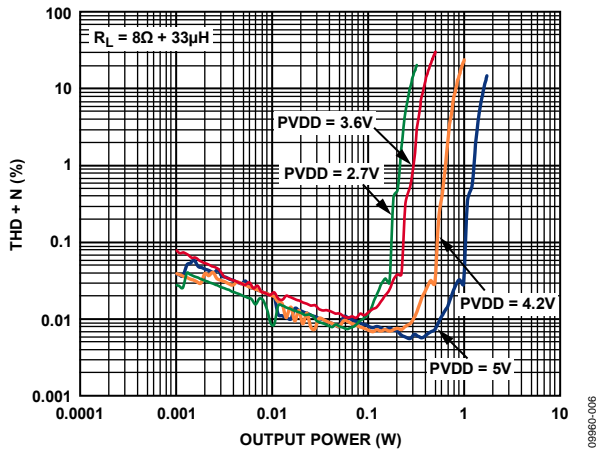


Figure 5. THD + N vs. Output Power into 8 Ω, Class-D Amplifier, Stereo Operation

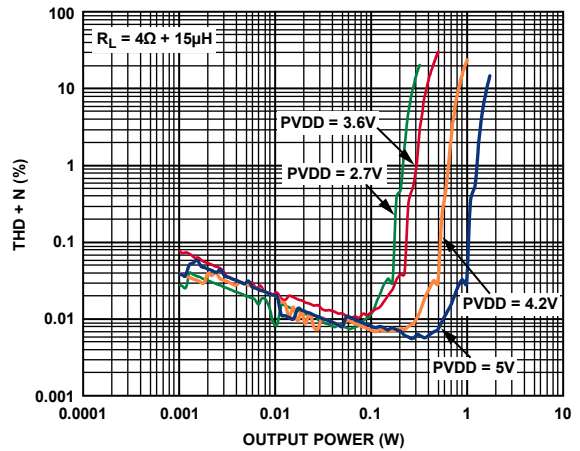


Figure 8. THD + N vs. Output Power into 4 Ω, Class-D Amplifier, Stereo Operation

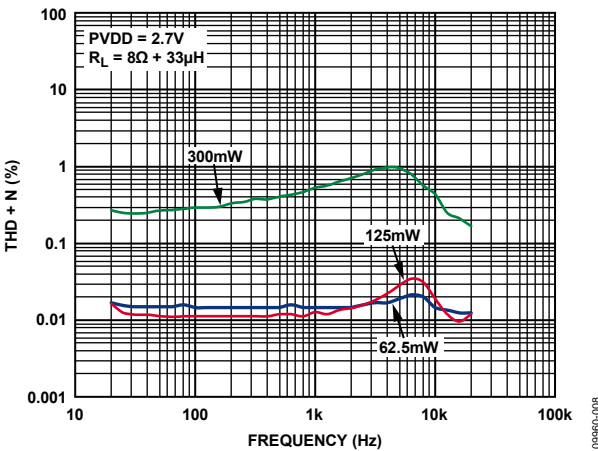


Figure 6. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 8 \Omega$ ,  $PVDD = 2.7 V$

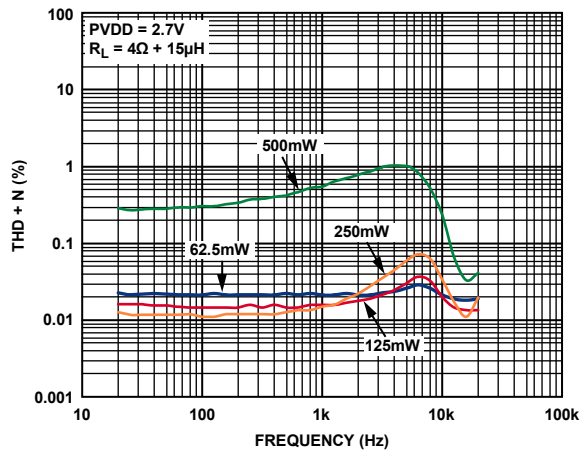


Figure 9. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 4 \Omega$ ,  $PVDD = 2.7 V$

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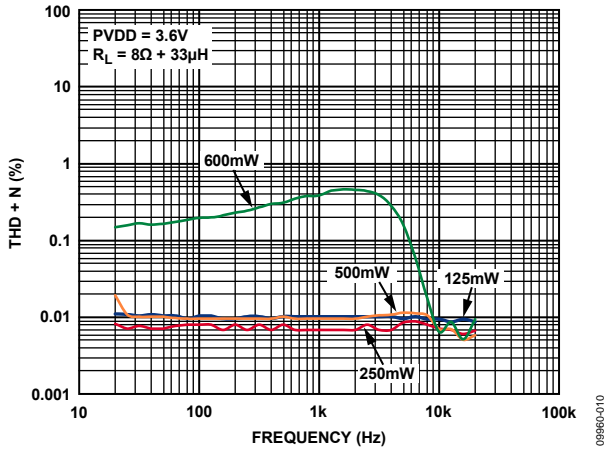


Figure 10. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 8 \Omega$ ,  $PVDD = 3.6 V$

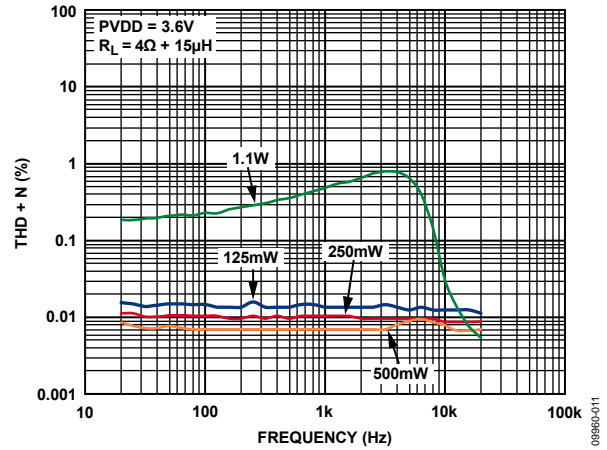


Figure 13. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 4 \Omega$ ,  $PVDD = 3.6 V$

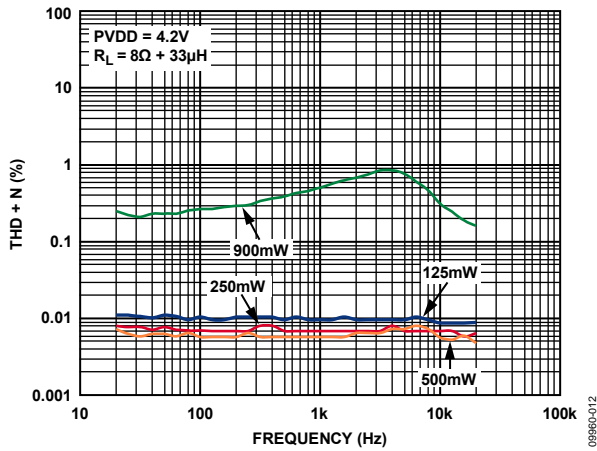


Figure 11. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 8 \Omega$ ,  $PVDD = 4.2 V$

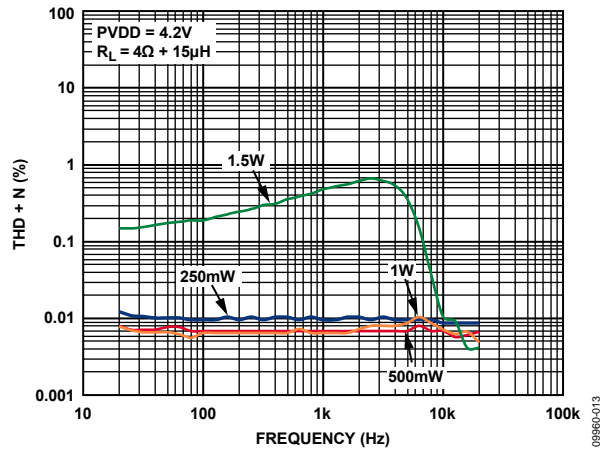


Figure 14. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 4 \Omega$ ,  $PVDD = 4.2 V$

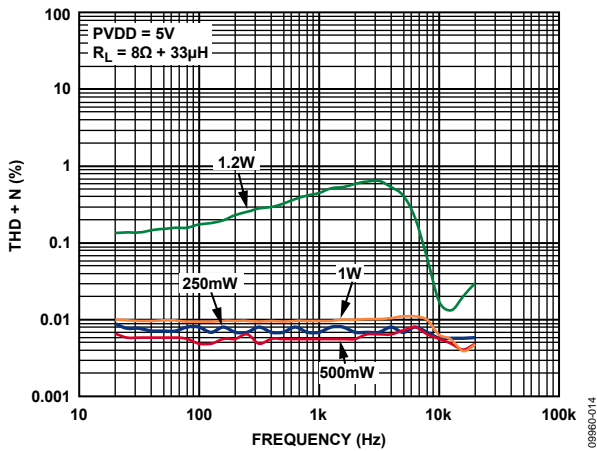


Figure 12. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 8 \Omega$ ,  $PVDD = 5.0 V$

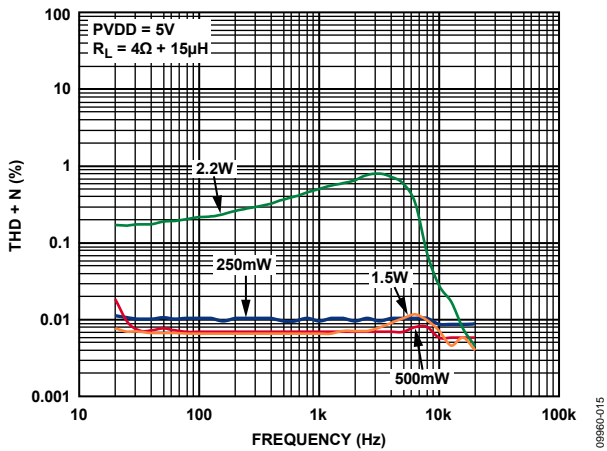


Figure 15. THD + N vs. Frequency, Class-D Amplifier, Mono Operation,  $R_L = 4 \Omega$ ,  $PVDD = 5.0 V$

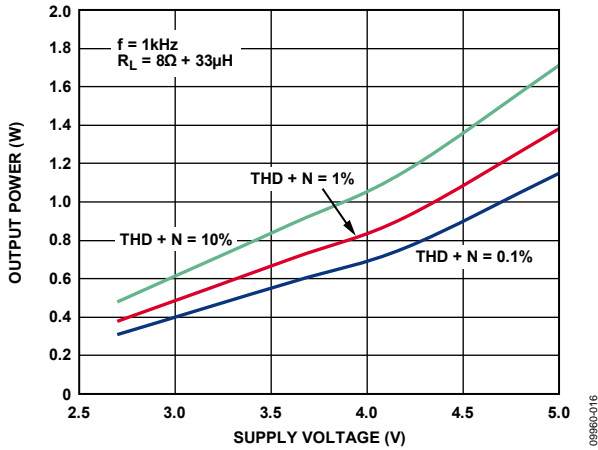


Figure 16. Output Power vs. Supply Voltage, Class-D Amplifier,  $R_L = 8 \Omega$

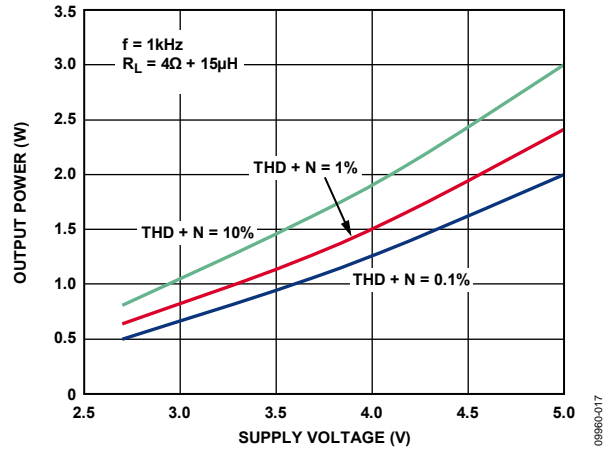


Figure 19. Output Power vs. Supply Voltage, Class-D Amplifier,  $R_L = 4 \Omega$

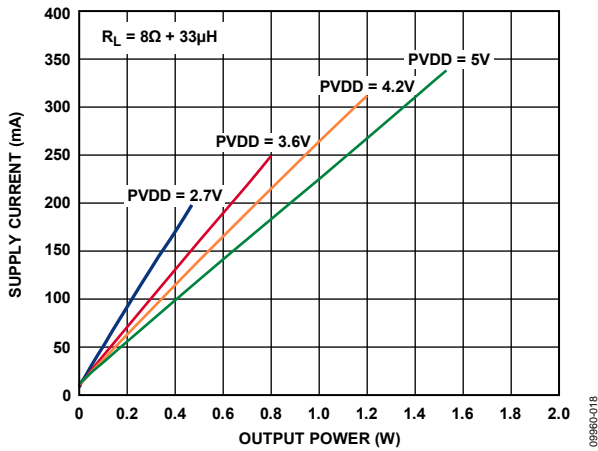


Figure 17. Supply Current vs. Output Power into  $8 \Omega$ , Class-D Amplifier

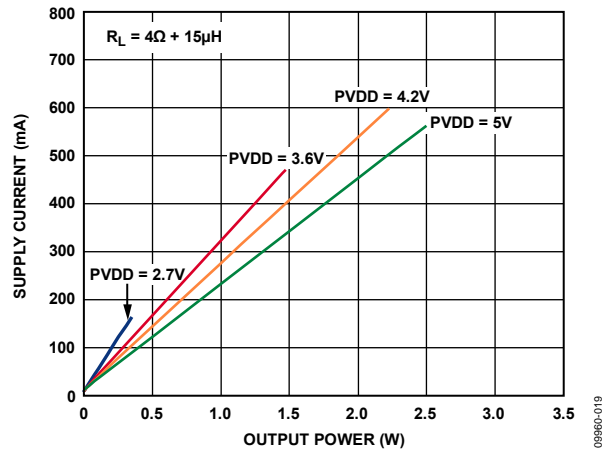


Figure 20. Supply Current vs. Output Power into  $4 \Omega$ , Class-D Amplifier

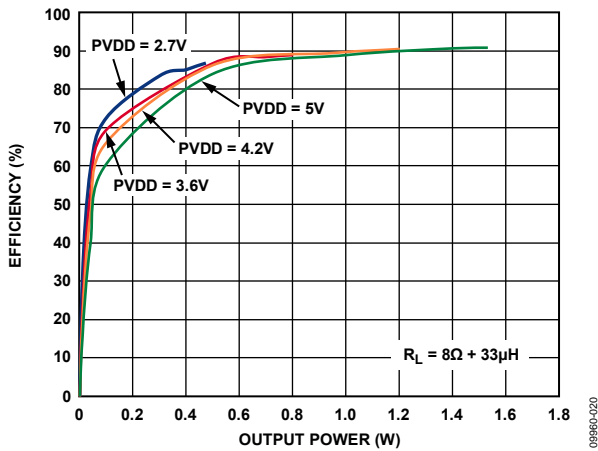


Figure 18. Efficiency vs. Output Power into  $8 \Omega$ , Class-D Amplifier

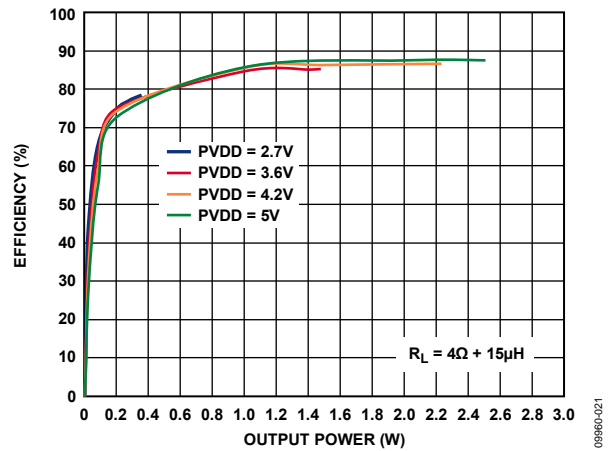


Figure 21. Efficiency vs. Output Power into  $4 \Omega$ , Class-D Amplifier

# SSM2804

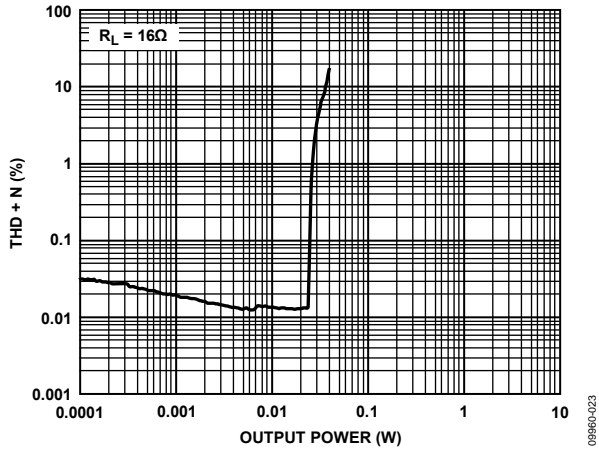


Figure 22. THD + N vs. Output Power into 16  $\Omega$ , Headphone Amplifier, Stereo Operation

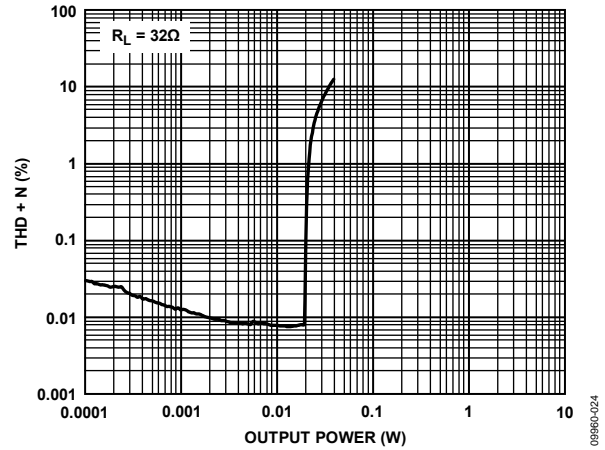


Figure 25. THD + N vs. Output Power into 32  $\Omega$ , Headphone Amplifier, Stereo Operation

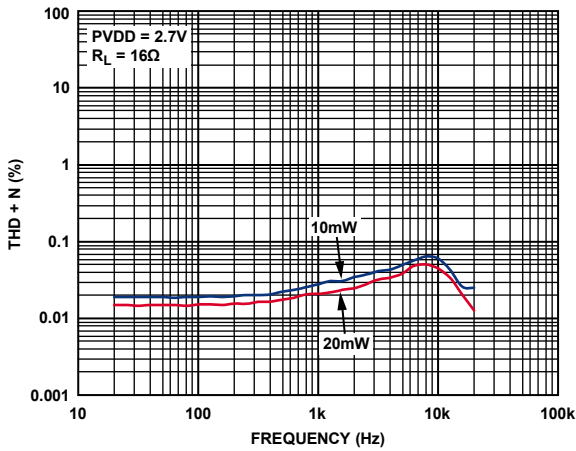


Figure 23. THD + N vs. Frequency, Headphone Amplifier,  $R_L = 16 \Omega$ ,  $PVDD = 2.7 V$

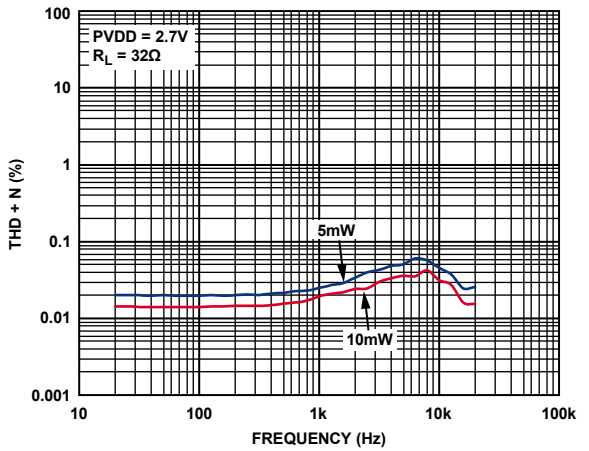


Figure 26. THD + N vs. Frequency, Headphone Amplifier,  $R_L = 32 \Omega$ ,  $PVDD = 2.7 V$

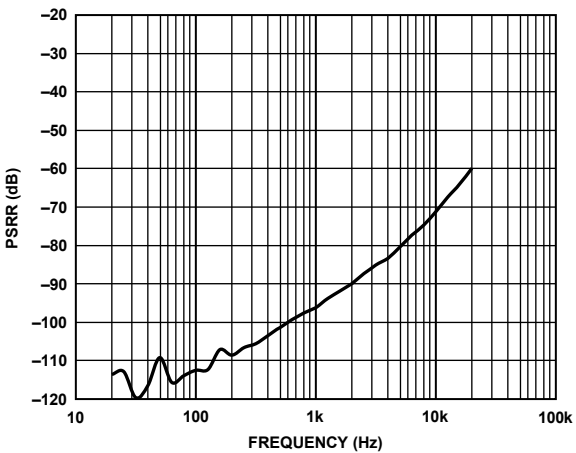


Figure 24. Power Supply Rejection Ratio (PSRR) vs. Frequency, Class-D Amplifier

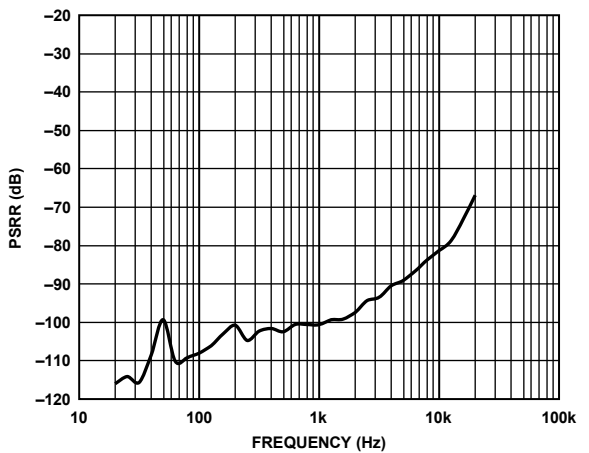


Figure 27. Power Supply Rejection Ratio (PSRR) vs. Frequency, Headphone Amplifier

## THEORY OF OPERATION

The **SSM2804** audio subsystem features a filterless modulation scheme that greatly reduces the external component count, conserving board space and, thus, reducing system cost. The **SSM2804** does not require an output filter but, instead, relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to fully recover the audio component of the square wave output.

Most Class-D amplifiers use some variation of pulse-width modulation (PWM), but the **SSM2804** uses  $\Sigma$ - $\Delta$  modulation to determine the switching pattern of the output devices, resulting in a number of important benefits.

- $\Sigma$ - $\Delta$  modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do.
- $\Sigma$ - $\Delta$  modulation provides the benefits of reducing the amplitude of spectral components at high frequencies, that is, reducing EMI emissions that might otherwise be radiated by speakers and long cable traces.
- The **SSM2804** does not require external EMI filtering for twisted speaker cable lengths shorter than 10 cm. If longer speaker cables are used, the **SSM2804** has emission limiting circuitry that allows significantly longer speaker cable.
- Due to the inherent spread-spectrum nature of  $\Sigma$ - $\Delta$  modulation, the need for modulator synchronization is eliminated for designs that incorporate multiple **SSM2804** amplifiers.

Using the I<sup>2</sup>C control interface, the gain of the **SSM2804** can be selected from a range of +12 dB to -63 dB in 32 steps. Other features accessed from the I<sup>2</sup>C interface include the following:

- Independent left/right channel shutdown
- Variable ultralow EMI emission limiting circuitry
- Automatic level control (ALC) for high quality speaker protection
- Stereo-to-mono mixing operation

The **SSM2804** also offers protection circuits for overcurrent and overtemperature protection.

### POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and, therefore, as not coming from the system input signal. Such transients may be generated when the amplifier system changes its operating mode. For example, the following may be sources of audible transients: system power-up and power-down, mute and unmute, input source change, and sample rate change.

The **SSM2804** has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

### OUTPUT MODULATION DESCRIPTION

The **SSM2804** uses three-level,  $\Sigma$ - $\Delta$  output modulation. Each output can swing from GND to  $V_{DD}$  and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to the constant presence of noise, a differential pulse is generated, when required, in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated.

Most of the time, however, the output differential voltage is 0 V, due to the Analog Devices, Inc., three-level,  $\Sigma$ - $\Delta$  output modulation. This feature ensures that the current flowing through the inductive load is small.

When the user wants to send an input signal, an output pulse (OUT+ and OUT-) is generated to follow the input voltage. The differential pulse density ( $V_{OUT}$ ) is increased by raising the input signal level. Figure 28 depicts three-level,  $\Sigma$ - $\Delta$  output modulation with and without input stimulus.

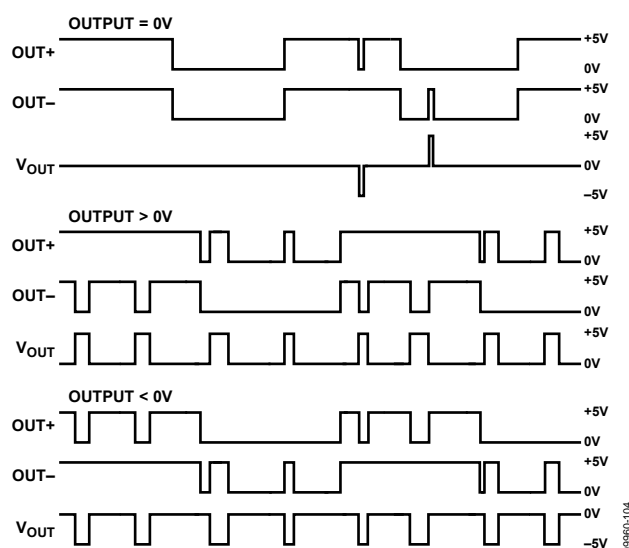


Figure 28. Three-Level,  $\Sigma$ - $\Delta$  Output Modulation With and Without Input Stimulus

# SSM2804

## HARDWARE-BASED HEADPHONE LIMITER

To provide fail-safe headphone level limiting independent of the register values sent to the amplifier over the I<sup>2</sup>C bus, the SSM2804 incorporates an optional hardware-based headphone limiter feature. The user controls the limiter level by supplying a voltage at the SD pin (see Table 7). The hardware limiter is activated by setting the LIM\_MODE bit to 0 in the additional control register (Bit D3 of Register 0x0E). After the desired limiter value is set, the user can lock the limiter setting by setting the LIMLOCK bit (Bit D7 of Register 0x0E).

**Table 7. Hardware Limiter Options**

| Limiter Level | Power into 32 Ω (mW) | Power into 16 Ω (mW) | SD Pin Voltage                    |
|---------------|----------------------|----------------------|-----------------------------------|
| Shutdown      | N/A                  | N/A                  | <0.87 V                           |
| ±0.40 V       | 2.5                  | 5                    | 0.87 V < V <sub>SD</sub> < 1.08 V |
| ±8 V          | 10                   | 20                   | 1.08 V < V <sub>SD</sub> < 1.29 V |
| ±1.13 V       | 20                   | 40                   | V <sub>SD</sub> > 1.29 V          |

Note that after the hardware limiter lock bit is set, the locked levels cannot be reset until the SSM2804 is powered down, the SD pin is strobed low, or all eight bits of the software reset register (Register 0x10) are set to 0.

In addition to the hardware-based limiter, several other limiter levels can be selected using the I<sup>2</sup>C-based limiter function (set the HPLIM bits of Register 0x0E; see Table 44). The effect of the limiter function on the headphone output is shown in Figure 29.

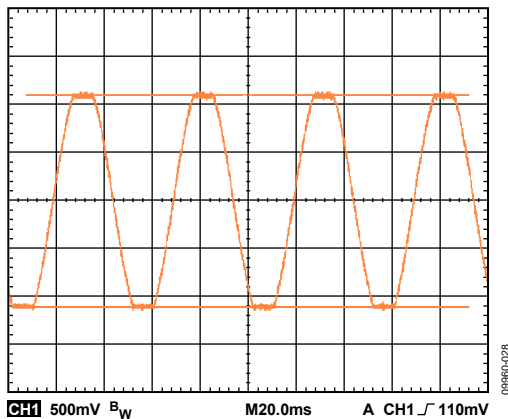


Figure 29. Limited Headphone Signal

## ACTIVATING OR DEACTIVATING THE EMISSION LIMITING CIRCUITRY

To activate or deactivate the emission limiting circuitry, change the value of the EDGE bits in the additional control register (Bits[D1:D0] of Register 0x0E). Four levels of emission control are available, allowing the user to determine the best trade-off between efficiency and EMI reduction.

In the default (fastest edge) mode, the user can pass FCC Class-B emission testing with 10 cm twisted pair speaker wire for loudspeaker connection. If longer speaker wire is desired, change the EDGE setting to a slower edge rate mode.

The trade-off is slightly lower efficiency and noise performance. The penalty for using the emission control circuitry is far less than the decreased performance observed when using a ferrite bead based EMI filter for emission limiting purposes.

## AUTOMATIC LEVEL CONTROL (ALC)

Automatic level control (ALC) is a function that automatically adjusts amplifier gain to generate the desired output amplitude with reference to a particular input stimulus. The primary use for the ALC is to protect an audio power amplifier or speaker load from the damaging effects of clipping or current overloading. This is accomplished by limiting the output amplitude of the amplifier upon reaching a preset threshold voltage. Another benefit of the ALC is that it makes sound sources with a wide dynamic range more intelligible by boosting low level signals and limiting very high level signals.

Before activating the ALC by setting the ALCEN bit (Bit D7 of Register 0x0B), the user has full control of the left and right channel PGA gain. After the ALC is activated (ALCEN = 1), the user has no control over the gain settings; the left channel PGA gain is locked into the device and controls the gain for both the left and right channels. To change the gain, the user must reset the ALCEN bit to 0 and then load the new gain settings.

Figure 30 shows the response of the SSM2804 to a linearly increasing input signal. When the output reaches the current threshold value, the amplifier gain decreases by 0.5 dB so that the output voltage remains under the threshold. As more attenuation is added to the system, the threshold increases according to a profile determined by the compressor setting bits in the ALC Control 2 register (Bits[D6:D5] of Register 0x0B), causing a rounded “knee” as the output voltage approaches the output limiter level. The effect of this compression curve is shown in Figure 30.

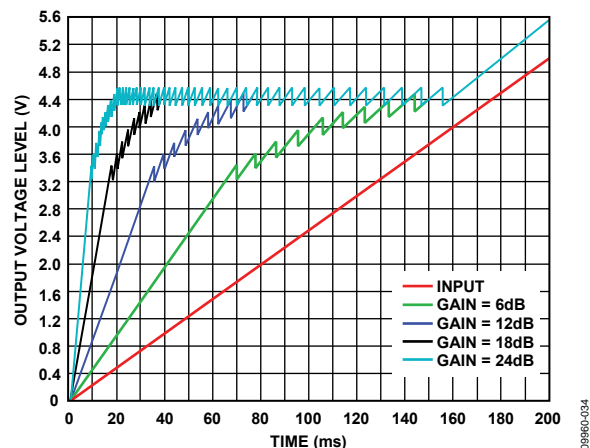


Figure 30. Output Response to Linearly Increasing Input Ramp Signal

When the input level is small and the output voltage is smaller than the ALC threshold value, the gain of the amplifier stays at the preset gain setting. When the input exceeds the ALC threshold value, the ALC gradually reduces the gain from the preset gain setting down to 1 dB.

### ALC Compression and Limiter Modes

The ALC implemented on the SSM2804 has two operation modes: compression mode and limiter mode. When the ALC is triggered for medium-level input signals, the ALC is in compression mode. In this mode, an increase of the output signal is one-third the increase of the input signal. For example, if the input signal increases by 3 dB, the ALC reduces the amplifier gain by 2 dB and, thus, the output signal increases by only 1 dB.

As the input signal becomes very large, the ALC transitions to limiter mode. In this mode, the output stays at a given threshold level,  $V_{TH}$ , even if the input signal grows larger. As an example of limiter mode operation, when a large input signal increases by 3 dB, the ALC reduces the amplifier gain by 3 dB and, thus, the output increases by 0 dB. When the amplifier gain is reduced to 1 dB, the ALC cannot reduce the gain further, and the output increases again. This is because the total range of the ALC operation has bottomed out due to extreme input voltage at high gain. To avoid potential speaker damage, the maximum input amplitude should not be large enough to exceed the maximum attenuation (to a level of 1 dB) of the limiter mode.

### Attack Time, Hold Time, and Release Time

When the amplifier input signal exceeds a preset threshold, the ALC reduces amplifier gain rapidly until the output voltage settles to a target level. This target level is maintained for a certain period. If the input voltage does not exceed the threshold again, the ALC increases the gain gradually.

The attack time is the time taken to reduce the gain from maximum to minimum. The hold time is the time that the reduced gain is maintained. The release time is the time taken to increase the gain from minimum to maximum. These times are shown in Table 8. The attack time and the release time can be set using the ALC 1 control register (Address 0x0A).

**Table 8. ALC Attack, Hold, and Release Times**

| Time <sup>1</sup> | Duration                             |
|-------------------|--------------------------------------|
| Attack Time       | 32 $\mu$ s to 4 ms (per 0.5 dB step) |
| Hold Time         | 90 ms to 120 ms                      |
| Release Time      | 4 ms to 512 ms (per 0.5 dB step)     |

<sup>1</sup> The attack time and release time can be adjusted using the I<sup>2</sup>C interface. The hold time cannot be adjusted.

### Soft-Knee Compression

Often performed using sophisticated DSP algorithms, soft-knee compression provides maximum sound quality with effective speaker protection. Instead of using a fixed compression setting prior to limiting, the SSM2804 allows for a much more subtle transition into limiting mode, preserving the original sound quality of the source audio. Figure 31 to Figure 33 show the various soft-knee compression settings that can be selected using the COMP bit settings (Bits[D6:D5] of Register 0x0B).

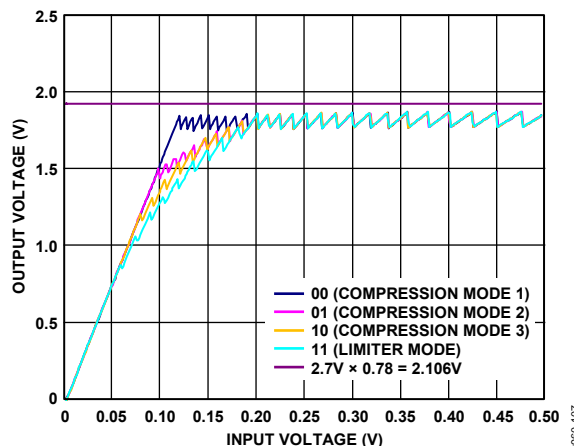


Figure 31. Adjustable Compression Settings, PVDD = 2.7 V, ALC Threshold Level = 78%

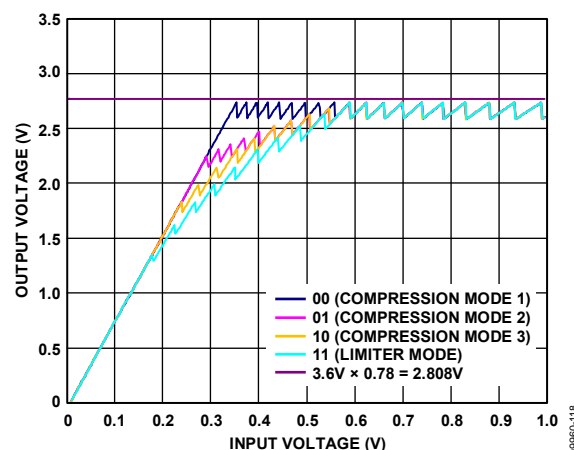


Figure 32. Adjustable Compression Settings, PVDD = 3.6 V, ALC Threshold Level = 78%

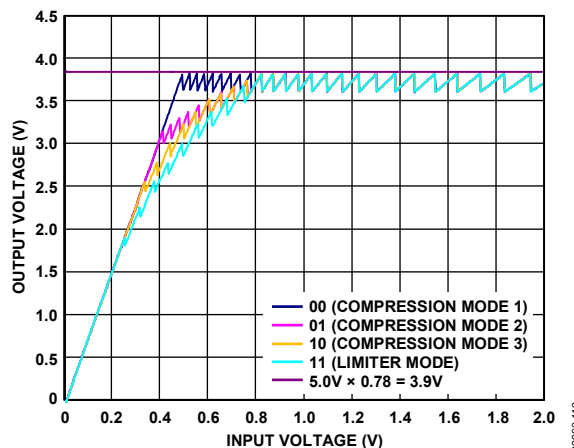


Figure 33. Adjustable Compression Settings, PVDD = 5.0 V, ALC Threshold Level = 78%

# SSM2804

## **ALC Soft Transition**

The ALC operation of the [SSM2804](#) incorporates techniques to reduce the audible artifacts associated with gain change transitions. First, the gain is changed in small increments of 0.5 dB. In addition to this small step size, the rate of gain change is reduced, proportional to the attack time setting. This feature drastically reduces and virtually eliminates the presence of zipper noise and other artifacts associated with gain transitions during ALC operation. Figure 34 shows the soft transition operation.

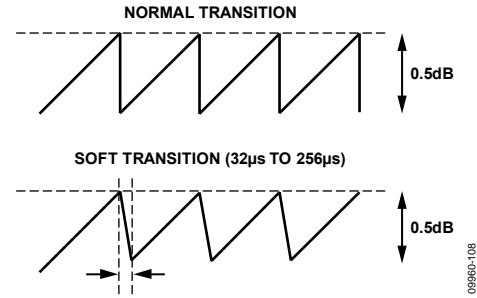


Figure 34. Soft Transition



# TYPICAL APPLICATION CIRCUITS

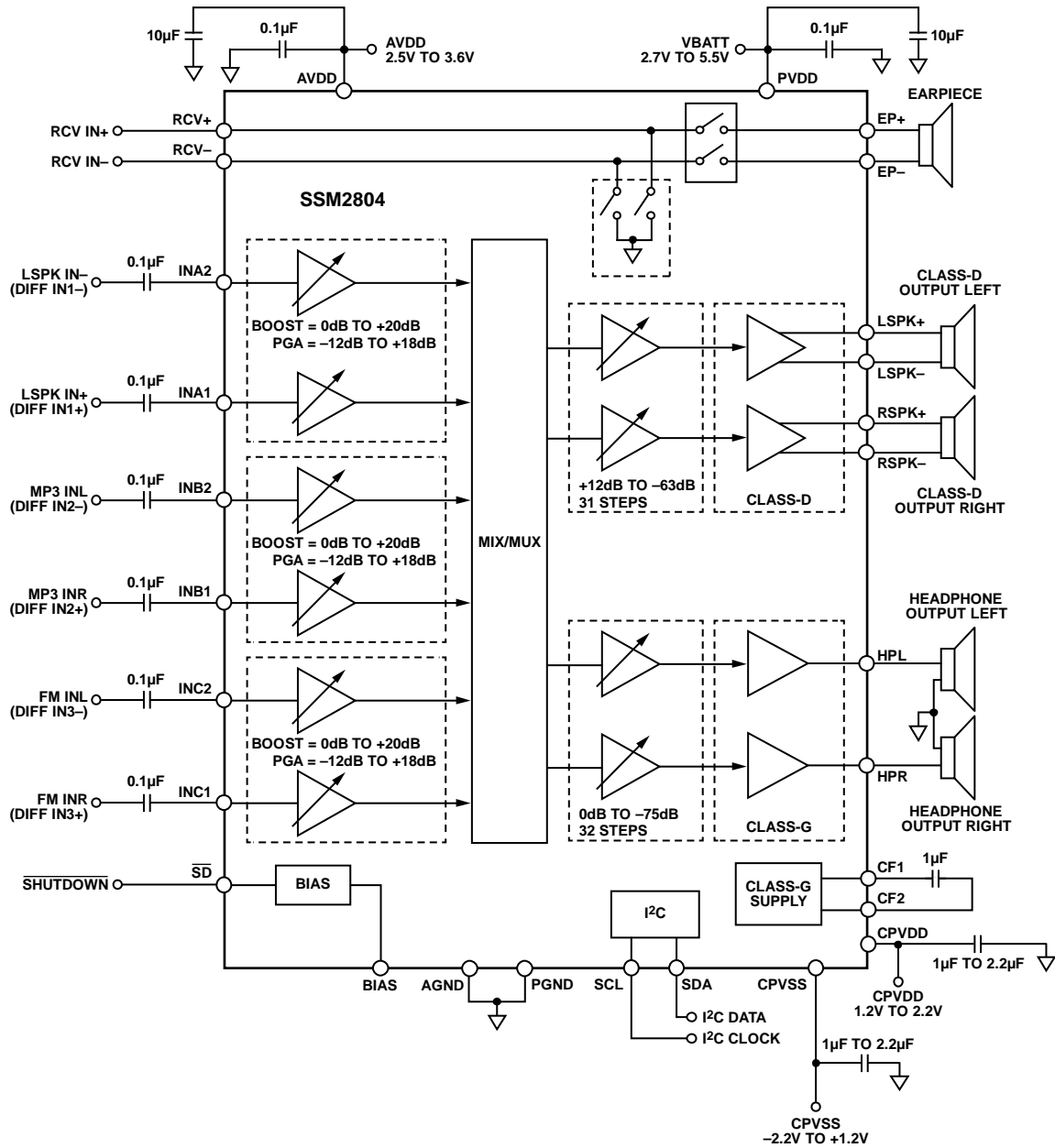
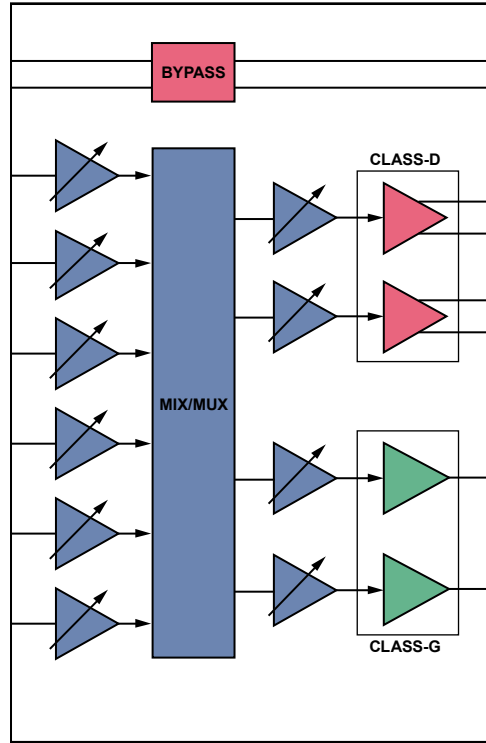


Figure 35. Application Circuit with External Components

09950-031



- 1.2V < CPVDD < +2.2V/-2.2V < CPVSS < -1.2V (INTERNALLY GENERATED)
- 2.7V < PVDD < 5V
- 2.5V < AVDD < 3.6V

09860-032

Figure 36. Power Supply Domains

## I<sup>2</sup>C SOFTWARE CONTROL INTERFACE

The I<sup>2</sup>C interface provides access to the user-selectable control registers and operates with a 2-wire interface.

Each control register consists of 16 bits, MSB first. Bits[B15:B9] are the register map address, and Bits[B8:B0] are the register data for the associated register map.

SDA generates the serial control data-word, and SCL clocks the serial data. The I<sup>2</sup>C bus address (Bits[A7:A1]) is 0x3B (01110110 for write and 01110111 for read). Bit A0 is the designated read/write bit.

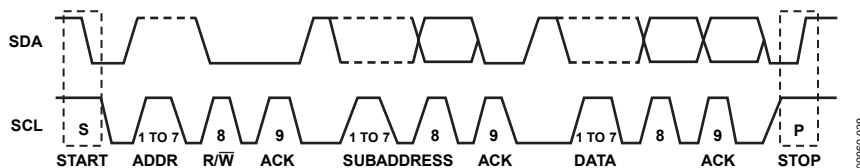
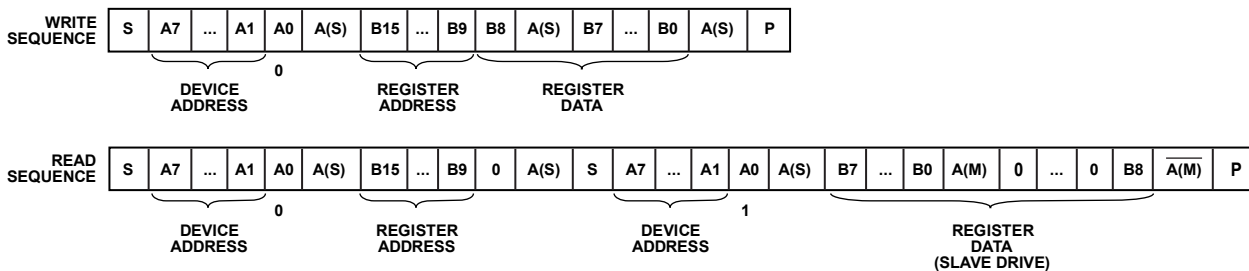


Figure 37. 2-Wire I<sup>2</sup>C Generalized Clocking Diagram



S/P = START/STOP BIT.  
 A0 = I<sup>2</sup>C R/W BIT.  
 A(S) = ACKNOWLEDGE BY SLAVE.  
 A(M) = ACKNOWLEDGE BY MASTER.  
 $\bar{A}(M)$  = ACKNOWLEDGE BY MASTER (INVERSION).

Figure 38. I<sup>2</sup>C Write and Read Sequences

# SSM2804

## REGISTER MAP

The 7-bit I<sup>2</sup>C address of the [SSM2804](#) is 0x3B (0111011).

**Table 9. Register Map**

| Address | Name                        | D7           | D6         | D5           | D4          | D3         | D2          | D1         | D0   | Default |
|---------|-----------------------------|--------------|------------|--------------|-------------|------------|-------------|------------|------|---------|
| 0x00    | Input mode                  | 0            | ZCD        | GAINMOD[2:0] |             |            | INMOD[2:0]  |            |      | 0x00    |
| 0x01    | INA volume                  | 0            | 0          | 0            | INAVOL[4:0] |            |             |            |      | 0x00    |
| 0x02    | INB volume                  | 0            | 0          | 0            | INBVOL[4:0] |            |             |            |      | 0x00    |
| 0x03    | INC volume                  | 0            | 0          | 0            | INCVOL[4:0] |            |             |            |      | 0x00    |
| 0x04    | Class-D left volume         | 0            | 0          | 0            | LCDVOL[4:0] |            |             |            |      | 0x00    |
| 0x05    | Class-D right volume        | 0            | 0          | 0            | RCDVOL[4:0] |            |             |            |      | 0x00    |
| 0x06    | LHP volume                  | 0            | 0          | 0            | LHPVOL[4:0] |            |             |            |      | 0x00    |
| 0x07    | RHP volume                  | 0            | 0          | 0            | RHPVOL[4:0] |            |             |            |      | 0x00    |
| 0x08    | HP input mixer              | POPTIME[1:0] |            | RHPMOD[2:0]  |             |            | LHPMOD[2:0] |            |      | 0x00    |
| 0x09    | Class-D input mixer         | CDSM[1:0]    |            | RCDMOD[2:0]  |             |            | LCDMOD[2:0] |            |      | 0x00    |
| 0x0A    | ALC Control 1               | 0            | 0          | RECTIME[2:0] |             |            | ATTIME[2:0] |            |      | 0x2B    |
| 0x0B    | ALC Control 2               | ALCEN        | COMP[1:0]  |              | ALCLV_FIX   | ALCLV[3:0] |             |            |      | 0x4B    |
| 0x0C    | ALC Control 3               | 0            | LCDBOOST   | RCDBOOST     | SOFTSTART   | SOFTCLIPEN | NGEN        | NGATE[1:0] |      | 0x00    |
| 0x0D    | Power-down control          | PASSPDB      | INCPDB     | INBPDB       | INAPDB      | RCDPDB     | LCDPDB      | HPPDB      | PWDB | 0x00    |
| 0x0E    | Additional control          | LIMLOCK      | HPLIM[2:0] |              |             | LIM_MOD    | TO          | EDGE[1:0]  |      | 0x00    |
| 0x0F    | Chip status <sup>1</sup>    | 0            | 0          | 0            | 0           | OCCD       | OCHP        | OW         | OT   | 0x00    |
| 0x10    | Software reset <sup>2</sup> | SOFTRESET    |            |              |             |            |             |            |      | 0x00    |

<sup>1</sup> This byte is read-only.

<sup>2</sup> This byte is write-only.

## REGISTER MAP DETAILS

### INPUT CHANNEL MODE CONTROL, ADDRESS 0x00

Table 10. Input Channel Mode Control Register Bit Map

| D7 | D6  | D5           | D4 | D3 | D2         | D1 | D0 |
|----|-----|--------------|----|----|------------|----|----|
| 0  | ZCD | GAINMOD[2:0] |    |    | INMOD[2:0] |    |    |

Table 11. Input Channel Mode Control Register Bit Descriptions

| Bit Name     | Description                | Settings   |
|--------------|----------------------------|--|
| ZCD          | Zero cross-detector enable | 0 = disable (default)<br>1 = enable  |
| GAINMOD[2:0] | Input amplifier gain mode  | xx0 = Input A PGA mode<br>xx1 = Input A boost mode<br>x0x = Input B PGA mode<br>x1x = Input B boost mode<br>0xx = Input C PGA mode<br>1xx = Input C boost mode   |
| INMOD[2:0]   | Input mode control         | xx0 = Input A stereo mode (INA1, INA2 > INAL, INAR)<br>xx1 = Input A differential mode (INA1, INA2 > INA+, INA-)<br>x0x = Input B stereo mode (INB1, INB2 > INBL, INBR)<br>x1x = Input B differential mode (INB1, INB2 > INB+, INB-)<br>0xx = Input C stereo mode (INC1, INC2 > INCL, INCR)<br>1xx = Input C differential mode (INC1, INC2 > INC+, INC-)<br>See Table 12 for complete information about the naming table |

Table 12. Input Mode Naming Table

| INMOD[2:0] | INA1 Pin | INA2 Pin | INB1 Pin | INB2 Pin | INC1 Pin | INC2 Pin |
|------------|----------|----------|----------|----------|----------|----------|
| 000        | INAL     | INAR     | INBL     | INBR     | INCL     | INCR     |
| 001        | INAL     | INAR     | INBL     | INBR     | INC+     | INC-     |
| 010        | INAL     | INAR     | INB+     | INB-     | INCL     | INCR     |
| 011        | INAL     | INAR     | INB+     | INB-     | INC+     | INC-     |
| 100        | INA+     | INA-     | INBL     | INBR     | INCL     | INCR     |
| 101        | INA+     | INA-     | INBL     | INBR     | INC+     | INC-     |
| 110        | INA+     | INA-     | INB+     | INB-     | INCL     | INCR     |
| 111        | INA+     | INA-     | INB+     | INB-     | INC+     | INC-     |

# SSM2804

## CHANNEL A LINE INPUT VOLUME, ADDRESS 0x01

Table 13. Channel A Line Input Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | INAVOL[4:0] |    |    |    |    |

Table 14. Channel A Line Input Volume Register Bit Descriptions

| Bit Name    | Description                           | Settings     |
|-------------|---------------------------------------|--------------|
| INAVOL[4:0] | Analog Channel A input volume control | See Table 15 |

Table 15. Descriptions of Channel A Volume Register Bits

| INAVOL[4:0] | PGA Mode (dB) | Boost Mode (dB) |
|-------------|---------------|-----------------|
| 00000       | Mute          | Mute            |
| 00001       | -12           | 0               |
| 00010       | -11           | 0               |
| 00011       | -10           | 0               |
| 00100       | -9            | 0               |
| 00101       | -8            | 0               |
| 00110       | -7            | 0               |
| 00111       | -6            | 0               |
| 01000       | -5            | 0               |
| 01001       | -4            | 0               |
| 01010       | -3            | 0               |
| 01011       | -2            | 0               |
| 01100       | -1            | 0               |
| 01101       | 0             | 0               |
| 01110       | 1             | 9               |
| 01111       | 2             | 9               |
| 10000       | 3             | 9               |
| 10001       | 4             | 9               |
| 10010       | 5             | 9               |
| 10011       | 6             | 9               |
| 10100       | 7             | 20              |
| 10101       | 8             | 20              |
| 10110       | 9             | 20              |
| 10111       | 10            | 20              |
| 11000       | 11            | 20              |
| 11001       | 12            | 20              |
| 11010       | 13            | 20              |
| 11011       | 14            | 20              |
| 11100       | 15            | 20              |
| 11101       | 16            | 20              |
| 11110       | 17            | 20              |
| 11111       | 18            | 20              |

**CHANNEL B LINE INPUT VOLUME, ADDRESS 0x02**

Table 16. Channel B Line Input Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | INBVOL[4:0] |    |    |    |    |

Table 17. Channel B Line Input Volume Register Bit Descriptions

| Bit Name    | Description                           | Settings     |
|-------------|---------------------------------------|--------------|
| INBVOL[4:0] | Analog Channel B input volume control | See Table 18 |

Table 18. Descriptions of Channel B Input Volume Register Bits

| INBVOL[4:0] | PGA Mode (dB) | Boost Mode (dB) |
|-------------|---------------|-----------------|
| 00000       | Mute          | Mute            |
| 00001       | -12           | 0               |
| 00010       | -11           | 0               |
| 00011       | -10           | 0               |
| 00100       | -9            | 0               |
| 00101       | -8            | 0               |
| 00110       | -7            | 0               |
| 00111       | -6            | 0               |
| 01000       | -5            | 0               |
| 01001       | -4            | 0               |
| 01010       | -3            | 0               |
| 01011       | -2            | 0               |
| 01100       | -1            | 0               |
| 01101       | 0             | 0               |
| 01110       | 1             | 9               |
| 01111       | 2             | 9               |
| 10000       | 3             | 9               |
| 10001       | 4             | 9               |
| 10010       | 5             | 9               |
| 10011       | 6             | 9               |
| 10100       | 7             | 20              |
| 10101       | 8             | 20              |
| 10110       | 9             | 20              |
| 10111       | 10            | 20              |
| 11000       | 11            | 20              |
| 11001       | 12            | 20              |
| 11010       | 13            | 20              |
| 11011       | 14            | 20              |
| 11100       | 15            | 20              |
| 11101       | 16            | 20              |
| 11110       | 17            | 20              |
| 11111       | 18            | 20              |

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## CHANNEL C LINE INPUT VOLUME, ADDRESS 0x03

Table 19. Channel C Line Input Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | INCVOL[4:0] |    |    |    |    |

Table 20. Channel C Line Input Volume Register Bit Descriptions

| Bit Name    | Description                           | Settings     |
|-------------|---------------------------------------|--------------|
| INCVOL[4:0] | Analog Channel C input volume control | See Table 21 |

Table 21. Descriptions of Channel C Input Volume Register Bits

| INCVOL[4:0] | PGA Mode (dB) | Boost Mode (dB) |
|-------------|---------------|-----------------|
| 00000       | Mute          | Mute            |
| 00001       | -12           | 0               |
| 00010       | -11           | 0               |
| 00011       | -10           | 0               |
| 00100       | -9            | 0               |
| 00101       | -8            | 0               |
| 00110       | -7            | 0               |
| 00111       | -6            | 0               |
| 01000       | -5            | 0               |
| 01001       | -4            | 0               |
| 01010       | -3            | 0               |
| 01011       | -2            | 0               |
| 01100       | -1            | 0               |
| 01101       | 0             | 0               |
| 01110       | 1             | 9               |
| 01111       | 2             | 9               |
| 10000       | 3             | 9               |
| 10001       | 4             | 9               |
| 10010       | 5             | 9               |
| 10011       | 6             | 9               |
| 10100       | 7             | 20              |
| 10101       | 8             | 20              |
| 10110       | 9             | 20              |
| 10111       | 10            | 20              |
| 11000       | 11            | 20              |
| 11001       | 12            | 20              |
| 11010       | 13            | 20              |
| 11011       | 14            | 20              |
| 11100       | 15            | 20              |
| 11101       | 16            | 20              |
| 11110       | 17            | 20              |
| 11111       | 18            | 20              |



**CLASS-D LEFT LOUDSPEAKER OUTPUT VOLUME, ADDRESS 0x04**

Table 22. Class-D Left Loudspeaker Output Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | LCDVOL[4:0] |    |    |    |    |

Table 23. Class-D Left Loudspeaker Output Volume Register Bit Descriptions

| Bit Name    | Description                         | Settings   |
|-------------|-------------------------------------|--|
| LCDVOL[4:0] | Left channel Class-D volume control | 00000 = mute (default)<br>00001 = -75 dB<br>00010 = -71 dB<br>00011 = -67 dB<br>00100 = -63 dB<br>00101 = -59 dB<br>00110 = -55 dB<br>00111 = -51 dB<br>01000 = -47 dB<br>01001 = -44 dB<br>01010 = -41 dB<br>01011 = -38 dB<br>01100 = -35 dB<br>01101 = -32 dB<br>01110 = -29 dB<br>01111 = -26 dB<br>10000 = -23 dB<br>10001 = -21 dB<br>10010 = -19 dB<br>10011 = -17 dB<br>10100 = -15 dB<br>10101 = -13 dB<br>10110 = -11 dB<br>10111 = -9 dB<br>11000 = -7 dB<br>11001 = -6 dB<br>11010 = -5 dB<br>11011 = -4 dB<br>11100 = -3 dB<br>11101 = -2 dB<br>11110 = -1 dB<br>11111 = 0 dB |

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## CLASS-D RIGHT LOUDSPEAKER OUTPUT VOLUME, ADDRESS 0x05

Table 24. Class-D Right Loudspeaker Output Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | RCDVOL[4:0] |    |    |    |    |

Table 25. Class-D Right Loudspeaker Output Volume Register Bit Descriptions

| Bit Name    | Description                          | Settings   |
|-------------|--------------------------------------|--|
| RCDVOL[4:0] | Right channel Class-D volume control | 00000 = mute (default)<br>00001 = -75 dB<br>00010 = -71 dB<br>00011 = -67 dB<br>00100 = -63 dB<br>00101 = -59 dB<br>00110 = -55 dB<br>00111 = -51 dB<br>01000 = -47 dB<br>01001 = -44 dB<br>01010 = -41 dB<br>01011 = -38 dB<br>01100 = -35 dB<br>01101 = -32 dB<br>01110 = -29 dB<br>01111 = -26 dB<br>10000 = -23 dB<br>10001 = -21 dB<br>10010 = -19 dB<br>10011 = -17 dB<br>10100 = -15 dB<br>10101 = -13 dB<br>10110 = -11 dB<br>10111 = -9 dB<br>11000 = -7 dB<br>11001 = -6 dB<br>11010 = -5 dB<br>11011 = -4 dB<br>11100 = -3 dB<br>11101 = -2 dB<br>11110 = -1 dB<br>11111 = 0 dB |

**LEFT HEADPHONE OUTPUT VOLUME, ADDRESS 0x06**

Table 26. Left Headphone Output Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | LHPVOL[4:0] |    |    |    |    |

Table 27. Left Headphone Output Volume Register Bit Descriptions

| Bit Name    | Description                          | Settings   |
|-------------|--------------------------------------|--|
| LHPVOL[4:0] | Left headphone output volume control | 00000 = mute (default)<br>00001 = -75 dB<br>00010 = -71 dB<br>00011 = -67 dB<br>00100 = -63 dB<br>00101 = -59 dB<br>00110 = -55 dB<br>00111 = -51 dB<br>01000 = -47 dB<br>01001 = -44 dB<br>01010 = -41 dB<br>01011 = -38 dB<br>01100 = -35 dB<br>01101 = -32 dB<br>01110 = -29 dB<br>01111 = -26 dB<br>10000 = -23 dB<br>10001 = -21 dB<br>10010 = -19 dB<br>10011 = -17 dB<br>10100 = -15 dB<br>10101 = -13 dB<br>10110 = -11 dB<br>10111 = -9 dB<br>11000 = -7 dB<br>11001 = -6 dB<br>11010 = -5 dB<br>11011 = -4 dB<br>11100 = -3 dB<br>11101 = -2 dB<br>11110 = -1 dB<br>11111 = 0 dB |

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## RIGHT HEADPHONE OUTPUT VOLUME, ADDRESS 0x07

Table 28. Right Headphone Output Volume Register Bit Map

| D7 | D6 | D5 | D4          | D3 | D2 | D1 | D0 |
|----|----|----|-------------|----|----|----|----|
| 0  | 0  | 0  | RHPVOL[4:0] |    |    |    |    |

Table 29. Right Headphone Output Volume Register Bit Descriptions

| Bit Name    | Description                           | Settings   |
|-------------|---------------------------------------|--|
| RHPVOL[4:0] | Right headphone output volume control | 00000 = mute (default)<br>00001 = -75 dB<br>00010 = -71 dB<br>00011 = -67 dB<br>00100 = -63 dB<br>00101 = -59 dB<br>00110 = -55 dB<br>00111 = -51 dB<br>01000 = -47 dB<br>01001 = -44 dB<br>01010 = -41 dB<br>01011 = -38 dB<br>01100 = -35 dB<br>01101 = -32 dB<br>01110 = -29 dB<br>01111 = -26 dB<br>10000 = -23 dB<br>10001 = -21 dB<br>10010 = -19 dB<br>10011 = -17 dB<br>10100 = -15 dB<br>10101 = -13 dB<br>10110 = -11 dB<br>10111 = -9 dB<br>11000 = -7 dB<br>11001 = -6 dB<br>11010 = -5 dB<br>11011 = -4 dB<br>11100 = -3 dB<br>11101 = -2 dB<br>11110 = -1 dB<br>11111 = 0 dB |

**HEADPHONE INPUT MIXER CONTROL, ADDRESS 0x08****Table 30. Headphone Input Mixer Control Register Bit Map**

| D7           | D6 | D5          | D4 | D3 | D2          | D1 | D0 |
|--------------|----|-------------|----|----|-------------|----|----|
| POPTIME[1:0] |    | RHPMOD[2:0] |    |    | LHPMOD[2:0] |    |    |

**Table 31. Headphone Input Mixer Control Register Bit Descriptions**

| Bit Name     | Description                             | Settings  |
|--------------|---|---|
| POPTIME[1:0] | Headphone turn-on time constant setting | 00 = 10 ms (default)<br>01 = 20 ms<br>10 = 40 ms<br>11 = 80 ms (smallest pop-and-click)   |
| RHPMOD[2:0]  | Right headphone input mixer             | xx0 = Analog Input A disabled (default)<br>xx1 = Analog Input A enabled<br>x0x = Analog Input B disabled (default)<br>x1x = Analog Input B enabled<br>0xx = Analog Input C disabled (default)<br>1xx = Analog Input C enabled |
| LHPMOD[2:0]  | Left headphone input mixer              | xx0 = Analog Input A disabled (default)<br>xx1 = Analog Input A enabled<br>x0x = Analog Input B disabled (default)<br>x1x = Analog Input B enabled<br>0xx = Analog Input C disabled (default)<br>1xx = Analog Input C enabled |

**CLASS-D INPUT MIXER CONTROL, ADDRESS 0x09****Table 32. Class-D Input Mixer Control Register Bit Map**

| D7        | D6 | D5          | D4 | D3 | D2          | D1 | D0 |
|-----------|----|-------------|----|----|-------------|----|----|
| CDSM[1:0] |    | RCDMOD[2:0] |    |    | LCDMOD[2:0] |    |    |

**Table 33. Class-D Input Mixer Control Register Bit Descriptions**

| Bit Name    | Description                      | Settings  |
|-------------|----------------------------------|---|
| CDSM[1:0]   | Class-D stereo/mono mode control | x0 = left channel disabled (default)<br>x1 = left channel enabled (left and right)<br>0x = right channel disabled (default)<br>1x = right channel enabled (left and right)  |
| RCDMOD[2:0] | Right Class-D input mixer        | xx0 = Analog Input A disabled (default)<br>xx1 = Analog Input A enabled<br>x0x = Analog Input B disabled (default)<br>x1x = Analog Input B enabled<br>0xx = Analog Input C disabled (default)<br>1xx = Analog Input C enabled |
| LCDMOD[2:0] | Left Class-D input mixer         | xx0 = Analog Input A disabled (default)<br>xx1 = Analog Input A enabled<br>x0x = Analog Input B disabled (default)<br>x1x = Analog Input B enabled<br>0xx = Analog Input C disabled (default)<br>1xx = Analog Input C enabled |

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## ALC CONTROL 1, ADDRESS 0x0A

Table 34. ALC Control 1 Register Bit Map

| D7 | D6 | D5           | D4 | D3 | D2          | D1 | D0 |
|----|----|--------------|----|----|-------------|----|----|
| 0  | 0  | RECTIME[2:0] |    |    | ATTIME[2:0] |    |    |

Table 35. ALC Control 1 Register Bit Descriptions

| Bit Name     | Description      | Settings   |
|--------------|------------------|--|
| RECTIME[2:0] | ALC release rate | 000 = 4 ms per 0.5 dB step (6 dB/48 ms)<br>001 = 8 ms<br>010 = 16 ms<br>011 = 32 ms<br>100 = 64 ms<br>101 = 128 ms (default)<br>110 = 256 ms<br>111 = 512 ms                               |
| ATTIME[2:0]  | ALC attack rate  | 000 = 32 $\mu$ s per 0.5 dB step (6 dB/384 $\mu$ s)<br>001 = 64 $\mu$ s<br>010 = 128 $\mu$ s<br>011 = 256 $\mu$ s (default)<br>100 = 512 $\mu$ s<br>101 = 1 ms<br>110 = 2 ms<br>111 = 4 ms |

**ALC CONTROL 2, ADDRESS 0x0B**

Table 36. ALC Control 2 Register Bit Map

| D7    | D6        | D5 | D4        | D3         | D2 | D1 | D0 |
|-------|-----------|----|-----------|------------|----|----|----|
| ALCEN | COMP[1:0] |    | ALCLV_FIX | ALCLV[3:0] |    |    |    |

Table 37. ALC Control 2 Register Bit Descriptions

| Bit Name   | Description   | Settings  |
|------------|---|---|
| ALCEN      | ALC enable  | 0 = ALC disabled (default)<br>1 = ALC enabled   |
| COMP[1:0]  | Compressor setting (see the Soft-Knee Compression section for more information) | 00 = Compression Mode 1 (1:4 to 1:∞)<br>01 = Compression Mode 2 (1:1.7 to 1:4 to 1:∞)<br>10 = Compression Mode 3 (1:1.3 to 1:2.5 to 1:∞)<br>11 = Limiter mode (1:∞) |
| ALCLV_FIX  | ALC threshold mode setting  | 0 = supply tracking (threshold is a constant fraction of supply voltage)<br>1 = fixed power (threshold is a fixed voltage)  |
| ALCLV[3:0] | ALC threshold level setting   | See Table 38  |

Table 38. ALC Threshold Levels

| ALCLV[3:0] Value | Supply Tracking Threshold (% of PVDD) | Fixed Power Threshold (V) |
|------------------|---------------------------------------|---------------------------|
|                  | (ALCLV_FIX = 0)                       | (ALCLV_FIX = 1)           |
| 0000             | 65                                    | 2.74                      |
| 0001             | 67                                    | 2.89                      |
| 0010             | 69                                    | 3.04                      |
| 0011             | 72                                    | 3.19                      |
| 0100             | 75                                    | 3.34                      |
| 0101             | 78                                    | 3.50                      |
| 0110             | 81                                    | 3.65                      |
| 0111             | 85                                    | 3.80                      |
| 1000             | 88                                    | 3.95                      |
| 1001             | 93                                    | 4.10                      |
| 1010             | 97                                    | 4.25                      |
| 1011             | 102                                   | 4.40                      |
| 1100             | 108                                   | 4.56                      |
| 1101             | 114                                   | 4.71                      |
| 1110             | 122                                   | 4.86                      |
| 1111             | 130                                   | 5.01                      |

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## ALC CONTROL 3, ADDRESS 0x0C

Table 39. ALC Control 3 Register Bit Map

| D7 | D6       | D5       | D4        | D3         | D2   | D1         | D0 |
|----|----------|----------|-----------|------------|------|------------|----|
| 0  | LCDBOOST | RCDBOOST | SOFTSTART | SOFTCLIPEN | NGEN | NGATE[1:0] |    |

Table 40. ALC Control 3 Register Bit Descriptions

| Bit Name   | Description                      | Settings  |
|------------|----------------------------------|---|
| LCDBOOST   | Left channel Class-D gain boost  | 0 = 0 dB (default)<br>1 = +6 dB boost                       |
| RCDBOOST   | Right channel Class-D gain boost | 0 = 0 dB (default)<br>1 = +6 dB boost                       |
| SOFTSTART  | Soft start enable                | 0 = soft start disabled (default)<br>1 = soft start enabled |
| SOFTCLIPEN | Soft clip enable                 | 0 = soft clip disabled (default)<br>1 = soft clip enabled   |
| NGEN       | Noise gate enable                | 0 = noise gate disabled (default)<br>1 = noise gate enabled |
| NGATE[1:0] | Noise gate level                 | 00 = 2 mV (default)<br>01 = 4 mV<br>10 = 8 mV<br>11 = 16 mV |

## POWER-DOWN CONTROL, ADDRESS 0x0D

Table 41. Power-Down Control Register Bit Map

| D7      | D6     | D5     | D4     | D3     | D2     | D1    | D0   |
|---------|--------|--------|--------|--------|--------|-------|------|
| PASSPDB | INCPDB | INBPDB | INAPDB | RCDPDB | LCDPDB | HPPDB | PWDB |

Table 42. Power-Down Control Register Bit Descriptions

| Bit Name | Description                      | Settings                                 |
|----------|----------------------------------|--|
| PASSPDB  | Passive switch power-down        | 0 = power down (default)<br>1 = power up |
| INCPDB   | Input Channel C power-down       | 0 = power down (default)<br>1 = power up |
| INBPDB   | Input Channel B power-down       | 0 = power down (default)<br>1 = power up |
| INAPDB   | Input Channel A power-down       | 0 = power down (default)<br>1 = power up |
| RCDPDB   | Class-D right channel power-down | 0 = power down (default)<br>1 = power up |
| LCDPDB   | Class-D left channel power-down  | 0 = power down (default)<br>1 = power up |
| HPPDB    | Headphone power-down             | 0 = power down (default)<br>1 = power up |
| PWDB     | System power-down                | 0 = power down (default)<br>1 = power up |



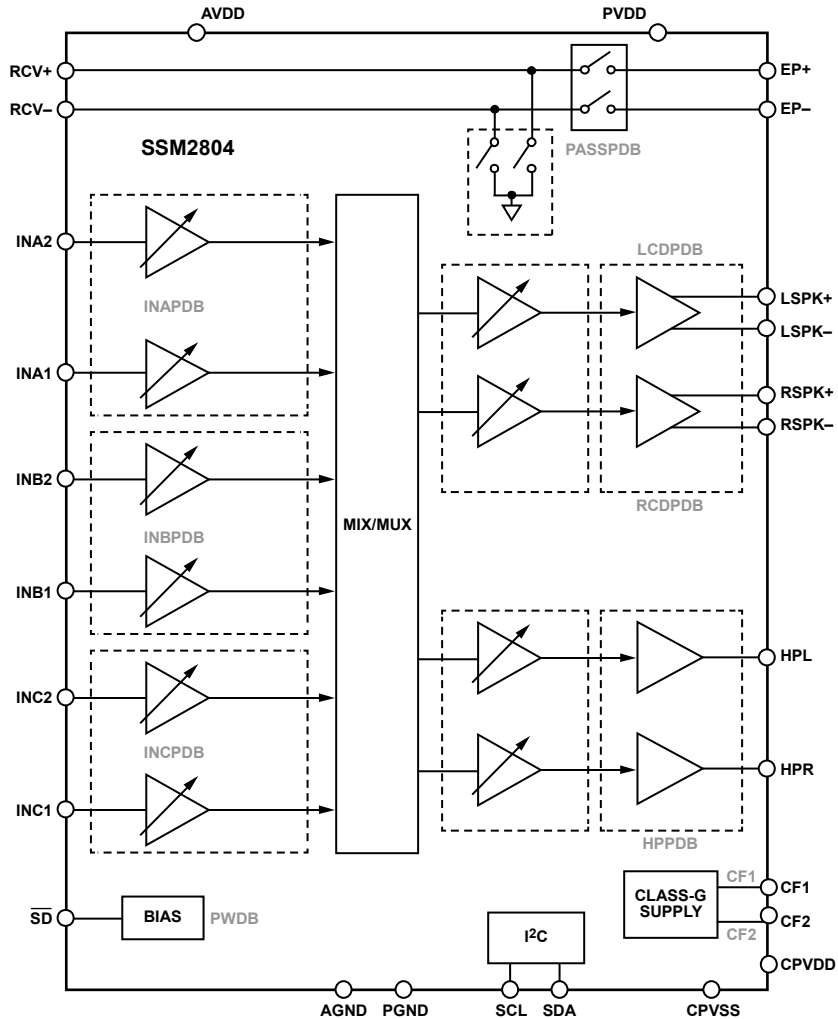


Figure 39. Power Management Control Register Blocks

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## ADDITIONAL CONTROL, ADDRESS 0x0E

Table 43. Additional Control Register Bit Map

| D7      | D6         | D5 | D4 | D3       | D2 | D1        | D0 |
|---------|------------|----|----|----------|----|-----------|----|
| LIMLOCK | HPLIM[2:0] |    |    | LIM_MODE | TO | EDGE[1:0] |    |

Table 44. Additional Control Register Bit Descriptions

| Bit Name   | Description  | Settings  |
|------------|--|---|
| LIMLOCK    | Headphone limiter lock bit. After the limiter is locked, the locked levels cannot be reset until the SSM2804 is powered down, the $\overline{SD}$ pin is strobed low, or all eight bits of the software reset register (Register 0x10) are set to 0. | 0 = disable (default)<br>1 = enable   |
| HPLIM[2:0] | Headphone limiter level adjust.  | 000 = off (default)<br>001 = $\pm 1.13$ V<br>010 = $\pm 0.98$ V<br>011 = $\pm 0.80$ V<br>100 = $\pm 0.57$ V<br>101 = $\pm 0.40$ V<br>110 = $\pm 0.28$ V<br>111 = $\pm 0.22$ V |
| LIM_MODE   | Headphone limiter mode selection.  | 0 = hardware mode (external resistor limiter via $\overline{SD}$ pin; default)<br>1 = software mode (I <sup>2</sup> C adjustable limiter)                                     |
| TO         | Timeout control.   | 0 = 30 ms (default)<br>1 = 60 ms  |
| EDGE[1:0]  | Class-D output stage edge control.   | 00 = normal mode (default)<br>01 = slow edge<br>10 = slower edge (PVDD > 3.0 V recommended)<br>11 = slowest edge (PVDD > 4.0 V recommended)                                   |

**CHIP STATUS REGISTER, ADDRESS 0x0F**

This register is read-only.

**Table 45. Chip Status Register Bit Map**

| D7 | D6 | D5 | D4 | D3   | D2   | D1 | D0 |
|----|----|----|----|------|------|----|----|
| 0  | 0  | 0  | 0  | OCCD | OCHP | OW | OT |

**Table 46. Chip Status Register Bit Descriptions**

| Bit Name | Description                              | Settings                                   |
|----------|--|--|
| OCCD     | Overcurrent for Class-D                  | 0 = normal<br>1 = overcurrent              |
| OCHP     | Overcurrent for headphone                | 0 = normal<br>1 = overcurrent              |
| OW       | Overtemperature warning                  | 0 = normal<br>1 = overtemperature warning  |
| OT       | Overtemperature error (thermal shutdown) | 0 = normal<br>1 = overtemperature shutdown |

**SOFTWARE RESET REGISTER, ADDRESS 0x10**

This register is write-only.

**Table 47. Software Reset Register Bit Map**

| D7        | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-----------|----|----|----|----|----|----|----|
| SOFTRESET |    |    |    |    |    |    |    |

**Table 48. Software Reset Register Bit Descriptions**

| Bit Name  | Description    | Settings                  |
|-----------|----------------|---------------------------|
| SOFTRESET | Software reset | 00000000 = software reset |

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## OUTLINE DIMENSIONS

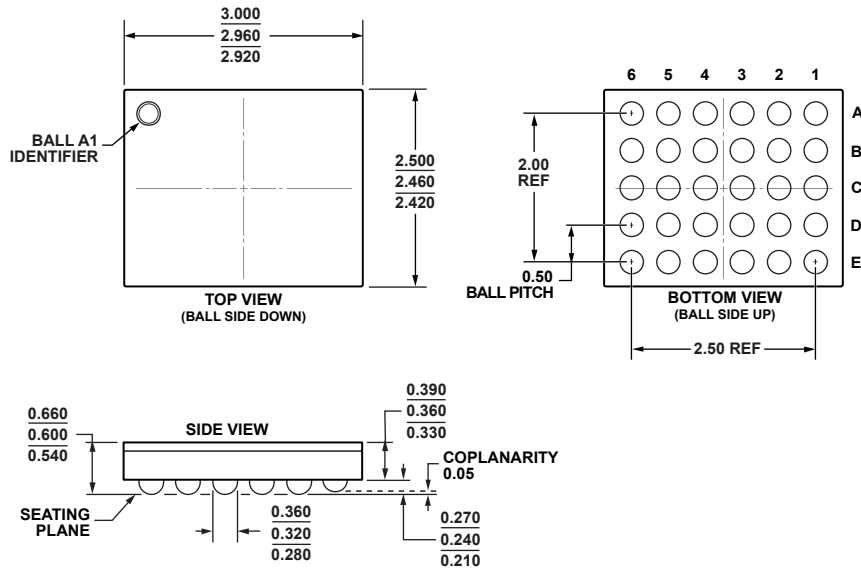


Figure 40. 30-Ball Wafer Level Chip Scale Package [WLCSP]  
(CB-30-4)  
Dimensions shown in millimeters

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## ORDERING GUIDE

| Model <sup>1</sup> | Temperature Range | Package Description                            | Package Option |
|--------------------|-------------------|--|----------------|
| SSM2804CBZ-RL      | -40°C to +85°C    | 30-Ball Wafer Level Chip Scale Package [WLCSP] | CB-30-4        |
| SSM2804CBZ-R7      | -40°C to +85°C    | 30-Ball Wafer Level Chip Scale Package [WLCSP] | CB-30-4        |
| EVAL-SSM2804Z      |                   | Evaluation Board                               |                |

<sup>1</sup> Z = RoHS Compliant Part.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).