# EIGHT OUTPUT DIFFERENTIAL BUFFER FOR PCIE GEN1 AND GEN2

# ICS9DB803D

## General Description

The ICS9DB803D is compatible with the Intel DB800v2 Differential Buffer Specification. This buffer provides 8 PCI-Express Gen2 clocks. The ICS9DB803D is driven by a differential output pair from a CK410B+, CK505 or CK509B main clock generator.

## Recommended Application

DB800v2 compatible part with PCIe Gen1 and Gen2 Support

## Output Features

- 8 - 0.7V current-mode differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available
- 50-100 MHz operation in PLL mode
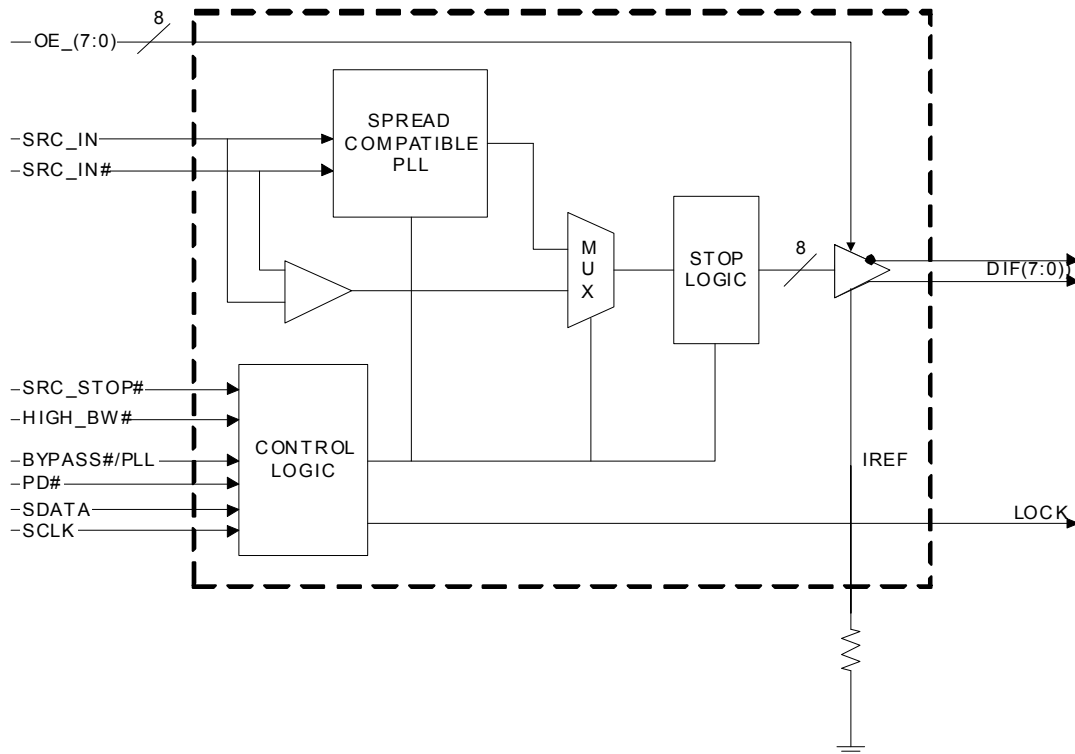- 50-400 MHz operation in Bypass mode

## Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports undriven differential outputs in PD# and SRC_STOP# modes for power management

## Key Specifications

- Outputs cycle-cycle jitter < 50ps
- Output to Output skew <50ps
- Phase jitter: PCIe Gen1 < 86ps peak to peak
- Phase jitter: PCIe Gen2 < 3.0/3.1ps rms

## Functional Block Diagram



**Note: Polarities shown are for OE_INV=0.**

## Pin Configuration

**ICS9DB803 (Same as ICS9DB108)** — OE_INV = 0

| Left Pin | # | | # | Right Pin |
|---|---|---|---|---|
| SRC_DIV# | 1 | | 48 | VDDA |
| VDDR | 2 | | 47 | GNDA |
| GND | 3 | | 46 | IREF |
| SRC_IN | 4 | | 45 | LOCK |
| SRC_IN# | 5 | | 44 | OE_7 |
| OE_0 | 6 | | 43 | OE_4 |
| OE_3 | 7 | | 42 | DIF_7 |
| DIF_0 | 8 | | 41 | DIF_7# |
| DIF_0# | 9 | | 40 | **OE_INV** |
| GND | 10 | | 39 | VDD |
| VDD | 11 | | 38 | DIF_6 |
| DIF_1 | 12 | | 37 | DIF_6# |
| DIF_1# | 13 | | 36 | OE_6 |
| OE_1 | 14 | | 35 | OE_5 |
| OE_2 | 15 | | 34 | DIF_5 |
| DIF_2 | 16 | | 33 | DIF_5# |
| DIF_2# | 17 | | 32 | GND |
| GND | 18 | | 31 | VDD |
| VDD | 19 | | 30 | DIF_4 |
| DIF_3 | 20 | | 29 | DIF_4# |
| DIF_3# | 21 | | 28 | HIGH_BW# |
| BYPASS#/PLL | 22 | | 27 | DIF_STOP# |
| SCLK | 23 | | 26 | PD# |
| SDATA | 24 | | 25 | GND |

**OE_INV = 0**

**ICS9DB803 (Same as ICS9DB801)** — OE_INV = 1

| Left Pin | # | | # | Right Pin |
|---|---|---|---|---|
| SRC_DIV# | 1 | | 48 | VDDA |
| VDDR | 2 | | 47 | GNDA |
| GND | 3 | | 46 | IREF |
| SRC_IN | 4 | | 45 | LOCK |
| SRC_IN# | 5 | | 44 | **OE7#** |
| **OE0#** | 6 | | 43 | **OE4#** |
| **OE3#** | 7 | | 42 | DIF_7 |
| DIF_0 | 8 | | 41 | DIF_7# |
| DIF_0# | 9 | | 40 | **OE_INV** |
| GND | 10 | | 39 | VDD |
| VDD | 11 | | 38 | DIF_6 |
| DIF_1 | 12 | | 37 | DIF_6# |
| DIF_1# | 13 | | 36 | **OE6#** |
| **OE1#** | 14 | | 35 | **OE5#** |
| **OE2#** | 15 | | 34 | DIF_5 |
| DIF_2 | 16 | | 33 | DIF_5# |
| DIF_2# | 17 | | 32 | GND |
| GND | 18 | | 31 | VDD |
| VDD | 19 | | 30 | DIF_4 |
| DIF_3 | 20 | | 29 | DIF_4# |
| DIF_3# | 21 | | 28 | HIGH_BW# |
| BYPASS#/PLL | 22 | | 27 | **DIF_STOP** |
| SCLK | 23 | | 26 | **PD** |
| SDATA | 24 | | 25 | GND |

**OE_INV = 1**

### Power Groups

| Pin Number | | Description |
|---|---|---|
| **VDD** | **GND** | |
| 2 | 3 | SRC_IN/SRC_IN# |
| 6,11,19, 31,39 | 10,18, 25,32 | DIF(7:0) |
| N/A | 47 | IREF |
| 48 | 47 | Analog VDD & GND for PLL core |

### Polarity Inversion Pin List Table

| Pins | OE_INV | |
|---|---|---|
| | **0** | **1** |
| 6 | OE_0 | OE_0# |
| 7 | OE_3 | OE_3# |
| 14 | OE_1 | OE_1# |
| 15 | OE_2 | OE_2# |
| 26 | PD# | PD |
| 27 | DIF_STOP# | DIF_STOP |
| 35 | OE_5 | OE_5# |
| 36 | OE_6 | OE_6# |
| 43 | OE_4 | OE_4# |
| 44 | OE_7 | OE_7# |

## Pin Descriptions for OE_INV=0

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | SRC_DIV# | IN | Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC |
| 2 | VDDR | PWR | 3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. |
| 3 | GND | PWR | Ground pin. |
| 4 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 5 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 6 | OE_0 | IN | Active high input for enabling output 0. 0 =disable outputs, 1= enable outputs |
| 7 | OE_3 | IN | Active high input for enabling output 3. 0 =disable outputs, 1= enable outputs |
| 8 | DIF_0 | OUT | 0.7V differential true clock output |
| 9 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 10 | GND | PWR | Ground pin. |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | DIF_1 | OUT | 0.7V differential true clock output |
| 13 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 14 | OE_1 | IN | Active high input for enabling output 1. 0 =disable outputs, 1= enable outputs |
| 15 | OE_2 | IN | Active high input for enabling output 2. 0 =disable outputs, 1= enable outputs |
| 16 | DIF_2 | OUT | 0.7V differential true clock output |
| 17 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 18 | GND | PWR | Ground pin. |
| 19 | VDD | PWR | Power supply, nominal 3.3V |
| 20 | DIF_3 | OUT | 0.7V differential true clock output |
| 21 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 22 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL mode |
| 23 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 24 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |

## Pin Descriptions for OE_INV=0 (cont.)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|-------------|
| 25 | GND | PWR | Ground pin. |
| 26 | PD# | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped. |
| 27 | DIF_STOP# | IN | Active low input to stop differential output clocks. |
| 28 | HIGH_BW# | PWR | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low |
| 29 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 30 | DIF_4 | OUT | 0.7V differential true clock output |
| 31 | VDD | PWR | Power supply, nominal 3.3V |
| 32 | GND | PWR | Ground pin. |
| 33 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 34 | DIF_5 | OUT | 0.7V differential true clock output |
| 35 | OE_5 | IN | Active high input for enabling output 5.<br>0 =disable outputs, 1= enable outputs |
| 36 | OE_6 | IN | Active high input for enabling output 6.<br>0 =disable outputs, 1= enable outputs |
| 37 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 38 | DIF_6 | OUT | 0.7V differential true clock output |
| 39 | VDD | PWR | Power supply, nominal 3.3V |
| 40 | OE_INV | IN | This latched input selects the polarity of the OE pins.<br>0 = OE pins active high, 1 = OE pins active low (OE#) |
| 41 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 42 | DIF_7 | OUT | 0.7V differential true clock output |
| 43 | OE_4 | IN | Active high input for enabling output 4.<br>0 =disable outputs, 1= enable outputs |
| 44 | OE_7 | IN | Active high input for enabling output 7.<br>0 =disable outputs, 1= enable outputs |
| 45 | LOCK | OUT | 3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved. |
| 46 | IREF | IN | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 47 | GNDA | PWR | Ground pin for the PLL core. |
| 48 | VDDA | PWR | 3.3V power for the PLL core. |

## Pin Descriptions for OE_INV=1

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|-------------|
| 1 | SRC_DIV# | IN | Active low Input for determining SRC output frequency SRC or SRC/2. 0 = SRC/2, 1= SRC |
| 2 | VDDR | PWR | 3.3V power for differential input clock (receiver).  This VDD should be treated as an analog power rail and filtered appropriately. |
| 3 | GND | PWR | Ground pin. |
| 4 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 5 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 6 | OE0# | IN | Active low input for enabling DIF pair 0. 1 =disable outputs,  0 = enable outputs |
| 7 | OE3# | IN | Active low input for enabling DIF pair 3. 1 =disable outputs,  0 = enable outputs |
| 8 | DIF_0 | OUT | 0.7V differential true clock output |
| 9 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 10 | GND | PWR | Ground pin. |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | DIF_1 | OUT | 0.7V differential true clock output |
| 13 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 14 | OE1# | IN | Active low input for enabling DIF pair 1. 1 =disable outputs,  0 = enable outputs |
| 15 | OE2# | IN | Active low input for enabling DIF pair 2. 1 =disable outputs,  0 = enable outputs |
| 16 | DIF_2 | OUT | 0.7V differential true clock output |
| 17 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 18 | GND | PWR | Ground pin. |
| 19 | VDD | PWR | Power supply, nominal 3.3V |
| 20 | DIF_3 | OUT | 0.7V differential true clock output |
| 21 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 22 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL  mode |
| 23 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 24 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |

## Pin Descriptions for OE_INV=1 (cont.)

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|-------------|
| 25 | GND | PWR | Ground pin. |
| 26 | PD | IN | Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped. |
| 27 | DIF_STOP | IN | Active High input to stop differential output clocks. |
| 28 | HIGH_BW# | PWR | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low |
| 29 | DIF_4# | OUT | 0.7V differential Complementary clock output |
| 30 | DIF_4 | OUT | 0.7V differential true clock output |
| 31 | VDD | PWR | Power supply, nominal 3.3V |
| 32 | GND | PWR | Ground pin. |
| 33 | DIF_5# | OUT | 0.7V differential Complementary clock output |
| 34 | DIF_5 | OUT | 0.7V differential true clock output |
| 35 | OE5# | IN | Active low input for enabling DIF pair 5.<br>1 =disable outputs,  0 = enable outputs |
| 36 | OE6# | IN | Active low input for enabling DIF pair 6.<br>1 =disable outputs,  0 = enable outputs |
| 37 | DIF_6# | OUT | 0.7V differential Complementary clock output |
| 38 | DIF_6 | OUT | 0.7V differential true clock output |
| 39 | VDD | PWR | Power supply, nominal 3.3V |
| 40 | OE_INV | IN | This latched input selects the polarity of the OE pins.<br>0 = OE pins active high, 1 = OE pins active low (OE#) |
| 41 | DIF_7# | OUT | 0.7V differential Complementary clock output |
| 42 | DIF_7 | OUT | 0.7V differential true clock output |
| 43 | OE4# | IN | Active low input for enabling DIF pair 4<br>1 =disable outputs,  0 = enable outputs |
| 44 | OE7# | IN | Active low input for enabling DIF pair 7.<br>1 =disable outputs,  0 = enable outputs |
| 45 | LOCK | OUT | 3.3V output indicating PLL Lock Status. This pin goes high when lock is achieved. |
| 46 | IREF | IN | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 47 | GNDA | PWR | Ground pin for the PLL core. |
| 48 | VDDA | PWR | 3.3V power for the PLL core. |

# Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS9DB803D. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| VDDA/R | 3.3V Core Supply Voltage | | 4.6 | V |
| VDD | 3.3V Logic Supply Voltage | | 4.6 | V |
| $V_{IL}$ | Input Low Voltage | GND-0.5 | | V |
| $V_{IH}$ | Input High Voltage | | $V_{DD}$+0.5V | V |
| Ts | Storage Temperature | -65 | 150 | °C |
| Tambient | Commerical Operating Range | 0 | 70 | °C |
| | Industrial Operating Range | -40 | 85 | °C |
| Tcase | Case Temperature | | 115 | °C |
| ESD prot | Input ESD protection human body model | 2000 | | V |

# Electrical Characteristics–Clock Input Parameters

$T_A$ = Tambient for the desired operating range, Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High Voltage - DIF_IN | $V_{IHDIF}$ | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | $V_{ILDIF}$ | Differential inputs (single-ended measurement) | $V_{SS}$ - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | $V_{COM}$ | Common Mode Input Voltage | 300 | | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | $V_{SWING}$ | Peak to Peak value (single-ended measurement) | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN}$ = $V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement | 0 | | 125 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing min centered around differential zero

# Electrical Characteristics–Input/Supply/Common Output Parameters

$T_A$ = Tambient for the desired operating range, Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IHSE}$ | Single Ended Inputs, 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | 1 |
| Input Low Voltage | $V_{ILSE}$ | | GND - 0.3 | | 0.8 | V | 1 |
| Input High Current | $I_{IHSE}$ | $V_{IN} = V_{DD}$ | -5 | | 5 | uA | 1 |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | 1 |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | 1 |
| 9DB803 Supply Current | $I_{DD3.3OPC}$ | Full Active, $C_L$ = Full load; Commerical Temp Range | | 175 | 200 | mA | 1 |
| | $I_{DD3.3OPI}$ | Full Active, $C_L$ = Full load; Industrial Temp Range | | 190 | 225 | mA | 1 |
| 9DB803 Powerdown Current | $I_{DD3.3PDC}$ | all diff pairs driven, C-Temp | | 50 | 60 | mA | 1 |
| | | all differential pairs tri-stated, C-Temp | | 4 | 6 | mA | 1 |
| | $I_{DD3.3PDI}$ | all diff pairs driven, I-temp | | 55 | 65 | mA | 1 |
| | | all differential pairs tri-stated, I-temp | | 6 | 8 | mA | 1 |
| 9DB403 Supply Current | $I_{DD3.3OPC}$ | Full Active, $C_L$ = Full load; Commerical Temp Range | | 105 | 125 | mA | 1 |
| | $I_{DD3.3OPI}$ | Full Active, $C_L$ = Full load; Industrial Temp Range | | 115 | 150 | mA | 1 |
| 9DB403 Powerdown Current | $I_{DD3.3PDC}$ | all diff pairs driven, C-Temp | | 25 | 30 | mA | 1 |
| | | all differential pairs tri-stated, C-Temp | | 2 | 3 | mA | 1 |
| | $I_{DD3.3PDI}$ | all diff pairs driven, I-Temp | | 30 | 35 | mA | 1 |
| | | all differential pairs tri-stated, I-Temp | | 3 | 4 | mA | 1 |
| Input Frequency | $F_{iPLL}$ | PCIe Mode (Bypass#/PLL= 1) | 50 | | 100 | MHz | 1 |
| | $F_{iBYPASS}$ | Bypass Mode ((Bypass#/PLL= 0) | 33 | | 400 | MHz | 1 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except SRC_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INSRC\_IN}$ | SRC_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| PLL Bandwidth | BW | -3dB point in High BW Mode | 2 | 3 | 4 | MHz | 1 |
| | | -3dB point in Low BW Mode | 0.7 | 1 | 1.4 | MHz | 1 |
| PLL Jitter Peaking | $t_{JPEAK}$ | Peak Pass band Gain | | 1.5 | 2 | dB | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency | $f_{MODIN}$ | Allowable Frequency (Triangular Modulation) | 30 | | 33 | kHz | 1 |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | cycles | 1,3 |
| Tdrive_SRC_STOP# | $t_{DRVSTP}$ | DIF output enable after SRC_Stop# de-assertion | | | 10 | ns | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of PD# and SRC_STOP# | | | 5 | ns | 1 |
| Trise | $t_R$ | Rise time of PD# and SRC_STOP# | | | 5 | ns | 2 |
| SMBus Voltage | $V_{MAX}$ | Maximum input voltage | | | 5.5 | V | 1 |
| Low-level Output Voltage | $V_{OL}$ | @ $I_{PULLUP}$ | | | 0.4 | V | 1 |
| Current sinking at $V_{OL}$ | $I_{PULLUP}$ | | 4 | | | mA | 1 |
| SCLK/SDATA Clock/Data Rise Time | $t_{RSMB}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Clock/Data Fall Time | $t_{FSMB}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 100 | kHz | 1,5 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3]Time from deassertion until outputs are >200 mV

[4]SRC_IN input

[5]The differential input clock must be running for the SMBus to be active

## Electrical Characteristics–DIF 0.7V Current Mode Differential Pair

$T_A$ =Tambient; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF, $R_S$=33Ω, $R_P$=49.9Ω, $R_{REF}$=475Ω

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | $Zo^1$ | | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,2 |
| Voltage Low | VLow | | -150 | | 150 | | 1,2 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | | 700 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | | 700 | ps | 1 |
| Rise Time Variation | d-$t_r$ | | | | 125 | ps | 1 |
| Fall Time Variation | d-$t_f$ | | | | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Skew, Input to Output | $t_{pdBYP}$ | Bypass Mode, $V_T$ = 50% | 2500 | | 4500 | ps | 1 |
| | $t_{pdPLL}$ | PLL Mode $V_T$ = 50% | -250 | | 250 | ps | 1 |
| Skew, Output to Output | $t_{sk3}$ | $V_T$ = 50% | | | 50 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode | | | 50 | ps | 1,3 |
| | | *Additive* Jitter in Bypass Mode | | | 50 | ps | 1,3 |
| Jitter, Phase | $t_{jphaseBYP}$ | PCIe Gen1 phase jitter (Additive in Bypass Mode) | | 7 | 10 | ps (pk2pk) | 1,4,5 |
| | | PCIe Gen 2 Low Band phase jitter (Additive in Bypass Mode) | | 0 | 0.1 | ps (rms) | 1,4,5 |
| | | PCIe Gen 2 High Band phase jitter (Additive in Bypass Mode) | | 0.3 | 0.5 | ps (rms) | 1,4,5 |
| | $t_{jphasePLL}$ | PCIe Gen 1 phase jitter | | 40 | 86 | ps (pk2pk) | 1,4,5 |
| | | PCIe Gen 2 Low Band phase jitter | | 1.5 | 3 | ps (rms) | 1,4,5 |
| | | PCIe Gen 2 High Band phase jitter | | 2.7/ 2.2 | 3.1 | ps (rms) | 1,4,5,6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] $I_{REF}$ = $V_{DD}$/(3x$R_R$). For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$=50Ω.

3 Measured from differential waveform

[4] See http://www.pcisig.com for complete specs

[5] Device driven by 932S421C or equivalent.

[6] First number is High Bandwidth Mode, second number is Low Bandwidth Mode

## Clock Periods–Differential Outputs with Spread Spectrum Enabled

| Measurement Window | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | Units | Notes |
| DIF 100 | 9.87400 | 9.99900 | 9.99900 | 10.00000 | 10.00100 | 10.05130 | 10.17630 | ns | 1,2,3 |
| DIF 133 | 7.41425 | 7.49925 | 7.49925 | 7.50000 | 7.50075 | 7.53845 | 7.62345 | ns | 1,2,4 |
| DIF 166 | 5.91440 | 5.99940 | 5.99940 | 6.00000 | 6.00060 | 6.03076 | 6.11576 | ns | 1,2,4 |
| DIF 200 | 4.91450 | 4.99950 | 4.99950 | 5.00000 | 5.00050 | 5.02563 | 5.11063 | ns | 1,2,4 |
| DIF 266 | 3.66463 | 3.74963 | 3.74963 | 3.75000 | 3.75038 | 3.76922 | 3.85422 | ns | 1,2,4 |
| DIF 333 | 2.91470 | 2.99970 | 2.99970 | 3.00000 | 3.00030 | 3.01538 | 3.10038 | ns | 1,2,4 |
| DIF 400 | 2.41475 | 2.49975 | 2.49975 | 2.50000 | 2.50025 | 2.51282 | 2.59782 | ns | 1,2,4 |

Signal Name (row group label for the table above)

## Clock Periods–Differential Outputs with Spread Spectrum Disabled

| Measurement Window | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
|---|---|---|---|---|---|---|---|---|---|
| Symbol | Lg- | -SSC | -ppm error | 0ppm | + ppm error | +SSC | Lg+ | | |
| Definition | Absolute Period | Short-term Average | Long-Term Average | Period | Long-Term Average | Short-term Average | Period | | |
| | Minimum Absolute Period | Minimum Absolute Period | Minimum Absolute Period | Nominal | Maximum | Maximum | Maximum | Units | Notes |
| DIF 100 | 9.87400 | | 9.99900 | 10.00000 | 10.00100 | | 10.17630 | ns | 1,2,3 |
| DIF 133 | 7.41425 | | 7.49925 | 7.50000 | 7.50075 | | 7.62345 | ns | 1,2,4 |
| DIF 166 | 5.91440 | | 5.99940 | 6.00000 | 6.00060 | | 6.11576 | ns | 1,2,4 |
| DIF 200 | 4.91450 | | 4.99950 | 5.00000 | 5.00050 | | 5.11063 | ns | 1,2,4 |
| DIF 266 | 3.66463 | | 3.74963 | 3.75000 | 3.75038 | | 3.85422 | ns | 1,2,4 |
| DIF 333 | 2.91470 | | 2.99970 | 3.00000 | 3.00030 | | 3.10038 | ns | 1,2,4 |
| DIF 400 | 2.41475 | | 2.49975 | 2.50000 | 2.50025 | | 2.59782 | ns | 1,2,4 |

Signal Name (row group label for the table above)

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK409/CK410/CK505 accuracy requirements. The 9DB403/803 itself does not contribute to ppm error.

[3] Driven by SRC output of main clock, PLL or Bypass mode

[4] Driven by CPU output of CK410/CK505 main clock, **Bypass mode only**

| SRC Reference Clock | | | |
|---|---|---|---|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|---|---|---|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|---|---|---|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing

Figure 2: PCI Express Connector Routing
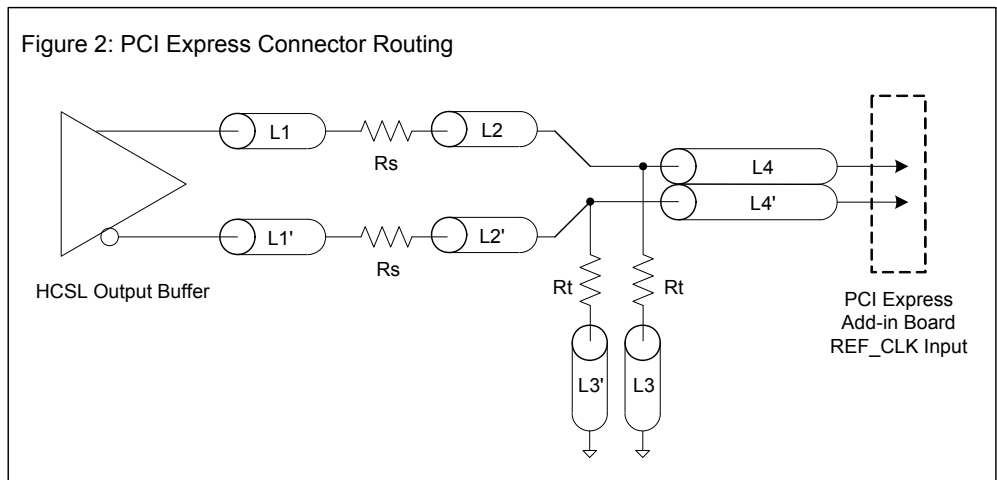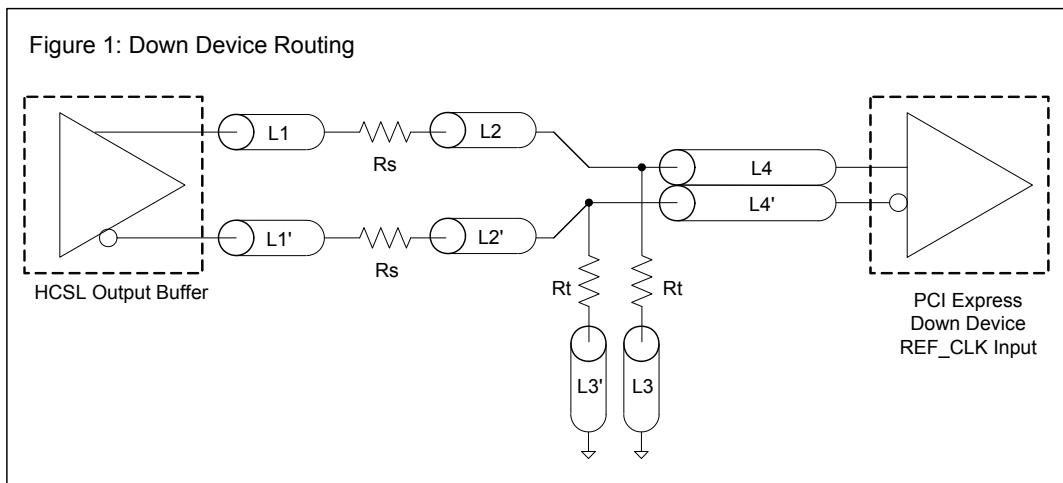
| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

R2a = R2b = R2
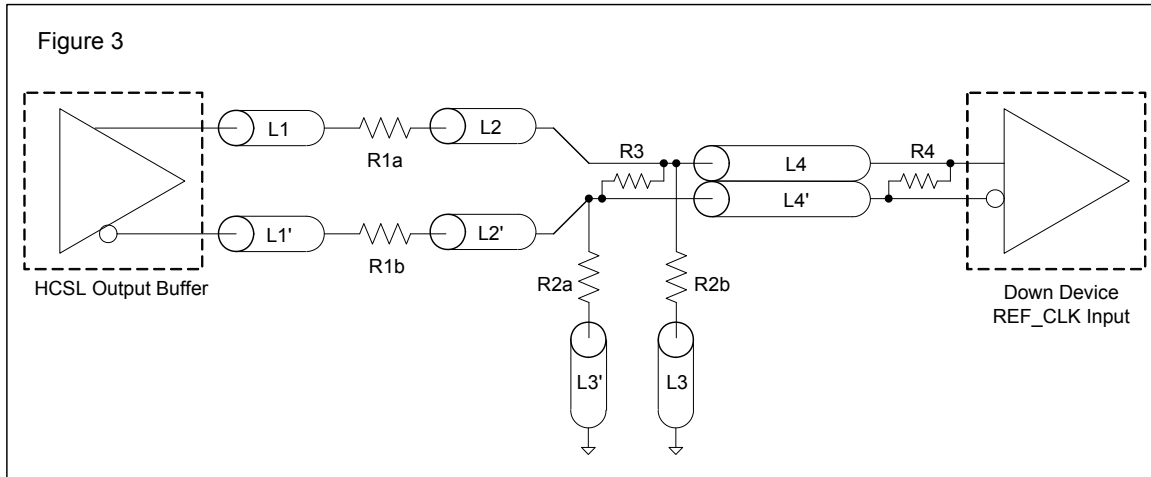


Figure 3

| Cable Connected AC Coupled Application (figure 4) | | |
|---|---|---|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 µF | |
| Vcm | 0.350 volts | |



Figure 4
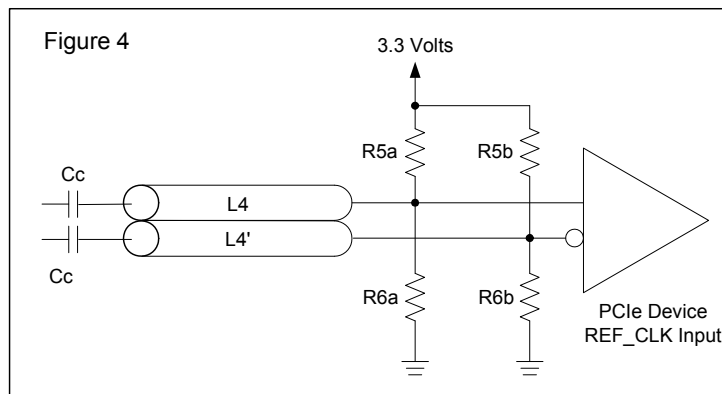
# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if X$_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Write Operation | | |
|---|---|---|
| **Controller (Host)** | | **IDT (Slave/Receiver)** |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| Data Byte Count = X | | |
| | | ACK |
| Beginning Byte N | | |
| | | ACK |
| O | | |
| O | | O |
| O | | O |
| | | O |
| Byte N + X - 1 | | |
| | | ACK |
| P | stoP bit | |

(X Byte)

| Read Address | Write Address |
|---|---|
| DD$_{(H)}$ | DC$_{(H)}$ |

| Index Block Read Operation | | |
|---|---|---|
| **Controller (Host)** | | **IDT (Slave/Receiver)** |
| T | starT bit | |
| Slave Address | | |
| WR | WRite | |
| | | ACK |
| Beginning Byte = N | | |
| | | ACK |
| RT | Repeat starT | |
| Slave Address | | |
| RD | ReaD | |
| | | ACK |
| | | Data Byte Count=X |
| ACK | | |
| | | Beginning Byte N |
| ACK | | |
| | | O |
| O | | O |
| O | | O |
| O | | |
| | | Byte N + X - 1 |
| N | Not acknowledge | |
| P | stoP bit | |

(X Byte)

**SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | - | PD_Mode | PD# drive mode | RW | driven | Hi-Z | 0 |
| Bit 6 | - | STOP_Mode | DIF_Stop# drive mode | RW | driven | Hi-Z | 0 |
| Bit 5 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 2 | - | PLL_BW# | Select PLL BW | RW | High BW | Low BW | 1 |
| Bit 1 | - | BYPASS# | BYPASS#/PLL | RW | fan-out | ZDB | 1 |
| Bit 0 | - | SRC_DIV# | SRC Divide by 2 Select | RW | x/2 | 1x | 1 |

**SMBus Table: Output Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | DIF_7 | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | | DIF_6 | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | | DIF_5 | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | | DIF_4 | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | | DIF_3 | Output Enable | RW | Disable | Enable | 1 |
| Bit 2 | | DIF_2 | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | | DIF_1 | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | | DIF_0 | Output Enable | RW | Disable | Enable | 1 |

**SMBus Table: OE Pin Control Register Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | DIF_7 | DIF_7 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 6 | | DIF_6 | DIF_6 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 5 | | DIF_5 | DIF_5 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 4 | | DIF_4 | DIF_4 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 3 | | DIF_3 | DIF_3 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 2 | | DIF_2 | DIF_2 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 1 | | DIF_1 | DIF_1 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |
| Bit 0 | | DIF_0 | DIF_0 Stoppable with DIFSTOP | RW | Free-run | Stoppable | 0 |

**SMBus Table: Reserved Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|---|---|---|---|---|---|---|---|
| Bit 7 | | | Reserved | RW | Reserved | | X |
| Bit 6 | | | Reserved | RW | Reserved | | X |
| Bit 5 | | | Reserved | RW | Reserved | | X |
| Bit 4 | | | Reserved | RW | Reserved | | X |
| Bit 3 | | | Reserved | RW | Reserved | | X |
| Bit 2 | | | Reserved | RW | Reserved | | X |
| Bit 1 | | | Reserved | RW | Reserved | | X |
| Bit 0 | | | Reserved | RW | Reserved | | X |

**SMBus Table: Vendor & Revision ID Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | RID3 | REVISION ID | R | - | - | X |
| Bit 6 | - | RID2 | | R | - | - | X |
| Bit 5 | - | RID1 | | R | - | - | X |
| Bit 4 | - | RID0 | | R | - | - | X |
| Bit 3 | - | VID3 | VENDOR ID | R | - | - | 0 |
| Bit 2 | - | VID2 | | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

**SMBus Table: DEVICE ID**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | | Device ID 7 (MSB) | RW | Device ID is 83 Hex for 9DB803 and 43 Hex for 9DB403 | | 0 |
| Bit 6 | - | | Device ID 6 | RW | | | X |
| Bit 5 | - | | Device ID 5 | RW | | | X |
| Bit 4 | - | | Device ID 4 | RW | | | 0 |
| Bit 3 | - | | Device ID 3 | RW | | | 0 |
| Bit 2 | - | | Device ID 2 | RW | | | 0 |
| Bit 1 | - | | Device ID 1 | RW | | | 1 |
| Bit 0 | - | | Device ID 0 | RW | | | 1 |

**SMBus Table: Byte Count Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | BC7 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |

Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

## PD#, Power Down

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

## PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with 2 x IREF and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.
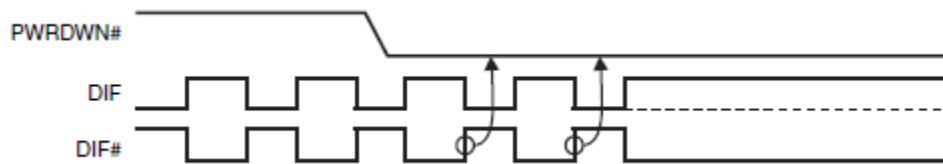


## PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 us of PD# de-assertion.
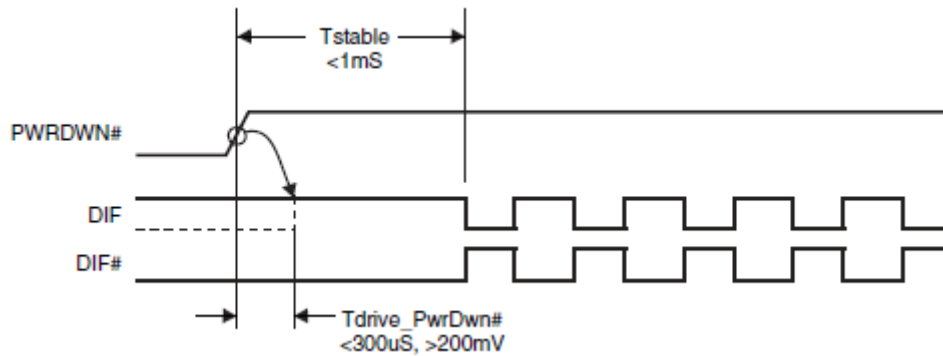
## SRC_STOP#

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs. A valid clock must be present on SRC_IN for this input to work properly. The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

### SRC_STOP# - Assertion

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop). When the SRC_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low. There is no change in output drive current. DIF is driven with 6xIREF. DIF# is not driven, but pulled low by the termination. When the SRC_STOP# drive bit is '1', the final state of all DIF output pins is Low. Both DIF and DIF# are not driven.

### SRC_STOP# - De-assertion (transition from '0' to '1')

All stopped differential outputs resume normal operation in a glitch-free manner. The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously. If the SRC_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.
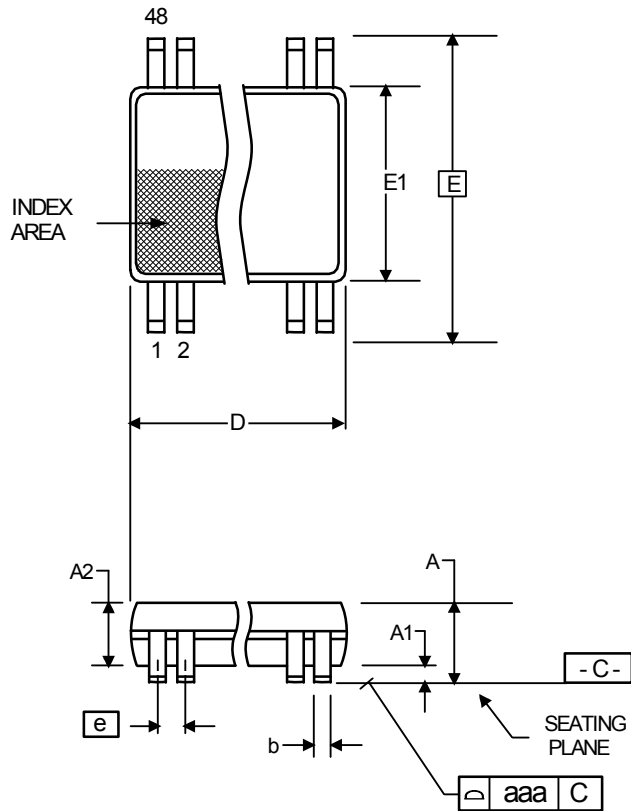
### SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)
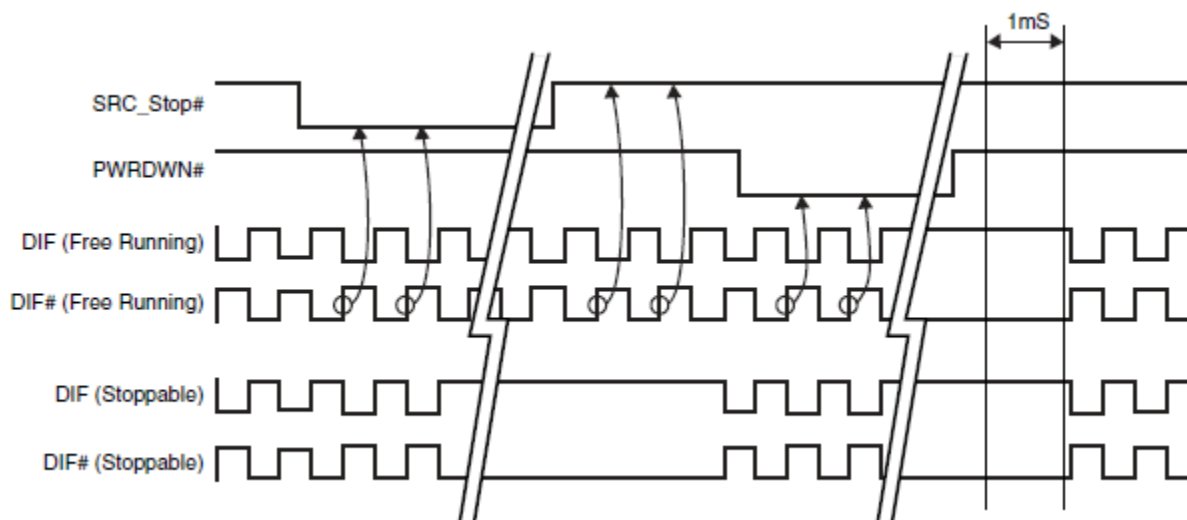


### SRC_STOP_2 (SRC_Stop =Tristate, PD = Driven)
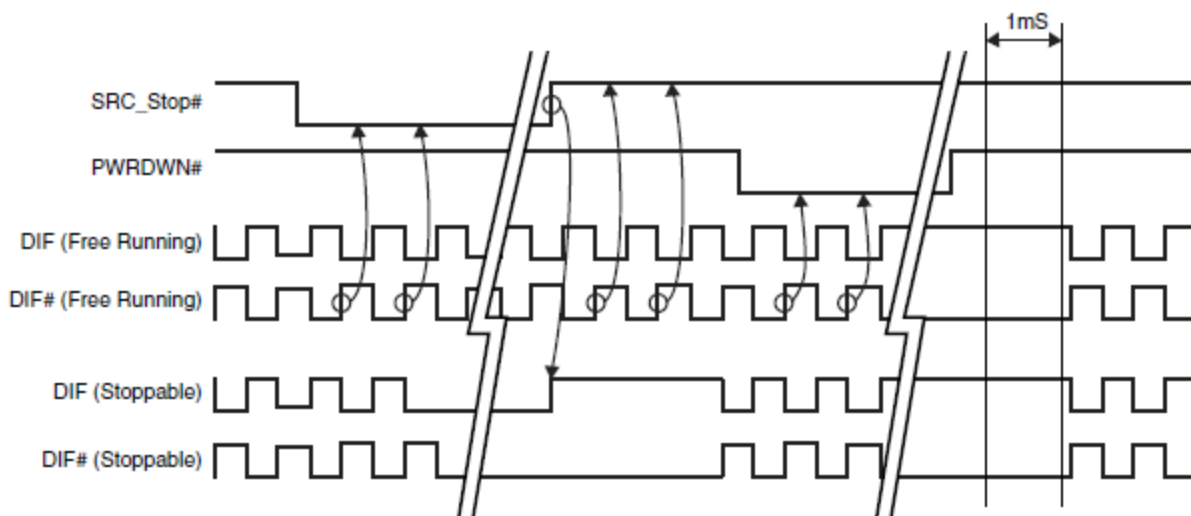
## SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)
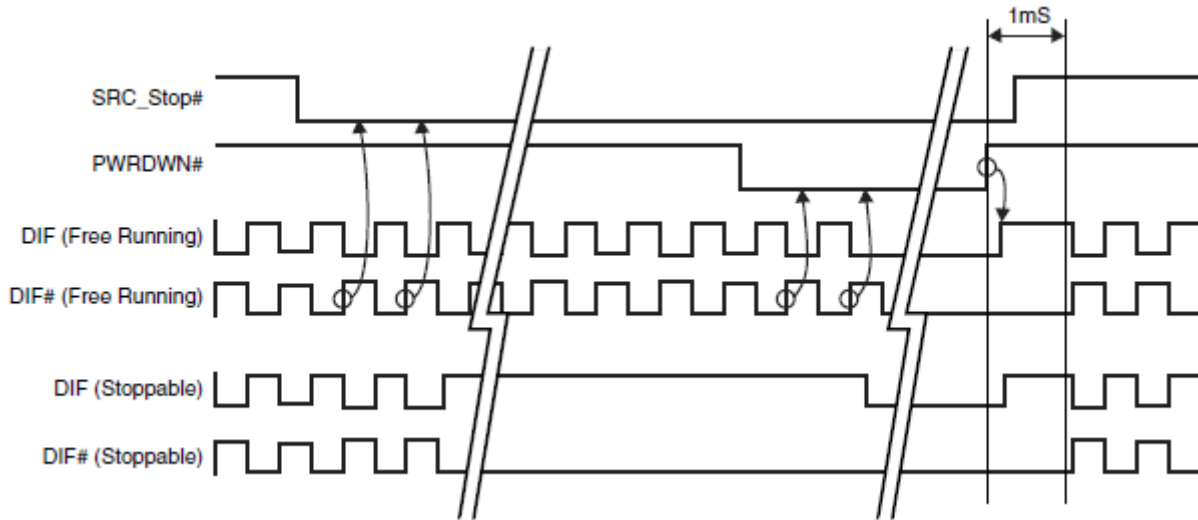


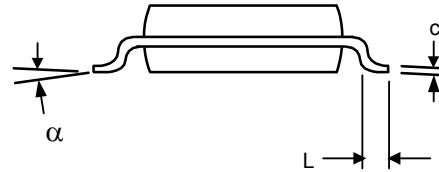## SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)
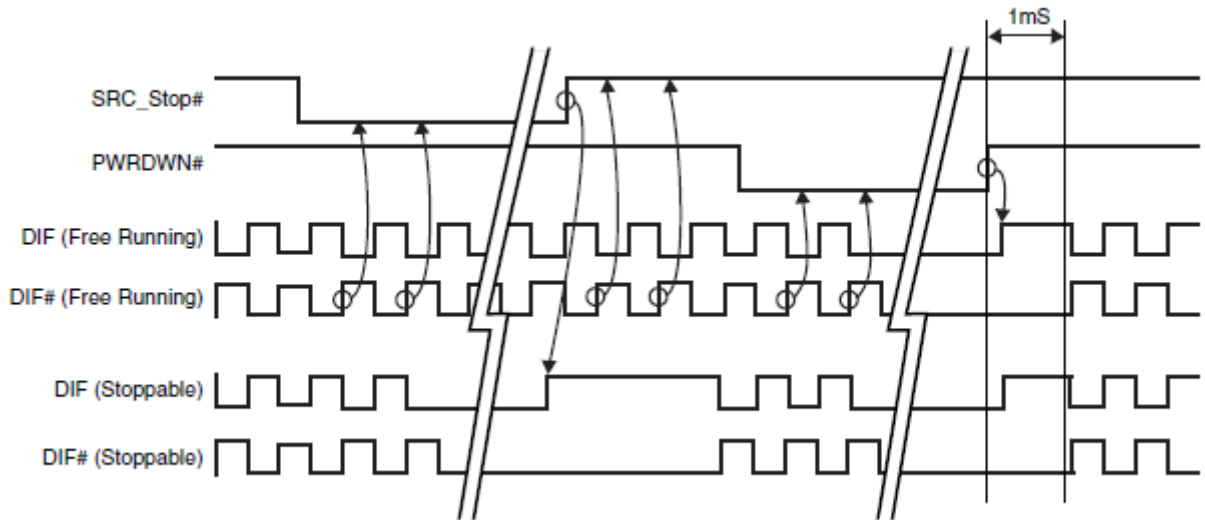
## Package Outline and Package Dimensions (48-pin TSSOP)

Package dimensions are kept current with JEDEC Publication No. 95

|  | Millimeters | | Inches* | |
|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** |
| A | -- | 1.20 | -- | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.17 | 0.27 | 0.007 | 0.011 |
| c | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 12.40 | 12.60 | 0.488 | 0.496 |
| E | 8.10 BASIC | | 0.319 BASIC | |
| E1 | 6.00 | 6.20 | 0.236 | 0.244 |
| e | 0.50 Basic | | 0.020 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| $\alpha$ | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

*For reference only. Controlling dimensions in mm.

## Package Outline and Package Dimensions (48-pin SSOP)

Package dimensions are kept current with JEDEC Publication No. 95
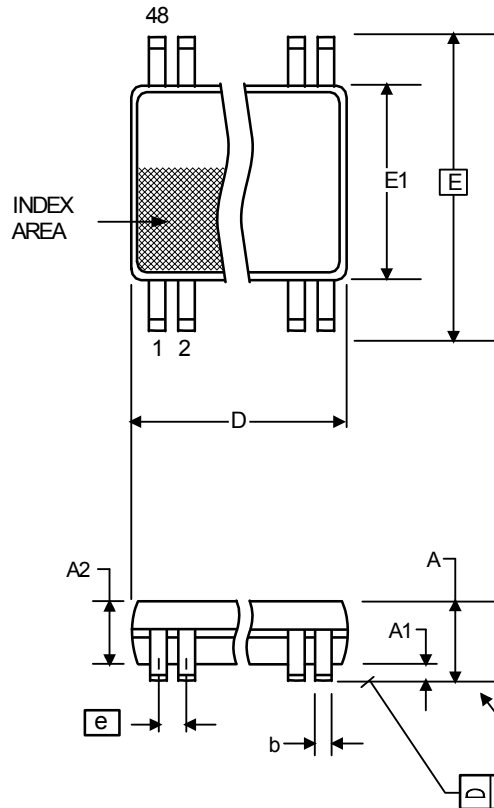
|        | Millimeters |      | Inches* |      |
|--------|-------------|------|---------|------|
| Symbol | Min | Max | Min | Max |
| A | 2.41 | 2.80 | .095 | .110 |
| A1 | 0.20 | 0.40 | .008 | .016 |
| b | 0.20 | 0.34 | .008 | .0135 |
| c | 0.13 | 0.25 | .005 | .010 |
| D | 15.75 | 16.00 | .620 | .630 |
| E | 10.03 | 10.68 | .395 | .420 |
| E1 | 7.40 | 7.60 | .291 | .299 |
| e | 0.635 BASIC | | 0.025 BASIC | |
| h | 0.38 | 0.64 | .015 | .025 |
| L | 0.50 | 1.02 | .020 | .040 |
| α | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.
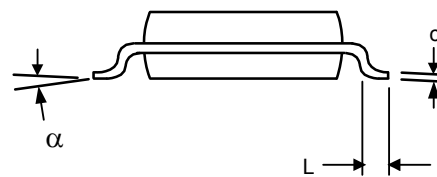
## Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|---------|--------------------|---------|-------------|
| 9DB803DGLF | 9DB803DGLF | Tubes | 48-pin TSSOP | 0 to +70° C |
| 9DB803DGLFT | 9DB803DGLF | Tape and Reel | 48-pin TSSOP | 0 to +70° C |
| 9DB803DGILF | 9DB803DGILF | Tubes | 48-pin TSSOP | –40 to +85° C |
| 9DB803DGILFT | 9DB803DGILF | Tape and Reel | 48-pin TSSOP | –40 to +85° C |
| 9DB803DFLF | 9DB803DFLF | Tubes | 48-pin SSOP | 0 to +70° C |
| 9DB803DFLFT | 9DB803DFLF | Tape and Reel | 48-pin SSOP | 0 to +70° C |
| 9DB803DFILF | 9DB803DFILF | Tubes | 48-pin SSOP | –40 to +85° C |
| 9DB803DFILFT | 9DB803DFILF | Tape and Reel | 48-pin SSOP | –40 to +85° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**
**"D" is the device revision designator (will not correlate with the datasheet revision).**

While the information presented herein has been checked for both accuracy and reliability, Integrated Device Technology (IDT) assumes no responsibility for either its use or for the infringement of any patents or other rights of third parties, which would result from its use. No other circuits, patents, or licenses are implied. This product is intended for use in normal commercial applications. Any other applications such as those requiring extended temperature range, high reliability, or other extraordinary environmental requirements are not recommended without additional processing by IDT. IDT reserves the right to change any circuitry or specifications without notice. IDT does not authorize or warrant any IDT product for use in life support devices or critical medical instruments.

## Revision History

| Rev. | Issue Date | Issuer | Description | Page # |
|------|-----------|--------|-------------|--------|
| A | 8/15/2006 | | Updated electrical characteristics for final data sheet | - |
| B | | | Added Input Clock Specs | |
| C | 2/29/2008 | | Updated Input Clock Specs | |
| D | 3/18/2008 | | Fixed typo in Input Clock Parameters | |
| E | 3/28/2008 | | Updated Electrical Char tables | |
| F | 4/10/2008 | | Updated Input Clock Specs | |
| G | 1/13/2009 | | Corrected part ordering information | |
| H | 10/7/2009 | | 1. Clarified that Vih and Vil values were for Single ended inputs<br>2. Added Differential Clock input parameters.<br>3. Updated Electrical Characteristics to add propagation delay and phase noise information.<br>4. Added SMBus electrical characteristics<br>5. Added foot note about DIF input running in order for the SMBus interface to work<br>6. Added foot note to Byte 1 about functionality of OE bits and OE pins.<br>7. Updated/Reformatted General Description | Various |
| J | 1/27/2011 | | Updated Termination Figure 4 | 12 |
| K | 5/9/2011 | | 1. Update pin 2 pin-name and pin description from VDD to VDDR. This highlights that optimal peformance is obtained by treating VDDR as in analog pin. This is a document update only, there is no silicon change. | Various |
| L | 8/27/2012 | | Updated Vswing conditions to include "single-ended measurement" | 7 |
| M | 9/18/2012 | | Updated Byte 2, bits 0~7 per char review. Outputs can be programmed with Byte 2 to be Stoppable or Free-Run with DIF_Stop pin, not the OE pins. | 14 |
| N | 7/10/2013 | R. Wei | Typo discovered on front page "Output Features" section. Was: "50 – **110**MHz operation in PLL mode"; changed to: "50 – **100**MHz operation in PLL mode" | 1 |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01  Jan 2024)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property  of their respective owners.

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.