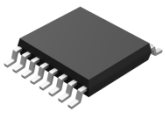
MLX90513

Inductive position sensor interface IC
Datasheet

1. Features and Benefits

- On Chip Signal Processing for Robust Absolute Position Sensing
- High accuracy: Maximum error +/- 0.1% FS
- Immune to magnetic stray fields (ISO 11452-8)
- Flexible Signal Conditioning and programmable 32-point linearization
- Single pin output configurable for SENT/SPC, PWM or Analog Ratiometric
- (fast) SENT according to SAE J2716 APR2016 featuring:
  - Enhanced serial data communication
  - Min. 0.5 µs tick time
- ASIL-C capable for all output modes, Safety Element out of Context
- Wide Operating Supply Voltage range
- Overvoltage and reverse-polarity protection: -24 V to +24 V maximum
- Ambient Operating Temperature Range from -40°C to 160°C
- TSSOP-16 Package RoHS Compliant
- Compliant to TS 16949 and ISO 26262 up to ASIL C(D)



TSSOP-16

2. Application Examples

- Absolute Linear Position Sensor
- Absolute Rotary Position Sensor
- Pedal Position Sensor
- Throttle Position Sensor
- Ride Height Position Sensor
- Steering Wheel Position Sensor
- Non-Contacting Potentiometer
- Small Angle Position Sensor

3. Description

An inductive position sensor is used for absolute rotary and linear motion/position sensing in automotive and industrial applications. The MLX90513 is designed to control an inductive sensor to process the captured analog sensor signals and to provide 3 output modes. The MLX90513 supports (fast) SENT frames encoded according to all formats of the SENT standard, including Secure Sensor format, as well as SPC frames. For SENT/SPC the circuit delivers enhanced serial messages providing error codes and user-defined values. The MLX90513 can also be configured to output a PWM (Pulse Width Modulated) signal and an analog ratio-metric output is also supported. The inductive sensor operation is based on the inductive coupling between a transmitting coil, the target and three receiver coils. The on-chip LC oscillator generates an electromagnetic field together with the transmitting coil. This electromagnetic field induces a target (rotor) angle dependent voltage in the three receiving coils. These three signals are captured and processed by the MLX90513 internal signal processing units. The receiving coils are arranged in a fixed staggered position to each other depending on the number of poles of the metallic target (rotor) above the coils. Typically, the coils are realized as printed circuit board tracks.

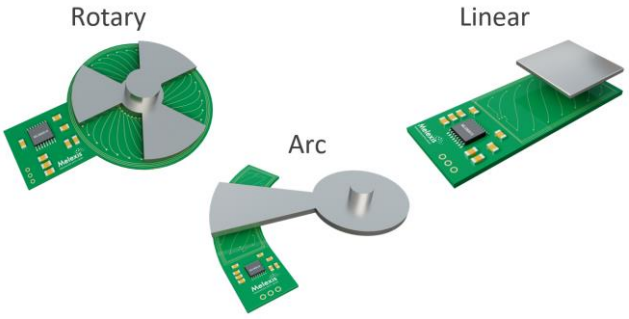


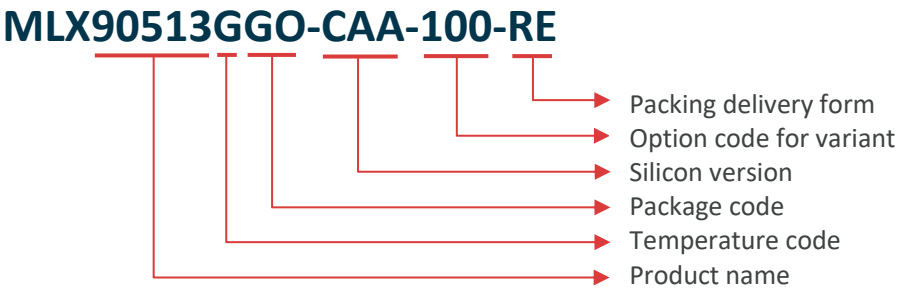
Figure 1 – Supported sensing modes

Contents

4. Ordering Information

Ordering Code	Temperature	Package	Output mode	Packing
MLX90513GGO-CAA-100-RE	-40°C to 160°C	TSSOP-16	SENT/PWM/ANALOG	Reel
MLX90513GGO-CAA-180-RE	-40°C to 160°C	TSSOP-16	SPC/SENT/PWM/ANALOG	Reel

Table 1 – Ordering codes



5. Glossary of Terms

Term	Description
°el	Electrical degree
ABE	Analog Back-end
ADC	Analog-to-Digital Converter
AGC	Automated Gain Control
AFE	Analog Front-end
AoU	Assumptions-of-Use
ASIL	Automotive Safety Integrity Level
CDM	Charge Device Model
CMRR	Common Mode Rejection Ratio
DAC	Digital-to-Analog Converter
DC	Direct Current
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable Read Only Memory
ECU	Electronic Control Unit
EMC	Electro-Magnetic Compatibility
e-rpm	Electrical Revolutions per Minute. 1 e-rpm = 6 °el/s
ESD	Electro-Static Discharge
FDTI	Fault Detection Time Interval
FHTI	Fault Handling Time Interval
GND	Ground
HBM	Human Body Model
Hi-Z	High Impedance
I/O	Input / Output
ISO	International Standardization Organization
LC	Inductor-Capacitor
LCO	LC Oscillator
LSB	Least Significant Bit
PCB	Printed Circuit Board
PGA	Programmable Gain Amplifier
PGI	Programming Interface

Term	Description
PLL	Phase-Locked Loop
POR	Power-On Reset
RCO	RC Oscillator
Rx	Receiver
SAD	Set Circuit Address
SEooC	Safety Element Out-of-Context
SM	Serial Message
TSSOP	Thin-Shrink Small-Outline Package
TA	Ambient Temperature
Tx	Transmitter
V_P	Peak Voltage
V_{PP}	Peak to Peak Voltage

Table 2 – Glossary of terms

6. Marking, Pin Definitions and Descriptions

For more information see application diagrams in chapter 15.

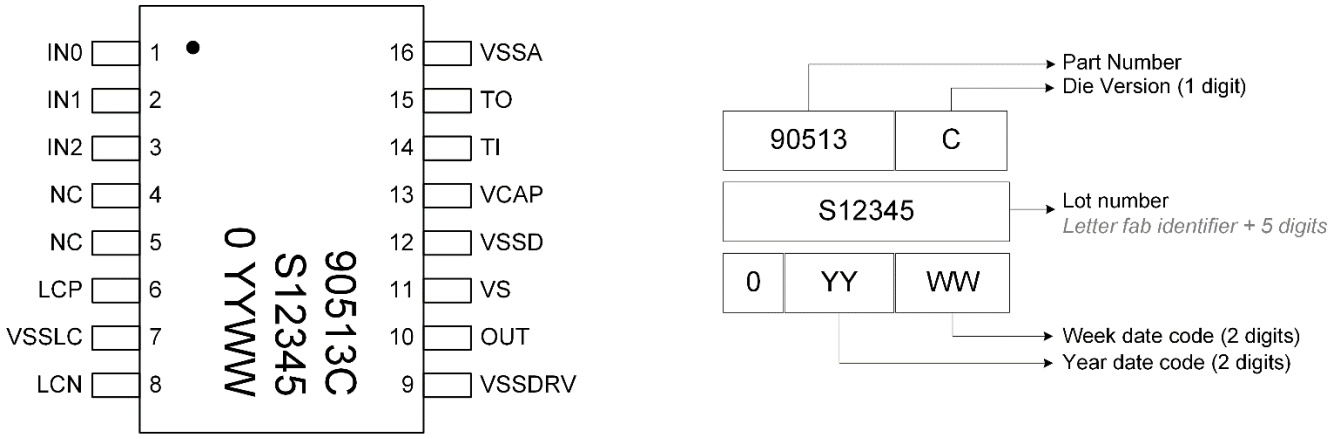


Figure 2 – TSSOP16 pin names and marking

6.1. Pin Definition

Pin #	Name	I/O type	Description
1	IN0	I	Sensor receiver coil signal input 0
2	IN1	I	Sensor receiver coil signal input 1
3	IN2	I	Sensor receiver coil signal input 2
4	NC		Not Connected
5	NC		Not Connected
6	LCP	I/O	Transmitter coil, positive connection
7	VSSLC	Ground	LCO ground
8	LCN	I/O	Transmitter coil, negative connection
9	VSSDRV	Ground	Output Driver ground
10	OUT	I/O	Output interface (application mode), configurable SENT, SPC, PWM or analog ratiometric - or PGI I/O (programming mode)
11	VS	Power	Power supply voltage and (optional) PGI input
12	VSSD	Ground	Digital ground
13	VCAP	Power	External supply buffer capacitor
14	TI	I	Test input (Connect to ground)
15	TO	O	Test output (Connect to ground)
16	VSSA	Ground	Analog ground

Table 3 – TSSOP-16 pins definition and description

7. Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Typ.	Max	Unit	Condition
Ambient temperature	T_A	-40.0		160.0	°C	
Junction temperature	T_{JUNC}			175.0	°C	
Storage temperature	$T_{STORAGE}$	-55.0		175.0	°C	
Supply Voltage	VS	-18.0		18.0	V	Continuous
	VS	-24.0		24.0	V	t < 1h
ESD CDM robustness	V_{CDM}			±500	V	All pins, according to AEC-Q100-011
	V_{CDM}			±750	V	Package corner pins
ESD HBM robustness	V_{HBM}			±4.0	kV	According AEC-Q100-002, for global pins VS, VSSA, VSSD, VSSLC, VSSDRV, OUT
	V_{HBM}			±2.0	kV	According AEC-Q100-002, for local pins INx, LCP, LCN, VCAP, TI, TO
Output overvoltage	V_{OUT}	-18.0		18.0	V	continuous
Pin voltage range INx, VCAP, TI, TO	V_{INx}, V_{VCAP}, V_{TI}, V_{TO}	-0.3		5.5	V	
Pin voltage range LCP, LCN	V_{LCP}, V_{LCN}	-2.0		5.5	V	
Pin voltage range VSS	VSS	-0.3		0.3	V	

Table 4 – Absolute maximum ratings

8. General Electrical Specifications

MLX90513 Electrical Specifications are given in Table 5.

T_A = -40°C to 160°C (unless otherwise specified)

Title	Symbol	Min	Typ	Max	Unit	Condition
Position signal accuracy [1]	$\Delta\phi_{position}$	-0.36		0.36	°el	
Position signal rms noise [2]	$\Delta\phi_{noise}$		0.035		°el	LFC = 0
			0.045		°el	LFC = 1
			0.070		°el	LFC = 2
Passive Diagnostic Output Level (Broken-Wire Detection)	V_{OUT_BVSPD}		0.0	0.5	%VS	Broken VS, R_{PD} < 10kΩ
Passive Diagnostic Output Level (Broken-Wire Detection)	V_{OUT_BVSPU}	95	98		%VS	Broken VS, R_{PU} < 10kΩ
Passive Diagnostic Output Level (Broken-Wire Detection)	V_{OUT_BVSSPD}		1	3	%VS	Broken GND, R_{PD} < 10kΩ
Passive Diagnostic Output Level (Broken-Wire Detection)	V_{OUT_BVSSPU}	99.5	100		%VS	Broken GND, R_{PU} < 10kΩ
Current limitation on pin OUT during short circuits	I_{OUT_SC}	-16		-8	mA	Short to voltages >VS
	I_{OUT_SC}	8		16	mA	Short to voltages <GND
Supply current operation	I_{VS}			7	mA	without LC tank coils, , f_{AC} ≤ 10 MHz
	I_{VS}			10	mA	LCO: Q=18, f_{AC} ≤ 10 MHz
Inrush current [3]	$I_{VS\_startup}$		35	75	mA	C_{VS} = 470 nF
Digital Open Drain Output Leakage	I_{leak_od}			300	µA	R_{PU} at external voltage V_{EXT} < 18V
	I_{leak_od}	-9		9	µA	V_{OUT}=90%VS in OD_{NMOS}, V_{OUT}=10%VS in OD_{PMOS}
Hi-Z Mode Output Leakage	I_{leak_HiZ}	1		15	µA	V_{OUT}=100%VS
	I_{leak_HiZ}	-5		5	µA	V_{OUT}=0%VS
Digital Output ON Resistance High Side	R_{OUT_H}	45		150	Ω	Push-pull, OD_{PMOS}
Digital Output ON Resistance Low Side	R_{OUT_L}	27		130	Ω	Push-pull, OD_{NMOS}
Digital Output ON Resistance Pulse-shaping	R_{OUT_PS}	100		190	Ω	Pulse-shaping

Title	Symbol	Min	Typ	Max	Unit	Condition
Thermal resistance - junction to ambient	R_{thja}			137	K/W	
Thermal resistance - junction to case	R_{thjc}			27.6	K/W	
Supply Voltage	VS	4.5	5.0	5.5	V	
VS POR voltage IC OFF	VS_{POR_OFF}	1.5	1.85	2.0	V	
VS POR voltage IC ON	VS_{POR_ON}	2.05	2.45	2.7	V	
SENT Output Dynamic Level high	V_{SENT_hi}	4.15		4.6	V	Pulse shaping mode, 10kΩ > R_{PU} > 55kΩ
SENT Output Dynamic Level low	V_{SENT_lo}	0.05		0.3	V	Pulse shaping mode, 10kΩ > R_{PU} > 55kΩ
EEPROM programming temperature	T_{EEPROM}	-40		125	°C	
EEPROM erase/write cycles				2000		per row and column

Table 5 – Electrical specifications and system level performance specification

[1] The value reported is a ±3σ value. The accuracy specification includes ±3σ noise assuming LFC=0 settings, but does not include latency contributions and contributions from the output physical layer, the latter being relevant for the analog and PWM output mode. These contributions are detailed in sections 11.1 and 11.4, respectively. The value reported is valid within the speed and acceleration ranges detailed in see section 10.4.1, and with ideal, offset free input signals. For errors related to the input signal offset compensation, refer to section 10.6.1.

[2] The value refers to room temperature

[3] VS rise time from 0 V to 5 V ≥ 100 µs.

9. Timing Specification

9.1. General Timing Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LCO start-up time	$T_{startup\_LCO}$		30	200	µs	
RC oscillator frequency	f_{RCO}	19.3	20	20.7	MHz	Factory trimmed
Application clock	f_{AC}	f_{RCO}/16		f_{RCO}	MHz	
Latency [1]	$\Delta\tau_{phi}$	12 1 -1		18 3 0	µs	ABE_AOUT_MODE=0 ABE_AOUT_MODE=1, 2, 3 ABE_AOUT_MODE=4, 5
Start-up time [2]	T_{STUP}		1	10	ms	

Table 6 – Timing specification

[1] Including the delay compensation according to the default DELAY_AOUT_x values (refer to Section 11.5) and C_{OUT} = 0.

[2] VS rise time from 0 V to 5 V ≥ 25µs.

The application clock frequency f_{AC} is controllable by field AC_SEL [2:0] with the following mapping:

AC_SEL [2:0]	3 (default)	5	6	else
f_{AC} [MHz] (typ.)	10	5	1.25	20

Table 7 – Application clock frequency f_{AC} programming

A lower application clock reduces the MLX90513 current consumption for digital signal processing and ADC but comes with restrictions on dynamic characteristics and communication speed, e.g. SENT tick times (refer to section 11.2).

9.2. Startup Time

In analog and PWM mode, the startup time is the time between the power on reset (POR) and the time the first valid angle transmitted on the output. During startup, the sensor output is in Hi-Z state or failure band is reported.

In SENT/SPC mode, the startup time also indicates the period between POR and the first frame containing valid angular data. By default, the first transmitted frame will be marked as initialization frame. Usually the SENT interface starts faster than the signal acquisition. During this period, after the initialization frame, SENT frames are set to invalid.

After POR the IC opens an activation time window for the PGI programming interface, whose duration can be controlled by field PGI_CAP (default: 10ms). During this period the pin OUT is in Hi-Z independent from the selected output mode. The PGI activation window can be disabled by setting PGI_CAP = 3. For more information about the programming of the MLX90513, refer to the application note “Getting started with the MLX90513 EEPROM programming”. The application note is available on request via http://softdist.melexis.com/. Please contact your local sales representative to get access.

10. Detailed Description

10.1. Block Diagram

The MLX90513 is an inductive position sensor which is used for absolute rotary or linear motion/position sensing (defined by the coil system). In Figure 3 shows the Block diagram.

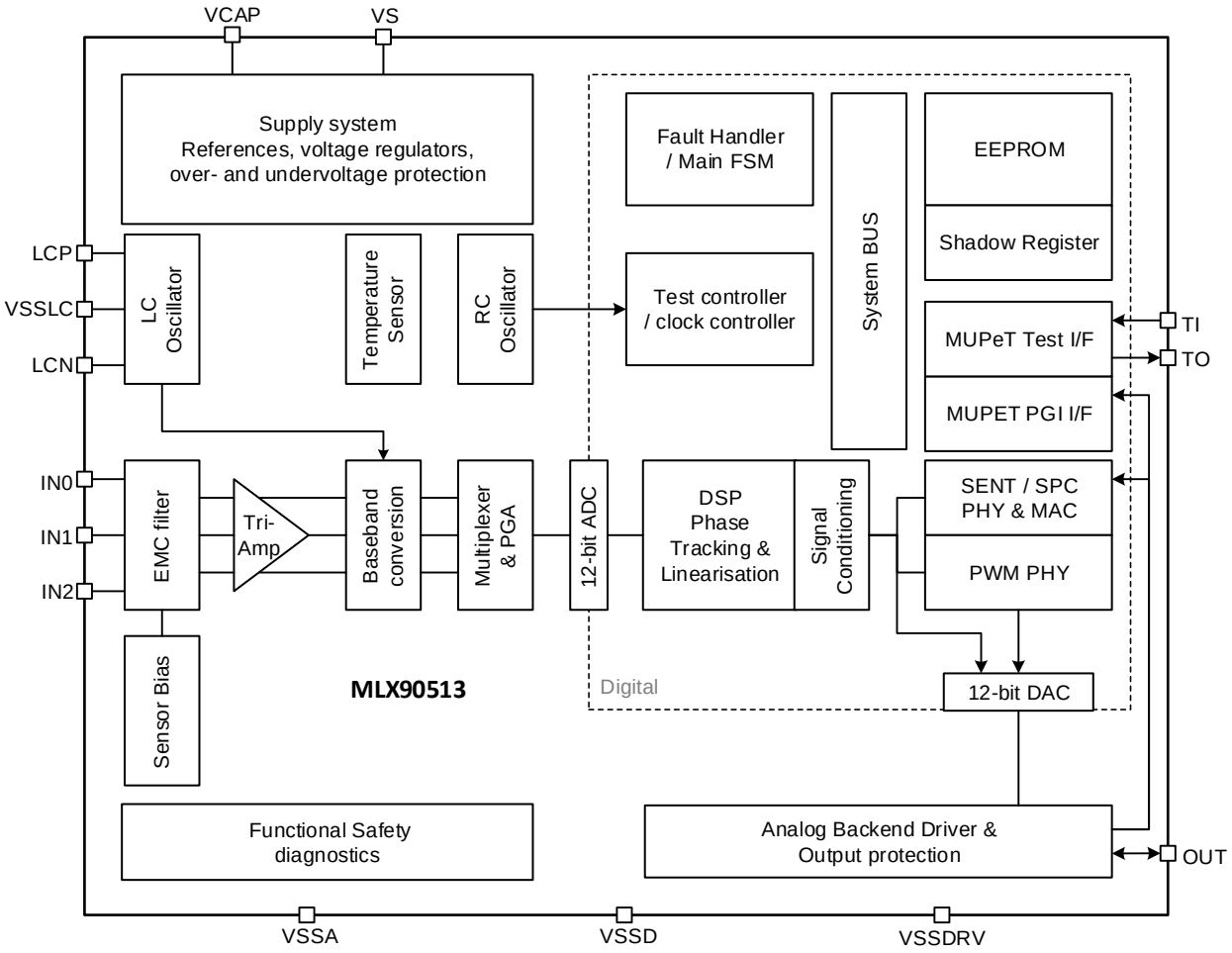


Figure 3 – Block diagram

The main functional sections are: sensor excitation with an LC Oscillator (LCO), the Analog Front-end (AFE) performing the sensor position signal analog pre-processing, the Analog-To-Digital Conversion (ADC) followed by the Digital Signal Processing (DSP) and an Analog Back-end (ABE) providing the output signal.

The AFE consists of an EMC Filter, Tri-Amplifier, Baseband conversion, Multiplexer and Programmable Gain Amplifier (PGA). The digital core provides the signal processing for angular computation and system control as well as the protocol engines for SENT, SPC and PWM modulation. The ABE consists of a 12-bit Digital Analog Converter (DAC) and the highly flexible output driver with output protection. The main supporting functionalities are the supply system, system diagnostics, a Customer Programming Interface (PGI) and an EEPROM for the system configuration data storage.

The functional safety concept provides self-diagnostic features to check the integrity of the sensor coil system, the integrity of the input and output signals, and the IC itself.

10.2. Supply System

The MLX90513 has an integrated supply system providing regulated supply and reference voltages, as well as bias currents.

These regulated supply voltages guarantee immunity against disturbances on the external power supply, required for the correct functionality of the sensor IC. The capacitance at the pin VCAP, refer to section 15, serves as an energy storage during short VS voltage dips.

The supply system offers safety mechanisms and monitors for over and under voltage protection, reverse-polarity protection and power control to ensure correct sensor operation.

10.3. Sensor Coil System

MLX90513 is designed for an external sensor (coil system) consisting of 1 transmitting coil (Tx) and 3 receiving coils (Rx). The parameters described in this section specify the electrical characteristics of the sensor coil system, but do not constitute a full inductive sensor design guideline. For details and support for the sensor and target design please contact our sales office.

10.3.1. Tx Coil and LC Oscillator

The LCO drives the Tx coil of the sensor coil system. The LCO frequency (f_{LCO}) is defined by the external inductance (L_{Tx}) and the two external capacitors C_{LCO} (see Figure 4). A customization of the frequency is possible by variation of L_{TX} and C_{LCO}. The R_{TX} represents the internal resistance of the Tx coil.

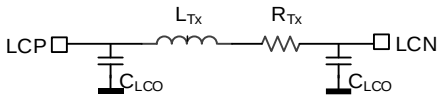


Figure 4 – LCO Tx coil model

The LCO frequency can be calculated using the flowing formula:

$$f_{LCO} = \frac{1}{2\pi}\sqrt{\frac{1}{L(C_{LCO}/2)} - \left(\frac{R_{Tx}}{LTx}\right)^2}$$

The LCO amplitude can be scaled by setting LC_OSC_AMP to 1. A reduced LCO amplitude is used for cases where the maximum input signal amplitude (A_{Rotor}) is exceeded, refer to section 10.4.1, or to reduce emissions.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LCO frequency range	f_{LCO}	2.0	3.0[1]	5.0	MHz	
LCO common mode voltage	V_{CM}		1.68		V	
LCO amplitude	A_{LCO}	2.05	2.4[2]	2.7	V_{PP}	LC_OSC_AMP= 0

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Reduced LCO amplitude	A_{LCO}	1	1.4[2][3]	1.55	V_{PP}	LC_OSC_AMP= 1
Tx coil inductance	L_{Tx}	1	4[4][5][6]	10	µH	
Tx coil internal resistance	R_{Tx}		5[4][5][6]		Ω	
Tx quality factor	Q_{Tx}		18[4][5][6]			
LCO current consumption	I_{VS_LCO}		3[4][5][6]		mA	

Table 8 – LCO electrical parameters

[1] The typical LCO frequency (f_{LCO}) is defined by the Tx coil inductance (L_{Tx}) and the external capacitors (C_{LCO}). A customization of the frequency is possible by variation of L_{Tx} and C_{LCO}. As an example, for a typical value of f_{LCO} = 3.5MHz, the external components can be set as L_{Tx} = 4µH and C_{LCO} = 1nF. However, other component value combinations within the specification range are applicable.
[2] The LCO amplitude is measured from LCN or LCP to GND.
[3] Reduce the LCO amplitude in case the input signal amplitude (A_{Rotor}) is exceeded or to reduce emissions.
[4] Typical value consistent with f_{LCO}=3.5MHz, L_{Tx} = 4µH. This corresponds to a R_{Tx}= 5Ω and C_{LCO} ESR within 1Ω.
[5] Tx Quality factor can be calculated with $Q_{TX} = 2\pi \cdot f_{LCO} \cdot L_{Tx} / R_{Tx}$
[6] The relation between Q_{Tx} and I_{VS_LCO} is depicted in Figure 5 (typical conditions)

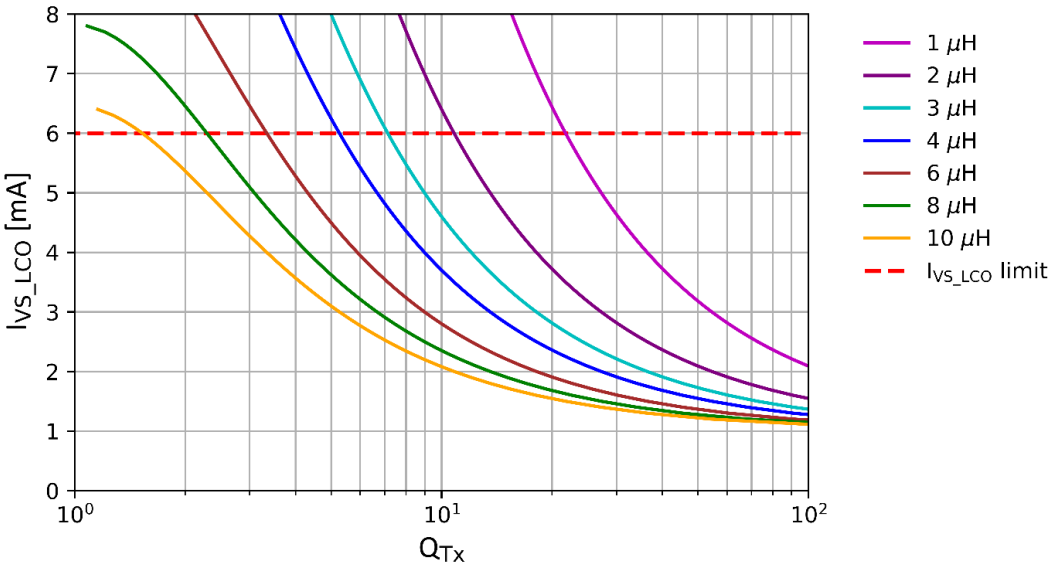


Figure 5 – I_{VS_LCO} as function of Q_{TX} for LCO frequency of 3.5MHz

10.3.2. Rx Coils

The Rx coils electrical specification is given in Table 9. For details and support regarding sensor coil system designs please contact the Melexis sales office.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rx Inductive component	L_{Rx}	40	200	500	nH

Table 9 – Rx coils specification

The Rx coils are DC biased by the 3 internal Sensor Bias circuits. Three individual DC operating points can be chosen by EEPROM register CID programming.

For a single sensor module, the default Sensor Bias setting can be used. For a multi-sensor module including two or more sensor coil systems, the DC operating point of the individual sensors must be programmed to different values (CID setting) for the correct safety function of the sensor short detection.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Sensor Bias operating point	V_{SOP}		0.7		V	CID = 0 (default)
			1.04			CID = 1
			1.41			CID = 2, 3

Table 10 – Sensor DC operating point programming

10.4. Analog Signal Processing

The transmit coil, excited by the LCO, inductively couples to the three Rx coils connected to the pins IN0, IN1 and IN2. The strength of the coupling is modulated by the rotor position and leads to amplitude modulated received signals at LCO frequency.

10.4.1. Input Signal Specification

The three input signal envelopes (INx) from the sensor coil system are composed of an angular signal of amplitude A_{Rotor}, a common mode signal A_{Common} and an asymmetry signal A_{Asym} according to the formulas below.

$$IN0 = A_{Rotor}\, sin\left(\phi - \frac{1}{6}\pi\right) + A_{Common} + A_{Asym0}$$
$$IN1 = A_{Rotor}\, sin\left(\phi - \frac{5}{6}\pi\right) + A_{Common} + A_{Asym1}$$
$$IN2 = A_{Rotor}\, sin\left(\phi - \frac{9}{6}\pi\right) + A_{Common} + A_{Asym2}$$

A_{Common} is caused by the direct coupling from the Tx coil into the Rx coils and is equal on all three inputs. The common mode voltage is suppressed by the MLX90513.

A_{Asym} is caused by the asymmetry of the Rx coils on the PCB, it can have different offset voltages on each INx signal caused by feeding lines from and to the sensor PCB or metal objects close to the PCB sensor. This coil system asymmetry level causes a first-order harmonic on the measured angle and should be compensated using the MLX90513 DC-compensation methods (refer to section 10.6.1).

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
INx input signal envelope	A_{Rotor}	2.5		100	mV_P	
INx common mode voltage	A_{Common}	-10 x A_{Rotor}		10 x A_{Rotor}	V	≤700 mV
INx asymmetry voltage	A_{Asym}	- min (10 mV, 0.7 x A_{Rotor})		min (10 mV, 0.7 x A_{Rotor})	V	A_{Asym} = max(|A_{Asym0}|, |A_{Asym1}|, |A_{Asym2}|)

Table 11 – Input signal requirements

The maximum input signals frequency (angular speed) is given in Table 12.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Electrical angular speed	v_{el}	-6 000		6 000	e-rpm	Analog output
	v_{el}	-240 000[1]		240 000[1]	e-rpm	PWM, SENT, SPC output, f_{AC} = 10 MHz

Table 12 – Electrical rotational speed

[1] If $f_{AC} \neq 10$ MHz, v_{el} should be rescaled by a factor f_{AC} [MHz] / 10. It is recommended to consider as well the Nyquist criteria with respect to the output protocol refresh rate as this may further limit the maximum absolute v_{el}.

The maximum input signals frequency variation (angular acceleration) depends on the bandwidth of the phase tracking loop (refer to section 10.6.2), which is controlled by the field LFC [1:0] as listed in Table 12. Note that Table 12 refers to an application clock f_{AC} = 20 MHz. For other values, the acceleration limits should be scaled by a factor $(f_{AC}$ [MHz]/20$)^2$.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Electrical angular acceleration	acc_{rotor}	300 000		300 000	e-rpm/s	LFC = 0 f_{AC} =20 MHz
	acc_{rotor}	2 400 000		2 400 000	e-rpm/s	LFC = 1 f_{AC} =20 MHz
	acc_{rotor}	10 000 000		10 000 000	e-rpm/s	LFC = 2 f_{AC} =20 MHz

Table 13 – Electrical rotation acceleration

10.5. Analog Signal Processing

10.5.1. Filtering, Amplification and Rectification

The input signals INx are filtered through the EMC filter to suppress high frequency noise. The common mode of the input signals voltage, caused by symmetrical coupling from the Tx coil, is suppressed by a differential amplifier stage.

The rectifier and low pass filter blocks perform a rectification of the amplifier output signals. The rectification is based on the clock derived from the LCO.

10.5.2. Automatic Gain Control

The rectified signals are subject to an amplification step before being converted to digital signals by the ADC block. The MLX90513 has an automatic gain control (AGC) with 5 gain settings. The fields AGC_GAIN_MIN [2:0] and AGC_GAIN_MAX [2:0] allow to restrict the AGC dynamic range or even to lock it by programming AGC_GAIN_MIN[2:0] equal to AGC_GAIN_MAX[2:0]. Restricting the AGC range is not recommended and may result in a reduced range for A_{Rotor} as shown in Figure 6, however the self-monitoring of the AGC operation is not affected.

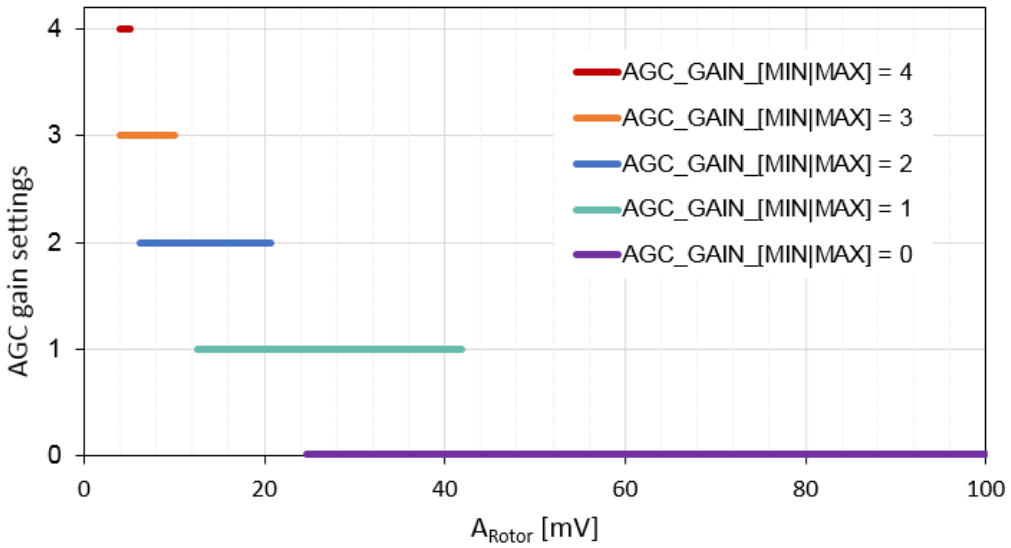


Figure 6 – AGC gain settings as a function of A_{Rotor}

10.6. Digital Signal Processing

The ADC permanently provides sequential samples to the DSP, including samples of the three input phase differences, LCO amplitude samples and other miscellaneous measures.

The DSP features a DC offset compensation, interpolation (to align all three phases to a common sampling point), conversion from 3-phase to I/Q domain, a tracking phase-locked loop and a linearization option. The resulting instant angle is compensated regarding processing delay utilizing estimated speed and acceleration.

10.6.1. Digital Offset Compensation Methods

In section 10.4.1 the composition of the INx signals is given. The signals A_{Asym0}, A_{Asym1} and A_{Asym2} are DC offsets of the input signals (INx), being mainly caused by asymmetries of the PCB coil design (Rx and Tx coils), and caused by feeding lines from and to the sensor or metal objects close to the sensor. This asymmetry can be compensated in the MLX90513 by setting the fields DC01_CONST[15:0], DC12_CONST[15:0] and DC20_CONST[15:0]. The compensation methods are fully automated in the PTC04 programming tool and described in the application note "Getting started with the MLX90513 EEPROM programming". The application note is available on request via http://softdist.melexis.com/. Please contact your local sales representative to get access. To ensure ASIL B compliance and accuracy, it is mandatory to perform DC offset compensation.

The offset compensation is subject to thermal drifts resulting in a temperature dependent 1st harmonic error whose amplitude is dependent on the LCO frequency and the ratio between the amount of compensated A_{Asym} and the useful signal strength A_{Rotor}. The offset error amplitude dependence on these two parameters is illustrated in Figure 7 assuming that the offset compensation is performed at 35 °C.

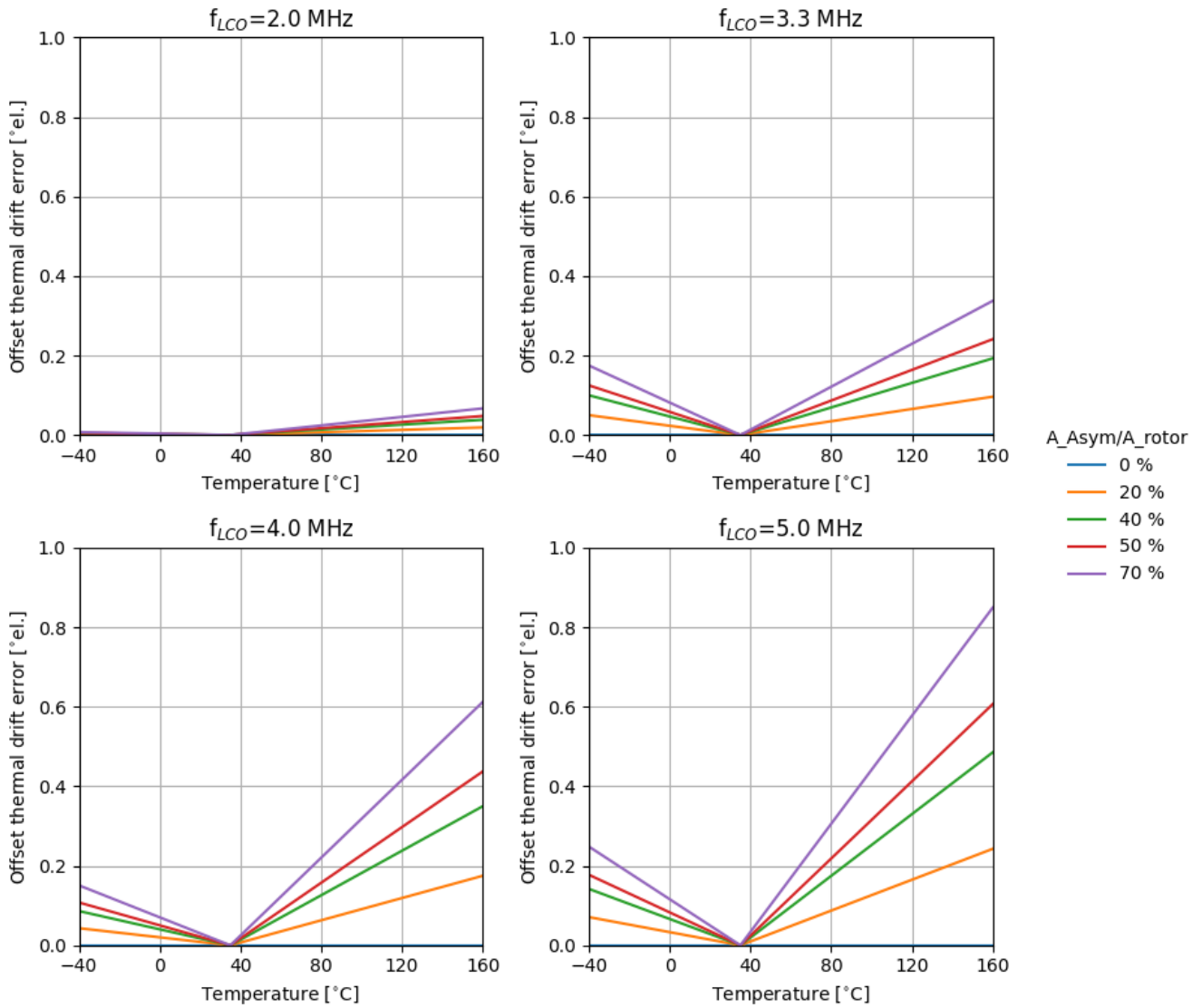


Figure 7 - Offset thermal drift error

10.6.2. Phase Tracking Loop

The phase tracking loop calculates the phase, speed and acceleration of the input signals envelope. The phase tracking loop has a low-pass characteristic to suppress noise which in turn limits the maximum acceleration allowed for the input signals. The bandwidth of the tracking loop can be controlled via the LFC [1:0] field, refer to section 10.4.1.

10.6.3. 32-Points Linearization

The 32-Points Linearization allows to equalize angular non-linearities which can be caused by asymmetries in the sensor coil system layout. Being a sub-block of the phase tracking DSP, the equalization works independent from speed.

The 32 equalization values PEQ00[7:0] to PEQ31 [7:0] (signed, 2's-complement) characterize an angular error curve at angular sample points 360°/32 * [0 .. 31] respectively, see Figure 8. All intermediate values are linearly interpolated. After equalization the residual error curve is the difference between input error curve and interpolated equalization curve. The characterization of the equalization coefficients PEQxx should be performed in quasi-static or low-speed application mode.

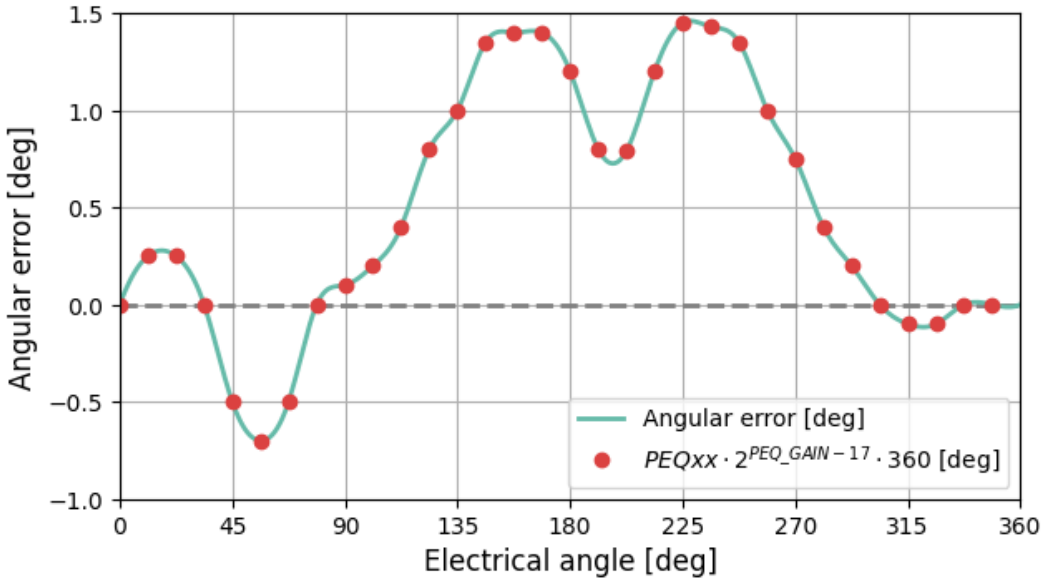


Figure 8 – Angular error curve compensation

The angular error curve should be measured with a quasi-static rotation. With increasing rotational speed, the 32-point linearization automatically adapts to the low pass band limitation of the error curve. Depending on PEQ_GAIN [2:0] the equalization strength versus resolution can be adjusted. If PEQ_GAIN is set to 0, no equalization is applied. For PEQ_GAIN [2:0] = [1 ... 7] the error curve is adjusted per sample point as:

$$\Delta\varphi = \text{signed}(\text{PEQxx}) * 2^{\text{PEQ\_GAIN}-17} * 360\ [\text{deg}]$$

The signed equalization values PEQ00 [7:0] to PEQ31 [7:0] have a range of [-127:127] each. Table 14 indicates the equalization range versus resolution per sample point.

PEQ_GAIN [2:0]	Resolution [deg]	Range (±) [deg]
0	0	0
1	0.0055	0.70
2	0.011	1.40
3	0.022	2.79
4	0.044	5.58
5	0.088	11.16
6	0.176	22.32
7	0.352	44.65

Table 14 – Equalization range

The calculated angle after linearization and before delay compensation and zero position adjustment can be monitored via the register LIN_PHASE [15:0] (refer to section 14.4).

10.6.4. Delay Compensation and Zero Position Adjustment

The speed signal provided by the phase tracking loop (refer to section 10.6.2) is used to compensate for phase errors due to the system latency, while the acceleration signal is used to compensate for phase errors during acceleration due to the latency of the speed calculation. The user furthermore disposes of five programmable fields DELAY_AOUT_0 … DELAY_AOUT_4, to compensate for additional delays associated to e.g. filter networks in between the IC and the ECU, in steps of $3.25/f_{RCO}$. Each of the DELAY_AOUT_x fields refers to a specific ABE output mode, specified in section 11.5.

As a final complement, the mechanical position of the target resulting in zero output value can be adjusted by setting the field PHASE_OFS[15:0]. The value of this field is systematically added to the position value calculated by the phase tracking loop.

The calculated angle after delay compensation and zero position adjustment, and before signal conditioning, can be monitored via the register DRIFTC_PHASE [15:0] (refer to section 14.4).

10.6.5. Signal Conditioning

The Signal conditioning allows to adapt the output protocol dependent signaling ranges to the DSP angle of interest with configurable parameters SC_X1 [15:0], SC_X2 [15:0], SC_Y1 [15:0] and SC_Y2 [15:0]. Figure 9 illustrates the main steps.

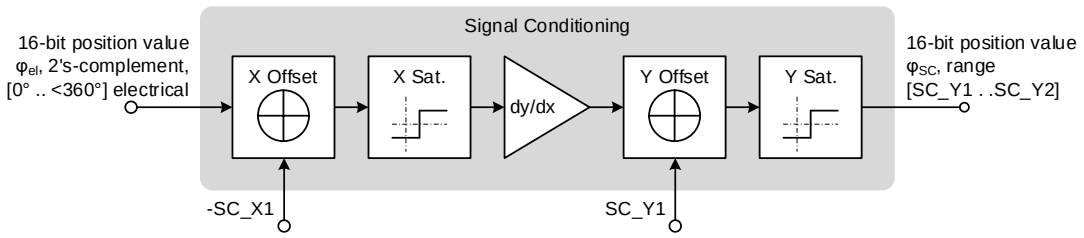


Figure 9 – Signal conditioning functional

Input is the 16-bit measured angle from DSP after delay compensation and offset shift by value PHASE_OFS [15:0], representing the electric angle over for full 360° range. The 16-bit 2's-complement number can be interpreted as [0° .. 360°] (unsigned) or likewise as [-180° .. <180°] (signed).

The input stage, defined by 2's-complement values SC_X1 [15:0], SC_X2 [15:0], restricts the angle of interest and saturates all measured angles exceeding the range [SC_X1 .. SC_X2]. Note that there is no limitation on the value of SC_X1 vs SC_X2 - input range selection overlapping with the zero-point is possible, e.g. [SC_X1 = -8192 (signed) = 51344 (unsigned) , SC_X2 = 8191 (signed/unsigned)] selects the electrical angle range [-45° .. <45°].

This stage can be bypassed by setting [SC_X1, SC_X2] = [0,0] or [0, 2^{16}-1]. The gain stage scales the signal with the ratio of output range width to the input range width.

The output stage, defined by 2's-complement values SC_Y1 [15:0], SC_Y2 [15:0], adds the offset SC_Y1 and saturates values exceeding the output range [min(SC_Y1, SC_Y2) .. max(SC_Y1, SC_Y2)]. It is recommended to understand SC_Y1 and SC_Y2 here as unsigned values in range [0 .. 2^{16}-1] and that in the linear transformation SC_Y1 refers to SC_X1, while SC_Y2 refers to SC_X2 respectively. This means that if SC_X1 < SC_X2 but SC_Y1 > SC_Y2 the transfer characteristic is inverted.

This stage can be bypassed by setting [SC_Y1, SC_Y2] = [0,0] or [0, 2^{16}-1].

Within the saturated region, the occurrence of the transition between the SC_Y1 and SC_Y2 defined outputs can be controlled via the SC_HL [7:0] parameter. SC_HL [7:0] defines the offset of the transition point from the center point (SC_X1+SC_X2)/2, in units of 360°/2^8.

Figure 10 depicts a configuration intended for 12-bit SENT output (valid signal range: [1 .. 4088]) and an input range restriction from 45° to -45° (span 270°).

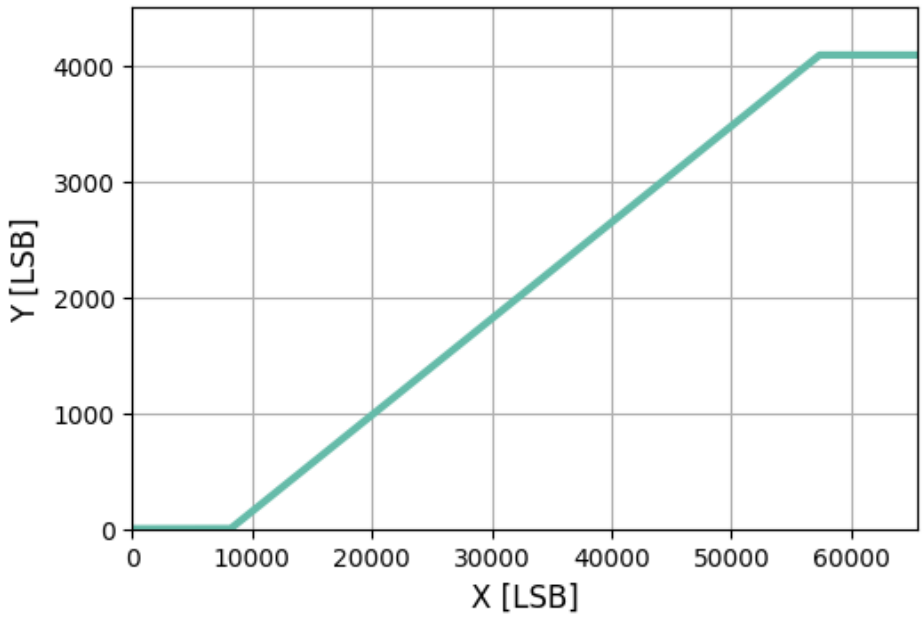


Figure 10 – SC transfer curve for SC_X1=8192; SC_X2=57344; SC_Y1=1; SC_Y2=4088, SC_HL=0

The signal condition transformation influences the signal resolution as follows:

Parameter	Symbol	Min.	Unit
Resolution of electrical angle	R_{angle_el}	$360/2^{16}$	deg
Resolution of angle after signal conditioning	R_{angle_SC}	$360/2^{16}$ * max(1, abs(unwrap(SC_X2-SC_X1)) / abs(SC_Y2 - SC_Y1))	deg

Table 15 – Signal resolution

The following settings for SC_Y1 [15:0], SC_Y2 [15:0] are recommended for different output modes to comply to valid signal ranges. It has to be noted that output protocols with <16 bits resolution make use only of the corresponding LSBs of the signal conditioning output.

Mode	SC_Y1 [15:0]	SC_Y2 [15:0]	Comment/Reference
SENT, H.7	1	65528	16-bit fast channel 1
SENT, H.6	1	16376	14-bit fast channel 1
SENT/SPC, else	1	4088	12-bit fast channel 1
Analog ratiometric	205	3890	12-bit DAC, 5% to 95% of VS valid signal range
PWM	80	T_{FRAME} - 80	minimum pulse width of 4 µs at 20 MHz f_{AC}. Refer to section 11.3 for other conditions

Table 16 – Signal condition settings for different output modes

The position value after signal conditioning can be monitored via the register SC_PHASE [15:0] (refer to section 14.4).

10.6.5.1. Fault Band Mapping

For functional safety in case of detected errors leading to safe state SS3, the signal conditioning outputs the fault band value as defined by field SC_YE [15:0].

If SC_YE is configured with a value within the output range (min(SC_Y1, SC_Y2) to max(SC_Y1, SC_Y2)) or if in case of a missing output range (e.g. SC_Y1 = SC_Y2) a fault band reporting is impossible and the MLX90513 switch the to the output safe state SS2 (Hi-Z).

11. Output modes

This chapter describes the output interfaces of the MLX90513. The output mode can be selected with the field PROTOCOL [2:0].

PROTOCOL [2:0]	Output Mode	Comment
0	SENT without pause	
1	PWM	
2	SENT with pause	default for the MLX90513GGO-CAA-100-RE option code
3	SPC	default for the MLX90513GGO-CAA-180-RE option code
4	ANALOG	

Table 17 – Output mode selection

11.1. Analog Ratiometric Output

With PROTOCOL [2:0] set to 4 and ABE_AOUT_MODE [2:0] set to 0, the MLX90513 does output on pin OUT an analog voltage with 12-bit resolution, ratiometric to the supply voltage VS, representing the 12-bit position value after signal conditioning (φ_{SC} [11:0]).

$$V_{OUT} = (\varphi_{SC}[11:0] + 0.5) * 2^{-12} * VS$$

The interface can be used outside the linear output range for e.g. fault band indication with SC_YE [15:0].

Due to factory trimming of the DAC offset, the input ranges [0 .. 31] and [4064 .. 4095] should not be used to prevent wrap-around.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Analog Output DAC Resolution			12.0		bit	
Analog Output Saturation Level	V_{satA_hi}	95.0	98.0		%VS	R_{PD} > 4.7kΩ
Analog Output Saturation Level	V_{satA_lo}		2.0	5.0	%VS	R_{PU} > 4.7kΩ
DAC differential non-linearity	DNL_{DAC}	-1.5		1.5	LSB_{12}	
DAC integral non-linearity	INL_{DAC}	-4.0		4.0	LSB_{12}	
Linear output range		5.0		95.0	%VS	R_{PU} or R_{PD} > 4.7 kΩ
Ratiometric error	$ANA_{VoutRatiometric}$	-0.05		0.05	%VS	Within the linear output range

Table 18 – Analog output specification

11.2. Single Edge Nibble Transmission (SENT) SAE J2716

11.2.1. SENT Message Sequence

In accordance to SENT SAE J2716, the encoding scheme consists of a sequence of pulses which is repeatedly sent by the transmitting module. The transmission consists of the following sequence (all times nominal):

1. Calibration/Synchronization pulse period 56 clock ticks
2. One 4-bit Status and Serial Communication nibble pulse

3. Three to six data nibble pulses according to the basic SENT formats H.1 to H.7 , see Table 22.
4. One 4-bit Checksum nibble pulse.
5. One optional pause pulse

Figure 11 provides an example of a SENT frame.

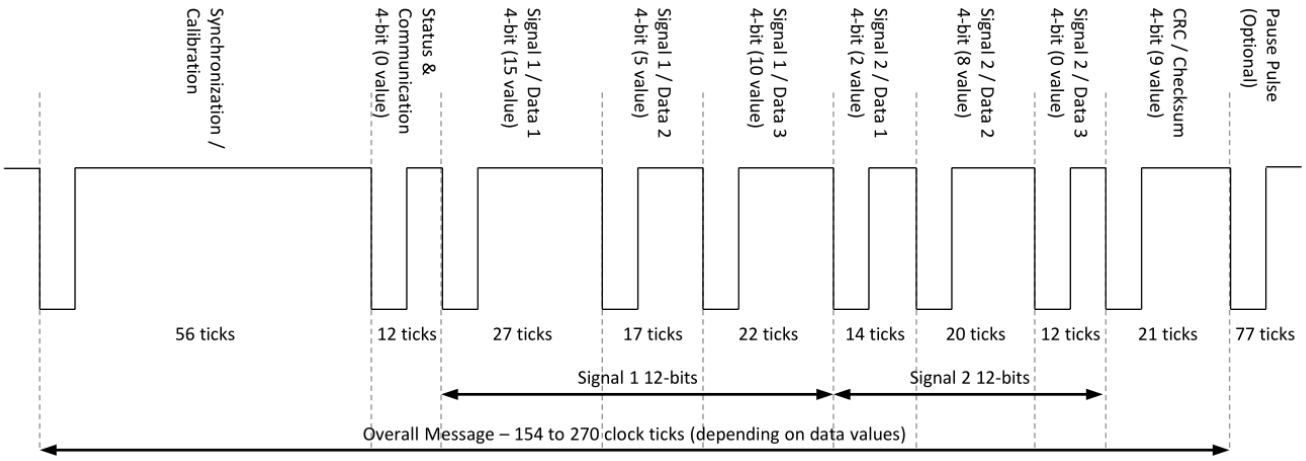


Figure 11 – SENT example encoding for two 12-bit signals

The SENT tick times are configurable by field SENT_TICK_TIME [2:0] as follows:

SENT_TICK_TIME [2:0]	0	1	2	3	4	Else
T_{tick} [µs], f_{AC}=20MHz	0.5	0.75	1	1.5	3	6
T_{tick} [µs], f_{AC}=10MHz	0.5	0.8	1	1.5	3	6
T_{tick} [µs], f_{AC}=5MHz	0.6	0.8	1	1.6	3	6
T_{tick} [µs], f_{AC}=1.25MHz	0.8	0.8	1.6	1.6	3.2	6.4

Table 19 – SENT tick times

Note that for tick times < 1.5µs the digital pulse shaping mode is required to ensure sufficient bandwidth of the ABE. When the output driver is configured in any of the binary modulation modes; the SENT nibble shape can be configured using the field SENT_SHAPE_CFG according to Table 20:

SENT_SHAPE_CFG[1:0]	Mode	Condition
0	5 ticks fixed low time	ABE_AOUT_MODE=1,2,3
1	6 ticks fixed high time	ABE_AOUT_MODE=1,2,3
2,3	50% duty cycle	ABE_AOUT_MODE=1,2,3

Table 20 – SENT nibble configuration

The Status and communication nibble can be included in the CRC computation by setting the field STATUS_IN_CRC to 1.

11.2.2. Frame period and Pause Pulse

With field PROTOCOL [2:0] two versions of SENT can be selected:

PROTOCOL [2:0]	Mode	Frame Length
0	SENT with pause pulse (ppc)	Max ((T_FRAME [11:0]+1) * T_{tick} , message sequence period including pause pulse)
2	SENT without pause pulse (npp)	message sequence period without pause pulse

Table 21 – SENT protocols

Note that "SENT without pause pulse" maximizes the SENT communication data rate while at the same time preventing equidistant sampling of the (transmitted) sensor data.

11.2.3. SENT Frame Formats

With field SENT_FC_FORMAT[2:0] all SENT basic frame formats (standard version 2016) are supported.

SENT_FC_ FORMAT [2:0]	Frame Format	Data Nibbles	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6
0, 1 (default)	H.1: Two 12-bit fast channels (CH1, CH2)	6	CH1 MSN	CH1 MidN	CH1 LSN	CH2 LSN	CH2 MidN	CH2 MSN
2	H.2: One 12-bit CH1	3	CH1 MSN	CH1 MidN	CH1 LSN	-	-	-
3	H.3: High-speed with one 12-bit CH1 (3-bit nibbles)	4	CH1 MSN	CH1 Bits 8-6	CH1 Bits 5-3	CH1 LSN	-	-
4	H.4: Secure sensor with 12-bit CH1 and secure sensor information on CH2	6	CH1 MSN	CH1 MidN	CH1 LSN	Ctr MSN	Ctr LSN	~(CH1 MSN)
5	H.5: Single sensor with 12-bit CH1 and zero value on CH2	6	CH1 MSN	CH1 MidN	CH1 LSN	0	0	0

SENT_FC_ FORMAT [2:0]	Frame Format	Data Nibbles	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6
6	H.6: Two fast channels with 14-bit CH1 and 10-bit CH2	6	CH1 MSN	CH1 MidMSN	CH1 MidLSN	CH1/CH2 LSN	CH2 MidN	CH2 MSN
7	H.7: Two fast channels with 16-bit CH1 and 8-bit CH2	6	CH1 MSN	CH1 MidMSN	CH1 MidLSN	CH1 LSN	CH2 LSN	CH2 MSN

Table 22 - SENT frame formats

11.2.4. Fast Channel 1 Capturing and Encoding

The SENT Fast channel 1 (CH1) carriers the measured angle information after signal conditioning. The signal conditioning output limits SC_Y1 [15:0] and SC_Y2 [15:0] should be configured to comply to the reserved signaling ranges according to SENT SAE J2716, refer to Table 16. Further restrictions of the output range are optional.

In SENT mode the DSP angular values after signal conditioning / interpolation are captured into CH1 with falling edge of the SYNC pulse and after an adjustable capture delay defined by field SENT_FC1_CPT_DLY [6:0] [ticks]. It is not recommended to program SENT_FC1_CPT_DLY to capture time later than the SCN nibbles, unless the captured value shall be transmitted with the NEXT SENT frame.

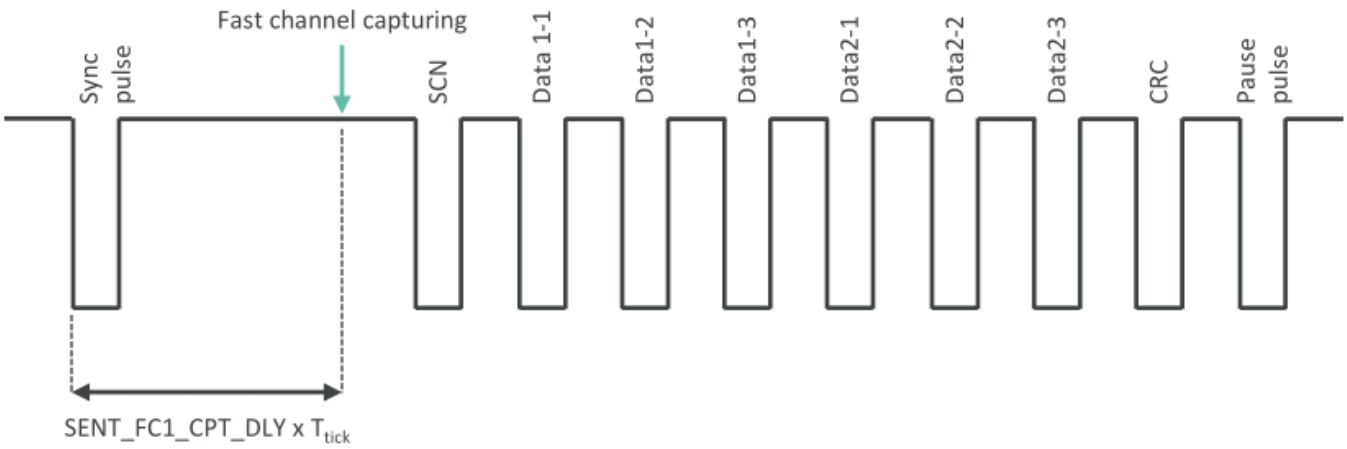


Figure 12 – SENT fast channel capturing timing

11.2.5. Fast Channel 2 Encoding

In SENT dual-channel modes H.1, H.6, H.7, the fast channel 2 (CH2) data is defined by the field SENT_FAST_CHANNEL_2 [1:0].

SENT_FAST_CHANNEL_2 [1:0]	Fast channel 2
0	Internal temperature sensor (default)
1	Inverted angle, calculated as 0xFF9 - CH1
2	Register probe
3	Inverted angle, calculated as 0xFFF - CH1

Table 23 - Fast channel 2 (CH2) encoding

The temperature sensor data is encoded depending on bit width according to SENT SAE J2716 section A.5.3.2 and E.2.2.1.

CH2 bit width [bit]	12	10	8
Transfer function slope [LSB/K]	8	4	1
Transfer function offset [K]	200	220	220
min(T)	200.125K (-73.025°C)	220.25K (-52.90°C)	221K (-52.15°C)
max(T)	711K (437.85°C)	474K (200.85°C)	468K (194.85°C)

Table 24 – Temperature sensor data encoding

When transmitting temperature data, the transmitted value can be clipped by setting the field TEMP_CLIP_EN to 1. In this case the reported temperature will be limited by the values defined in fields DIAG_TEMP_THR_LO and DIAG_TEMP_THR_HI even if the ambient temperature is below or above these values.

If SENT_FAST_CHANNEL_2 is set to 2 (Register probe), the fast channel 2 transmits the content of a register or memory address, which is specified by SENT_FC2_ADR[7:0]. The byte aligned address (see section 14) maps to 16-bit word aligned value for SENT_FC2_ADR[7:0] by omitting the LSB, e.g. address 86 (SPEED_LO) is configured by SENT_FC2_ADR=43. The selected 16 bits register is transmitted over two successive frames with two different offsets, programmable via EE_SENT_FC2_OFS0 [3:0] (rolling counter LSB = 0) and EE_SENT_FC2_OFS1 [3:0] (rolling counter LSB = 1). Refer to Chapter 13.5.1 for the address values.

11.2.6. Start-Up Behavior

After start-up and after leaving safe state SS2 the circuit will send initialization frame(s) with fast channel 1 (CH1) content chosen by bit SENT_INIT_GM.

SENT_INIT_GM	CH1 initialization value	Comment
0	0	SAE compliant
1	SC_YE	OEM compliant

Table 25 – Initialization frame selection

In frame format H.4 the startup behavior of the rolling counter can be configured by bit SENT_RC_INIT as follows:

SENT_RC_INIT	Description
0	Rolling counter stays at 0 during the initialization frame(s)
1 (default)	Rolling counter is incrementing during initialization frame(s)

Table 26 – Rolling counter initialization behavior

11.2.7. Serial Message Channel (Slow Channel)

Serial data is transmitted sequentially in bit number 3 and 2 of the status and communication nibble.

11.2.7.1. Enhanced Serial Message (ESM)

The MLX90513 supports enhanced serial messages with 12-bit data and 8-bit message ID (SAE J2716 APR2016 5.2.4.2, Figure 5.2.4.2-1) if bit SENT_SC_FORMAT is set to 1. An enhanced serial message frame stretches over 18 consecutive SENT data messages from the transmitter. According to the standard, Serial Data bit # 2 contains a 6-bits CRC followed by a 12-bits data. The message content is defined by an 8-bit message ID transmitted by the Serial Data bit # 3.

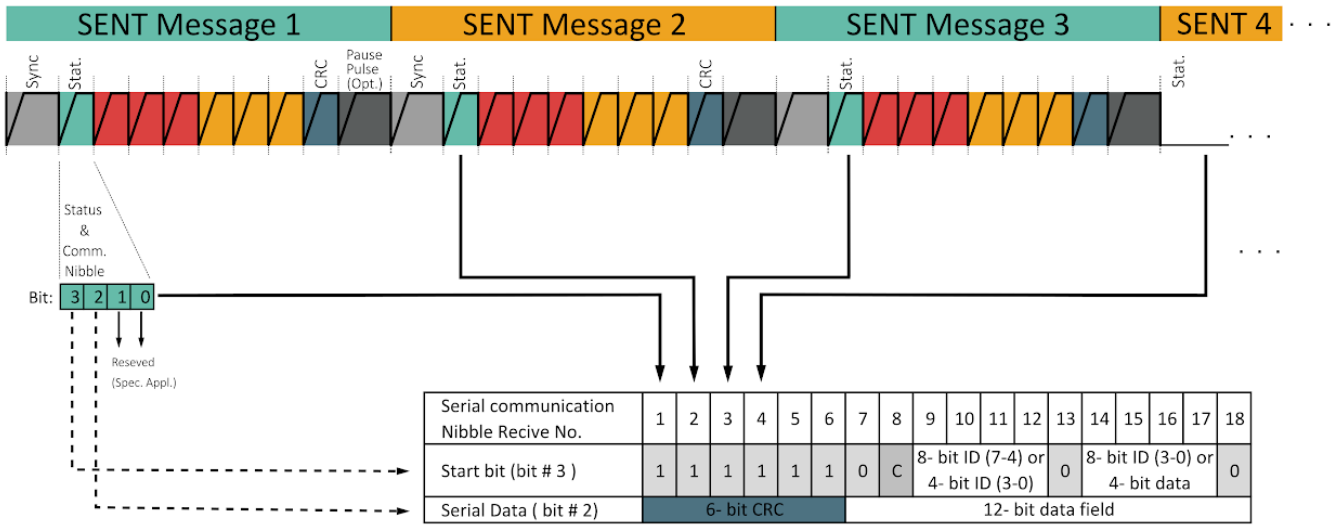


Figure 13 – Enhanced serial message

By default, a sequence consisting of a cycle of 26 data is transmitted. An extended sequence can be configured with bit SENT_SLOW_EXTENDED set to 1.

If bit SENT_SC_FORMAT=1 and bit SENT_SLOW_EXTENDED=0, the following sequence of enhanced serial messages is transmitted.

#	ID (8bits)	Definition	Value (12-bit)
1	0x01	Diagnostic error code	ESM status code
2	0x06	SENT standard revision	{8'd0, SENT_REV[3:0]}
3	0x01	Diagnostic error code	ESM status code
4	0x05	Manufacturer code	SENT_MAN_CODE
5	0x01	Diagnostic error code	ESM status code
6	0x03	Channel 1 / 2 Sensor type	SENT_SENSOR_TYPE
7	0x01	Diagnostic error code	ESM status code
8	0x07	Fast channel 1: X1	SC_X1[15:4]
9	0x01	Diagnostic error code	ESM status code
10	0x08	Fast channel 1: X2	SC_X2[15:4]
11	0x01	Diagnostic error code	ESM status code
12	0x09	Fast channel 1: Y1	H.6: SC_Y1[13:2], H.7: SC_Y1[15:4], else SC_Y1[11:0]
13	0x01	Diagnostic error code	ESM status code
14	0x0A	Fast channel 1: Y2	H.6: SC_Y2[13:2], H.7: SC_Y2[15:4], else SC_Y2[11:0]
15	0x01	Diagnostic error code	ESM status code
16	0x23	(Internal) temperature	Current temperature
17	0x01	Diagnostic error code	ESM status code
18	0x29	Sensor ID #1	SENT_SENSOR_ID1
19	0x01	Diagnostic error code	ESM status code
20	0x2A	Sensor ID #2	SENT_SENSOR_ID2
21	0x01	Diagnostic error code	ESM status code

#	ID (8bits)	Definition	Value (12-bit)
22	0x2B	Sensor ID #3	SENT_SENSOR_ID3
23	0x01	Diagnostic error code	ESM status code
24	0x2C	Sensor ID #4	SENT_SENSOR_ID4
25	0x01	Diagnostic error code	ESM status code
26	0x24	Signal strength indicator	{4'd0, SSI [7:0]}

Table 27 – SENT enhanced slow channel standard data sequence

If bit SENT_SLOW_EXTENDED is set to 1, the sequence of enhanced serial messages is extended as follows:

#	ID (8 bits)	Definition	Value (12-bit)
27	0x01	Diagnostic error code	ESM status code
28	0x90	OEM Code #1	SENT_OEM_CODE1
29	0x01	Diagnostic error code	ESM status code
30	0x91	OEM Code #2	SENT_OEM_CODE2
31	0x01	Diagnostic error code	ESM status code
32	0x92	OEM Code #3	SENT_OEM_CODE3
33	0x01	Diagnostic error code	ESM status code
34	0x93	OEM Code #4	SENT_OEM_CODE4
35	0x01	Diagnostic error code	ESM status code
36	0x94	OEM Code #5	SENT_OEM_CODE5
37	0x01	Diagnostic error code	ESM status code
38	0x95	OEM Code #6	SENT_OEM_CODE6
39	0x01	Diagnostic error code	ESM status code
40	0x96	OEM Code #7	SENT_OEM_CODE7
41	0x01	Diagnostic error code	ESM status code
42	0x97	OEM Code #8	SENT_OEM_CODE8

Table 28 – SENT enhanced slow channel extended data sequence

11.2.7.2. Short Serial Message (SSM)

The MLX90513 supports short serial messages with 8-bit data and 4-bit message ID (SAE J2716 APR2016 5.2.4.2, Figure 5.2.4.1-1) if bit SENT_SC_FORMAT is set to 0. A short serial message frame stretches over 16 consecutive SENT data messages from the transmitter. According to the standard, Serial Data bit # 2 contains a 4-bit message ID followed by an 8-bit message content and a 4-bit CRC.

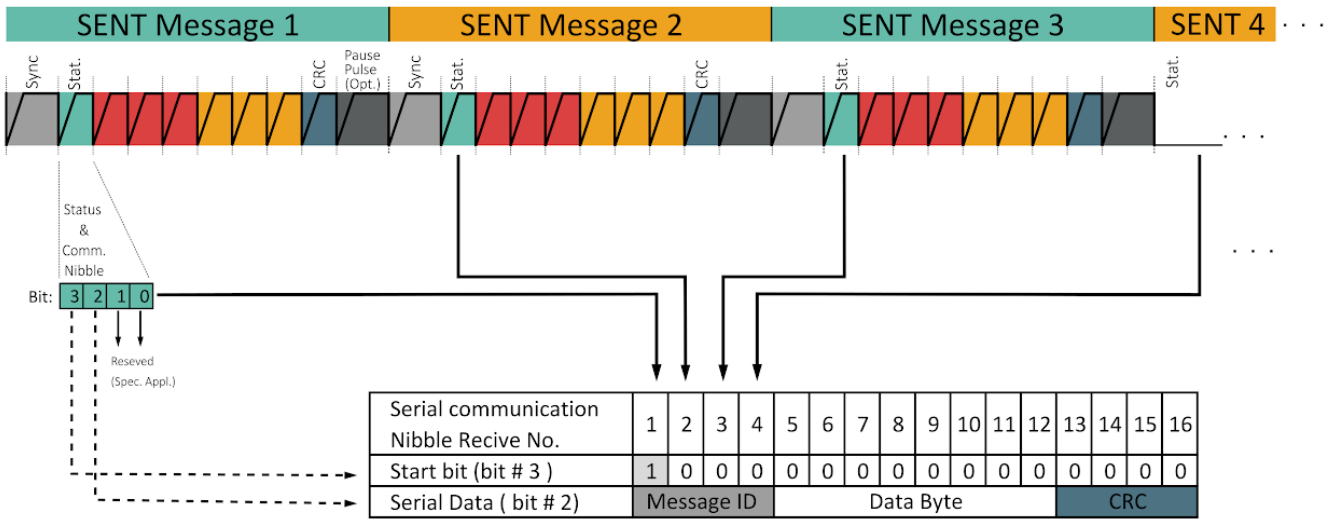


Figure 14 – Short serial message

The following sequence of 26 data is transmitted:

#	ID (4 bits)	Definition	Value (8 bit)
1	0x01	Diagnostic error code	SSM status code
2	0x06	SENT standard revision	{4'd0, SENT_REV[3:0]}
3	0x01	Diagnostic error code	SSM status code
4	0x05	Manufacturer code	SENT_MAN_CODE[11:4]
5	0x01	Diagnostic error code	SSM status code
6	0x03	Channel 1 / 2 Sensor type	SENT_SENSOR_TYPE[11:4]
7	0x01	Diagnostic error code	SSM status code
8	0x07	Fast channel 1: X1	SENT_CHANNEL_X1[15:8]
9	0x01	Diagnostic error code	SSM status code

#	ID (4 bits)	Definition	Value (8 bit)
10	0x08	Fast channel 1: X2	SENT_CHANNEL_X2[15:8]
11	0x01	Diagnostic error code	SSM status code
12	0x09	Fast channel 1: Y1	H.6: SC_Y1[13:6], H.7: SC_Y1[15:8], else SC_Y1[11:4]
13	0x01	Diagnostic error code	SSM status code
14	0x0A	Fast channel 1: Y2	H.7: SC_Y2[13:6], H.7: SC_Y2[15:8], else SC_Y2[11:4]
15	0x01	Diagnostic error code	SSM status code
16	0x02	(Internal) temperature	Current temperature
17	0x01	Diagnostic error code	SSM status code
18	0x0B	Sensor ID #1	SENT_SENSOR_ID1[11:4]
19	0x01	Diagnostic error code	SSM status code
20	0x0C	Sensor ID #2	SENT_SENSOR_ID2[11:4]
21	0x01	Diagnostic error code	SSM status code
22	0x0D	Sensor ID #3	SENT_SENSOR_ID3[11:4]
23	0x01	Diagnostic error code	SSM status code
24	0x0E	Sensor ID #4	SENT_SENSOR_ID4[11:4]
25	0x01	Diagnostic error code	SSM status code
26	0x04	Signal strength indicator	SSI

Table 29 – SENT short serial message data sequence

11.2.7.3. SSM and ESM Status Code

The 8-bit short serial message status code (SSM_SC), reporting safe state SS3, is composed as follows:

SENT SSM status code bit	Diagnostic	Description
0	Internal / acceleration error	General signal processing error, or DSP PLL unlock due to high rotor acceleration
1	Signal out of range	AGC monitor exceeds minimum gain limit or SSI monitor exceeds lower signal strength limit
2	Signal out of range	AGC monitor exceeds maximum gain limit or SSI monitor exceeds lower signal strength limit
3	LCO error	LCO amplitude or frequency error
4	Rotation too fast	Rotor frequency exceeds dynamic range of DSP PLL for application clock f_{AC}
5	Sensor short / open	PCB sensor shorted or open
6	Temperature too low	Temperature value exceeds DIAG_TEMP_THR_LO limit
7	Temperature too high	Temperature value exceeds DIAG_TEMP_THR_HI limit

Table 30 – SENT short serial message status code

All bits are independent - multiple diagnostics can trigger at the same time. The SSM status code equal to 0 indicates normal operation (no error).

The 12-bit enhanced serial message status code (ESM_SC), reporting safe state SS3, is derived from SSM_SC as per Table 31.

SSM_SC	ESM_SC
0	0
> 0	0x800 + SSM_SC

Table 31 – Enhanced serial message status code definition

11.3. Short PWM code (SPC)

The MLX90513 supports the SPC extension to enable the following features overcoming SENT limitations:

- Synchronous transmissions, whereby the master initiates the transfer

- Exact data sampling point
- Constant sampling interval, triggered by the ECU
- Bidirectional functionality to allow bus systems
- Improved data integrity and diagnosis methods, including a more efficient checksum algorithm beside several CRC methods

The physical layer properties of transmission in SPC mode are equivalent to the SENT, see section 13.2 - Single Edge Nibble Transmission (SENT) SAE J2716. The SPC mode is activated with PROTOCOL [2:0] set to 3.

11.3.1. SPC Frame Formats

The MLX90513 supports all frame formats according to SPC, and can also transmit a SENT frame in response to the master trigger pulse. See Figure 15 for all the possible SPC configurations.

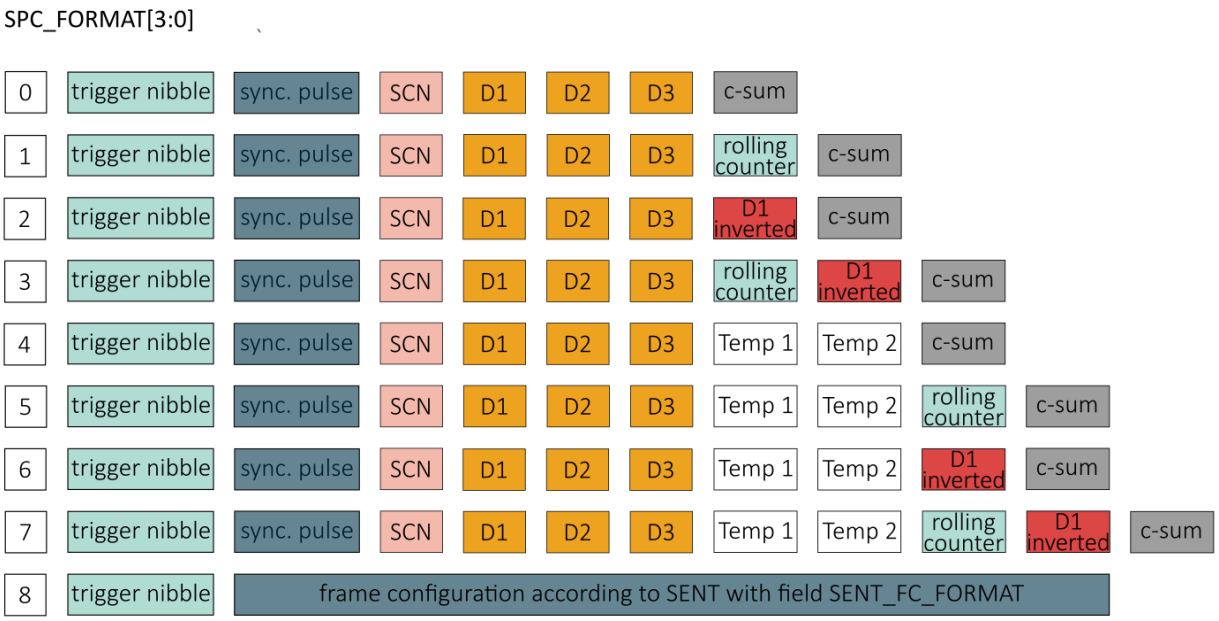


Figure 15 – SPC configurations

Fast channel 1 (CH1, 12 bit) data is transmitted with most significant nibble first (D1: MSN;D2: MidN; D3: LSN). Temp1 and Temp2 refers to the fast channel 2 (CH2) 8-bit temperature value according to SENT.

The MLX90513 implements a 4-bits SPC rolling counter which is updated on every frame transmitted, also in case the sensor is determined to be in error condition and also when the frame content with the application layer data is not updated. The rolling counter initialization is controlled by the SENT_RC_INIT as per Table 26.

The SPC frame format can be selected with the following fields:

- SPC_FORMAT [3:0] to select the content of the data nibbles (see Figure 15)

SPC_FORMAT [3:0]	SPC format
0 (default)	CH1 + c-sum
1	CH1 + rolling counter + c-sum
2	CH1 + D1 inverted + c-sum
3	CH1 + rolling counter + D1 inverted + c-sum
4	CH1 + temp(2 nibbles) + c-sum
5	CH1 + temp(2 nibbles) + rolling counter + c-sum
6	CH1 + temp(2 nibbles) + D1 inverted+ c-sum
7	CH1 + temp(2 nibbles) + rolling counter + D1 inverted + c-sum
8	frame configuration according to [SENT] with field SENT_FC_FORMAT[2:0], see section 11.2.3 [1]

Table32 – SPC format selection

[1] Frame formats according to the SENT standards are still possible and can be used for compatibility reasons.

- ID_IN_STATUS to define the SCN field (SENT status & communication nibble)

ID_IN_STATUS	SCN field status
0 (default)	the two slow-message bits are as described in Section 11.2.7
1	the two slow-message bits are replaced by the 2-bit chip ID

Table 33 – SCN field status selection

- If ID_IN_STATUS=1, SPC_SCN_BIT_ORDER defines the bit order in the SCN field:

Figure 16 – SCN bit order configurations

- SPC_CSUM_MODE[1:0] to selected the fields for the checksum (CRC) computation

SPC_CSUM_MODE [1:0]	Checksum nibble calculation method
0 (default)	c-sum = checksum only
1	c-sum = checksum + ID
2	c-sum = checksum + Rolling Counter
3	c-sum = checksum + ID + Rolling Counter

Table 34 – CRC computation selection

The checksum (CRC) calculation method can be selected via the SPC_CSUM_CFG [1:0] field:

SPC_CSUM_CFG [1:0]	Method
0, 1	SAE standard (SENT J2716 specification)
2	SPC Method “O”: check sum is a modulo-16 sum of nibble values, where each second nibble value sign is inverted
3	SPC method "E": having the simple sum as the MSB and the alternating sum as LSB

Table 35 – Checksum calculation method

11.3.2. SPC master trigger pulse, bus line handling and synchronous transmission

SPC uses a master trigger pulse, which initiates the data transmission from the slave. The master trigger pulse and its position within an SPC frame is depicted in Figure 17.

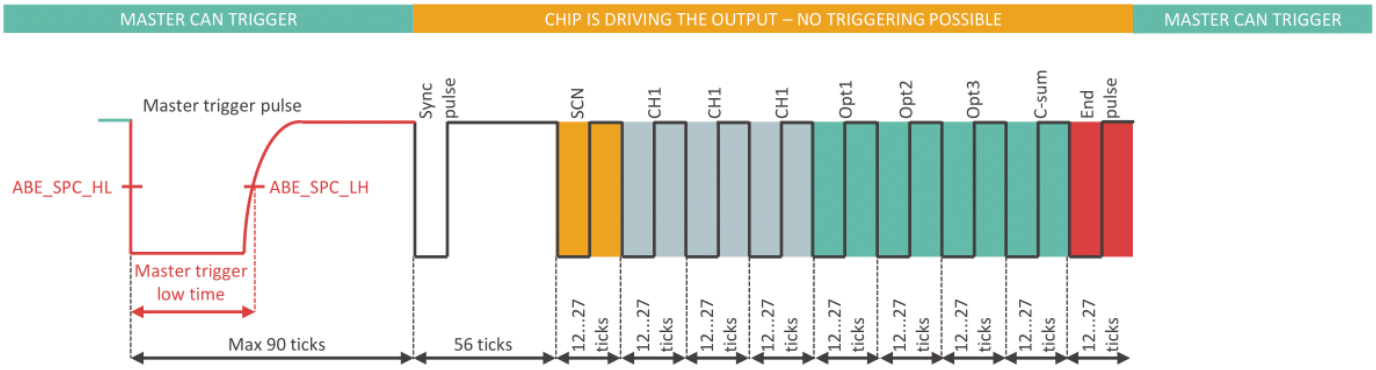


Figure 17 – SPC frame example highlighting the master trigger pulse

The MLX90513 allows to operate in a point-to-point configuration as well as in different bus modes. This is controlled by the SPC_TRIGGER_MODE [1:0] field as per Table 36.

SPC_TRIGGER_MODE [1:0]	SPC trigger mode
0	Synchronous point-to-point
1 (default)	Bus mode w/ constant length trigger pulse
2	Bus mode w/ variable length trigger pulse
3	Bus mode w/ fully overlapping trigger pulse

Table 36 – SPC trigger modes

The master trigger pulse duration in the various trigger modes is detailed in Figure 18.

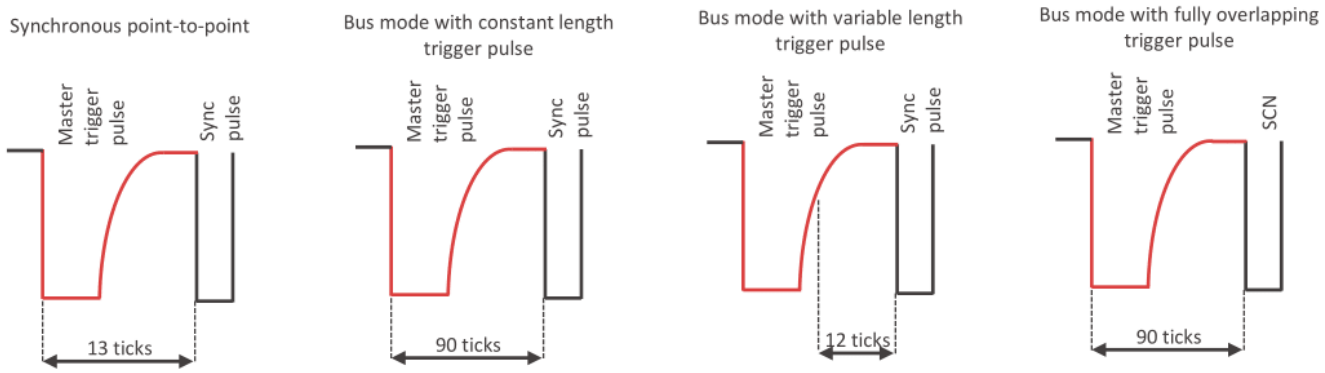


Figure 18 – SPC master trigger pulse duration

The protocol transfer is started after detection of a valid master low time as per Table 37. The threshold voltages for the detection of the falling and rising edge are detailed in Table 38. In SPC bus modes, a response frame is transmitted only if the received master trigger low time matches to the one corresponding to the configured chip ID as defined by CUS_CHIP_ID [1:0]. The fields SPC_TRIGLL_OFS0 [3:0], SPC_TRIGLL_OFS1 [3:0], SPC_TRIGLL_OFS2 [3:0], SPC_TRIGLL_OFS3 [3:0] can be used to tune the length of the valid master trigger low time. The SPC bus modes allow a parallel connection of up to 4 sensors on a common bus line.

Trigger mode	CUS_CHIP_ID [1:0]	Min [tcks]	Typ [tcks]	Max [tcks]
SPC_TRIGGER_MODE = 0	n/a	2 + SPC_TRIGLL_OFS0		5 + SPC_TRIGLL_OFS1
SPC_TRIGGER_MODE > 1	00	8 + SPC_TRIGLL_OFS0		15 + SPC_TRIGLL_OFS1
	01	16 + SPC_TRIGLL_OFS1		28 + SPC_TRIGLL_OFS2
	10	29 + SPC_TRIGLL_OFS2		49 + SPC_TRIGLL_OFS3
	11	50 + SPC_TRIGLL_OFS3		82

Table 37 – SPC master low times during trigger pulse

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master trigger pulse falling edge detection threshold	ABE_SPC_HL	1.0	1.15	1.4	V
Master trigger pulse raising edge detection threshold	ABE_SPC_LH	1.1	1.35	1.5	V
Master trigger pulse detection threshold hysteresis	ABE_SPC_Hyst	0.1	0.2	0.3	V

Table 38 – SPC master trigger pulse edges detection thresholds

After the reception of an invalid trigger pulse (e.g. non-matching ID) , the reception of further master trigger pulses is suppressed for a configurable time defined by the field SPC_BLANK_TIME [8:0], in [ticks].

11.3.3. SPC Rx-Tx transition timing

In SPC mode, during Rx mode (master pulse period), the OUT pin is in Hi-Z, while during Tx mode (frame transmission) it operates according to the ABE_AOUT_MODE [2:0] settings (refer to Section 11.5). The timing of the Hi-Z phase is defined by the SPC_OUT_ON_DLY [6:0] and SPC_OUT_OFF_DLY [8:0] fields as per Table 39 and Table 40.

SPC_OUT_ON_DLY [6:0]	
0	Hi-Z to TX transition at frame start (sync pulse falling edge)
> 0	Hi-Z to TX transition at SPC_OUT_ON_DLY ticks before the sync pulse falling edge, but only if master pulse is validated

Table 39 – SPC Hi-Z to Tx mode transition timing

SPC_OUT_OFF_DLY [8:0]	
0	TX to Hi-Z transition at end of (minimum length) pause pulse
> 0	TX to Hi-Z transition at SPC_OUT_OFF_DLY ticks after frame start (sync pulse falling edge)

Table 40 – SPC Tx to Hi-Z mode transition timing

11.3.4. SPC fast channels capturing

In SPC bus modes, data capturing is enabled only if the received master trigger pulse ID matches to the configured SPC_MEAS_ID [1:0]. This allows combining synchronized measurements with sequential data transfer on the joined bus. The rationale is that the ECU has the possibility to trigger the measurement at the same time for different sensors on the bus. The "Measurement ID" is intended to synchronize the measurement acquisition. Having a transmission buffer supports this need.

In SPC mode, angular values after signal conditioning / interpolation are captured into CH1 and CH2 with falling edge of the master trigger pulse or the SYNC pulse, depending on bit SPC_FC1_CPT_MST. An adjustable delay is controlled as in SENT mode by field SENT_FC1_CPT_DLY [6:0] [ticks].

SPC_FC1_CPT_MST	Capture timing
0 (default)	falling edge of SYNC pulse + SENT_FC1_CPT_DLY
1	falling edge of master trigger pulse + SENT_FC1_CPT_DLY

Table 41 – Capture timing selection

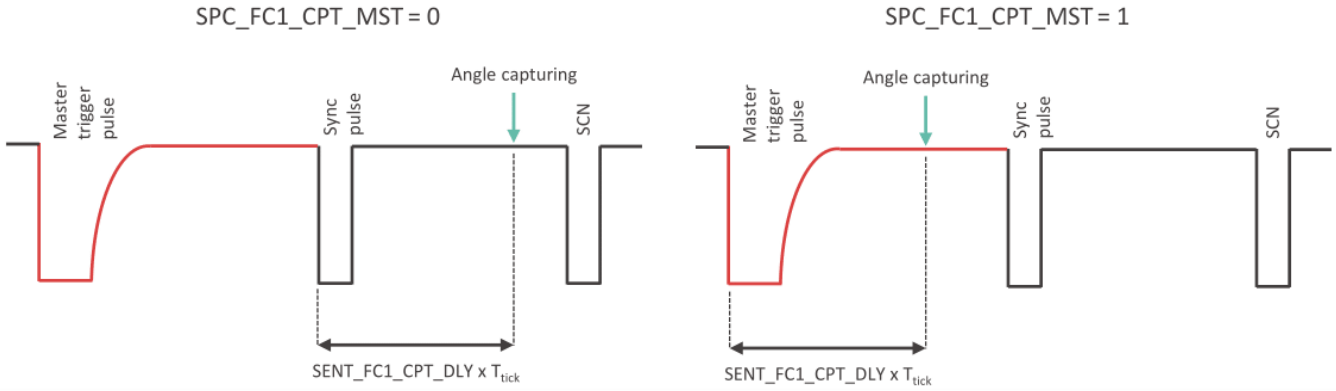


Figure 19 – SPC fast channels capturing timing

It is not recommended to program SENT_FC1_CPT_DLY to capture time later than the SCN nibbles, unless the captured value shall be transmitted with the next SENT frame.

11.4. Pulse Width Modulation (PWM)

If PROTOCOL [2:0] is set to 1, the MLX90513 performs pulse width modulation (PWM) output with a time resolution of $1/f_{AC}$.

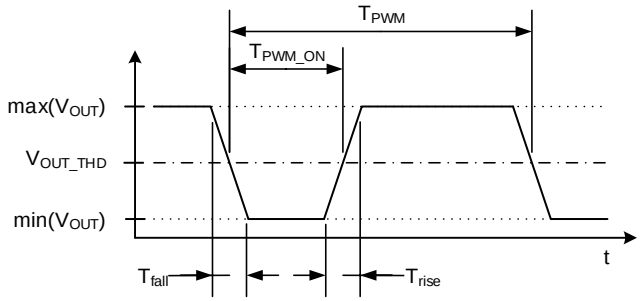


Figure 20 – PWM signal definitions

The PWM total period T_{PWM} is configured by the frame length parameter T_FRAME [15:0] and depends on the application clock frequency f_{AC}:

$$T_{PWM} = \frac{T_{FRAME}[15:0]}{f_{AC}}$$

The PWM pulse duration T_{PWM_ON} is proportional to the angular value after signal conditioning (φ_{SC}) and interpolation, captured at the beginning of the PWM period:

$$T_{PWM\_ON} = \frac{\varphi_{SC}[15:0]}{f_{AC}}$$

As a consequence, the lower and upper limit of the PWM pulse duration as well as the fault band value are defined by SC_Y1, SC_Y2 and SC_YE respectively, see section 10.6.5. This implies that T_{PWM} must be greater/equal to the maximum pulse duration defined by the signal conditioning. This is achieved on the following condition:

$$T_{FRAME} > \max(SC\_Y1, SC\_Y2, SC\_YE)$$

Note that the finite rise/fall times (see section 11.5) constraints the minimum and maximum pulse durations. This is achieved by respecting the following formulas:

$$\min(SC\_Y1, SC\_Y2, SC\_YE) \geq \max(T_{rise}, T_{fall}) \cdot f_{AC}$$

$$\max(SC\_Y1, SC\_Y2, SC\_YE) \leq T_{FRAME} - \max(T_{rise}, T_{fall}) \cdot f_{AC}$$

The polarity of the PWM pulse can be adjusted with bit SENTPWM_INV. If SENTPWM_INV = 0 (default), the low-state duration is proportional to the transmitted data (T_{PWM_ON}), else the high-state respectively.

11.4.1. PWM Performance Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
PWM output resolution	R_{PWM}		12	16	bit	
PWM frequency tolerance	df_{PWM}	-5.0		5.0	%	
PWM frequency range	f_{PWM}	100.0		5000.0	Hz	f_{AC} adapted
PWM duty cycle jitter [1]	J_{DC}	-0.03		0.03	%	
PWM period jitter [1]	J_{PWM}	-500		500	ns	
PWM T_{ON} drift				250	ns	ABE_AOUT_MODE = 3 ABE_AOUT_SR = 0
PWM T_{ON} offset		-1.5		1.5	µs	ABE_AOUT_MODE = 3 ABE_AOUT_SR = 0

Table 42 – PWM timing specifications

[1] ±3σ values

To compensate for mismatches between the rising and falling edge delays, the field PWM_DC_OFS [8:0] (signed) can be used to adjust the T_{PWM_ON} time by adding to T_{PWM_ON} a systematic offset ΔT_{PWM_ON} according to the following formula:

$$\Delta T_{PWM\_ON} = \frac{\text{PWM\_DC\_OFS}[8:0]}{f_{AC}}$$

11.5. Physical Layer Output configuration

For the analog output the MLX90513 OUT driver must be configured with ABE_AOUT_MODE [2:0] as per Table 43 , which specifies in addition the relevant programmable delay compensation field relative to this mode (refer to section 10.6.4).

ABE_AOUT_MODE [2:0]	Output configuration	Programmable delay compensation field
0	Analog OUT configuration	DELAY_AOUT_0 [7:0]

Table 43 – OUT mode selection for analog mode

For digital protocols (SENT and PWM), the MLX90513 OUT driver can be configured with field ABE_AOUT_MODE [2:0] as per Table 44, which specifies in addition the relevant programmable delay compensation field for the selected configuration.

ABE_AOUT_MODE [2:0]	Output configuration	Programmable delay compensation field
1	binary modulation with open-drain-NMOS	DELAY_AOUT_1 [7:0]
2	binary modulation with open-drain-PMOS	DELAY_AOUT_2 [7:0]
3	binary modulation with push-pull	DELAY_AOUT_3 [7:0]
4 (default)	digital pulse-shaping with improved emissions, 5 V amplitude	DELAY_AOUT_4 [7:0]
5	digital pulse-shaping with improved emissions, 3.3 V amplitude	DELAY_AOUT_5 [7:0]

Table 44 – OUT mode selection for SENT/PWM output mode

For binary modulation modes, the resistive load on pin OUT, e.g. the external pull-up or pull-down resistor should be carefully selected, because the MLX90513 has a built-in high order low pass filter. A large resistive load will deteriorate the generated SENT/SPC signal, and could make the output signal not comply to the SENT/SPC specifications, such as the fall times and the minimum output voltages. The values in Table 59 should be considered, which means it is not recommended to have a resistive load value smaller than 10kΩ, and a resistive load value smaller than 3kΩ should be avoided. The maximum output resistive load value should be less than 55kΩ to avoid unexpected impact from leakage current.

Furthermore, the output capacitance should also be properly chosen, together with the output resistive load to correspondingly match the application, e.g. tick time, to allow appropriate time constant for the transmission of the SENT/SPC signal.

11.5.1. Open Drain and Push-Pull Mode

The following table for rise (T_{rise}) and fall (T_{fall}) times refer to the binary driven output modes (ABE_OUT_MODE [2:0] in [1,2,3]). The rise/fall times for the digital pulse-shaped mode (ABE_OUT_MODE = 4) are listed in section 11.5.2. Slower rise/fall times are achieved by setting ABE_AOUT_SR to 1.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Rise Time	T_{rise_pp}	1.0	2.0	4.0	µs	ABE_AOUT_MODE=2, 3 ABE_AOUT_SR=0, C_{OUT}<10nF, step 30%-70% of VS
Fall Time	T_{fall_pp}	1.0	2.0	4.0	µs	ABE_AOUT_MODE=1, 3 ABE_AOUT_SR=0, C_{OUT}<10nF, step 70%-30% of VS
Slow Rise Time	$T_{rise\_pp\_slow}$	2.0	3.5	5.5	µs	ABE_AOUT_MODE=3 ABE_AOUT_SR=1, C_{OUT}<15nF, step 30%-70% of VS
Slow Fall Time	$T_{fall\_pp\_slow}$	2.0	3.5	5.5	µs	ABE_AOUT_MODE=3 ABE_AOUT_SR=1, C_{OUT}<15nF, step 70%-30% of VS
Fall Time NMOS open-drain mode	T_{fall_od}	4.0	7.5	15.0	µs	ABE_AOUT_MODE=1, C_{OUT}=10nF, R_{PU}=10kOhm, VS_PU=18V, step 30%-70% of VS_PU

Table 45 – Rise and fall time for open drain and push-pull modes

11.5.2. Digital Pulse Shaping

With ABE_AOUT_MODE = 4, 5 the MLX90513 supports digital pulse shaping for binary modulation modes for improved EMC emissions and reduced dependency on external load components. For ABE_AOUT_MODE = 4, the output voltage range is 5 V, while for ABE_AOUT_MODE = 5 the output voltage range is 3.3 V. The slope of the pulse shaping is dependent on SENT_TICK_TIME [2:0] as per Table 46. For SENT/SPC the pulse shaping defines the nibble falling and rising slopes, with rise time slower than fall time. In PWM mode the pulse shape on rising and falling edge are inverse and symmetrical around VS/2 and leading to equal rise and fall time. Pulse shaping does not influence duty cycle and period of the modulation when measured at VS/2. The MLX90513 internally compensates for digital processing delays of the pulse shaping.

SENT_TICK_TIME	SENT Fall Time [us] 90% to 10%	SENT Rise Time [us] 10% to 90%	PWM Fall/Rise Time [us] 10% to 90%
0, 1	1.0	2.2	1.0
2	2.0	4.4	2.0
3	3.0	6.6	3.0
4	6.0	13.2	6.0
else	12.0	26.4	12.0

Table 46 – Rise and fall time for pulse shaping mode

In SENT mode, the length of the pulse shaping low time can be configured by setting the field SENT_PS_PWT[3:0]. This defines a delay *T* between the end of the falling slope and the beginning of the rising slope according to the following formula:

$$T = \frac{SENT\_PS\_PWT + 1}{f_{AC}}$$

12. Identification Items

To ensure traceability and unique identification of the individual parts, the user disposes of six fields that can be freely programmable to arbitrary values: USER_ID0 … USER_ID5 [7:0].

13. Functional Safety

The IC is designed compliant to ISO26262 and reaches ASIL B metrics, while the rigor of the development is according to ASIL C.

13.1. Safety Manual

The safety manual, available upon request, contains the necessary information to integrate the MLX90513 component in a safety related item, as Safety Element Out-of-Context (SEooC).

In particular, it includes:

- The description of the Product Development lifecycle tailored for the Safety Element
- An extract of the Technical Safety concept
- The description of Assumptions-of-Use (AoU) of the element with respect to its intended use, including:
  - assumption on the device safe state
  - assumptions on fault tolerant time interval and multiple-point faults detection interval
  - assumptions on the context, including its external interfaces
- The description of safety analysis results at the device level useful for the system integrator; HW architectural metrics and description of dependent failures initiators
- The description and the result of the functional safety assessment process, the list of confirmation measures and the description of the independency level.

13.2. MLX90513 Safety goal

Description	Electrical Angle error	ASIL	FHTI
Internal failures in sensors which lead to signaling a false but valid angle shall be detected and signal shall be marked as invalid.	+/- 3° el.	ASIL C	5 ms
Failures on coils and target wheel, and on sensor pins shall be diagnosed and signal shall be marked as invalid.			

Table 47 – Functional safety specification

13.3. Safe States

13.3.1. Safe State 0

An optional Safe State 0 (SS0) can be enabled by setting the field EN_POR_RDY to 1. If enabled, Safe State 0 is issued during the transition between Safe State 1 and normal operating mode. In SS0 the sensor application function is active and the LCO is enabled. Indication of SS0 is made by actively driving the output to the opposite fault band value specified by the field PULL_DIR for a period until no fault is present, but at least according to the field EH_MIN_PERIOD, see section 13.3.3 for the definition of these parameters.

13.3.2. Safe State 1

In Safe State 1 (SS1) the IC OUT pin is switched to tri-state (Hi-Z). SS1 is issued after power on reset (POR) during boot phase until a the EEPROM content has been verified. In SS1 the sensor application function is not active and the LCO is disabled. The IC indicates failure band high or low depending on the use of a pull-up or pull-down resistor at the corresponding ECU input, respectively.

13.3.3. Safe State 2

In Safe State 2 (SS2) the IC OUT pin is switched to tri-state (Hi-Z). SS2 is to be used for all faults after start-up that might affect the controlled reporting via the output interface (SS3), except of digital brown-out.

To speed-up the transition from the valid signal range to the failure band region, the OUT pin is actively driven to the failure band for a duration defined in the EEPROM register EH_DRV_SS2_PERIOD [5:3]. The active failure band transition can be bypassed if EH_DRV_SS2_PERIOD [5:3] is set to 0. After the transition, the output will go in Hi-Z mode. Note that during the active drive phase, if a pull-up resistor is used, the output will follow the IC supply voltage, which may be different from the ECU supply voltage, even in case of IC supply overvoltage conditions.

In SS2 the sensor application function and the LCO stays active as far as possible. In conjunction with a pull-up resistor R_{PU} to VS placed at the corresponding ECU inputs, the IC indicates failure-band-high. The EEPROM register PULL_DIR shall be programmed to 1 in this case. In conjunction with a pull-down resistor R_{PD} to GND placed at the corresponding ECU inputs, the IC indicates failure-band-low; the EEPROM register PULL_DIR shall be programmed to 0 in this case.

13.3.4. Safe State 3

Safe State 3 (SS3) is the default reporting mode for all faults which do not affect the operation of the output interface. In SS3 the output interface remains active and reports the fault as part the protocol as follows:

Interface	SS3 reporting
SENT/SPC	Pin OUT transmits a SENT frame with following characteristics: • status bit 0 which is set to 1 • fast channel 1 data is set to a programmed value that indicates a fault band, e.g Reserved Signaling Range 4089 .. 4095 as defined in SENT Standard Section E.1.2. Reserved signaling ranges, or equal 0 • the serial message status is non-zero indicating the fault source, see section 11.2.7.3

Interface	SS3 reporting
PWM	Pin OUT PWM signal is set to a programmed duty-cycle that indicates a fault band, or Hi-Z if this is not possible
ANALOG	Pin OUT Analog signal is set to a programmed voltage that indicated a fault band, or Hi-Z if this is not possible

Table 48 – SS3 reporting overview per interface

Note:

- The "programmed value / duty-cycle / voltage" for all interfaces is defined by SC_YE [15:0] (see section 10.6.5). The IC verifies if this value is set outside the signaling band between SC_Y1 [15:0] and SC_Y2 [15:0]. If this is violated the device reports SS2.

13.4. Safety Mechanism and Monitors

The MLX90513 provides numerous self-diagnostic features (safety mechanisms). Those features increase the robustness of the IC functionality by preventing the IC to provide an erroneous output signal. Table 49 provides the monitors list. For more details on the main sensor related monitors, refer to the next subsections. For the exhaustive description of the monitors, refer to the safety manual.

Category and Safety mechanism name	Reporting Mode	FHTI type [1]
AFE / Sensor Diagnostics		
LCO amplitude monitor	SS2	1
LCO period monitor	SS3	1
LCO overcurrent monitor	SS3	3
Sensor short / loss monitor	SS3	3
Frontend monitor	SS3	1
AGC monitor	SS3	1
ADC linearity test	SS3	2
Digital-IC Diagnostics		
RCO monitor	SS2	1
EEPROM double-bit protection	SS2	1
EEPROM shadow register monitor	SS2	2
DSP scheduler monitor	SS3	1
DSP PLL lock monitor	SS3	1

Category and Safety mechanism name	Reporting Mode	FHTI type [1]
DSP speed monitor	SS3	1
DSP delay compensation monitor	SS3	1
SSI monitor	SS3	1
ABE / Interface Diagnostics		
ABE / DAC monitor	SS2	2
PWM monitor	SS2	1
SENT Frame Counter, CRC and redundant Nibble	n/a	1
Supply System Diagnostics		
Supply voltage monitors	SS2	3
External supply over-voltage monitor	SS2	3
Digital supply under-voltage monitor	POR	3
Bias current monitor	SS2	2
AFE voltage reference monitor	SS2	2
Ground comparator monitors	SS2	3
Temperature sensor monitor	SS3	2
Over/-Under-temperature monitor	SS3	2
Maximum temperature monitor	SS2	2
Mechanisms on start-up only		
EEPROM content CRC	SS1	n/a
Supply system and ground comparator LF checks	SS1	n/a
Sensor monitor LF checks	SS1	n/a
LCO frequency monitor LF check	SS1	n/a

Table 49 – List of diagnostics

[1] FHTI types are defined in Table 54

13.4.1. LCO Frequency Monitor

The LCO frequency is monitored by an RCO based counter over a fixed window of 16 periods of the LC clock. The limits can be adjusted by using the fields LC_P_MON_LIM_LO [7:0] and LC_P_MON_LIM_HI [7:0] in steps

of $1/f_{RCO}$. In order to ensure detection of LCO frequencies beyond a threshold value of $f_{LCO_{max}}$ and below a threshold value of $f_{LCO_{min}}$, the following formulas can be used to compute the limits:

$$\mathrm{LC\_P\_MON\_LIM\_LO} = \mathrm{int}\left(\mathrm{f_{RCO_{min}}} * {}^{16}/_{\mathrm{f_{LCO_{max}}}}\right)$$
$$\mathrm{LC\_P\_MON\_LIM\_HI} = \mathrm{int}\left(\mathrm{f_{RCO_{max}}} * {}^{16}/_{\mathrm{f_{LCO_{min}}}}\right)$$

13.4.2. Signal strength monitor

The signal strength monitor (SSI monitor) compares the measured signal strength (A_{Rotor}) with programmable high and low limits defined by the DIAG_SSI_HI [7:0] and DIAG_SSI_LO [7:0] fields. The corresponding A_{Rotor_High} and A_{Rotor_Low} signal strength limits are linked to the values of DIAG_SSI_HI and DIAG_SSI_LO, respectively, by the gain parameter G:

$$A_{Rotor\_High} = G \cdot DIAG\_SSI\_HI$$
$$A_{Rotor\_Low} = G \cdot DIAG\_SSI\_LO$$

Parameter	Symbol	Min.	Typ.	Max.	Unit
SSI monitor gain	G	0.56	0.59	0.62	mV/LSB

Table 50 – SSI monitor gain

13.4.3. Sensor Monitor

The sensor coil system is monitored and reporting is done via the interfaces. There are two short detection monitors built in (see Figure 21 and Figure 22) and one open or high ohmic connection monitor (see Figure 21).

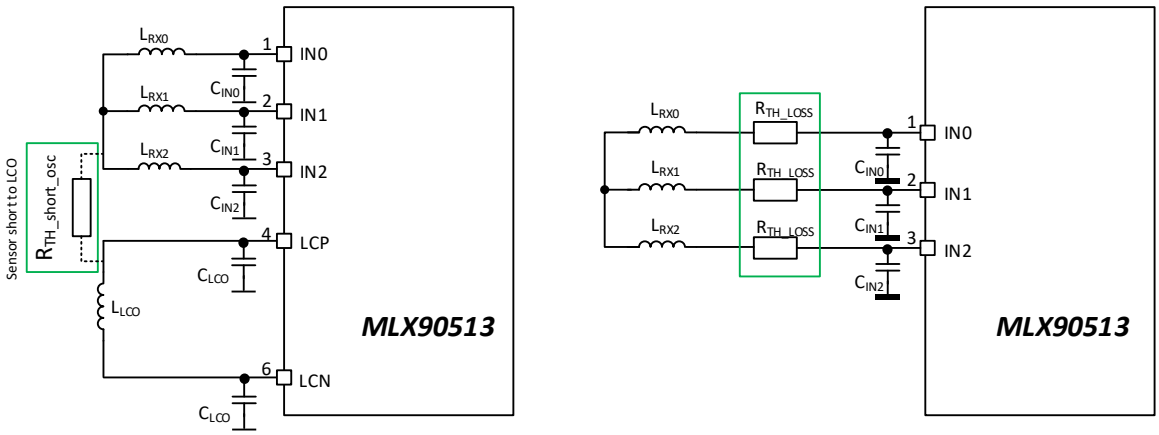


Figure 21 – Left: Rx to Tx coil short detection, Right: sensor loss detection

The short detection monitor shown in Figure 22 targets multi-sensor modules using two sensor coil systems within one inductive sensor system, for example a redundant coil system. In this case the sensor bias for each of the coil systems need to be biased at different voltages (see section 10.3.2).

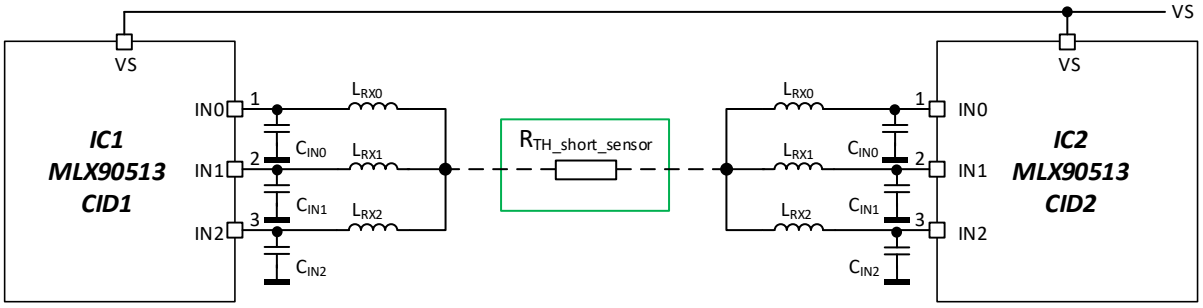


Figure 22 – Multi-sensor module. Sensor coil system #1 to sensor coil system #2 short detection

The characteristics of the sensor monitor are given in Table 51.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Rx coil(s) to Tx coil short detection threshold resistance	$R_{TH\_short\_osc}$	100		300	kΩ	Short between Rx and Tx coil(s)
Sensor loss detection resistance threshold	R_{TH_loss}	30		120	kΩ	
Rx coil 1 to Rx coil 2 short detection threshold resistance	$R_{TH\_short\_sensor}$	20		80	kΩ	Short between two sensors with different CID settings

Table 51 – Sensor monitor functions

13.4.4. Supply System Monitoring

The MLX90513 has a supply monitoring system to detect under and overvoltage events. Figure 23 describes the operating modes as a function of VS supply range including start-up, VS undervoltage (red), VS normal operating range (green) and VS overvoltage range (yellow). The supply system undervoltage and overvoltage monitors are described in Table 52 whereas the POR levels are described in Table 5.

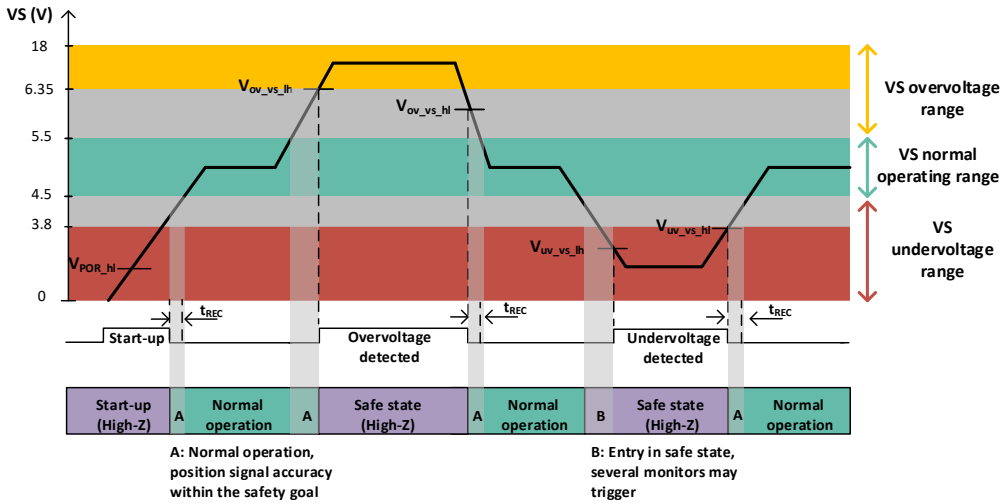


Figure 23 – MLX90513 operating modes

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VS undervoltage detection	$V_{uv\_vs\_lh}$	3.23	3.50[1]	3.73	V	VS decreasing
	$V_{uv\_vs\_hl}$	3.55	3.80	4.03	V	VS rising
VS overvoltage detection	$V_{ov\_vs\_lh}$	6.05	6.35	6.55	V	VS rising
	$V_{ov\_vs\_hl}$	5.80	6.05	6.20	V	VS decreasing
VS voltage detection hysteresis	V_{hyst_vs}		0.3		V	

Table 52 – Supply system monitoring

[1] Several safety monitors may trigger when VS is below 4.5V

13.4.5. Temperature Monitors

The temperature limits below and beyond which the IC reports SS3 can be configured by setting the fields DIAG_TEMP_THR_LO and DIAG_TEMP_THR_HI, respectively, refer to section 14.2.

The maximum temperature monitor threshold beyond which the IC reports SS2 state can be configured by setting the field DIAG_TEMP_THR_MAX. Factory programming ensures this value is set to 170°C, refer to section 14.2.

13.5. Fault Handling Time Interval

The fault handling time (FHTI) is composed of several contributions, defined in Table 53.

Time	Definition
DTI	Diagnostic Time Interval: worst-case time between 2 consecutive runs of a specific diagnostic
EXE	Execution Time: worst-case time between the measurement start of a given diagnostic and the availability of the result of this measurement
REP	Reporting Time: worst-case time needed between an internal diagnostic error event and a switch of the output to fail-safe state
FHTI	Fault Handling Time Interval: the time interval between the start of the first frame with invalid position value without notice, and the end of the last frame preceding a fail-safe state of the IC. It is calculated as the sum of DTI, EXE, and REP figures. The following equation is valid for any diagnostic: FHTI = DTI + EXE + REP

Table 53 – Time interval definition

The MLX90513 categorizes the FHTI according to Table 54.

FHTI Type	Description	DTI	EXE/REP	FHTI
1	Digital type monitor, running continuously, no de-bouncing	<100 µs * f_{RCO} / f_{AC}	<1 µs * f_{RCO}/ f_{AC}	≅ DTI
2	ADC BIST cycle based monitor	416 µs * f_{RCO} / f_{AC}	<1 µs * f_{RCO}/ f_{AC}	≅ DTI

FHTI Type	Description	DTI	EXE/REP	FHTI
3	Analog type monitor, with de-bouncing	continuously (analog)	160 µs	~160µs

Table 54 – FHTI type definition

13.5.1. Transition from a Safe State into Normal Operation

When all safety mechanisms indicate return to operational conditions within the safety goal, the output exits safe state and returns to operating mode. With EEPROM register EH_MIN_SS_PERIOD [2:0], a minimum period for the safe state indication can be programmed to support the detection of a safe state in the ECU. Note that EH_MIN_SS_PERIOD does not only apply to transitions from safe state to normal operating mode, but also to transitions from any safe state into another safe state.

14. Description of Memory and Registers

14.1. Device Version

This section depicts the IC version.

Field	Address	Bit	R/W	Default	Description
ANA_VERSION	138	[7:0]	R	0xCA	Analog version
DIG_VERSION_L		[15:8]	R	145	Digital version (8 LSB)
DIG_VERSION_H	140	[15:0]	R	353	Digital version (16 MSB)

Table 55 – Device version memory block map

14.2. EEPROM

The EEPROM (non-volatile memory) allows accessing the device configurations and calibration values. Both programming and register reading, are supported by using the PTC04 programming tool.

Field	Address [1]	Bit	R/W	Default	Description
CID	512 (250)	[1:0]	R/W	0	Chip ID for sensor monitor. Defines sensor DC operating point
Reserved		2	R/W	1	Do not modify
PULL_DIR		3	R/W	1	Output pull resistor connection; 1: pull-up 0: pull-down
CUS_CHIP_ID		[6:5]	R/W	0	Device ID for MUPeT PGI or SPC. IC addressable via MUPeT SAD command, if MLX_CHIP_ID=0
LC_OSC_EN		7	R/W	1	LCO enable
LC_OSC_AMP		8	R/W	0	LCO amplitude: 0: full amplitude; 1: half amplitude
Reserved		[12:9]	R/W	0	Do not modify

Field	Address [1]	Bit	R/W	Default	Description
AC_SEL		[15:13]	R/W	3	Application clock selector: 3: 10MHz; 5: 5MHz; 6: 1MHz; else 20MHz
ABE_OUT_MODE	514 (320)	[2:0]	R/W	4	Analog backend output mode: 0: Analog output (12 bit); 1: Digital output with open-drain-NMOS; 2: Digital output with open-drain-PMOS; 3: Digital output with Push-Pull; 4: Digital output with improved emission, 5V 5: Digital output with improved emission, 3.3V
ABE_AOUT_SR		3	R/W	0	ABE_AOUT_MODE in [1,2,3]: Slew rate in binary output modes: 0: fast, 1: slow ABE_AOUT_MODE = [0, 4]: 1: improved emission > 400 kHz
PROTOCOL		[6:4]	R/W	2 (-100 option code) 3 (-180 option code)	Output protocol: 0: SENT without pause; 1: PWM; 2: SENT with pause; 3: SPC; 4:Analog output
SENTPWM_INV		7	R/W	0	Invert binary waveforms (SENT / PWM) & pulse shaping
Reserved		8	R/W	1	Do not modify
EN_ALF		12	R/W	1	DSP phase tracking adaptive loop filter control enable
LFC		[14:13]	R/W	0	DSP phase tracking adaptive loop filter control: if EN_ALF==0, values [0..3] select a fixed loop filter bandwidth (BW) setting [lowest .. highest] BW if EN_ALF==1, values [0..3] select the lower bound BW of the adaptive loop filter control
DC01_CONST	516 (252)	[15:0]	R/W	0	DC Offset Compensation constant for channel D01
DC12_CONST	518 (254)	[15:0]	R/W	0	DC Offset Compensation constant for channel D12
DC20_CONST	520 (256)	[15:0]	R/W	0	DC Offset Compensation constant for channel D20
EH_MIN_SS_PERIOD	522 (258)	[2:0]	R/W	5	Minimum period the device will remain in safe state If>0, T=2^(9+EH_MIN_SS_PERIOD)/ f_{AC} µs, else 0
EH_DRV_SS2_PERIOD		[5:3]	R/W	2	Period the device will actively drive to fault-band If>0, T=2^(9+EH_DRV_SS_PERIOD)/ f_{AC} µs, else 0

Field	Address [1]	Bit	R/W	Default	Description
EN_POR_RDY		6	R/W	0	1: Readiness after POR is indicated by inverse failure-band after latent fault checks for period according to EH_MIN_SS2_PERIOD
AGC_GAIN_MAX		[9:7]	R/W	4	AGC: maximum PGA gain setting, range [0..4]
AGC_GAIN_MIN		[12:10]	R/W	0	AGC: minimum PGA gain setting, range [0..4]
PEQ_GAIN		[15:13]	R/W	0	Phase Equalizer gain. If > 0, phase offsets are POFSxx[15:0] = signed(PEQxx) * 2^(PEQ_GAIN-1) , else 0
PEQ00	524 (260)	[7:0]	R/W	0	Linearization value at 0/32 * 360 deg
PEQ01		[15:8]	R/W	0	Linearization value at 1/32 * 360 deg
PEQ02	526 (262)	[7:0]	R/W	0	Linearization value at 2/32 * 360 deg
PEQ03		[15:8]	R/W	0	Linearization value at 3/32 * 360 deg
PEQ04	528 (264)	[7:0]	R/W	0	Linearization value at 4/32 * 360 deg
PEQ05		[15:8]	R/W	0	Linearization value at 5/32 * 360 deg
PEQ06	530 (266)	[7:0]	R/W	0	Linearization value at 6/32 * 360 deg
PEQ07		[15:8]	R/W	0	Linearization value at 7/32 * 360 deg
PEQ08	532 (268)	[7:0]	R/W	0	Linearization value at 8/32 * 360 deg
PEQ09		[15:8]	R/W	0	Linearization value at 9/32 * 360 deg
PEQ10	534 (270)	[7:0]	R/W	0	Linearization value at 10/32 * 360 deg
PEQ11		[15:8]	R/W	0	Linearization value at 11/32 * 360 deg
PEQ12	536 (272)	[7:0]	R/W	0	Linearization value at 12/32 * 360 deg
PEQ13		[15:8]	R/W	0	Linearization value at 13/32 * 360 deg
PEQ14	538 (274)	[7:0]	R/W	0	Linearization value at 14/32 * 360 deg
PEQ15		[15:8]	R/W	0	Linearization value at 15/32 * 360 deg
PEQ16	540 (276)	[7:0]	R/W	0	Linearization value at 16/32 * 360 deg
PEQ17		[15:8]	R/W	0	Linearization value at 17/32 * 360 deg

Field	Address [1]	Bit	R/W	Default	Description
PEQ18	542 (278)	[7:0]	R/W	0	Linearization value at 18/32 * 360 deg
PEQ19		[15:8]	R/W	0	Linearization value at 19/32 * 360 deg
PEQ20	544 (280)	[7:0]	R/W	0	Linearization value at 20/32 * 360 deg
PEQ21		[15:8]	R/W	0	Linearization value at 21/32 * 360 deg
PEQ22	546 (282)	[7:0]	R/W	0	Linearization value at 22/32 * 360 deg
PEQ23		[15:8]	R/W	0	Linearization value at 23/32 * 360 deg
PEQ24	548 (284)	[7:0]	R/W	0	Linearization value at 24/32 * 360 deg
PEQ25		[15:8]	R/W	0	Linearization value at 25/32 * 360 deg
PEQ26	550 (286)	[7:0]	R/W	0	Linearization value at 26/32 * 360 deg
PEQ27		[15:8]	R/W	0	Linearization value at 27/32 * 360 deg
PEQ28	552 (288)	[7:0]	R/W	0	Linearization value at 28/32 * 360 deg
PEQ29		[15:8]	R/W	0	Linearization value at 29/32 * 360 deg
PEQ30	554 (290)	[7:0]	R/W	0	Linearization value at 30/32 * 360 deg
PEQ31		[15:8]	R/W	0	Linearization value at 31/32 * 360 deg
DELAY_AOUT_0	556	[7:0]	R/W	18	Analog processing delay for ABE_AOUT_MODE=0, range [0:255] * 26/8 / f_RCO
DELAY_AOUT_1		[15:8]	R/W	18	Analog processing delay for ABE_AOUT_MODE=1, range [0:255] * 26/8 / f_RCO
DELAY_AOUT_2	558	[7:0]	R/W	18	Analog processing delay for ABE_AOUT_MODE=2, range [0:255] * 26/8 / f_RCO
DELAY_AOUT_3		[15:8]	R/W	18	Analog processing delay for ABE_AOUT_MODE=3, range [0:255] * 26/8 / f_RCO
DELAY_AOUT_4	560	[7:0]	R/W	18	Analog processing delay for ABE_AOUT_MODE=4, range [0:255] * 26/8 / f_RCO
DELAY_AOUT_5		[15:8]	R/W	18	Analog processing delay for ABE_AOUT_MODE=5, range [0:255] * 26/8 / f_RCO
Reserved	562	[7:0]	R/W	107	Do not modify

Field	Address [1]	Bit	R/W	Default	Description
DELAY_PS		[15:8]	R/W	25	Digital processing delay for SENT/SPC/PWM pulse shaping (ABE_AOUT_MODE>=4), range [0:63] * 26/32 / f_RCO * N_tick, with N_tick=[1,1,2,3,6,12] for tick times [0.5,0.75,1.0,1.5,3.0,6.0]us
PHASE_OFS	564 (292)	[15:0]	R/W	0	Phase/Angle offset before signal conditioning, resolution 360/2^16 deg (signed 2's-complement)
SC_X1	566 (294)	[15:0]	R/W	0	Signal conditioning: X1, input range low
SC_X2	568 (296)	[15:0]	R/W	0	Signal conditioning: X2, input range high
SC_Y1	570 (298)	[15:0]	R/W	205	Signal conditioning: Y1, output range low
SC_Y2	572 (300)	[15:0]	R/W	3891	Signal conditioning: Y2, output range high
SC_YE	574 (302)	[15:0]	R/W	3994	Signal conditioning: output fault band level in SS3, if min(SC_Y1,SC_Y2) <= SC_YE <= max (SC_Y1,SC_Y2) and PROTOCOL = [1,4], SS3 changes to SS2 (OUT to Hi-Z).
T_FRAME	576 (304)	[15:0]	R/W	4095	Frame period: SENT: frame length [ticks] = T_FRAME[11:0] PWM mode: PWM period [1/f_{AC}]
USER_ID0	578	[7:0]	R/W	0	Reserved for end-user to program information to keep traceability
USER_ID1		[15:8]	R/W	0	Reserved for end-user to program info to keep traceability
USER_ID2	580	[7:0]	R/W	0	Reserved for end-user to program info to keep traceability
USER_ID3		[15:8]	R/W	0	Reserved for end-user to program info to keep traceability
USER_ID4	582	[7:0]	R/W	0	Reserved for end-user to program info to keep traceability
USER_ID5		[15:8]	R/W	0	Reserved for end-user to program info to keep traceability
SPC_FORMAT	584 (306)	[3:0]	R/W	0	SPC frame format: 0: data + checksum (default) 1: data + rolling counter + checksum 2: data + inverted nibble + checksum 3: data + rolling counter + inverted nibble + checksum 4: data + temp(2 nibbles) + checksum 5: data + temp(2 nibbles) + rolling counter +

Field	Address [1]	Bit	R/W	Default	Description
					checksum 6: data + temp(2 nibbles) + inverted nibble + checksum 7: data + temp(2 nibbles) + rolling counter + inverted nibble + checksum 8: frame configuration set according to SENT_FC_FORMAT[2:0]
SPC_MEAS_ID		[6:5]	R/W	0	SPC master pulse ID to trigger angle measurement
SPC_TRIGGER_MODE		[8:7]	R/W	1	SPC trigger pulse mode: 0: Synchronous point-to-point; 1: Bus mode w/ constant length trigger pulse (default) 2: Bus mode w/ variable length trigger pulse 3: Bus mode w/ fully overlapping trigger pulse
SPC_CSUM_CFG		[10:9]	R/W	0	Fast-channel checksum calculation method: 0/1: checksum in line with SAE J2716 (default); 2: Method “O” 3: Method "E" in line with SPC2014 Specification
SPC_CSUM_MODE		[12:11]	R/W	0	Checksum nibble calculation mode in SPC: 0: checksum only (default) 1: checksum + ID 2: checksum + RC 3: checksum + ID + RC
SPC_SCN_BIT_ORDER		13	R/W	1	Bit order in Status & Communication Nibble including chip ID and Status bit 0: SENT flavor 1: SPC flavor (default) Note: used only SPC mode, if ID_IN_STATUS=1
SPC_OUT_ON_DLY	586 (308)	[6:0]	R/W	2	Lead time [ticks] between of ABE output mode switching Hi-Z -> TX and the SPC sync pulse trigger falling edge. If 0, the transition happens at frame start (sync pulse falling edge).
SPC_OUT_OFF_DLY		[15:7]	R/W	0	Delay [ticks] between frame start (sync pulse falling edge) and the ABE output mode switch: TX -> Hi-Z. If 0, the transition happens at end of pause pulse. SPC_OUT_OFF_DLY[8:0] must be <= T_FRAME[11:0]
SPC_TRIGLL_OFS0	588 (310)	[3:0]	R/W	0	Offset for lower detection limit of trigger pulse for ID0
SPC_TRIGLL_OFS1		[7:4]	R/W	0	Offset for lower detection limit of trigger pulse for ID1

Field	Address [1]	Bit	R/W	Default	Description
SPC_TRIGLL_OFS2		[11:8]	R/W	0	Offset for lower detection limit of trigger pulse for ID2
SPC_TRIGLL_OFS3		[15:12]	R/W	0	Offset for lower detection limit of trigger pulse for ID3
SPC_BLANK_TIME	590 (312)	[8:0]	R/W	5	Blank period [ticks] for which master pulse detection is disabled after unsuccessful trial.
SENT_FC_FORMAT	592 (314)	[2:0]	R/W	0	SENT format option 0: format H.1 1: format H.1 (default) 2: format H.2 3: format H.3 4: format H.4 5: format H.5 6: format H.6 7: format H.7
SENT_FAST_CHANNEL_2		[4:3]	R/W	0	Content of SENT fast channel 2 in case SENT_FC_FORMAT=1, 6 or 7: 0: Internal temperature sensor (default) 1: Inverted angle: fast_channel_2 = 0xFF9 - fast_channel_1 2: Register probe 3: Inverted angle: fast_channel_2 = 0xFFF - fast_channel_1
SENT_SLOW_EXTENDED		5	R/W	1	SENT serial message definition 0: normal SENT slow message 1: extended SENT slow message (default)
SENT_INIT_GM		6	R/W	0	SENT / SPC initialization frame fast channel 1 definition 0: Initialization frame FC1=0 (SENT compliant); In SPC mode only transmitted in case if SS3 1: Initialization frame FC1=SC_YE
SENT_TICK_TIME		[9:7]	R/W	4	SENT tick duration: 0: 0.5 µs, 1: 0.75 µs, 2: 1.0 µs, 3:1.5 µs 4: 3.0µs (normal SENT, default) else: 6.0 µs (slow SENT) Note, depending on AC_SEL[2:0] the tick times are rounded to the nearest integer multiple of the application clock period
SENT_SHAPE_CFG		[11:10]	R/W	2	SENT nibble high/low-time configuration: 0: fixed low time (5 ticks); 1: fixed high time (6 ticks); else: 50% duty cycle Note, only effective if ABE_AOUT_MODE in [1,2,3]
SENT_SC_FORMAT		12	R/W	1	Slow Channel configuration: 0: short, 1: enhanced serial message

Field	Address [1]	Bit	R/W	Default	Description
STATUS_IN_CRC		13	R/W	1	1: Status and serial comm. nibble is included in the Fast Channel CRC (default); 0: not included
ID_IN_STATUS		14	R/W	0	SENT status & communication nibble definition 0: the two slow-message bits are as described in the SENT SAE standard (default) 1: the two slow-message bits are replaced by the 2-bit chip ID.
SENT_REPORT_MODE_ANA		15	R/W	0	Redundant nibble configuration in SENT H.4 format 1: Redundant nibble is inverted; 0: not inverted
SENT_FC1_CPT_DLY	594 (316)	[6:0]	R/W	0	SENT/SPC capture delay [ticks] for fast channel 1 data from: SENT: falling edge of the SYNC pulse SPC: according to SPC_FC1_CPT_MST
SPC_FC1_CPT_MST		7	R/W	0	if 1 in SPC mode, data capturing is triggered by falling edge of SPC master pulse, else by falling edge of SYNC pulse (equal to master pulse in SPC fully overlapping mode)
SENT_PS_PWT		[11:8]	R/W	12	Pulse-shaping preamble low time - 3 [ticks]
SENT_RC_INIT		12	R/W	1	Rolling counter initialization behavior 0: RC counter stays at 0 during initialization frames 1: RC counter incrementing during initialization (default)
SENT_SC_DIAG_BUF		13	R/W	1	Enable SENT Slow-channel diagnostic message buffering
SENT_FC2_ADR	596 (318)	[7:0]	R/W	43	Address for FC2 register probe; word-aligned
SENT_FC2_OFS0		[11:8]	R/W	4	Bit offset for FC2 register data at even RC
SENT_FC2_OFS1		15:12]	R/W	0	Bit offset for FC2 register data at odd RC
SENT_SENSOR_TYPE	598	[11:0]	R/W	80	Part of SENT slow message: Channel 1/2 sensor type
SENT_REV		[15:12]	R/W	4	Part of SENT slow message: SENT standard revision = 0x004
SENT_MAN_CODE	600	[11:0]	R/W	6	Part of SENT slow message: Manufacturer code
SENT_SENSOR_ID1	602	[11:0]	R/W	0	Part of slow SENT message: Sensor ID-1
SENT_SENSOR_ID2	604	[11:0]	R/W	0	Part of slow SENT message: Sensor ID-2
SENT_SENSOR_ID3	606	[11:0]	R/W	0	Part of slow SENT message: Sensor ID-3

Field	Address [1]	Bit	R/W	Default	Description
SENT_SENSOR_ID4	608	[11:0]	R/W	0	Part of slow SENT message: Sensor ID-4
SENT_OEM_CODE1	610	[11:0]	R/W	0	Part of slow SENT message: OEM code 1
SENT_OEM_CODE2	612	[11:0]	R/W	0	Part of slow SENT message: OEM code 2
SENT_OEM_CODE3	614	[11:0]	R/W	0	Part of slow SENT message: OEM code 3
SENT_OEM_CODE4	616	[11:0]	R/W	0	Part of slow SENT message: OEM code 4
SENT_OEM_CODE5	618	[11:0]	R/W	0	Part of slow SENT message: OEM code 5
SENT_OEM_CODE6	620	[11:0]	R/W	0	Part of slow SENT message: OEM code 6
SENT_OEM_CODE7	622	[11:0]	R/W	0	Part of slow SENT message: OEM code 7
SENT_OEM_CODE8	624	[11:0]	R/W	0	Part of slow SENT message: OEM code 8
LC_P_MON_LIM_LO	626 (322)	[7:0]	R/W	60	LCO period monitor, lower limit
LC_P_MON_LIM_HI		[15:8]	R/W	166	LCO period monitor, upper limit
DIAG_TEMP_THR_LO	628 (324)	[7:0]	R/W	14	Temperature threshold for under-temperature diagnostic, unit 2*[K]: ER_TEMP_LO is issued, if TEMP[11:0] < (DIAG_TEMP_THR_LO < < 4); If TEMP_CLIP_EN==1, TEMP[11:0] is saturated with lower boundary (DIAG_TEMP_THR_LO < < 4)
DIAG_TEMP_THR_HI		[15:8]	R/W	119	Temperature threshold for over-temperature diagnostic, unit 2*[K]: ER_TEMP_HI is issued, if TEMP[11:0] > (DIAG_TEMP_THR_HI < < 4) if TEMP_CLIP_EN==1, TEMP[11:0] is saturated with upper boundary (DIAG_TEMP_THR_HI < < 4)
DIAG_TEMP_THR_MAX	630 (326)	[7:0]	R/W	122	Temperature threshold for over-temperature diagnostic, unit 2*[K]: ER_TEMP_LO is issued, if TEMP[11:0] < (DIAG_TEMP_THR_LO << 4); If TEMP_CLIP_EN==1, TEMP[11:0] is saturated with lower boundary (DIAG_TEMP_THR_LO << 4)
SC_HL		[15:8]	R/W	128	Signal conditioning: Transition point for clamping high to clamping low as offset from center point of X range; resolution 360deg/2^8
PWM_DC_OFS	632 (328)	[8:0]	R/W	0	PWM duty-cycle offset: ΔTPWM_ON = PWM_DC_OFS / f_{AC} [s]
TEMP_CLIP_EN		9	R/W	0	Enable temperature clipping within [DIAG_TEMP_THR_LO, DIAG_TEMP_THR_HI]

Field	Address [1]	Bit	R/W	Default	Description
PGI_CAP		[13:12]	R/W	0	PGI cold-activation period: 2'b00: 10ms cold-activation period (default) 2'b01, 2'b10: 2.5ms cold-activation period 2'b11: cold-activation disabled for PGI
DIAG_SSI_LO	634 (330)	[7:0]	R/W	0	Signal strength monitor low limit
DIAG_SSI_HI		[15:8]	R/W	255	Signal strength monitor high limit
DE_OV_VS	640 (332)	0	R/W	0	Disable overvoltage error for VS (external supply)
DE_UV_VS		1	R/W	0	Disable undervoltage error for VS (external supply)
DE_OV_VDDD		2	R/W	0	Disable overvoltage error for VDDD (digital supply)
DE_VDDA		3	R/W	0	Disable over-/undervoltage error for VDDA (analog supply)
DE_VAUX		4	R/W	0	Disable over-/undervoltage error for VAUX (auxiliary supply)
DE_BG		5	R/W	0	Disable bandgap related errors
DE_LC_P		6	R/W	0	Disable LCO period error
DE_LC_A		7	R/W	0	Disable LCO amplitude error
DE_SS		8	R/W	0	Disable sensor short error
DE_SL		9	R/W	0	Disable sensor loss error
DE_AGC		10	R/W	0	Disable AGC error
DE_DSP		11	R/W	0	Disable DSP related errors
DE_RCO		12	R/W	0	Disable RCO monitor
DE_LFSS		13	R/W	0	Disable latent fault checks of supply system
DE_LFSM		14	R/W	0	Disable latent fault checks of sensor monitor
DE_LC_OC		15	R/W	0	Disable overcurrent detection for LCO
DE_DEIM	642 (334)	0	R/W	0	Disable die edge integrity error
DE_GC_LC		1	R/W	0	Disable ground comparator error for LCO ground
DE_GC_DRV		2	R/W	0	Disable ground comparator error for driver ground
DE_GC_D		3	R/W	0	Disable ground comparator error for digital ground
DE_GC_A		4	R/W	0	Disable ground comparator error for analog ground

Field	Address [1]	Bit	R/W	Default	Description
DE_BIAS		5	R/W	0	Disable bias error
DE_FE		6	R/W	0	Disable frontend error
DE_TRIA		7	R/W	1	Disable AFE amplifier error
DE_ADC_ZERO		8	R/W	0	Disable ADC minimum value error
DE_ADC_V8		9	R/W	0	Disable ADC maximum value error
DE_ADC_LIN		10	R/W	0	Disable ADC linearity error
DE_REFGEN		11	R/W	0	Disable AFE voltage reference error
DE_ADC		12	R/W	0	Disable ADC related errors
DE_TEMPC		13	R/W	1	Disable temperature sensor error
DE_LFLCO		15	R/W	0	Disable LCO latent fault checks
DE_PWM	644 (336)	0	R/W	0	Disable PWM monitor
DE_SPEED		2	R/W	0	Disable speed error
DE_REG		[6:4]	R/W	0	If 3, register monitor is disabled
DE_TEMP		7	R/W	0	Disable over/under temperature error
DE_TEMP_MAX		8	R/W	0	Disable maximum temperature error
DE_INTP		9	R/W	0	Disable DSP interpolator error
DE_SCXY		10	R/W	0	Disable DSP signal conditioning error

Table 56 – EEPROM map

[1] Address between brackets is the shadow register address

14.3. Error Handler

The error handler covers register bits indicating the diagnostic status of the IC. It also handles the IC locking mechanism and can be used to trigger a CRC calculation on the memory.

Field	Address	Bit	R/W	Default	Description
ER_TEMPC	50	0	R	0	Temperature sensors average error
ER_DACMON		1	R	0	DAC or analog backend error
ER_DSP		2	R	0	DSP related error
ER_FE		3	R	0	Frontend error
ER_TRIA		4	R	0	AFE amplifier error
ER_REFGEN		5	R	0	AFE voltage reference error
ER_ADC_LIN		6	R	0	ADC linearity error

Field	Address	Bit	R/W	Default	Description
ER_ADC_V8		7	R	0	ADC maximum value error
ER_ADC_ZERO		8	R	0	ADC minimum value error
ER_ADC		9	R	0	ADC related errors
AGC_MON_LO		10	R	0	AGC monitoring limit (lower bound) triggered
AGC_MON_HI		11	R	0	AGC monitoring limit (upper bound) triggered
LC_LOW		12	R	0	LC oscillator period too low
LC_HIGH		13	R	0	LC oscillator period too high
ER_INTP		14	R	0	Interpolator error
ER_SCXY		15	R	0	SCXY error
ER_SS	52	[1:0]	R	0	Sensor short detected: 0: no short detected 1: short to VS or to another sensor with higher VSOP 2: short to GND or to another sensor with lower VSOP 3: not allowed
ER_SL		[4:2]	R	0	Sensor loss detection on the coil [IN2, IN1, IN0]: 0: no sensor loss detected Bit 0 = 1: IN0 open if ER_SS=0; ignore if ER_SS>0 Bit 1 = 1: IN1 open if ER_SS=0; ignore if ER_SS>0 Bit 2 = 1: IN2 open if ER_SS=0; ignore if ER_SS>0
ER_LCA		5	R	0	LC oscillator amplitude out of range
ER_RCO		6	R	0	RC oscillator frequency error
ER_DEIM		7	R	0	Die edge integrity error
REG_MON		8	R	0	Shadow register error
ER_BG		9	R	0	Bandgap related errors
OV_VDDA		10	R	0	Overvoltage on VDDA (analog Supply)
OV_VDDD		11	R	0	Overvoltage on VDDD (digital Supply)
OV_VAUX		12	R	0	Overvoltage on VAUX (auxiliary supply)
OV_VSINT		13	R	0	Overvoltage on VS (Vov_VS)
ER_GC	54	[3:0]	R	0	Ground comparator error
OV_VS		4	R	0	Overvoltage on VS (PGI entry level)
EE_DED		5	R	0	EEPROM double bit error
ER_CHECKSUM		6	R	0	EEPROM checksum error
ER_BIAS		7	R	0	Bias error
UV_VS		8	R	0	Undervoltage on VS
UV_VDDA		9	R	0	Undervoltage on VDDA

Field	Address	Bit	R/W	Default	Description
ER_PWM		10	R	0	PWM error
ER_LC_OC		11	R	0	LCO overcurrent error
ER_TEMP_HI		12	R	0	Over-temperature wrt. DIAG_TEMP_THR_HI
ER_TEMP_LO		13	R	0	Under-temperature wrt. DIAG_TEMP_THR_LO
ER_TEMP_MAX		14	R	0	Over-temperature wrt. DIAG_TEMP_THR_MAX
CRC	56	[15:0]	R	0	EEPROM checksum result
STRT_CALC_CRC	58	0	R/W	0	Write Only, 1 active. Starts EEPROM checksum computation Always reads 0
CRC_CALC_DONE		1	R	0	If 1, EEPROM checksum computation finished, CRC updated
Reserved		2	R/W	0	Do not modify
LOCK_KEY	62	[3:0]	W	0	Writing this register with sequence 0x7, 0x9, 0x4, 0xF will activate a procedure to permanently lock the EEPROM preventing write access.
STATE	64	[7:0]	R	0	Device state 8'h00: EEPROM verification phase 8'h01: Shadow register initialization 8'h02: Latent faults check 1 8'h04: Latent faults check 1 8'h08: Normal 8'h10: Safe State 0 8'h20: Safe State 2 8'h40: Safe State 1 8'h80: Safe State 3

Table 57 - Error handler memory block map

14.4. Digital Signal Processing

The digital signal processing section covers the registers used within the DSP, including phase and speed and allows controlling the offset calibration procedure.

Field	Address	Bit	R/W	Default	Description
AGC_GAIN	66	[2:0]	R/W		R: Read current AGC gain setting, W: Override AGC gain works in conjunction with bit 3
AMP_ADC		[15:8]	R		Current ADC amplitude, reference for comparison against AGC_MON_LIM_HI/LO and AGC_LIM_HI/LO
TEMP	68	[11:0]	R		Temperature according to SENT, range [200 : 0.125 : 711.875] [K]
DCCALIB_REQ	70	0	R/W	0	Write Only, 1 active. Start DC offset calibration cycle. Always read 0.

Field	Address	Bit	R/W	Default	Description
DCCALIB_DONE		1	R		If 1, DC offset calibration cycle finished, CALRESxxx fields updated
NACC		[4:2]	R/W		Length of DC offset calibration cycle; T_acc = 2^(NACC+5) * 5.2us; higher values increase DC compensation resolution
DIS_AGC		5	R/W		Disable(hold) AGC
CALRES01_HI		[9:8]	R		Measured average 18-bit baseband DC offset for difference of inputs IN0 and IN1 (D01); bit [17:16]
CALRES12_HI		[11:10]	R		Measured average 18-bit baseband DC offset for difference of inputs IN1 and IN2 (D12); bit [17:16]
CALRES20_HI		[13:12]	R		Measured average 18-bit baseband DC offset for difference of inputs IN2 and IN0 (D20); bit [17:16]
CALRES01_LO	72	[15:0]	R		Measured average 18-bit baseband DC offset for difference of inputs IN0 and IN1 (D01); bit [15:0]; CALRESxx = signed({CALRESxx_HI[1:0], CALRESxx_LO[15:0]})
CALRES12_LO	74	[15:0]	R		Measured average 18-bit baseband DC offset for difference of inputs IN1 and IN2 (D12); bit [15:0]
CALRES20_LO	76	[15:0]	R		Measured average 18-bit baseband DC offset for difference of inputs IN2 and IN0 (D20); bit [15:0]
CALRESAOSC	78	[13:0]	R		Measured average LC oscillator amplitude
LIN_PHASE	86	[15:0]	R/W		Angular value after linearization, resolution 360/2^16 deg; writable only with PHASE_LOCK=1
SPEED_LO	88	[15:0]	R/W		LSB of measured speed; v[Hz] = $signed{SPEED_LO} / 2^22 * f_{AC}/26; v[e-rpm] = v[Hz] * 60; range +/-6009,43 @ f_{AC}=20MHz
ACC	90	[8:0]	R		Angular acceleration
LOCK_SPEED		10	R/W		1: lock speed value; disable speed tracking; active only with programming interface
LOCK_PHASE		11	R/W		1: lock phase value; disable phase tracking; active only with programming interface
DIS_DRIFTC		12	R/W		1: disable drift compensation; active only with programming interface
SPEED_HI		15	R/W		MSB of measured speed; v[Hz] = $signed{SPEED_HI, SPEED_LO} / 2^22 *

Field	Address	Bit	R/W	Default	Description
					f_{AC}/26; v[e-rpm] = v[Hz] * 60; range +/- 12018.87Hz @ f_{AC}=20MHz
FESUM	94	[7:0]	R		Result of summation of differences (D01+D12+D20)
SSI		[15:8]	R		Signal strength indicator
DRIFTC_PHASE	96	[15:0]	R		Angular value after delay compensation and zero-point offset correction, resolution: 360/2^16 deg
SC_PHASE	98	[15:0]	R		Position value after signal conditioning

Table 58 – DSP memory block map

15. Recommended Application Diagrams

In Figure 24 is the application diagram given. The ground pins VSSLC, VSSDRV, VSSA, VSSD and ground connections of other pins and components should be connected by low-impedance vias and interconnects to common system ground plane on the PCB.

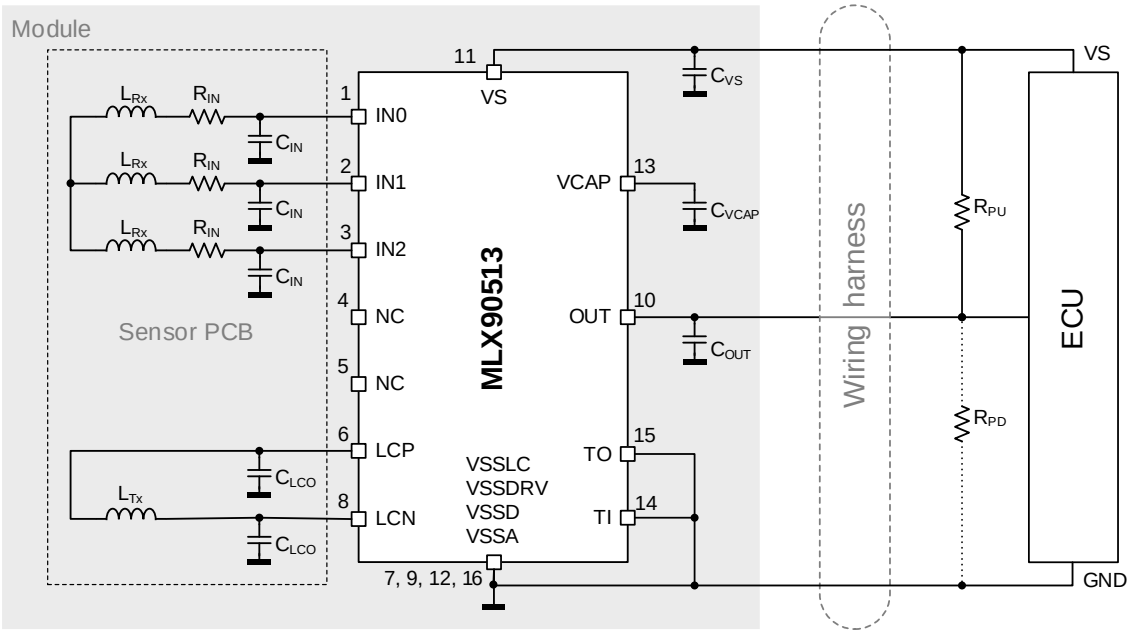


Figure 24 – Application schematic

The application circuit components are given in Table 59.

Component	Symbol	Min.	Typ.	Max.	Unit	Comment
Inductor	L_{Tx}	1	4	10	µH	
Inductor	L_{Rx}	40	200	500	nH	
Capacitor	C_{IN}		100		pF	
Capacitor	C_{LCO}		1.2		nF	Referring to VSSLC
Capacitor	C_{VS}	10	470		nF	
Capacitor	C_{VCAP}	100	470		nF	
Capacitor	C_{OUT}	4.7	100	200	nF	Analog ratiometric output

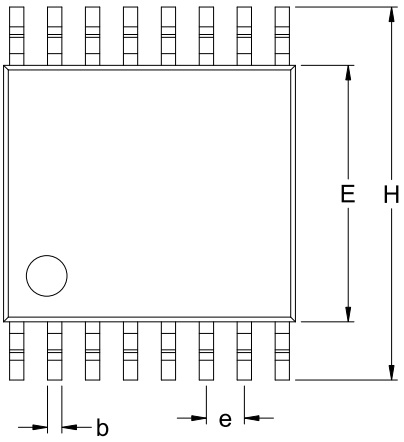
Component	Symbol	Min.	Typ.	Max.	Unit	Comment
Capacitor	C_{OUT}	2.2	4.7	10	nF	SENT, PWM output ABE_AOUT_MODE = 4, 5, T_{tick} = 3 µs. For other tick times C_{OUT} should be proportionally scaled
Capacitor	C_{OUT}	1	2.2	4.7	nF	SENT output ABE_AOUT_MODE = 1, 2, 3 T_{tick} = 1.5 µs ABE_AOUT_SR = 0
Capacitor	C_{OUT}	2.2	4.7	10	nF	SENT, PWM output ABE_AOUT_MODE = 1, 2, 3 T_{tick} = 3 µs, 6 µs ABE_AOUT_SR = 0
Capacitor	C_{OUT}	4.7	10	15	nF	SENT, PWM output ABE_AOUT_MODE = 1, 2, 3 T_{tick} = 3 µs, 6 µs ABE_AOUT_SR = 1
Output load resistance	R_{PU}/ R_{PD}	5	10	12	kΩ	Analog mode
Output load resistance	R_{PU}/ R_{PD}	3	10	55	kΩ	SENT, PWM output ABE_AOUT_MODE = 4, 5 only
Output load resistance	R_{PU}/ R_{PD}	1.5	10	55	kΩ	SENT, PWM output ABE_AOUT_MODE = 1, 2, 3 In open drain modes the non-driven (pulled) edge timing is determined by the RC time constant of the pull resistor and the load capacitor

Table 59 – Application circuit component

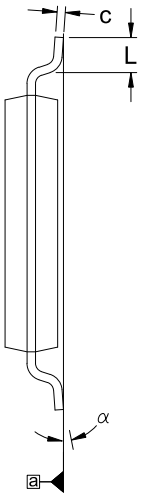
For specific components that are connected to ground with at least one terminal the preferred IC-related ground terminal is listed in above table. However, in general the recommendation is to connect all grounds to a common low impedance ground plane on PCB.

16. Package Information

16.1. TSSOP-16 Package Dimensions

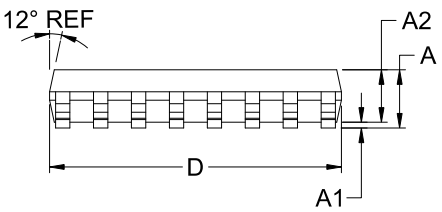


TOP VIEW



SIDE VIEW

SYMBOL	MINIMUM	MAXIMUM
A	---	1.10
A1	0.05	0.15
A2	0.85	0.95
D	4.90	5.10
E	4.30	4.50
H	6.40 REF	
L	0.50	0.75
b	0.19	0.30
c	0.09	0.20
e	0.65 BSC	
α	0°	8°



SIDE VIEW

NOTE :

1. ALL DIMENSIONS IN MILLIMETERS (mm) UNLESS OTHERWISE STATED.
2. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS OF MAX 0.15 mm PER SIDE.
3. DIMENSION E DOES NOT INCLUDE INTERLEADS FLASH OR PROTRUSIONS OF MAX 0.25 mm PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION OF MAX 0.08 mm.
5. LEAD TO LEAD COPLANARITY MAX 0.100 MILLIMETERS (mm) WITH RESPECT TO SEATING PLANE a.

Figure 25 – TSSOP16 package dimensions

17. IC handling and assembly

17.1. Storage and handling of plastic encapsulated ICs

Plastic encapsulated ICs shall be stored and handled according to their MSL categorization level (specified in the packing label) as per J-STD-033.

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD). The component assembly shall be handled in EPA (Electrostatic Protected Area) as per ANSI S20.20

For more information refer to Melexis *Guidelines for storage and handling of plastic encapsulated ICs* [1]

17.2. Assembly of encapsulated ICs

For Surface Mounted Devices (SMD, as defined according to JEDEC norms), the only applicable soldering method is reflow.

Melexis products soldering on PCB should be conducted according to the requirements of IPC/JEDEC and J-STD-001. Solder quality acceptance should follow the requirements of IPC-A-610.

Environmental protection of customer assembly with Melexis products for harsh media application, is applicable by means of coating, potting or overmolding considering restrictions listed in the relevant application notes [1]

For other specific process, contact Melexis via www.melexis.com/technical-inquiry

17.3. Environment and sustainability

Melexis is contributing to global environmental conservation by promoting non-hazardous solutions. For more information on our environmental policy and declarations (RoHS, REACH…) visit www.melexis.com/environmental-forms-and-declarations

[1] www.melexis.com/ic-handling-and-assembly

18. Revision History Table

27/03/2024 (001)	Official release

Table 60 – Revision history table

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