Data Sheet

LTC2320-12

Octal, 12-Bit + Sign, 1.5Msps/Ch Simultaneous Sampling ADC

FEATURES

- 1.5 Msps/Ch Throughput Rate
- Eight Simultaneously Sampling Channels
- Guaranteed 12-Bit, No Missing Codes
- 8 V_{P-P} Differential Inputs with Wide Input Common Mode Range
- 77 dB SNR (Typ) at f_{IN} = 500 kHz
- –90 dB THD (Typ) at f_{IN} = 500 kHz
- Guaranteed Operation to 125°C
- Single 3.3 V or 5 V Supply
- Low Drift (20 ppm/°C Max) 2.048 V or 4.096 V Internal Reference
- 1.8 V to 2.5 V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 20 mW/Ch (Typ)
- Small 52-Lead (7 mm × 8 mm) QFN Package

APPLICATIONS

- High Speed Data Acquisition Systems
- Communications
- Remote Data Acquisition
- Imaging
- Optical Networking
- Multiphase Motor Control

GENERAL DESCRIPTION

The LTC2320-12 is a low noise, high speed octal 12-bit + sign successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3 V or 5 V supply, the LTC2320-12 has an 8 V_{P-P} differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2320-12 achieves ±0.25 LSB INL typical, no missing codes at 12 bits and 77 dB SNR.

The LTC2320-12 has an onboard low drift (20 ppm/°C max) 2.048 V or 4.096 V temperature-compensated reference. The LTC2320-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 1.5 Msps per channel throughput with no latency makes the LTC2320-12 ideally suited for a wide variety of high speed applications. The LTC2320-12 dissipates only 20 mW per channel and offers nap and sleep modes to reduce the power consumption to 26 µW for further power savings during inactive periods.

TYPICAL APPLICATION

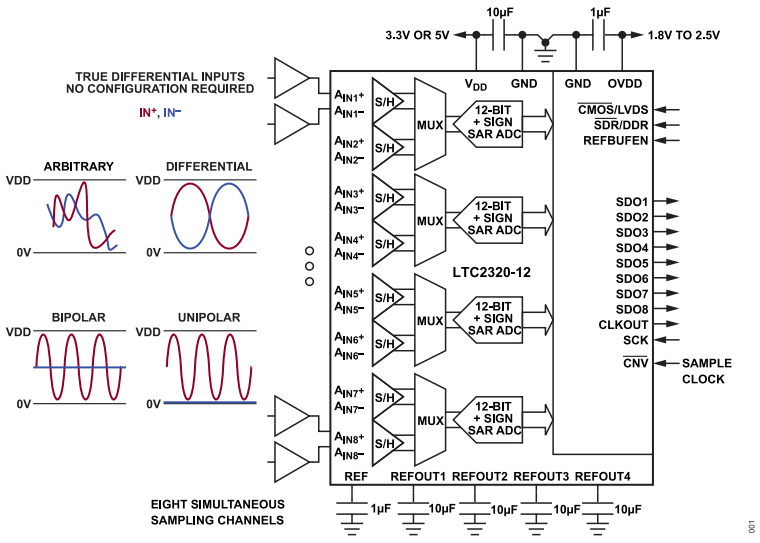


Figure 1. Typical Application of LTC2320-12

Rev. C

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Typical Application ... 1
Functional Block Diagram ... 3
Specifications ... 5
  Electrical Characteristics ... 5
  Converter Characteristics ... 5
  Dynamic Accuracy ... 6
  Internal Reference Characteristics ... 6
  Digital Inputs and Digital Outputs ... 7
  Power Requirements ... 7
  ADC Timing Specifications ... 8
Absolute Maximum Ratings ... 11
  ESD Caution ... 11
Pin Configuration and Function Descriptions ... 12
Typical Performance Characteristics ... 15
Applications Information ... 18
  Overview ... 18
  Converter Operation ... 18
  Transfer Function ... 18
  Input Drive Circuits ... 22
  ADC Reference ... 22
  Dynamic Performance ... 24
  Power Considerations ... 24
  Timing and Control ... 25
  Digital Interface ... 28
  Board Layout ... 30
Typical Application ... 31
  Related Parts ... 31
Outline Dimensions ... 32
  Ordering Guide ... 33
  Evaluation Boards ... 33

REVISION HISTORY

4/2024—Rev. B to Rev. C

Updated Format (Universal) ... 1
Change to Applications Section ... 1
Deleted Figure 2; Renumbered Sequentially ... 1
Change to Figure 2 ... 3
Changes to Electrical Characteristics Section ... 5
Changes to Converter Characteristics Section ... 5
Changes to Dynamic Accuracy Section ... 6
Changes to Internal Reference Characteristics Section ... 6
Changes to Digital Inputs and Digital Outputs Section ... 7
Changes to Power Requirements Section ... 7
Changes to ADC Timing Specifications Section ... 8
Changes to Figure 5 to Figure 8 ... 9
Changes to Internal Reference Section ... 22
Changes to Table 11 ... 22
Changes to Figure 39 ... 23
Added Figure 40 and Figure 41; Renumbered Sequentially ... 23
Changes to Figure 49 ... 27
Added Figure 50 ... 27
Added Evaluation Boards ... 33

FUNCTIONAL BLOCK DIAGRAM

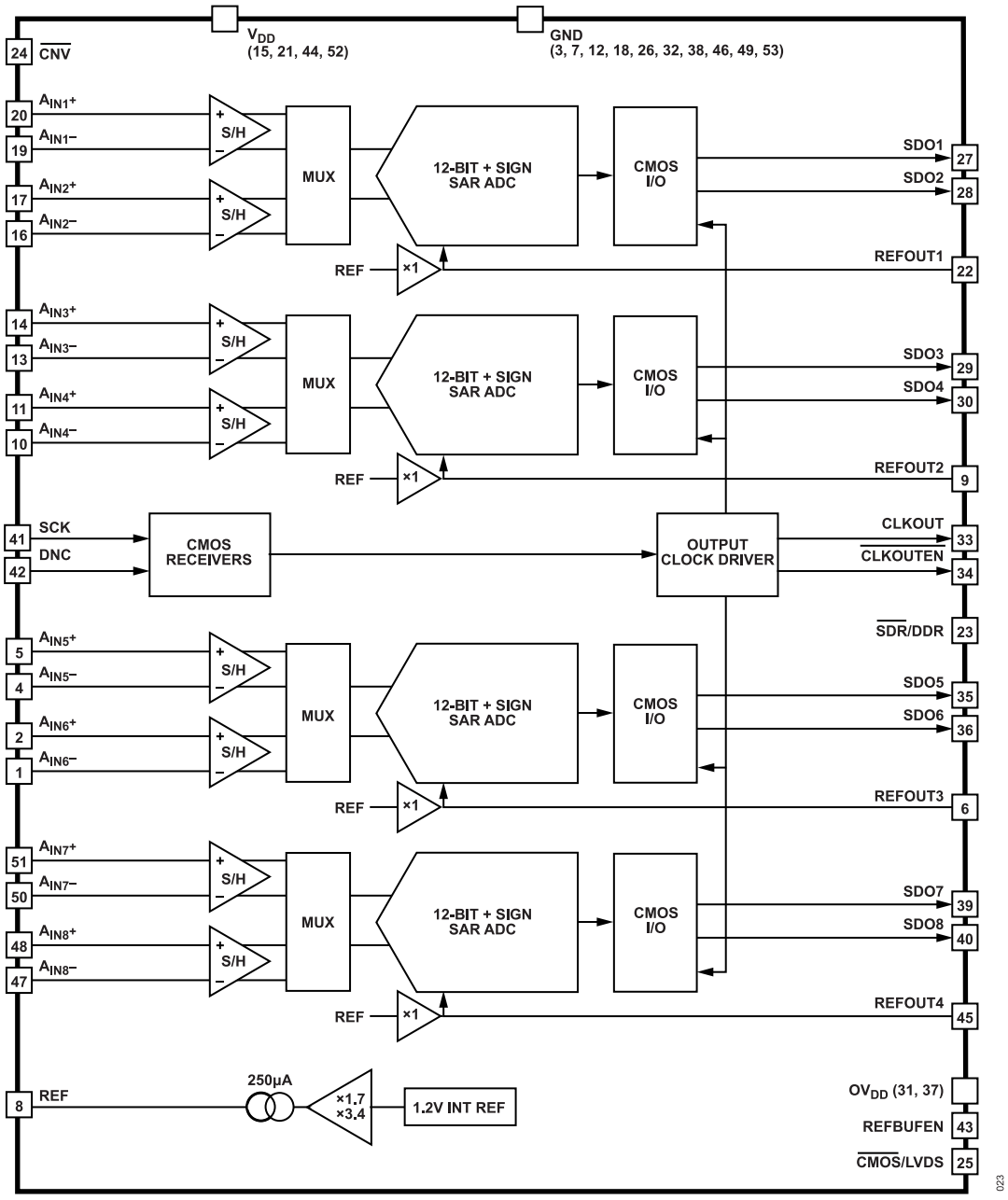


Figure 2. CMOS IO Mode

FUNCTIONAL BLOCK DIAGRAM

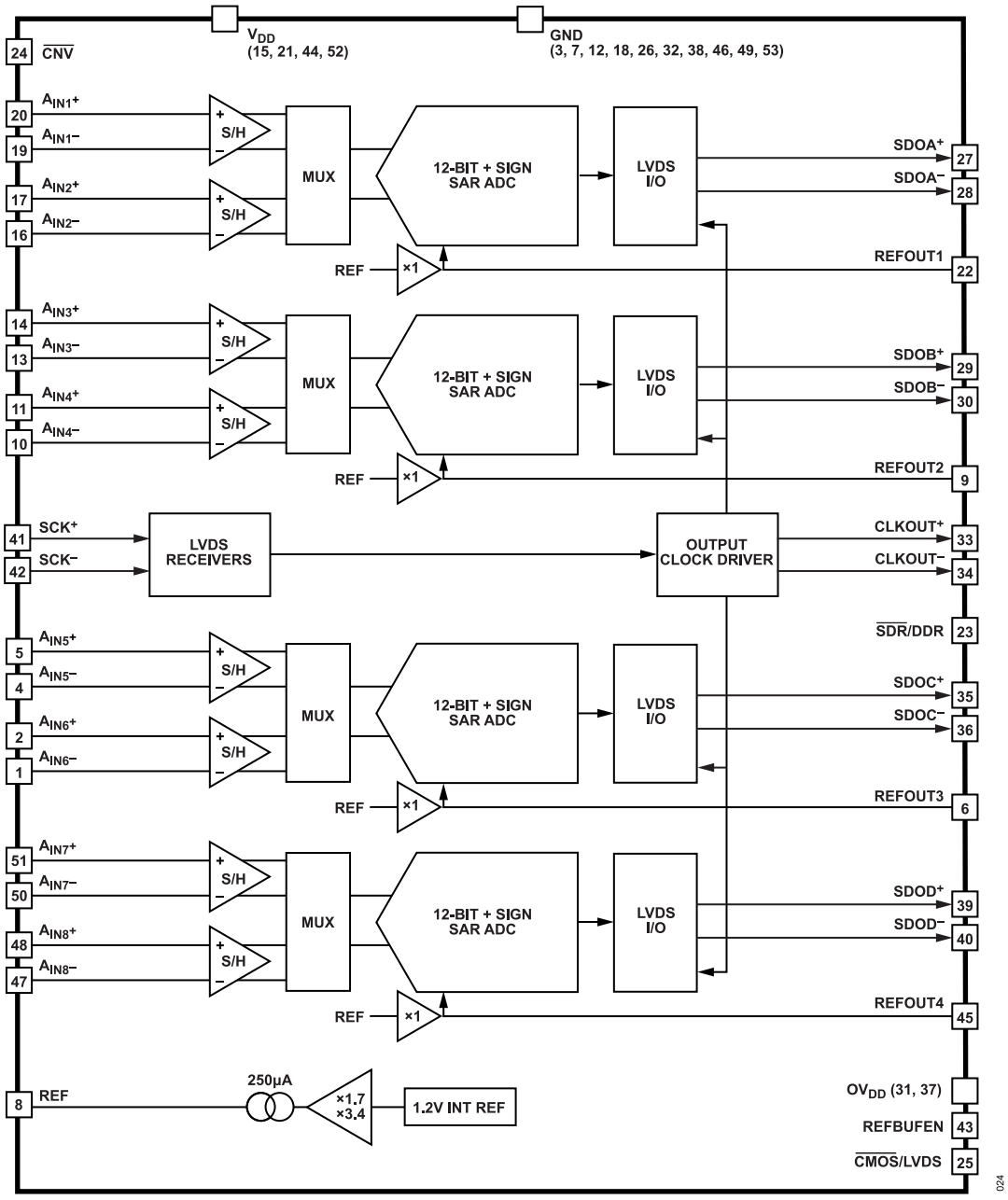


Figure 3. LVDS IO Mode

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
ELECTRICAL CHARACTERISTICS[1]						
Absolute Input Range (A_{IN+} to A_{IN-})	V_{IN+}		0		V_{DD}	V
	V_{IN-}		0		V_{DD}	V
Input Differential Voltage Range	$V_{IN+} - V_{IN-}$	$V_{IN} = V_{IN+} - V_{IN-}$	–REFOUT1,2,3,4		REFOUT1,2,3,4	V
Common Mode Input Range	V_{CM}	$V_{CM} = (V_{IN+} - V_{IN-})/2$	0		V_{DD}	V
Analog Input DC Leakage Current	I_{IN}		–1		1	µA
Analog Input Capacitance	C_{IN}	T_A = 25°C		10		pF
Input Common Mode Rejection Ratio	CMRR	f_{IN} = 500 kHz T_A = 25°C		102		dB
$\overline{CNV}$ High Level Input Voltage	V_{IHCNV}		1.5			V
$\overline{CNV}$ Low Level Input Voltage	V_{ILCNV}				0.5	V
$\overline{CNV}$ Input Current	I_{INCNV}		–10		10	µA

[1] Recommended operating conditions.

CONVERTER CHARACTERISTICS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CONVERTER CHARACTERISTICS						
Resolution			12			Bits
No Missing Codes			12			Bits
Transition Noise		T_A = 25°C		0.2		LSB_{RMS}
Integral Linearity Error[1]	INL		–1	±0.25	1	LSB
Differential Linearity Error	DNL		–0.99	±0.4	0.99	LSB
Bipolar Zero-Scale Error[2]	BZE		–1.5	0	1.5	LSB
Bipolar Zero-Scale Error Drift		T_A = 25°C		0.005		LSB/°C
Bipolar Full-Scale Error[2]	FSE	$V_{REFOUT1,2,3,4}$ = 4.096 V (REFBUFEN Grounded)	–3	0	3	LSB
Bipolar Full-Scale Error Drift		$V_{REFOUT1,2,3,4}$ = 4.096 V (REFBUFEN Grounded) T_A = 25°C		15		ppm/°C

[1] Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

[2] Bipolar zero error is the offset voltage measured from –0.5 LSB when the output code flickers between 0000 0000 0000 0 and 1111 1111 1111 1. Full-scale bipolar error is the worst-case of –FS or +FS untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

SPECIFICATIONS

DYNAMIC ACCURACY

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C and AIN = –1 dBFS. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC ACCURACY						
Signal-to-(Noise + Distortion) Ratio[1]	SINAD	f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 4.096 V, Internal Reference	74	77		dB
		f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1 dBFS		77		dB
Signal-to-Noise Ratio[1]	SNR	f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 4.096 V, Internal Reference	75	77		dB
		f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1 dBFS		77.5		dB
Total Harmonic Distortion[1]	THD	f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 4.096 V, Internal Reference		–90	–76	dB
		f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1 dBFS		–91		dB
Spurious Free Dynamic Range[1]	SFDR	f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 4.096 V, Internal Reference	76	93		dB
		f_{IN} = 500 kHz, $V_{REFOUT1,2,3,4}$ = 5 V, External Reference T_A = 25°C and A_{IN} = –1 dBFS		93		dB
–3 dB Input Bandwidth		T_A = 25°C and A_{IN} = –1 dBFS		55		MHz
Aperture Delay		T_A = 25°C and A_{IN} = –1 dBFS		500		ps
Aperture Delay Matching		T_A = 25°C and A_{IN} = –1 dBFS		500		ps
Aperture Jitter		T_A = 25°C and A_{IN} = –1 dBFS		1		ps_{RMS}
Transient Response		Full-Scale Step T_A = 25°C and A_{IN} = –1 dBFS		30		ns

[1] All specifications in dB are referred to a full-scale ±4.096 V input with REF = 4.096 V.

INTERNAL REFERENCE CHARACTERISTICS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INTERNAL REFERENCE CHARACTERISTICS						
Internal Reference Output Voltage	$V_{REFOUT1,2,3,4}$	4.75 V < V_{DD} < 5.25 V	4.078	4.096	4.115	V
		3.13 V < V_{DD} < 3.47 V	2.034	2.048	2.064	V
V_{REF} Temperature Coefficient[1]				3	20	ppm/°C
REFOUT1,2,3,4 Output Impedance		T_A = 25°C		0.25		Ω
$V_{REFOUT1,2,3,4}$ Line Regulation		4.75 V < V_{DD} < 5.25 V T_A = 25°C		0.3		mV/V
External Reference Current[2, 3]	$I_{REFOUT1,2,3,4}$	REFBUFEN = 0 V T_A = 25°C				
		REFOUT1,2,3,4 = 4.096 V		385		µA
		REFOUT1,2,3,4 = 2.048 V		204		µA

[1] Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

[2] When REFOUT1,2,3,4 is overdriven, the internal reference buffer must be turned off by setting REFBUFEN = 0 V.

[3] f_{SMPL} = 1.5 MHz, $I_{REFOUT1,2,3,4}$ varies proportionally with sample rate.

SPECIFICATIONS

DIGITAL INPUTS AND DIGITAL OUTPUTS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 5.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CMOS DIGITAL INPUTS AND OUTPUTS		$\overline{CMOS}$/LVDS = GND				
High Level Input Voltage	V_{IH}		0.8 • OV_{DD}			V
Low Level Input Voltage	V_{IL}				0.2 • OV_{DD}	V
Digital Input Current	I_{IN}	V_{IN} = 0 V to OV_{DD}	–10		10	µA
Digital Input Capacitance	C_{IN}			5		pF
High Level Output Voltage	V_{OH}	I_O = –500 µA	OV_{DD} – 0.2			V
Low Level Output Voltage	V_{OL}	I_O = 500 µA			0.2	V
Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0 V to OV_{DD}	–10		10	µA
Output Source Current	I_{SOURCE}	V_{OUT} = 0 V		–10		mA
Output Sink Current	I_{SINK}	V_{OUT} = OV_{DD}		10		mA
LVDS DIGITAL INPUTS AND OUTPUTS		$\overline{CMOS}$/LVDS = OV_{DD}				
LVDS Differential Input Voltage	V_{ID}	100 Ω Differential Termination OV_{DD} = 2.5 V	240		600	mV
LVDS Common Mode Input Voltage	V_{IS}	100 Ω Differential Termination OV_{DD} = 2.5 V	1		1.45	V
LVDS Differential Output Voltage	V_{OD}	100 Ω Differential Termination OV_{DD} = 2.5 V	220	350	600	mV
LVDS Common Mode Output Voltage	V_{OS}	100 Ω Differential Termination OV_{DD} = 2.5 V	0.85	1.2	1.4	V
Low Power LVDS Differential Output Voltage	V_{OD_LP}	100 Ω Differential Termination OV_{DD} = 2.5 V	100	200	350	mV
Low Power LVDS Common Mode Output Voltage	V_{OS_LP}	100 Ω Differential Termination OV_{DD} = 2.5 V	0.85	1.2	1.4	V

POWER REQUIREMENTS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY VOLTAGE	V_{DD}	5 V Operation	4.75		5.25	V
		3.3 V Operation	3.13		3.47	V
SUPPLY CURRENT	IV_{DD}	1.5 Msps Sample Rate (IN^+ = IN^- = 0V)		31	38	mA
CMOS I/O MODE		$\overline{CMOS}$/LVDS = GND				
Supply Voltage	OV_{DD}		1.71		2.63	V
Supply Current	I_{OVDD}	1.5 Msps Sample Rate (C_L = 5 pF)		4.4	7	mA
Nap Mode Current	I_{NAP}	Conversion Done (I_{VDD})		5.3	6.2	mA
Sleep Mode Current	I_{SLEEP}	Sleep Mode (I_{VDD} + I_{OVDD})		20	110	µA
Power Dissipation	$P_{D\_3.3V}$	V_{DD} = 3.3 V, 1.5 Msps Sample Rate		102	130	mW
		Nap Mode		18	26.6	mW
		Sleep Mode		20	355	µW
	P_{D_5V}	V_{DD} = 5 V, 1.5 Msps Sample Rate		162	208	mW
		Nap Mode		27	31.2	mW
		Sleep Mode		30	525	µW
LVDS I/O MODE		$\overline{CMOS}$/LVDS = OV_{DD}, OV_{DD} = 2.5 V				
Supply Voltage	OV_{DD}		2.37		2.63	V
Supply Current	I_{OVDD}	1.5 Msps Sample Rate (C_L = 5 pF, R_L = 100 Ω)		26	34	mA
Nap Mode Current	I_{NAP}	Conversion Done (I_{VDD})		5.3	6.2	mA
Sleep Mode Current	I_{SLEEP}	Sleep Mode (I_{VDD} + I_{OVDD})		20	110	µA
Power Dissipation	$P_{D\_3.3V}$	V_{DD} = 3.3 V, 1.5 Msps Sample Rate		151	196	mW
		Nap Mode		52	60	mW

SPECIFICATIONS

Table 6. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
	P_{D_5V}	Sleep Mode		80	355	µW
		V_{DD} = 5 V, 1.5 Msps Sample Rate		214	275	mW
		Nap Mode		51	68.5	mW
		Sleep Mode		30	525	µW

ADC TIMING SPECIFICATIONS

All specifications apply over the full operating temperature range. Otherwise, specifications are at T_A = 25°C. V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 MHz.

Table 7.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Maximum Sampling Frequency	f_{SMPL}				1.5	Msps
Time Between Conversions[1]	t_{CYC}	$t_{CYC} = t_{CNVH} + t_{CONV} + t_{READOUT}$	0.667		1000	µs
Conversion Time	t_{CONV}				450	ns
$\overline{CNV}$ High Time	t_{CNVH}		30			ns
Sampling Aperture[1]	$t_{ACQUISITION}$	$t_{ACQUISITION} = t_{CYC} - t_{CONV}$ T_A = 25°C		215		ns
REFOUT1,2,3,4 Wake-Up Time	t_{WAKE}	$C_{REFOUT1,2,3,4}$ = 10 µF T_A = 25°C		50		ms
CMOS I/O Mode, SDR		$\overline{CMOS}$/LVDS = GND, $\overline{SDR}$/ DDR = GND				
SCK Period[2]	t_{SCK}		9.1			ns
SCK High Time	t_{SCKH}		4.1			ns
SCK Low Time	t_{SCKL}		4.1			ns
SDO Data Remains Valid Delay from CLKOUT↓[3]	t_{HSDO_SDR}	CL = 5 pF	0		1.5	ns
SCK to CLKOUT Delay[3]	$t_{DSCKCLKOUT}$		2		4.5	ns
Bus Relinquish Time After $\overline{CNV}$↑[1]	$t_{DCNVSDOZ}$				3	ns
SDO Valid Delay from $\overline{CNV}$↓[1]	$t_{DCNVSDOV}$				3	ns
SCK Delay Time to $\overline{CNV}$↑[1]	$t_{DSCKHCNVH}$		0			ns
CMOS I/O Mode, DDR		$\overline{CMOS}$/LVDS = GND, $\overline{SDR}$/ DDR = OV_{DD}				
SCK Period	t_{SCK}		18.2			ns
SCK High Time	t_{SCKH}		8.2			ns
SCK Low Time	t_{SCKL}		8.2			ns
SDO Data Remains Valid Delay from CLKOUT↓[3]	t_{HSDO_DDR}	CL = 5 pF	0		1.5	ns
SCK to CLKOUT Delay[3]	$t_{DSCKCLKOUT}$		2		4.5	ns
Bus Relinquish Time After $\overline{CNV}$↑[1]	$t_{DCNVSDOZ}$				3	ns
SDO Valid Delay from $\overline{CNV}$↓[1]	$t_{DCNVSDOV}$				3	ns
SCK Delay Time to $\overline{CNV}$↑[1]	$t_{DSCKHCNVH}$		0			ns
LVDS I/O Mode, SDR		$\overline{CMOS}$/LVDS = OV_{DD}, $\overline{SDR}$/DDR = GND				
SCK Period	t_{SCK}		3.3			ns
SCK High Time	t_{SCKH}		1.5			ns
SCK Low Time	t_{SCKL}		1.5			ns
SDO Data Remains Valid Delay from CLKOUT↓	t_{HSDO_SDR}	C_L = 5 pF, OV_{DD} = 2.5 V	0		1.5	ns
SCK to CLKOUT Delay	$t_{DSCKCLKOUT}$	OV_{DD} = 2.5 V	2		4	ns
SCK Delay Time to $\overline{CNV}$↑[1]	$t_{DSCKHCNVH}$		0			ns
LVDS I/O Mode, DDR		$\overline{CMOS}$/LVDS = OV_{DD}, $\overline{SDR}$/DDR = OV_{DD}				
SCK Period	t_{SCK}		6.6			ns
SCK High Time	t_{SCKH}		3			ns
SCK Low Time	t_{SCKL}		3			ns

SPECIFICATIONS

Table 7. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SDO Data Remains Valid Delay from CLKOUT↓	t_{HSDO_DDR}	C_L = 5 pF, OV_{DD} = 2.5 V	0		1.5	ns
SCK to CLKOUT Delay	$t_{DSCKCLKOUT}$	OV_{DD} = 2.5 V	2		4	ns
SCK Delay Time to $\overline{CNV}$↑[1]	$t_{DSCKHCNVH}$		0			ns

[1] Guaranteed by design, not subject to test.

[2] t_{SCK} of 9.1 ns allows a shift clock frequency up to 105 MHz for rising edge capture.

[3] Parameter tested and guaranteed at OV_{DD} = 1.71 V and OV_{DD} = 2.5 V.

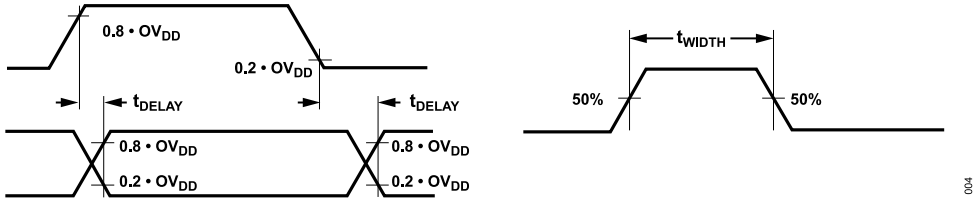


Figure 4. Voltage Levels for Timing Specifications

Timing Diagrams

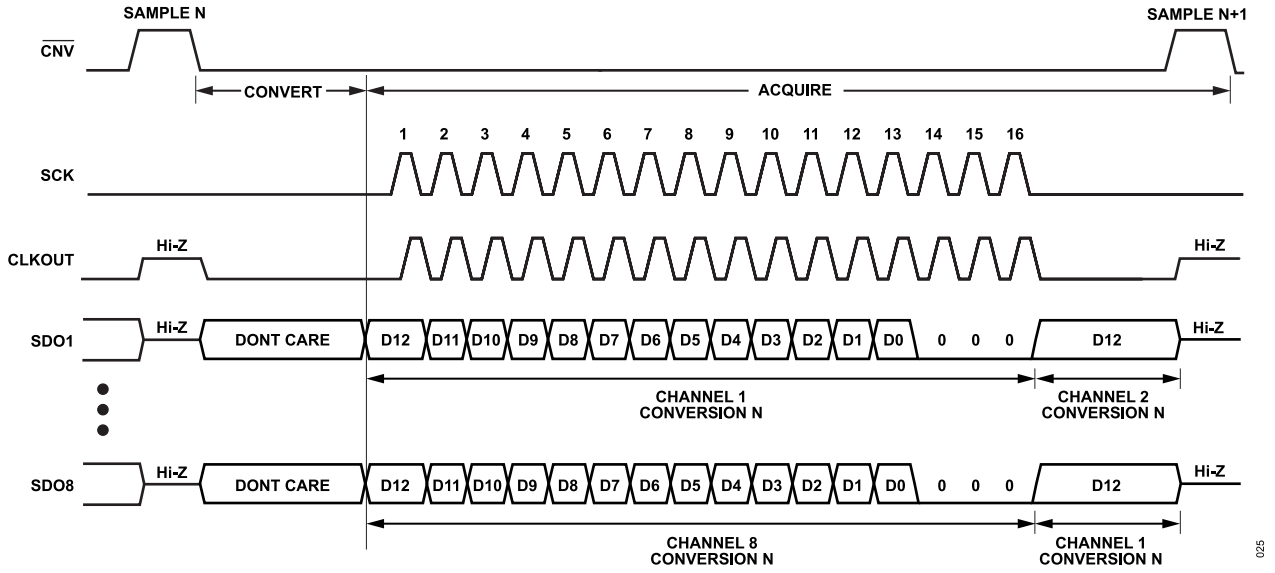


Figure 5. SDR Mode, CMOS (Reading 1 Channel per SDO)

SPECIFICATIONS

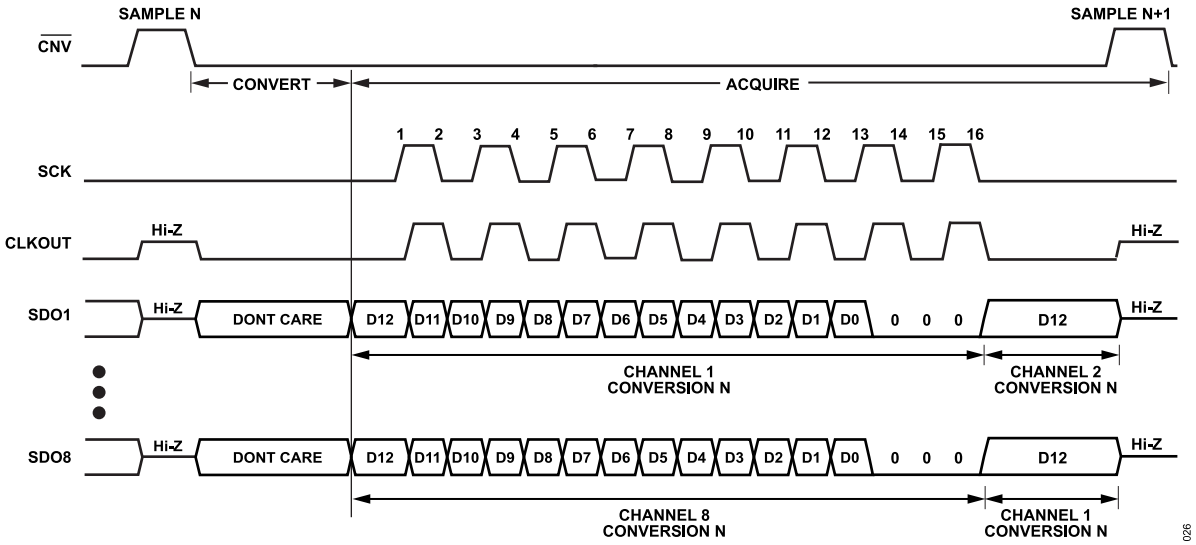


Figure 6. DDR Mode, CMOS (Reading 1 Channel per SDO)

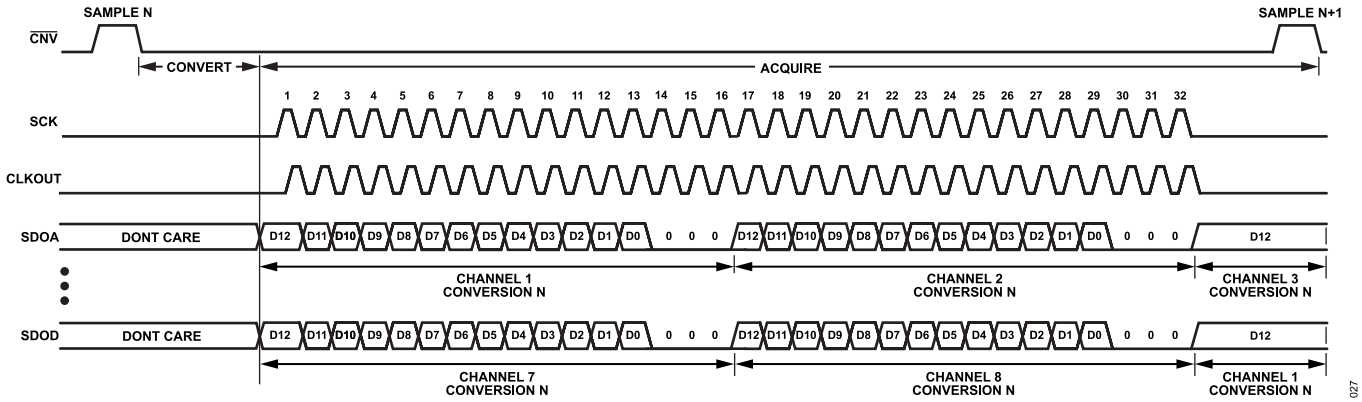


Figure 7. SDR Mode, LVDS (Reading 2 Channels per SDO Pair)

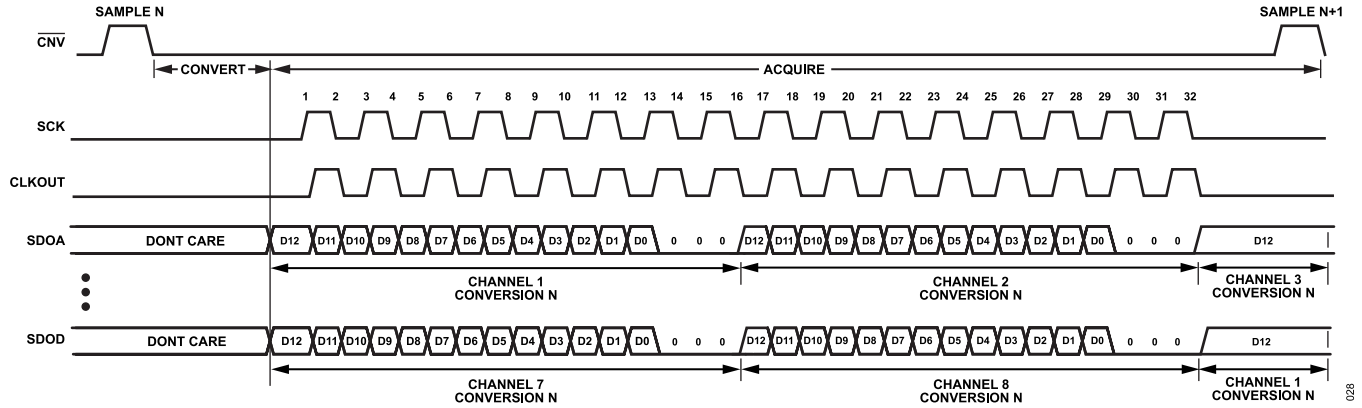


Figure 8. DDR Mode, LVDS (Reading 2 Channels per SDO Pair)

ABSOLUTE MAXIMUM RATINGS

All voltage values are with respect to ground.

Table 8.

Parameter	Rating
Supply Voltage (V_{DD})	6 V
Supply Voltage (OV_{DD})	3 V
Analog Input Voltage	
A_{IN+}, A_{IN-}[1]	–0.3 V to (V_{DD} + 0.3 V)
REFOUT1,2,3,4	–0.3 V to (V_{DD} + 0.3 V)
$\overline{CNV}$[2]	–0.3 V to (OV_{DD} + 0.3 V)
Digital Input Voltage[1]	(GND – 0.3 V) to (OV_{DD} + 0.3 V)
Digital Output Voltage[1]	(GND – 0.3 V) to (OV_{DD} + 0.3 V)
Operating Temperature Range	
LTC2320C	0°C to 70°C
LTC2320I	–40°C to 85°C
LTC2320H	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

[1] When these pin voltages are taken below ground, or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100 mA below ground, or above V_{DD} or OV_{DD}, without latch-up.

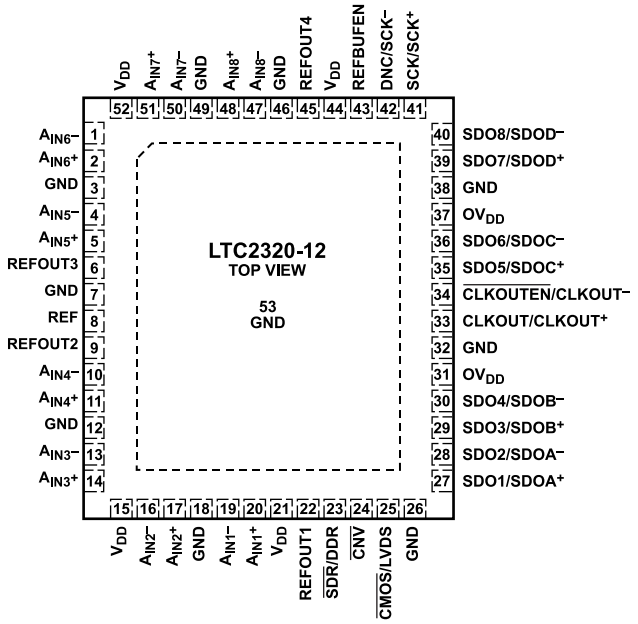
[2] $\overline{CNV}$ is driven from a low jitter digital source, typically at OV_{DD} logic levels.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



UKG PACKAGE
52-LEAD (7mm × 8mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 31°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB.

Figure 9. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	A_{IN6^-}, A_{IN6^+}	Analog Differential Input Pins. Full-scale range (A_{IN6^+} – A_{IN6^-}) is ±REFOUT3 voltage. These pins can be driven from V_{DD} to GND.
3, 7, 12, 18, 26, 32, 38, 46, 49	GND	Ground. These pins and exposed pad (Pin 53) must be tied directly to a solid ground plane.
4, 5	A_{IN5^-}, A_{IN5^+}	Analog Differential Input Pins. Full-scale range (A_{IN5^+} – A_{IN5^-}) is ±REFOUT3 voltage. These pins can be driven from V_{DD} to GND.
6	REFOUT3	Reference Buffer 3 Output. An onboard buffer nominally outputs 4.096 V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25 V to V_{DD} − 0.4 V.
8	REF	Common 4.096 V reference output. Decouple to GND with a 1 µF low ESR ceramic capacitor. May be overdriven with a single external reference to establish a common reference for ADC cores 1 through 4.
9	REFOUT2	Reference Buffer 2 Output. An onboard buffer nominally outputs 4.096 V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25 V to V_{DD} − 0.4 V.
10, 11	A_{IN4^-}, A_{IN4}^+	Analog Differential Input Pins. Full-scale range (A_{IN4^+} – A_{IN4^-}) is ±REFOUT2 voltage. These pins can be driven from V_{DD} to GND.
13, 14	A_{IN3^-}, A_{IN3^+}	Analog Differential Input Pins. Full-scale range (A_{IN3^+} – A_{IN3^-}) is ±REFOUT2 voltage. These pins can be driven from V_{DD} to GND.
15, 21, 44, 52	V_{DD}	Power Supply. Bypass V_{DD} to GND with a 10 µF ceramic capacitor and a 0.1 µF ceramic capacitor close to the part. The V_{DD} pins should be shorted together and driven from the same supply.
16, 17	A_{IN2^-}, A_{IN2^+}	Analog Differential Input Pins. Full-scale range (A_{IN2^+} – A_{IN2^-}) is ±REFOUT1 voltage. These pins can be driven from V_{DD} to GND.
19, 20	A_{IN1^-}, A_{IN1^+}	Analog Differential Input Pins. Full-scale range (A_{IN1^+} – A_{IN1^-}) is ±REFOUT1 voltage. These pins can be driven from V_{DD} to GND.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
22	REFOUT1	Reference Buffer 1 Output. An onboard buffer nominally outputs 4.096 V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25 V to V_{DD} − 0.4 V.
23	$\overline{SDR}$/DDR	Double Data Rate Input. Controls the frequency of SCK and CLKOUT. Tie to GND for the falling edge of SCK to shift each serial data output (Single Data Rate, SDR). Tie to OV_{DD} to shift serial data output on each edge of SCK (Double Data Rate, DDR). CLKOUT will be a delayed version of SCK for both pin states.
24	$\overline{CNV}$	Convert Input. This pin, when high, defines the acquisition phase. When this pin is driven low, the conversion phase is initiated and output data is clocked out. This input must be driven at OV_{DD} levels with a low jitter pulse. This pin is unaffected by the $\overline{CMOS}$/LVDS pin
25	$\overline{CMOS}$/LVDS	I/O Mode Select. Ground this pin to enable CMOS mode, tie to OV_{DD} to enable LVDS mode. Float this pin to enable low power LVDS mode.
31, 37	OV_{DD}	I/O Interface Digital Power. The range of OV_{DD} is 1.71 V to 2.63 V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8 V or 2.5 V, LVDS: 2.5 V). Bypass OV_{DD} to GND (Pins 32 and 38) with 0.1 µF capacitors.
43	REFBUFEN	Reference Buffer Output Enable. Tie to V_{DD} when using the internal reference. Tie to ground to disable the internal REFOUT1–4 buffers for use with external voltage references. This pin has a 500 k internal pull-up to V_{DD}.
45	REFOUT4	Reference Buffer 4 Output. An onboard buffer nominally outputs 4.096 V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 µF (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25 V to V_{DD} − 0.4 V.
47, 48	A_{IN8^-}, A_{IN8^+}	Analog Differential Input Pins. Full-scale range (A_{IN8^+} – A_{IN8^-}) is ±REFOUT4 voltage. These pins can be driven from V_{DD} to GND.
50, 51	A_{IN7^-}, A_{IN7^+}	Analog Differential Input Pins. Full-scale range (A_{IN7^+} – A_{IN7^-}) is ±REFOUT4 voltage. These pins can be driven from V_{DD} to GND.
53	Exposed Pad	Ground. Solder this pad to ground.
CMOS Data Output Option ($\overline{CMOS}$/LVDS = Low)		
27	SDO1	CMOS Serial Data Output for ADC Channel 1. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO1 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH2, CH3, CH4, CH5, CH6, CH7, CH8).
28	SDO2	CMOS Serial Data Output for ADC Channel 2. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO2 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH3, CH4, CH5, CH6, CH7, CH8, CH1).
29	SDO3	CMOS Serial Data Output for ADC Channel 3. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO3 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH4, CH5, CH6, CH7, CH8, CH1, CH2).
30	SDO4	CMOS Serial Data Output for ADC Channel 4. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO4 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH5, CH6, CH7, CH8, CH1, CH2, CH3).
33	CLKOUT	Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver (FPGA). The logic level is determined by OV_{DD}. This pin echoes the input at SCK with a small delay.
35	SDO5	CMOS Serial Data Output for ADC Channel 5. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO5 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH6, CH7, CH8, CH1, CH2, CH3, CH4).
36	SDO6	CMOS Serial Data Output for ADC Channel 6. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO6 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH7, CH8, CH1, CH2, CH3, CH4, CH5).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 9. Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Description
39	SDO7	CMOS Serial Data Output for ADC Channel 7. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO7 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH8, CH1, CH2, CH3, CH4, CH5, CH6).
40	SDO8	CMOS Serial Data Output for ADC Channel 8. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 13 SCK edges are required for 13-bit conversion data to be read from SDO8 in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH1, CH2, CH3, CH4, CH5, CH6, CH7).
41	SCK	Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins in SDR mode (DDR = LOW). In DDR mode ($\overline{SDR}$/DDR = HIGH) each edge of this clock shifts the conversion result MSB first onto the SDO pins. The logic level is determined by OV_{DD}.
42	DNC	In CMOS mode do not connect this pin.
LVDS Data Output Option ($\overline{CMOS}$/LVDS = High or FLOAT)		
27, 28	$SDOA^+$, $SDOA^-$	LVDS Serial Data Output for ADC Channels 1 and 2. The conversion result is shifted CH1 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 32 SCK edges are required for 13-bit conversion data to be read from A_{IN1} and A_{IN2} on SDOA in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH3, CH4, CH5, CH6, CH7, CH8).Terminate with a 100 Ω resistor at the receiver (FPGA).
29, 30	$SDOB^+$, $SDOB^-$	LVDS Serial Data Output for ADC Channels 3 and 4. The conversion result is shifted CH3 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 32 SCK edges are required for 13-bit conversion data to be read from A_{IN3} and A_{IN4} on SDOB in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH5, CH6, CH7, CH8, CH1, CH2).Terminate with a 100 Ω resistor at the receiver (FPGA).
33, 34	$CLKOUT^+$, $CLKOUT^-$	Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. These pins echo the input at SCK with a small delay. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA).
35, 36	$SDOC^+$, $SDOC^-$	LVDS Serial Data Output for ADC channels 5 and 6. The conversion result is shifted CH5 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 32 SCK edges are required for 13-bit conversion data to be read from A_{IN5} and A_{IN6} on SDOA in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH7, CH8, CH1, CH2, CH3, CH4).Terminate with a 100 Ω resistor at the receiver (FPGA).
39, 40	$SDOD^+$, $SDOD^-$	LVDS Serial Data Output for ADC Channels 7 and 8. The conversion result is shifted CH7 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 32 SCK edges are required for 13-bit conversion data to be read from A_{IN7} and A_{IN8} on SDOA in SDR mode, 13 SCK edges in DDR mode. Supplying more clocks will yield data from subsequent channels (CH1, CH2, CH3, CH4, CH5, CH6).Terminate with a 100 Ω resistor at the receiver (FPGA).
41, 42	SCK^+, SCK^-	Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins in SDR mode ($\overline{SDR}$/DDR = LOW). In DDR mode ($\overline{SDR}$/DDR = HIGH) each edge of this clock shifts the conversion result MSB first onto the SDO pins. These pins must be differentially terminated by an external 100Ω resistor at the receiver (ADC).

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5 V, OV_{DD} = 2.5 V, REFOUT1,2,3,4 = 4.096 V, f_{SMPL} = 1.5 Msps, unless otherwise noted.

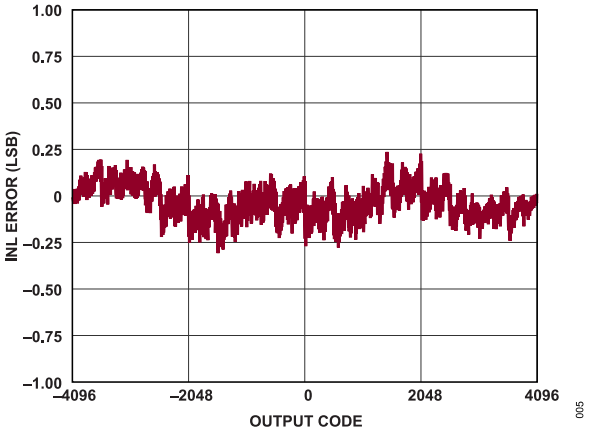


Figure 10. Integral Nonlinearity vs. Output Code

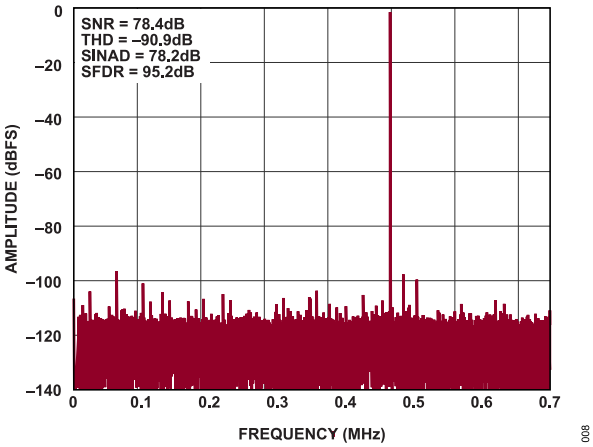


Figure 13. 32 k Point FFT, f_{SMPL} = 1.5 Msps, f_{IN} = 500 kHz

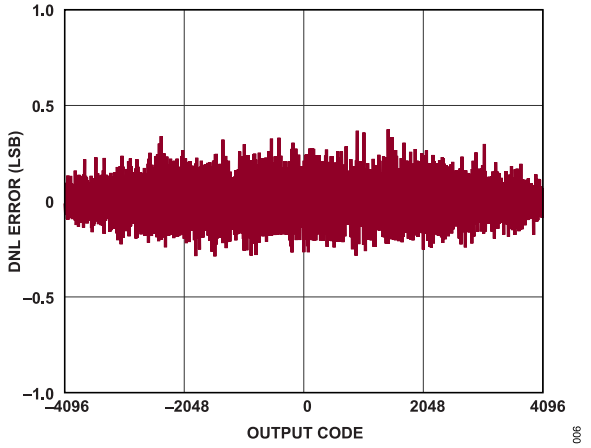


Figure 11. Differential Nonlinearity vs. Output Code

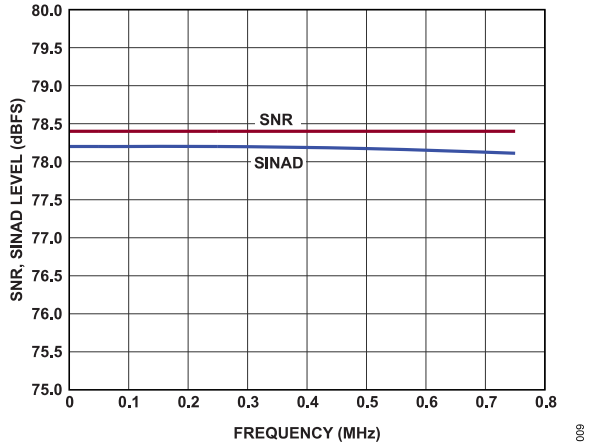


Figure 14. SNR, SINAD vs. Input Frequency (1 kHz to 750 kHz)

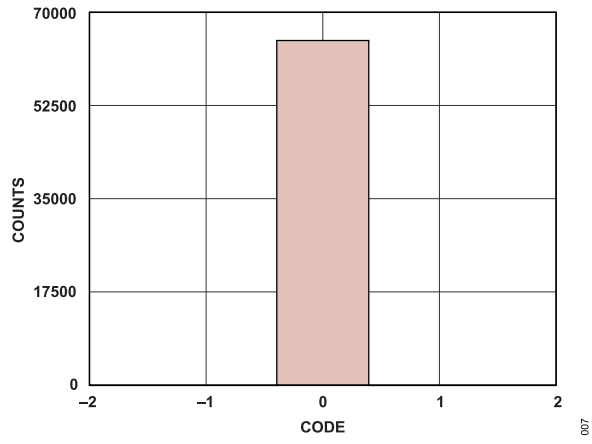


Figure 12. DC Histogram

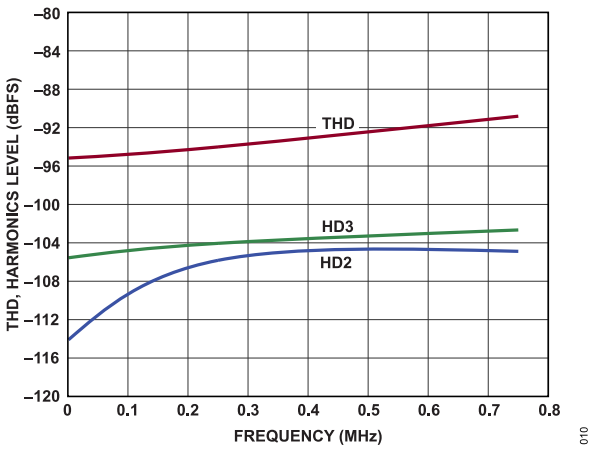


Figure 15. THD, Harmonics vs. Input Frequency (1 kHz to 750 kHz)

TYPICAL PERFORMANCE CHARACTERISTICS

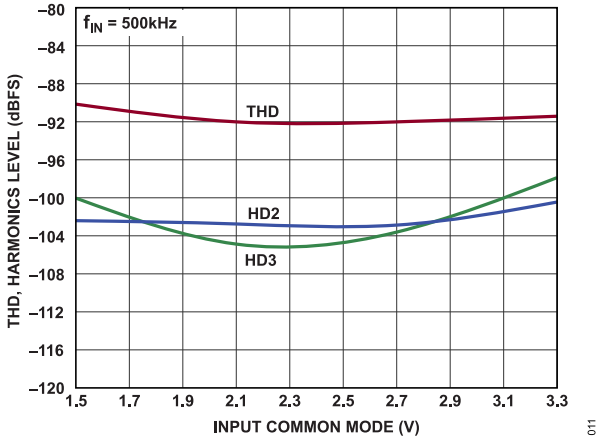


Figure 16. THD, Harmonics vs. Input Common Mode

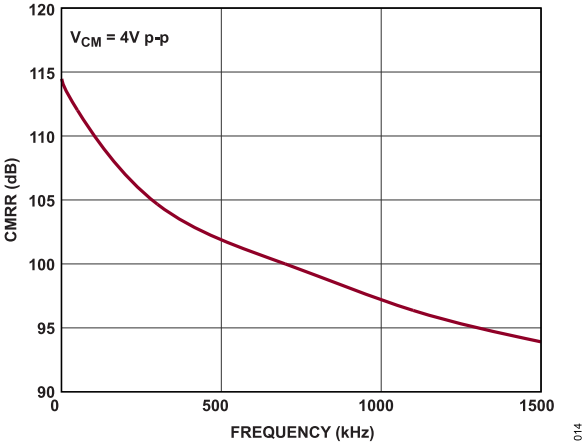


Figure 19. CMRR vs. Input Frequency

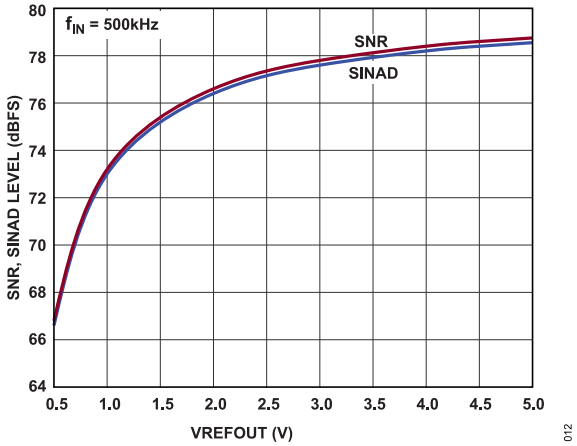


Figure 17. SNR, SINAD vs. Reference Voltage, f_{IN} = 500 kHz

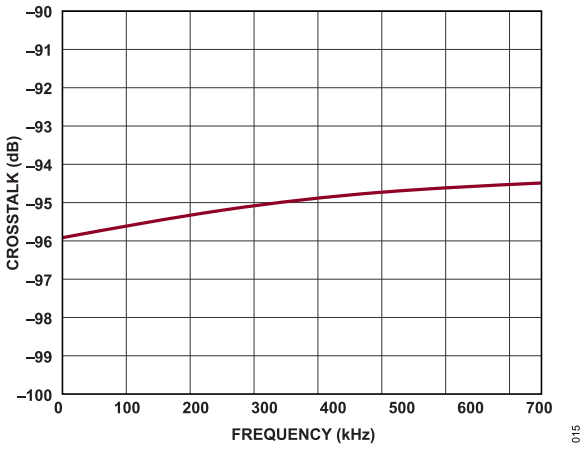


Figure 20. Crosstalk vs. Input Frequency

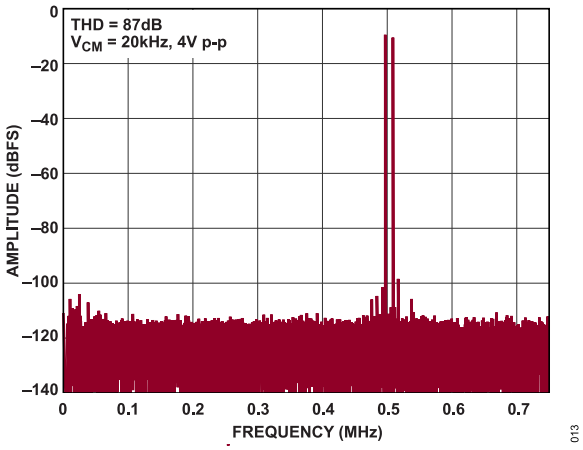


Figure 18. 32 k Point FFT, IMD, f_{SMPL} = 1.5 Msps, A_{IN+} = 490 kHz, A_{IN-} = 510 kHz

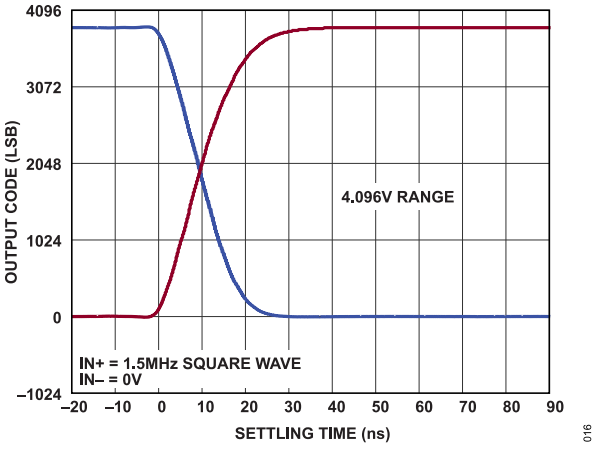


Figure 21. Step Response (Large Signal Settling)

TYPICAL PERFORMANCE CHARACTERISTICS

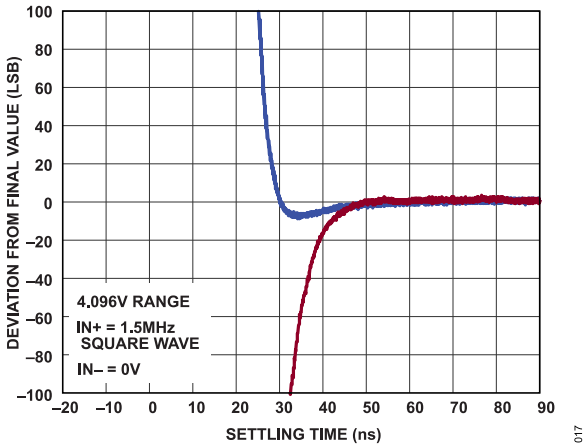


Figure 22. Step Response (Fine Settling)

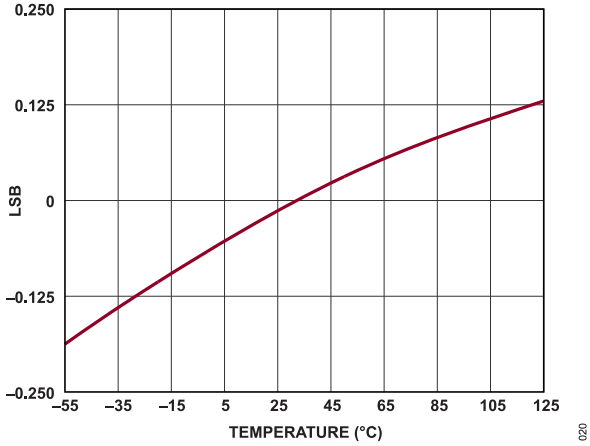


Figure 25. Offset Error vs. Temperature

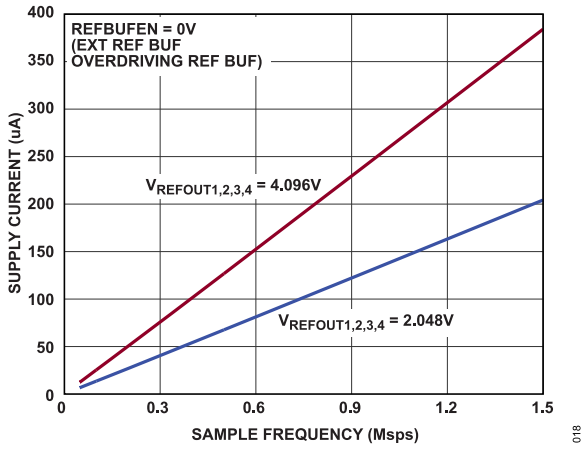


Figure 23. External Reference Supply Current vs. Sample Frequency

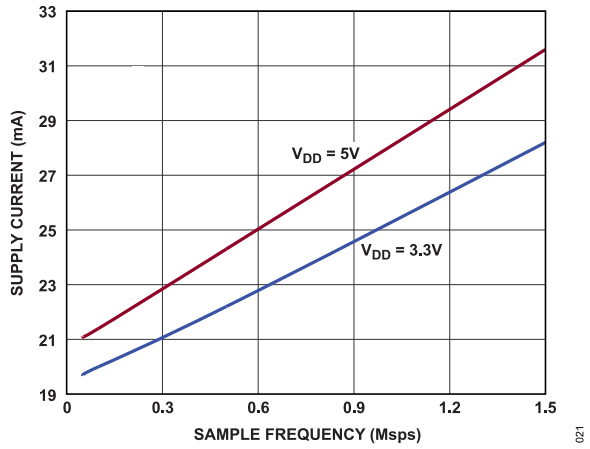


Figure 26. Supply Current vs. Sample Frequency

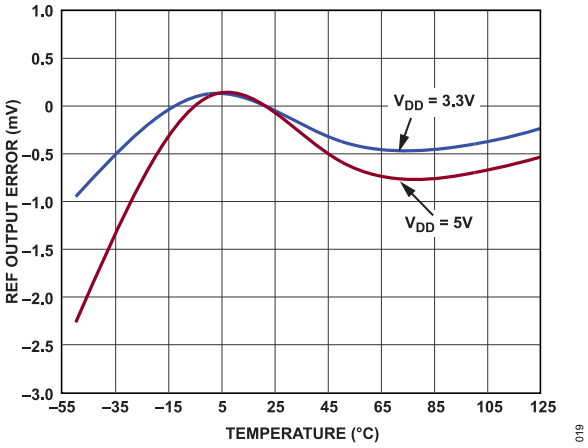


Figure 24. REF Output vs. Temperature

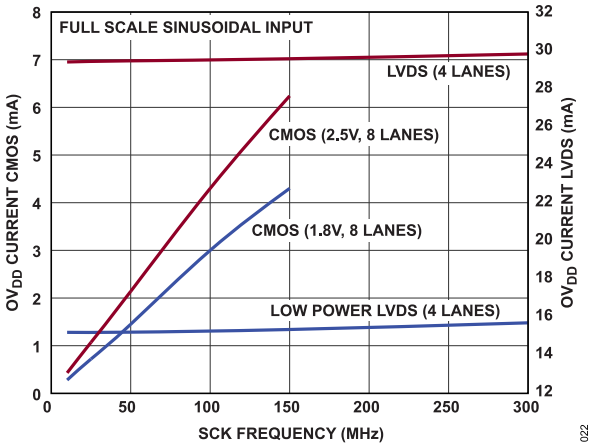


Figure 27. OV_{DD} Current vs. SCK Frequency, C_{LOAD} = 10 pF

APPLICATIONS INFORMATION

OVERVIEW

The LTC2320-12 is a low noise, high speed 12-bit successive approximation register (SAR) ADC with differential inputs and a wide input common mode range. Operating from a single 3.3 V or 5 V supply, the LTC2320-12 has a 4 V_{P-P} or 8 V_{P-P} differential input range, making it ideal for applications which require a wide dynamic range. The LTC2320-12 achieves ±0.25 LSB INL typical, no missing codes at 12 bits and 77 dB SNR.

The LTC2320-12 has an onboard reference buffer and low drift (20 ppm/°C max) 4.096 V temperature-compensated reference. The LTC2320-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 1.5 Msps per channel throughput with no latency makes the LTC2320-12 ideally suited for a wide variety of high speed applications. The LTC2320-12 dissipates only 20 mW per channel. Nap and sleep modes are also provided to reduce the power consumption of the LTC2320-12 during inactive periods for further power savings.

CONVERTER OPERATION

The LTC2320-12 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A_{IN^+} and A_{IN^-} to sample the differential analog input voltage, as shown in Figure 29. A falling edge on the $\overline{CNV}$ pin initiates a conversion. During the conversion phase, the 12-bit CDAC is sequenced through a successive approximation algorithm effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., $V_{REFOUT}/2$, $V_{REFOUT}/4$ … $V_{REFOUT}/32768$) using a differential comparator. At the end of conversion, a CDAC output approximates the sampled analog input. The ADC control logic then prepares the 12-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2320-12 digitizes the full-scale voltage of 2 • REFOUT into 2^{13} levels, resulting in an LSB size of 1mV with REFBUF = 4.096V. The ideal transfer function is shown in Figure 28. The output data is in 2's complement format. When driven by fully differential inputs, the transfer function spans 2^{13} codes. When driven by pseudo-differential inputs, the transfer function spans 2^{12} codes.

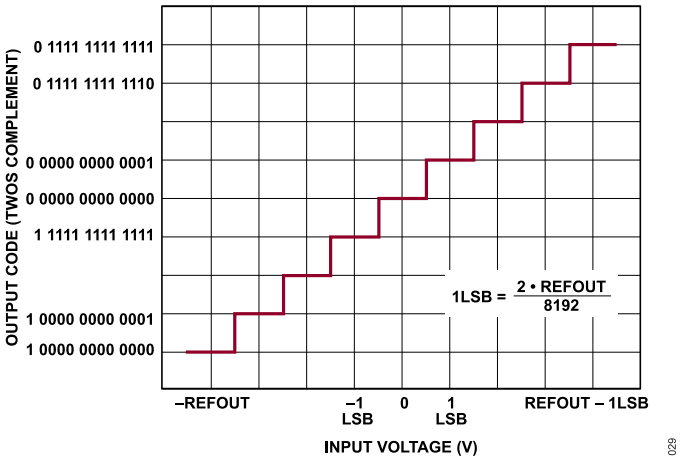


Figure 28. LTC2320-12 Transfer Function

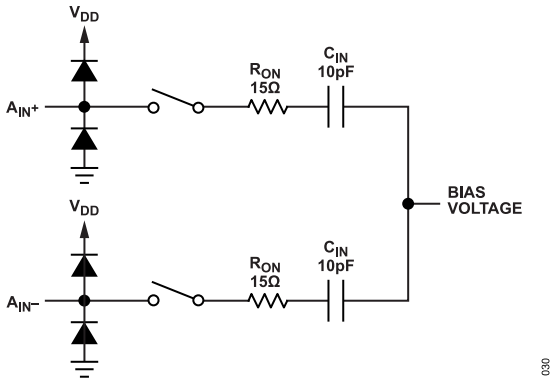


Figure 29. The Equivalent Circuit for the Differential Analog Input of the LTC2320-12

APPLICATIONS INFORMATION

Table 10. Code Ranges for the Analog Input Operational Modes

Mode	Span ($V_{IN^+} - V_{IN^-}$)	Min Code	Min Code
Fully Differential	–REFOUT to +REFOUT	1 0000 0000 0000	0 1111 1111 1111
Pseudo-Differential Bipolar	–REFOUT/2 to +REFOUT/2	1 1000 0000 0000	0 0111 1111 1111
Pseudo-Differential Unipolar	0 to REFOUT	0 0000 0000 0000	0 1111 1111 1111

Analog Input

The differential inputs of the LTC2320-12 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2320-12 digitizes the difference voltage between the A_{IN^+} and A_{IN^-} pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between V_{DD} and GND. The LTC2320-12 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2320-12 can be modeled by the equivalent circuit shown in Figure 29. The back-to-back diodes at the inputs form clamps that provide ESD protection. In the acquisition phase, 10 pF (C_{IN}) from the sampling capacitor in series with approximately 15 Ω (R_{ON}) from the on-resistance of the sampling switch is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the C_{IN} capacitors during acquisition.

Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2320-12. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other A_{IN} pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2320-12 flexibility handles both pseudo-differential unipolar and bipolar signals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically $V_{REF}/2$, and applying a signal to the other A_{IN} pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 30, and the corresponding transfer function in Figure 31. The fixed analog input pin need not be set at $V_{REF}/2$, but at some point within the V_{DD} rails allowing the alternate input to swing symmetrically around this voltage. If the input signal ($A_{IN^+} - A_{IN^-}$) swings beyond ±REFOUT1,2,3,4/2, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other A_{IN} pin. In this case, the analog input swings between ground and V_{REF} yielding unipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 32, and the corresponding transfer function in Figure 33. If the input signal ($A_{IN^+} - A_{IN^-}$) swings negative, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

APPLICATIONS INFORMATION

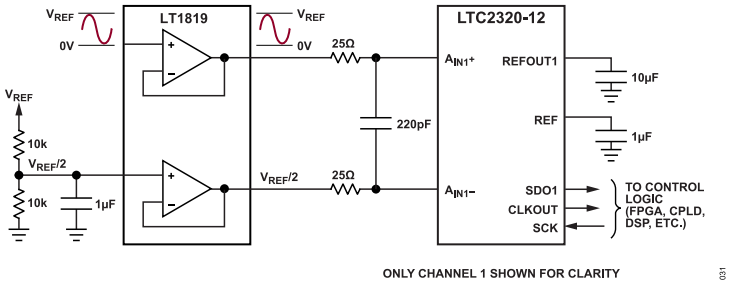


Figure 30. Pseudo-Differential Bipolar Application Circuit

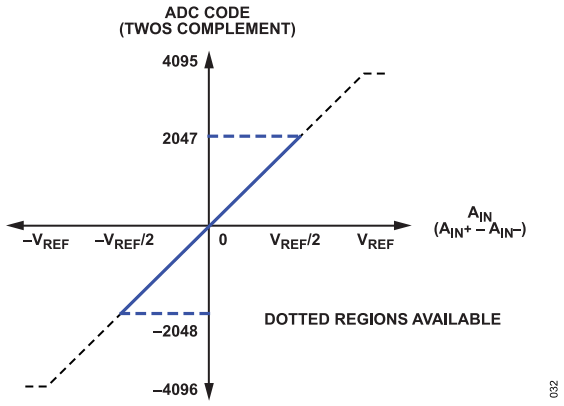


Figure 31. Pseudo-Differential Bipolar Transfer Function

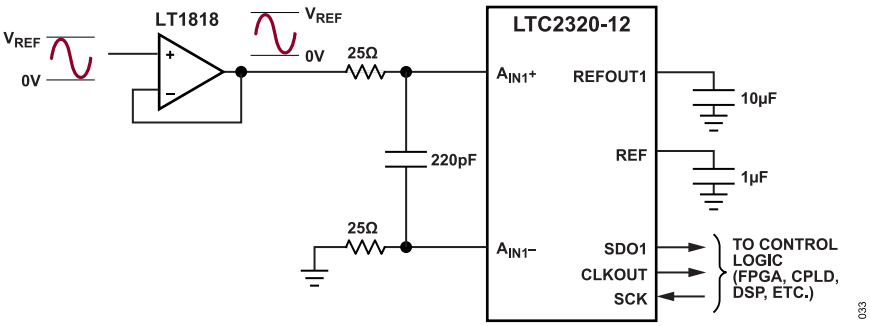


Figure 32. Pseudo-Differential Unipolar Application Circuit

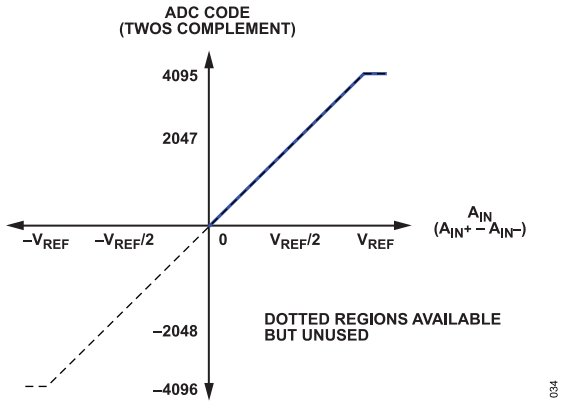


Figure 33. Pseudo-Differential Unipolar Transfer Function

APPLICATIONS INFORMATION

Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2320-12, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 34. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

Fully-Differential Inputs

To achieve the best distortion performance of the LTC2320-12, we recommend driving a fully-differential signal through LT1819 amplifiers configured as two unity-gain buffers, as shown in Figure 35. This circuit achieves the full data sheet THD specification of –90 dB at input frequencies up to 500 kHz. A fully-differential input signal can span the maximum full-scale of the ADC, up to ±REFOUT1,2,3,4. The common mode input voltage can span the entire supply range up to V_{DD}, limited by the input signal swing. The fully-differential configuration is illustrated in Figure 36, with the corresponding transfer function illustrated in Figure 37.

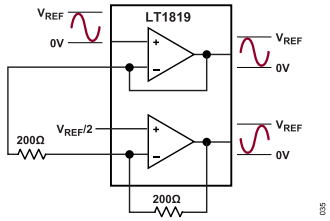


Figure 34. Single-Ended to Differential Driver

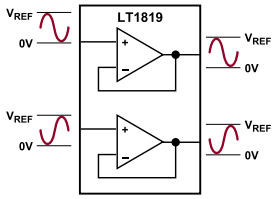


Figure 35. LT1819 Buffering a Fully-Differential Signal Source

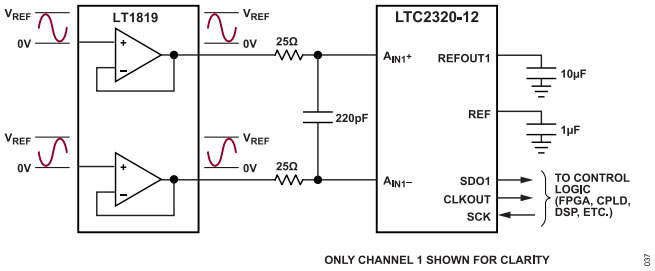


Figure 36. Fully-Differential Application Circuit

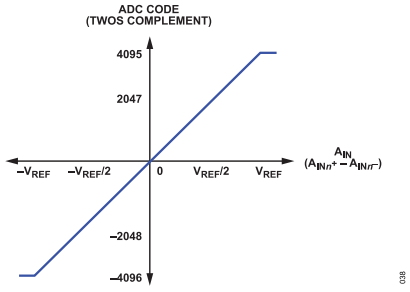


Figure 37. Fully-Differential Transfer Function

APPLICATIONS INFORMATION

INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2320-12 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike when during acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2320-12. The amplifier provides low output impedance to minimize gain error and allows for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 38 is sufficient for many applications.

The sampling switch on-resistance (R_{ON}) and the sample capacitor (C_{IN}) form a second lowpass filter that limits the input bandwidth to the ADC core to 110 MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

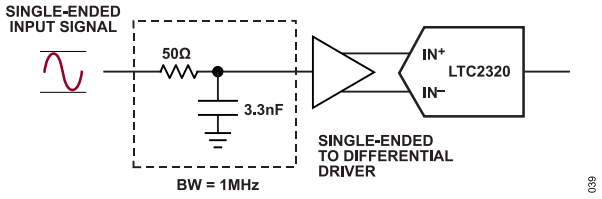


Figure 38. Input Signal Chain

ADC REFERENCE

Internal Reference

The LTC2320-12 has an on-chip, low noise, low drift (20 ppm/°C max), temperature compensated bandgap reference. It is internally buffered and is available at REF (Pin 8). The reference buffer gains the internal reference voltage to 4.096 V for supply voltages V_{DD} = 5 V and to 2.048 V for V_{DD} = 3.3 V. The REF pin also drives the four internal reference buffers with a current limited output (250 µA) so it may be easily overdriven with an external reference in the range of 1.25 V to V_{DD} – 0.4 V. Bypass REF to GND with a 1 µF (X5R, 0805 size) ceramic capacitor to compensate the reference buffer and minimize noise. The 1 µF capacitor should be as close as possible to the LTC2320-12 package to minimize wiring inductance. The voltage on the REF pin must be externally buffered if used for external circuitry.

External Reference

The internal REFOUT1,2,3,4 buffers can also be overdriven from 1.25 V to 5 V with an external reference at REFOUT1,2,3,4 as shown in Figure 41. To do so, REFBUFEN must be grounded to disable the REF buffers. A 55 k internal resistance loads the REFOUT1,2,3,4 pins when the REF buffers are disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5 V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a 10 µF ceramic capacitor (X5R, 0805 size) close to each of the REFOUT1,2,3,4 pins. If the REF pin voltage is used as a REFOUT reference when REFBUFEN is connected to GND, it should be buffered externally.

Table 11. Reference Configurations and Ranges

Reference Configuration	V_{DD}	REFBUFEN	REF Pin	REFOUT1,2,3,4 Pin	Differential Input Range
Internal Reference with Internal Buffers	5 V	5 V	4.096 V	4.096 V	±REFOUT
	3.3 V	3.3 V	2.048 V	2.048 V	±REFOUT
Common External Reference with Internal Buffer (REF Pin Externally Overdriven)	5 V	5 V	1.25 V to V_{DD} – 0.4 V	1.25 V to V_{DD} – 0.4 V	±REFOUT
	3.3 V	3.3 V	1.25 V to V_{DD} – 0.4 V	1.25 V to V_{DD} – 0.4 V	±REFOUT
External Reference with REF Buffers Disabled	5 V	0 V	4.096 V	1.25 V to V_{DD}	±REFOUT
	3.3 V	0 V	2.048 V	1.25 V to V_{DD}	±REFOUT

APPLICATIONS INFORMATION

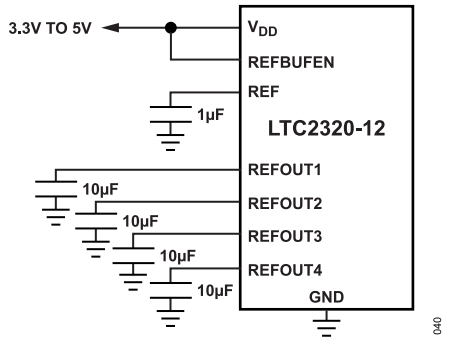


Figure 39. LTC2320-12 Internal Reference Circuit

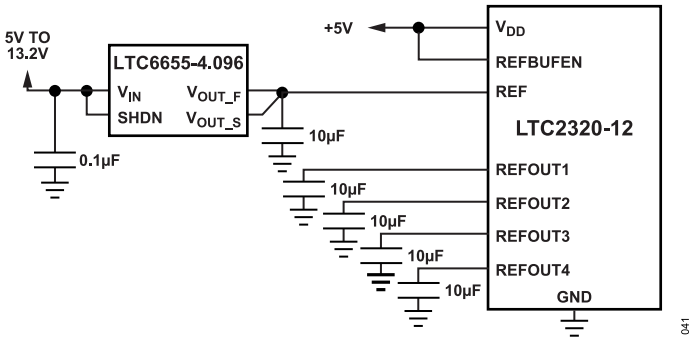


Figure 40. LTC2320-12 with a Shared External Reference Circuit

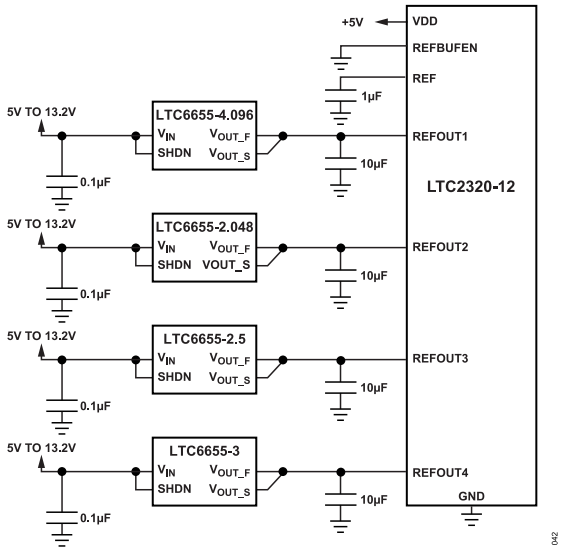


Figure 41. LTC2320-12 with Different External Reference Voltages

APPLICATIONS INFORMATION

Internal Reference Buffer Transient Response

The REFOUT1,2,3,4 pins of the LTC2320-12 draw charge (Q_{CONV}) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to $I_{REF} = Q_{CONV}/t_{CYC}$. Thus, the DC current draw of $I_{REFOUT1,2,3,4}$ depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 42, I_{REFBUF} quickly goes from approximately ~75 µA to a maximum of 500 µA for REFOUT = 5 V at 1.5 Msps. This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT will affect the accuracy of the output code. If an external reference is used to overdrive REFOUT1,2,3,4, the fast settling LTC6655 reference is recommended.

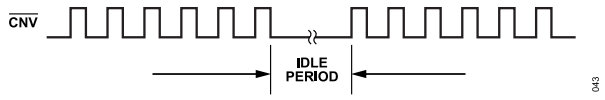


Figure 42. $\overline{CNV}$ Waveform Showing Burst Sampling

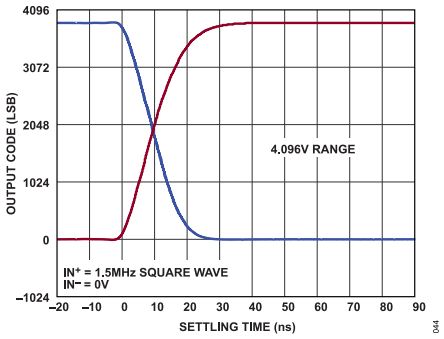


Figure 43. Transient Response of the LTC2320-12

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2320-12 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling frequency. Figure 44 shows that the LTC2320-12 achieves a typical SINAD of 77 dB at a 1.5 MHz sampling rate with a 500 kHz input.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 44 shows that the LTC2320-12 achieves a typical SNR of 77 dB at a 1.5 MHz sampling rate with a 500 kHz input.

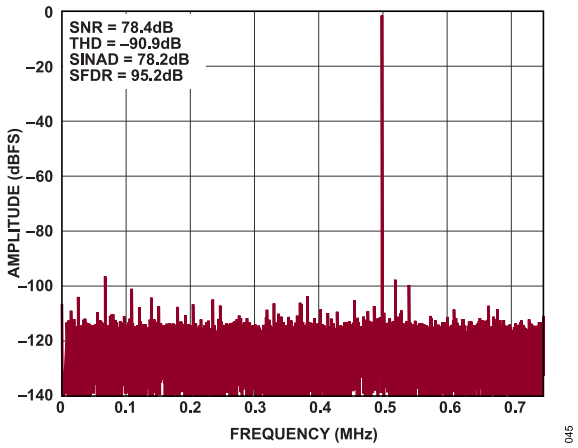


Figure 44. 32 k Point FFT of the LTC2320-12

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V2^2 + V3^2 + V4^2 + \ldots + V_N{}^2}}{V1} \quad (1)$$

where *V1* is the RMS amplitude of the fundamental frequency and *V2* through V_N are the amplitudes of the second through Nth harmonics.

POWER CONSIDERATIONS

The LTC2320-12 requires two power supplies: the 3.3 V to 5 V power supply (V_{DD}), and the digital input/output interface power supply (OV_{DD}). The flexible OV_{DD} supply allows theLTC2320-12 to communicate with any digital logic operating between 1.8 V and 2.5 V. When using LVDS I/O, the OV_{DD} supply must be set to 2.5 V.

Power Supply Sequencing

The LTC2320-12 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2320-12 has a power-on-reset (POR) circuit that will reset the LTC2320-12 at initial power-up or whenever the power supply voltage drops below 2 V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10 ms after a

APPLICATIONS INFORMATION

POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

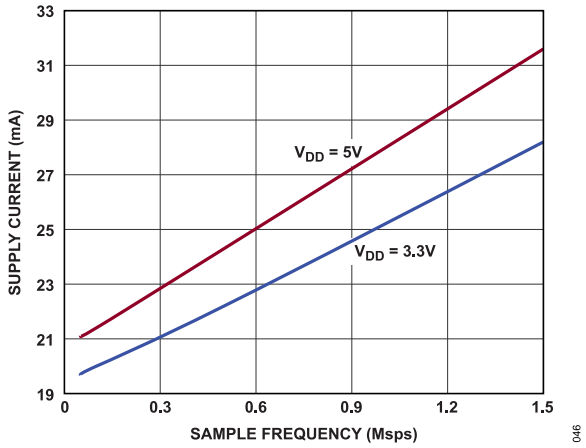


Figure 45. Power Supply Current of the LTC2320-12 Versus Sampling Rate

TIMING AND CONTROL

$\overline{CNV}$ Timing

The LTC2320-12 sampling and conversion is controlled by $\overline{CNV}$. A rising edge on $\overline{CNV}$ will start sampling and the falling edge starts the conversion and readout process. The conversion process is timed by the SCK input clock. For optimum performance, $\overline{CNV}$ should be driven by a clean low jitter signal. The Typical Application at the back of the data sheet illustrates a recommended implementation to reduce the relatively large jitter from an FPGA $\overline{CNV}$ pulse source. Note the low jitter input clock times the falling edge of the $\overline{CNV}$ signal. The rising edge jitter of $\overline{CNV}$ is much less critical to performance. The typical pulse width of the $\overline{CNV}$ signal is 30 ns with < 1.5 ns rise and fall times at a 1.5 Msps conversion rate.

SCK Serial Data Clock Input

In SDR mode ($\overline{SDR}$/DDR Pin 23 = GND), the falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 100 MHz external clock must be applied at the SCK pin to achieve 1.5 Msps throughput using all eight SDO outputs. In DDR mode ($\overline{SDR}$/DDR Pin 23 = OV_{DD}), each input edge of SCK shifts the conversion result MSB first onto the SDO pins. A 50 MHz external clock must be applied at the SCK pin to achieve 1.5 Msps throughput using all eight SDO1 through SDO8 outputs.

CLKOUT Serial Data Clock Output

The CLKOUT output provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. For low throughput speed applications, CLKOUT can be disabled by tying Pin 34 to OV_{DD}.

Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2320-12, the SCK signal must be held high or low and a series of two $\overline{CNV}$ pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of $\overline{CNV}$ initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further $\overline{CNV}$ pulses are applied. The SCK rising edge will put the LTC2320-12 back into the operational (full-power) state. When in nap mode, two additional pulses will put the LTC2320-12 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2320-12 into operational mode. A 10ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth $\overline{CNV}$ pulse. The fifth pulse will return the LTC2320-12 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive $\overline{CNV}$ pulses will cycle the LTC2320-12 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 46, Figure 47, Figure 48, and Figure 49 for more detailed timing information about sleep and nap modes.

APPLICATIONS INFORMATION

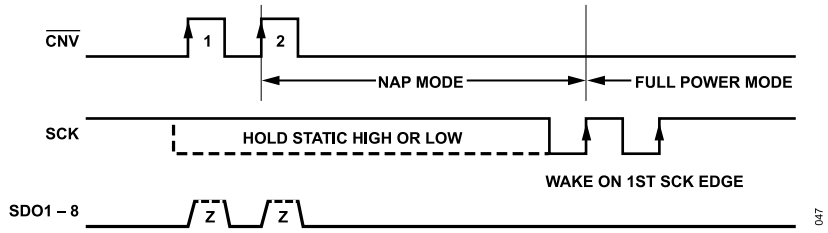


Figure 46. CMOS and LVDS Mode NAP and WAKE Using SCK

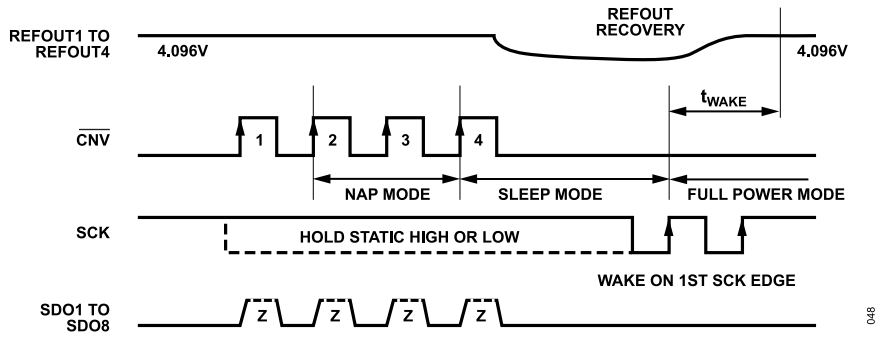


Figure 47. CMOS Mode SLEEP and WAKE Using SCK

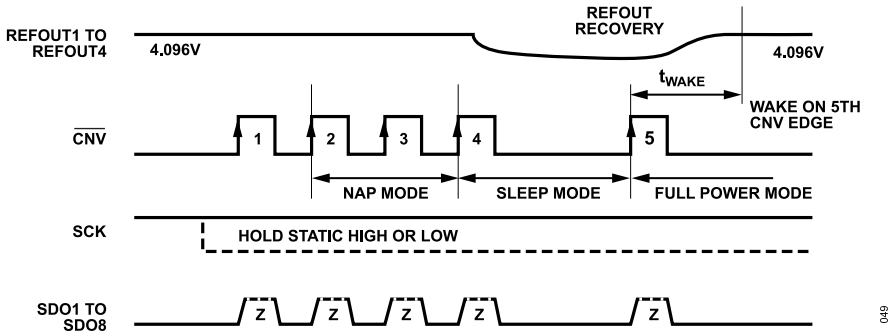


Figure 48. LVDS and CMOS Mode SLEEP and WAKE Using $\overline{CNV}$

APPLICATIONS INFORMATION

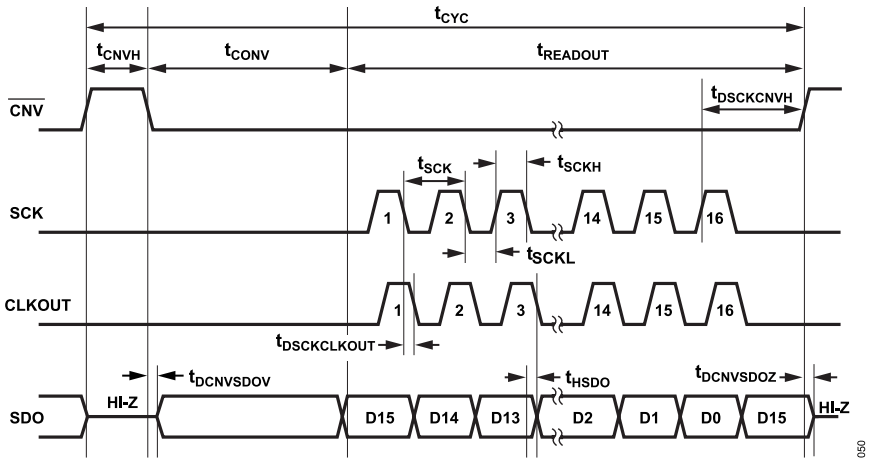


Figure 49. LTC2320-12 Timing Diagram (SDR Mode Timing)

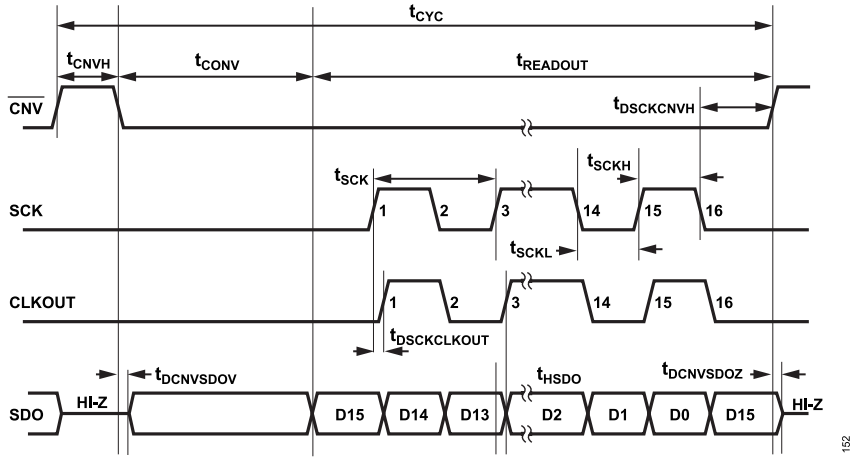


Figure 50. LTC2320-12 Timing Diagram (DDR Mode Timing)

APPLICATIONS INFORMATION

DIGITAL INTERFACE

The LTC2320-12 features a serial digital interface that is simple and straightforward to use. The flexible OV_{DD} supply allows the LTC2320-12 to communicate with any digital logic operating between 1.8 V and 2.5 V. In addition to a standard CMOS SPI interface, the LTC2320-12 provides an optional LVDS SPI interface to support low noise digital design. The $\overline{CMOS}$/LVDS pin is used to select the digital interface mode. The SCK input clock shifts the conversion result MSB first on the SDO pins. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. In CMOS mode, use the SDO1 – SDO8, and CLKOUT pins as outputs. Use the SCK pin as an input. In LVDS mode, use the $SDOA^+/SDOA^-$ through $SDOD^+/SDOD^-$ and $CLKOUT^+/CLKOUT^-$ pins as differential outputs. Each LVDS lane yields two channels worth of data: SDOA yields CH1 and CH2 data, SDOB yields CH3 and CH4 data, SDOC yields CH5 and CH6 data and SDOD yields CH7 and CH8 data. These pins must be differentially terminated by an external 100 Ω resistor at the receiver (FPGA). The SCK^+/SCK^- pins are differential inputs and must be terminated differentially by an external 100 Ω resistor at the receiver (ADC).

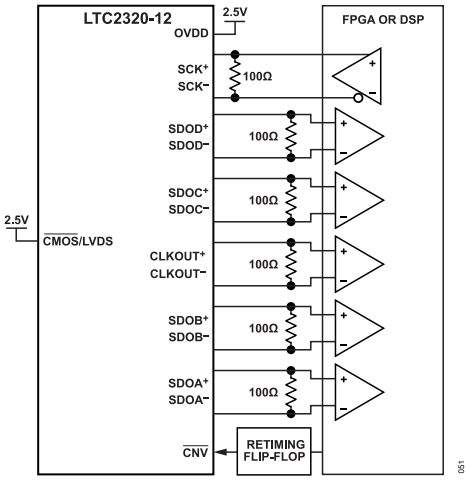


Figure 51. LTC2320-12 Using the LVDS Interface

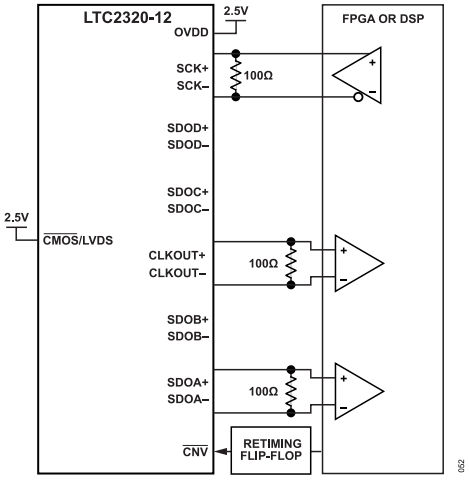


Figure 52. LTC2320-12 Using the LVDS Interface with One Lane

APPLICATIONS INFORMATION

SDR/DDR Modes

The LTC2320-12 has an SDR (single data rate) and DDR (double data rate) mode for reading conversion data from the SDO pins. In both modes, CLKOUT is a delayed version of SCK. In SDR mode, each negative edge of SCK shifts the conversion data out the SDO pins. In DDR mode, each edge of the SCK input shifts the conversion data out. In DDR mode, the required SCK frequency is half of what is required in SDR mode. Tie $\overline{SDR}$/DDR to ground to configure for SDR mode and to OV_{DD} for DDR mode. The CLKOUT signal is a delayed version of the SCK input and is phase aligned with the SDO data. In SDR mode, the SDO transitions on the falling edge of CLKOUT as illustrated in Figure 49. We recommend using the rising edge of CLKOUT to latch the SDO data into the FPGA register in SDR mode. In DDR mode, The SDO transitions on each input edge of SCK. We recommend using the CLKOUT rising and falling edges to latch the SDO data into the FPGA registers in DDR mode. Since CLKOUT and SDO data is phase aligned, the SDO signals will need to be digitally delayed in the FPGA to provide adequate setup and hold timing margins in DDR mode.

Multiple Data Lanes

The LTC2320-12 has up to eight SDO data lanes in CMOS mode and four SDO lanes in LVDS mode. In CMOS mode, the number of possible data lanes range from eight (SDO1 – SDO8), four (SDO1, SDO3, SDO5 and SDO7), two (SDO1 and SDO5) and one (SDO1). Generally, the more data lanes used, the lower the required SCK frequency. When using less than eight lanes in CMOS mode, there is a limit on the maximum possible conversion frequency (see Table 12). Each SDO pin will hold the MSB of the conversion data. In DDR mode you can use a SCK frequency half the SDR mode. See Table 12 for examples of various possibilities and the resulting SCK frequency required.

CMOS

In CMOS mode, the number of possible data lanes range from eight (SDO1 – SDO8), four (SDO1, SDO3, SDO5 and SDO7), two (SDO1 and SDO5) and one (SDO1). As suggested in the CMOS Timing Diagrams, each SDO lane outputs the conversion results for all analog input channels in a sequential circular manner. For example, the first conversion result on SDO1 corresponds to analog input channel 1, followed by the conversion results for channels 2 through 8. The data output on SDO1 then wraps back to channel 1 and this pattern repeats indefinitely. Other SDO lanes follow a similar circular pattern except the first conversion result presented on each lane corresponds to its associated analog input channel.

Applications that cannot accommodate the full eight lanes of serial data may employ fewer lanes without reconfiguring the LTC2320-12. For example, capturing the first two conversion results (32 SCK cycles total in SDR mode and 32 SCK edges in DDR mode) from SDO1, SDO3, SDO5, and SDO7 provides data for analog input channels 1 and 2, 3 and 4, 5 and 6, and 7 and 8, respectively, using four output lanes. Similarly, capturing the first four conversion results (64 SCK cycles total in SDR mode and 64 SCK edges in DDR mode) from SDO1 and SDO5 provides data for analog input channels 1 to 4 and 5 to 8, respectively, using two output lanes. If only one lane can be accommodated, capturing the first eight conversion results (128 SCK cycles total in SDR mode and 128 SCK edges in DDR mode) from SDO1 provides data for all analog input channels. Generally, the more data lanes used, the lower the required SCK frequency. When using less than eight lanes in CMOS mode, there is a limit on the maximum possible conversion frequency. See Table 12 for examples of various possibilities and the resulting SCK frequency required.

LVDS

In LVDS mode, the number of possible data lane pairs range from four (SDOA – SDOD), two (SDOA and SDOC) and one (SDOA). As suggested in the LVDS Timing Diagrams, each SDO lane pair outputs the conversion results for all analog input channels in a sequential circular manner. For example, the first conversion result on SDOA corresponds to analog input channel pair 1 and 2, followed by the conversion results for channels 3 through 8. The data output on SDOA then wraps back to channel 1 and this pattern repeats indefinitely. Other SDO lanes follow a similar circular pattern except the first conversion result presented on each lane corresponds to its associated analog input channel pairs (SDOA: analog inputs 1 and 2, SDOB: analog inputs 3 and 4, SDOC: analog inputs 5 and 6 and SDOD: analog inputs 7 and 8).

Applications that cannot accommodate the full four lanes of serial data may employ fewer lanes without reconfiguring the LTC2320-12. For example, capturing the first four conversion results (64 SCK cycles total in SDR mode and 64 SCK edges in DDR mode) from SDOA and SDOC provides data for analog input channels 1 through 4, and 5 through 8, respectively, using two output lanes. If only one lane can be accommodated, capturing the first eight conversion results (128 SCK cycles total in SDR mode and 128 SCK edges in DDR mode) from SDOA provides data for all analog input channels. Generally, the more data lanes used, the lower the required SCK frequency. When using less than four lanes in LVDS mode, there is a limit on the maximum possible conversion frequency. See Table 12 for examples of various possibilities and the resulting SCK frequency required.

APPLICATIONS INFORMATION

BOARD LAYOUT

To obtain the best performance from the LTC2320-12, a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

Recommended Layout

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to DC2395A, the evaluation kit for the LTC2320-12.

Table 12. Conversion Frequency for Various I/O Modes

I/O Mode	$\overline{CMOS}$/ LVDS Pin	$\overline{SDR}$[1]/DDR[2] Pin	SDO1 – 8 Lanes	SDOA – D Lanes	SCK FREQ (MHz)	CLKOUT FREQ (MHz)	SCK Cycles[3, 4]	OV_{DD}	Conversion Frequency (Msps/CH)[5]
CMOS	GND (CMOS)	GND (SDR)	SDO1 – SDO8		100	100	16	1.8 V to 2.5 V	1.5
		OV_{DD} (DDR)	SDO1 – SDO8		50	50	8		1.5
		OV_{DD} (DDR)	SDO1, SDO3, SDO5, SDO7		50	50	16		1.25
		GND (SDR)	SDO1		100	100	128		0.5
LVDS	OV_{DD} (LVDS)	GND (SDR)		SDOA – SDOD	200	200	32	2.5 V	1.5
		OV_{DD} (DDR)		SDOA – SDOD	100	100	16		1.5
		OV_{DD} (DDR)		SDOA, SDOC	150	150	32		1.4
		GND (SDR)		SDOA	300	300	128		1.0

1 Conversion Period (SDR) = t_{CNV_MIN} + t_{CONV_MAX} + (128/(Lanes • f_{SCK})).

2 Conversion Period (DDR) = t_{CNV_MIN} + t_{CONV_MAX} + (64/(Lanes • f_{SCK})).

3 SCK Cycles (SDR) = 128/Lanes.

4 SCK Cycles (DDR) = 64/Lanes.

5 Conversion Frequency = 1/Conversion Period.

TYPICAL APPLICATION

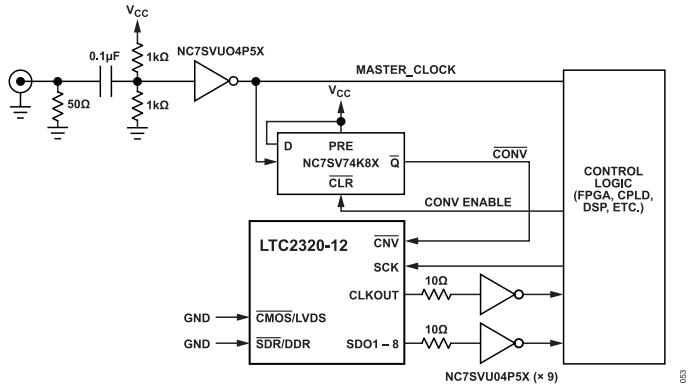


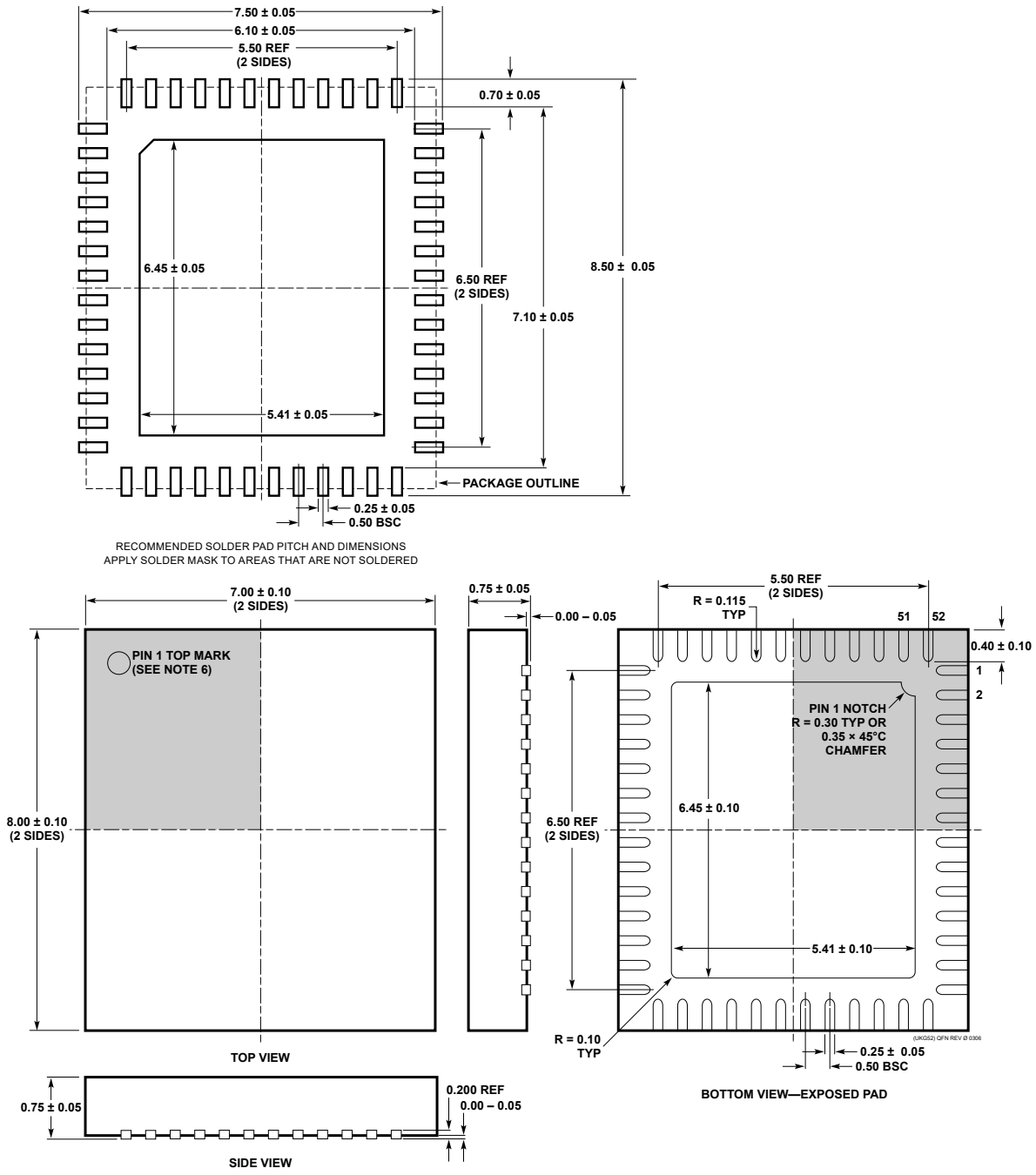
Figure 53. Low Jitter Clock Timing with RF Sine Generator Using Clock Squaring/Level-Shifting Circuit and Retiming Flip-Flop

RELATED PARTS

Table 13.

Part Number	Description	Comments
ADCs		
LTC2310-16/LTC2310-14/ LTC2310-12	16-/14-/12-Bit Differential Input ADC with Wide Input Common Mode	3.3 V/5 V Supply, Single-Channel, 35 mW, 20 ppm/°C Max Internal Reference, Flexible Inputs, 16-Lead MSOP Package
LTC2321-16/LTC2321-14/ LTC2321-12	Dual 16-/14-/12-Bit, 2 Msps/Ch, Simultaneous Sampling ADCs	3.3 V/5 V Supply, 33 mW/Ch, 20 ppm°C Max Internal Reference, Flexible Inputs, 4 mm × 5 mm QFN-28 Package
LTC2324-16/LTC2324-14/ LTC2324-12	Quad 16-/14-/12-Bit 2 Msps/Ch Simultaneous Sampling ADCs	3.3 V/5 V Supply, Single-Channel, 40 mW, 20 ppm/°C Max Internal Reference, Flexible Inputs, 52-Lead QFN Package
LTC2370-16/LTC2368-16/ LTC2367-16/LTC2364-16	16-Bit, 2 Msps/1 Msps/500 ksps/250 ksps Serial, Low Power ADCs	2.5 V Supply, Pseudo-Differential Unipolar Input, 94 dB SNR, 5 V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4 mm × 3 mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2 Msps/1 Msps/500 ksps/250 ksps Serial, Low Power ADCs	2.5 V Supply, Differential Input, 96.2 dB SNR, ±5 V Input Range, DGC, Pin-Compatible Family in MSOP-16 and 4 mm × 3 mm DFN-16 Packages
DACs		
LTC2632	Dual 12-/10-/8-Bit, SPI V_{OUT} DACs with Internal Reference	2.7 V to 5.5 V Supply Range, 10 ppm/°C Reference, External REF Mode, Rail-to-Rail Output, 8-Pin ThinSOT™ Package
LTC2602/LTC2612/LTC2622	Dual 16-/14-/12-Bit SPI V_{OUT} DACs with External Reference	300 µA per DAC, 2.5 V to 5.5 V Supply Range, Rail-to-Rail Output, 8-Lead MSOP Package
References		
LTC6655	Precision Low Drift, Low Noise Buffered Reference	5 V/4.096 V/3.3 V/3 V/2.5 V/2.048 V/1.25 V, 2 ppm/°C, 0.25 ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift, Low Noise Buffered Reference	5 V/4.096 V/3.3 V/3 V/2.5 V/2.048 V/1.25 V, 5 ppm/°C, 2.1 ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1818/LT1819	400 MHz, 2500 V/µs, 9 mA Single/Dual Operational Amplifiers	–85 dBc Distortion at 5 MHz, 6 nV/√Hz Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT1806	325 MHz, Single, Rail-to-Rail Input and Output, Low Distortion, Low Noise Precision Op Amps	–80 dBc Distortion at 5 MHz, 3.5 nV/√Hz Input Noise Voltage, 9mA Supply Current, Unity-Gain Stable
LT6200	165 MHz, Rail-to-Rail Input and Output, 0.95 nV/√Hz Low Noise, Op Amp Family	Low Noise, Low Distortion, Unity-Gain Stable

OUTLINE DIMENSIONS



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Figure 54. 52-Lead Plastic QFN (7mm × 8mm)
(Reference LTC DWG # 05-08-1729 Rev Ø)

OUTLINE DIMENSIONS

Updated: March 07, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
LTC2320CUKG-12#PBF	0°C to +70°C	52-Lead QFN (7mm x 8mm x 0.75mm w/ EP)		05-08-1729
LTC2320CUKG-12#TRPBF	0°C to +70°C	52-Lead QFN (7mm x 8mm x 0.75mm w/ EP)	Reel, 2000	05-08-1729
LTC2320HUKG-12#PBF	-40°C to +125°C	52-Lead QFN (7mm x 8mm x 0.75mm w/ EP)		05-08-1729
LTC2320HUKG-12#TRPBF	-40°C to +125°C	52-Lead QFN (7mm x 8mm x 0.75mm w/ EP)	Reel, 2000	05-08-1729
LTC2320IUKG-12#PBF	-40°C to +85°C	52-Lead QFN (7mm x 8mm x 0.75mm w/ EP)		05-08-1729
LTC2320IUKG-12#TRPBF	-40°C to +85°C	52-Lead QFN (7mm x 8mm x 0.75mm w/ EP)	Reel, 2000	05-08-1729

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
DC2395A-G	Evaluation Board
DC890B	Evaluation Board

[1] All models are RoHS compliant.