

# NCN1188

## Data Switch, 3:1 High Speed USB Switch with Audio and MHL Capability

The NCN1188 allows portable systems to share a single USB 2.0 or 3.0 receptacle to transmit and receive paired signals from three separate locations. All of the three differential channels are compliant to High Speed USB 2.0, Full Speed USB 1.1, Low Speed USB 1.0 and any generic UART protocol. The two dedicated high speed data paths also support Mobile High Definition Link (MHL) video up to resolutions of 1080i (2.25 Gbps) and 1080p (3 Gbps in Packed Pixel mode). The multi-purpose audio path is capable of passing signals with negative voltages as low as 2 V below ground and features shunt resistors to reduce Pop and Click noise in the audio system. The NCN1188 is housed in a space saving, ultra low profile 2.0 x 1.7 x 0.5 mm, 12 pins UQFN package.

### Features

- High Bandwidth of 1.8 GHz
- $V_{CC}$  Operating Range from 2.7 V to 5.5 V
- $V_{IS}$  Signal from 0 V to 3.7 V for Data Transfer
- $V_{IS}$  Signal from -2 V to 2 V for Stereo Headphone Connection
- Audio Shunt resistor for Pop & Click Noise Reduction
- $V_{IO}$  Control Pins Compatible to 1.8V Interfaces
- Low Power Consumption of 23  $\mu$ A
- Small UQFN 2.0 x 1.7 x 0.5 mm Package
- These Devices are Pb-Free and are RoHS Compliant

### Typical Applications

- USB 2.0 / 3.0 Micro-B Applications
- USB to HDMI Video Interfaces via MHL
- Features Phones and Smart Phones
- Digital Cameras
- Handset Media Players

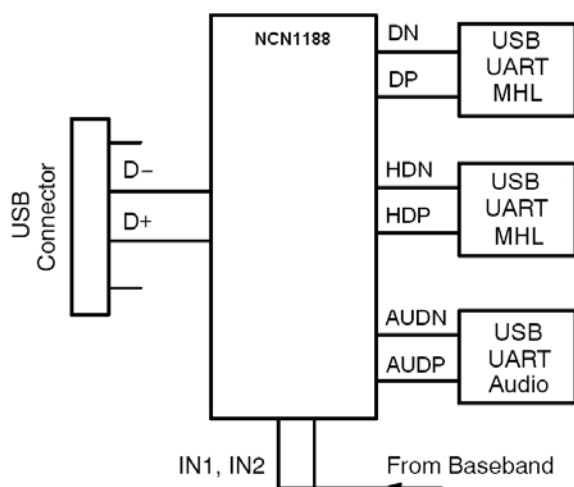


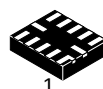
Figure 1. NCN1188 Typical Application Schematic



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### MARKING DIAGRAM

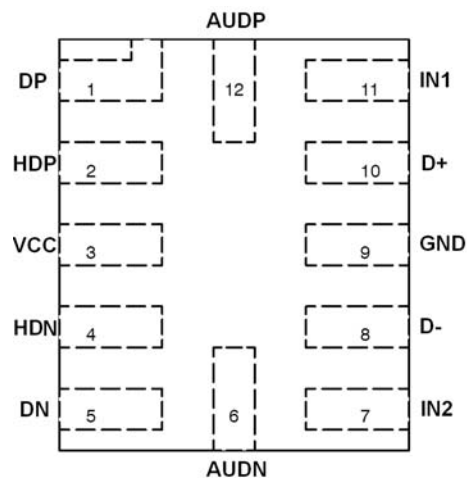


UQFN12  
MU SUFFIX  
CASE 523AE



AG = Specific Device Code  
M = Date Code  
■ = Pb-Free Package

### PIN ASSIGNMENTS



(Top View)

### ORDERING INFORMATION

| Device       | Package          | Shipping†          |
|--------------|------------------|--------------------|
| NCN1188MUTAG | UQFN12 (Pb-Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCN1188

NCN1188 TRUTH TABLE

| Function    | IN1 | IN2 | Shunt   |
|-------------|-----|-----|---------|
| Hi-Z        | 0   | 0   | Enable  |
| DN / DP     | 0   | 1   | Enable  |
| AUDN / AUDP | 1   | 0   | Disable |
| HDN / HDP   | 1   | 1   | Enable  |

SIMPLIFIED BLOCK DIAGRAM

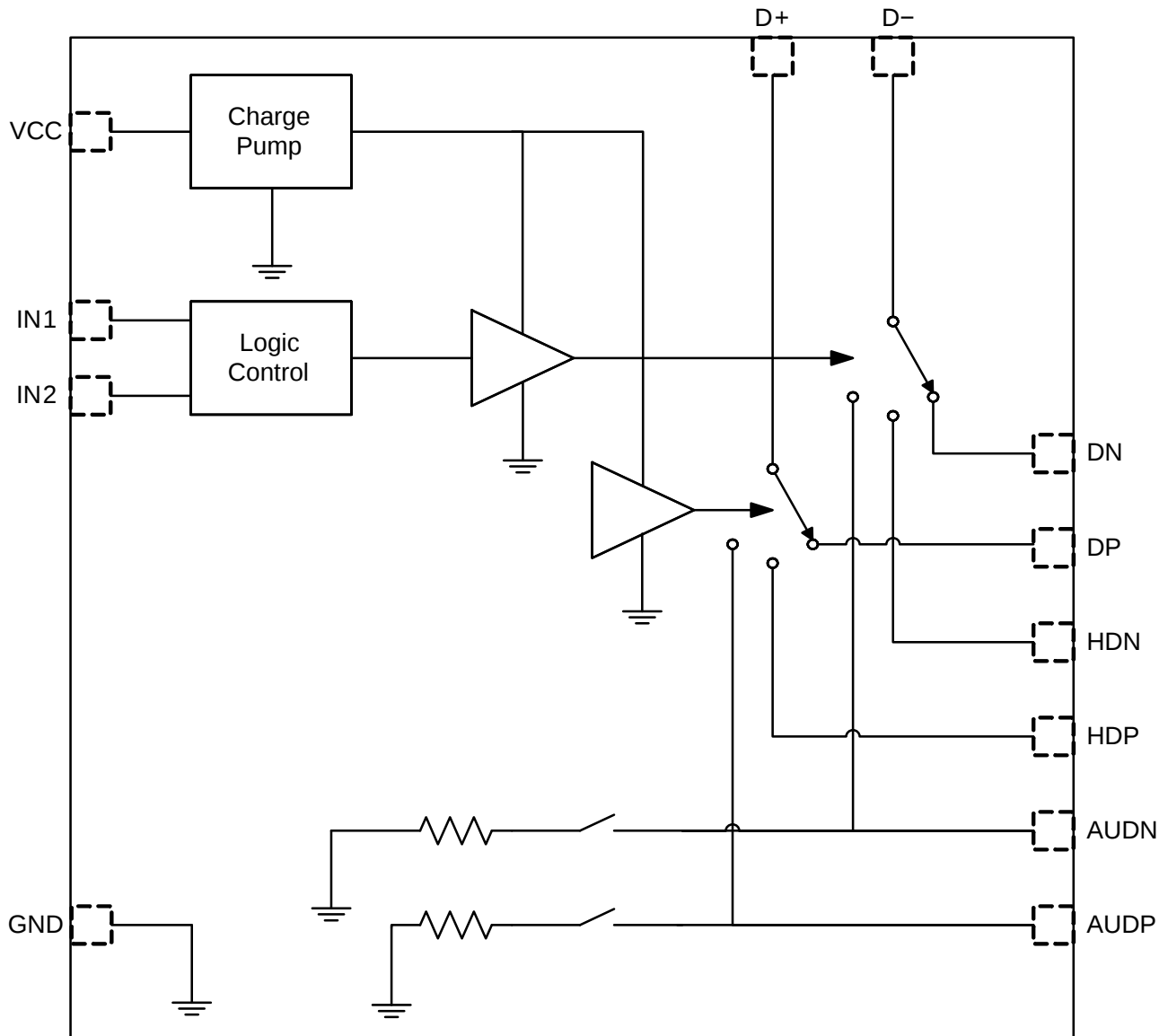


Figure 2. Simplified Block Diagram

# NCN1188

## PIN DIAGRAM

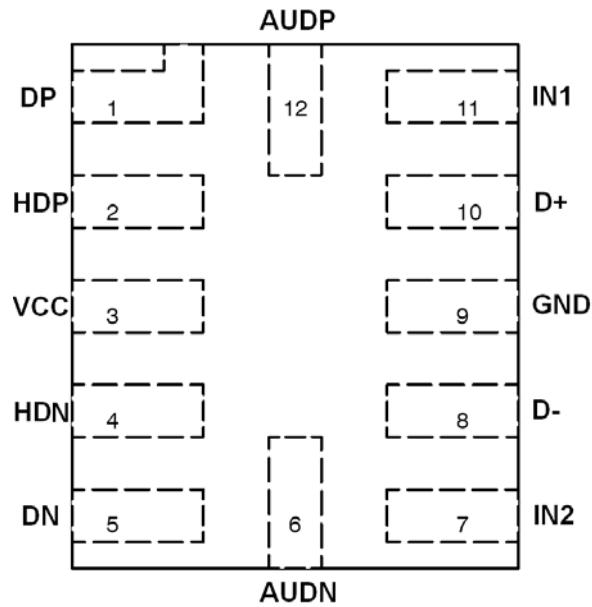


Figure 3. Pin Assignments (Top View)

## PIN DESCRIPTION

| Name | Pin | Description                                                                                                                                                                                                                  |
|------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DP   | 1   | <b>USB Positive Path.</b> If active, this pin is connected to D+ pin.                                                                                                                                                        |
| HDP  | 2   | <b>HD Positive Path.</b> If active, this pin is connected to D+ pin.                                                                                                                                                         |
| VCC  | 3   | <b>Analog Supply.</b> This pin is the analog and digital supply of the device. A 100 nF ceramic capacitor or larger must bypass this input to the ground. This capacitor should be placed as close a possible to this input. |
| HDN  | 4   | <b>HD Negative Path.</b> If active, this pin is connected to D- pin.                                                                                                                                                         |
| DN   | 5   | <b>USB Negative Path.</b> If active, this pin is connected to D- pin.                                                                                                                                                        |
| AUDN | 6   | <b>Audio N.</b> If active, this pin is connected to D- pin.                                                                                                                                                                  |
| IN2  | 7   | <b>Input Selection 2.</b> Do not float this pin.                                                                                                                                                                             |
| D-   | 8   | <b>Negative data line.</b> Must be connected to the D- pin of USB receptacle.                                                                                                                                                |
| GND  | 9   | <b>Ground Reference.</b> Must be connected to the system ground.                                                                                                                                                             |
| D+   | 10  | <b>Positive data line.</b> Must be connected to the D+ pin of USB receptacle.                                                                                                                                                |
| IN1  | 11  | <b>Input Selection 1.</b> Do not float this pin.                                                                                                                                                                             |
| AUDP | 12  | <b>Audio P.</b> If active, this pin is connected to D+ pin.                                                                                                                                                                  |

**MAXIMUM RATINGS** (Note 1)

| Rating                                                       | Symbol              | Value                         | Unit |
|--------------------------------------------------------------|---------------------|-------------------------------|------|
| Maximum Supply Voltage Range on VCC pin                      | V <sub>CCMAX</sub>  | – 0.3 to 6.0                  | V    |
| Maximum Analog Signal Voltage Range on DN, DP, HDN, HDP pins | V <sub>ISMAX</sub>  | – 0.3 to 5.5                  | V    |
| Maximum Analog Signal Voltage Range on D+, D– pins           | V <sub>COMMAX</sub> | – 2.5 to 5.5                  | V    |
| Maximum Analog Signal Voltage Range on IN1, IN2 pins         | V <sub>IOMAX</sub>  | –0.3 to V <sub>CC</sub> + 0.3 | V    |
| Maximum Analog Signal Voltage Range on AUDN, AUDP pins       | V <sub>AUDMAX</sub> | –2.5 to V <sub>CC</sub> + 0.3 | V    |
| Latch up Current (Note 2)                                    | I <sub>LU</sub>     | ±100                          | mA   |
| Human Body Model (HBM) ESD Rating (Note 3)                   | ESD HBM             | 4000                          | V    |
| Machine Model (MM) ESD Rating (Note 3)                       | ESD MM              | 100                           | V    |
| Maximum Junction Temperature                                 | T <sub>JMAX</sub>   | +150                          | °C   |
| Storage Temperature Range                                    | T <sub>STG</sub>    | –55 to + 150                  | °C   |
| Moisture Sensitivity (Note 4)                                | MSL                 | Level 1                       |      |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T<sub>A</sub> = 25°C.
- Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
- This device series contains ESD protection and passes the following tests:  
Human Body Model (HBM) ±4.0 kV per JEDEC standard: JESD22–A114 for all pins.  
Machine Model (MM) ±100 V per JEDEC standard: JESD22–A115 for all pins.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J–STD–020A.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

**VOLTAGE RANGES**

|                 |                                      |                          |           |        |            |   |
|-----------------|--------------------------------------|--------------------------|-----------|--------|------------|---|
| V <sub>CC</sub> | VCC pin operating range              |                          | 2.7       | –      | 5.5        | V |
| V <sub>IS</sub> | Analog Signal Voltage range (Note 5) | High Speed Data<br>Audio | 0<br>–2.0 | –<br>– | 3.7<br>2.0 | V |

**TEMPERATURE RANGES**

|                |                                |  |     |   |     |    |
|----------------|--------------------------------|--|-----|---|-----|----|
| T <sub>A</sub> | Operating Ambient Temperature  |  | –40 | – | 85  | °C |
| T <sub>J</sub> | Operating Junction Temperature |  | –40 | – | 125 | °C |

- If the audio channel is not in use, it is recommended that no signals are applied on the audio inputs AUDN and AUDP

**ELECTRICAL CHARACTERISTICS**

Min and Max limits apply for T<sub>A</sub> from –40°C to +85°C (unless otherwise noted). Typical values are referenced to V<sub>CC</sub> = 3.6 V, T<sub>A</sub> = +25°C (unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

**CURRENT CONSUMPTION**

|                 |                        |                                              |   |    |    |    |
|-----------------|------------------------|----------------------------------------------|---|----|----|----|
| I <sub>CC</sub> | Product Supply Current | V <sub>CC</sub> = 4.2 V, I <sub>IS</sub> = 0 | – | 23 | 35 | μA |
|-----------------|------------------------|----------------------------------------------|---|----|----|----|

**CONTROL LOGIC (IN1, IN2 pins)**

|                   |                              |                                                                               |                   |             |                   |    |
|-------------------|------------------------------|-------------------------------------------------------------------------------|-------------------|-------------|-------------------|----|
| V <sub>IL</sub>   | Low Voltage Input Threshold  | V <sub>CC</sub> = 2.7 V<br>V <sub>CC</sub> = 3.6 V<br>V <sub>CC</sub> = 4.2 V | –<br>–<br>–       | –<br>–<br>– | 0.4<br>0.4<br>0.4 | V  |
| V <sub>IH</sub>   | High Voltage Input Threshold | V <sub>CC</sub> = 2.7 V<br>V <sub>CC</sub> = 3.6 V<br>V <sub>CC</sub> = 4.2 V | 1.3<br>1.4<br>1.5 | –<br>–<br>– | –<br>–<br>–       | V  |
| V <sub>IHYS</sub> | Voltage Input Hysteresis     |                                                                               | –                 | 250         | –                 | mV |
| I <sub>IN</sub>   | Leakage Current              |                                                                               | –                 | –           | ±100              | nA |

# **ELECTRICAL CHARACTERISTICS**

Min and Max limits apply for  $T_A$  from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (unless otherwise noted). Typical values are referenced to  $V_{CC} = 3.6\text{ V}$ ,  $T_A = +25^{\circ}\text{C}$  (unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

## **DATA SWITCHES DC CHARACTERISTICS**

|               |                        |                                                                                |   |      |           |          |
|---------------|------------------------|--------------------------------------------------------------------------------|---|------|-----------|----------|
| $R_{ON}$      | On Resistance          | $V_{CC} = 3.0\text{ V}$<br>$V_{IS}$ from 0 V to 2.4 V, $I_{IS} = 15\text{ mA}$ | – | 5    | 7.5       | $\Omega$ |
| $R_{ON\_MAT}$ | On Resistance Matching | $V_{CC} = 3.0\text{ V}$<br>$V_{IS}$ from 0 V to 1.7 V, $I_{IS} = 15\text{ mA}$ | – | 0.09 | –         | $\Omega$ |
| $R_{ON\_FLT}$ | On Resistance Flatness | $V_{CC} = 3.0\text{ V}$<br>$V_{IS}$ from 0 V to 1.7 V, $I_{IS} = 15\text{ mA}$ | – | 0.06 | –         | $\Omega$ |
| $I_{SW\_OFF}$ | Off State Leakage      | $V_{CC} = 3.6\text{ V}$<br>$V_{IS}$ From 0 V to 3.6 V                          | – | –    | 200       | nA       |
| $I_{SW\_ON}$  | On State Leakage       | $V_{CC} = 3.6\text{ V}$<br>$V_{IS}$ From 0 V to 3.6 V                          | – | –    | $\pm 200$ | nA       |

## **DATA SWITCHES AC CHARACTERISTICS**

|             |                               |                                                                        |   |                      |   |    |
|-------------|-------------------------------|------------------------------------------------------------------------|---|----------------------|---|----|
| $C_{ON}$    | Equivalent On Capacitance     | Switch ON, $f = 1\text{ MHz}$                                          | – | 4.5                  | – | pF |
| $C_{OFF}$   | Equivalent Off Capacitance    | Switch OFF, $f = 1\text{ MHz}$                                         | – | 3                    | – | pF |
| $D_{IL}$    | Differential Insertion Loss   | $f = 10\text{ MHz}$<br>$f = 800\text{ MHz}$<br>$f = 1.1\text{ GHz}$    | – | –0.5<br>–1.8<br>–2.1 | – | dB |
| $D_{ISO}$   | Differential Off Isolation    | $f = 10\text{ MHz}$<br>$f = 800\text{ MHz}$<br>$f = 1.1\text{ GHz}$    | – | –53<br>–19<br>–18    | – | dB |
| $D_{CTK}$   | Differential Crosstalk        | $f = 10\text{ MHz}$<br>$f = 800\text{ MHz}$<br>$f = 1.1\text{ GHz}$    | – | –55<br>–20<br>–18    | – | dB |
| $PSRR_{SW}$ | Power Supply Ripple Rejection | From $V_{CC}$ onto D+ / D–<br>$f = 217\text{ Hz}$ , $R_L = 50\ \Omega$ | – | 90                   | – | dB |

## **AUDIO SWITCHES DC CHARACTERISTICS**

|               |                        |                                                                                                      |   |      |     |          |
|---------------|------------------------|------------------------------------------------------------------------------------------------------|---|------|-----|----------|
| $R_{ON}$      | On Resistance          | $V_{CC} = 3.0\text{ V}$<br>$V_{IS}$ from $-2.0\text{ V}$ to $2.0\text{ V}$ , $I_{IS} = 50\text{ mA}$ | – | 3    | 5   | $\Omega$ |
| $R_{ON\_MAT}$ | On Resistance Matching | $V_{CC} = 3.0\text{ V}$<br>$V_{IS}$ from $-2.0\text{ V}$ to $2.0\text{ V}$ , $I_{IS} = 50\text{ mA}$ | – | 0.04 | –   | $\Omega$ |
| $R_{ON\_FLT}$ | On Resistance Flatness | $V_{CC} = 3.0\text{ V}$<br>$V_{IS}$ from $-2.0\text{ V}$ to $2.0\text{ V}$ , $I_{IS} = 50\text{ mA}$ | – | 0.02 | –   | $\Omega$ |
| $R_{SH}$      | Shunt Resistance       | $V_{CC} = 3.6\text{ V}$                                                                              | – | 125  | 200 | $\Omega$ |

## **AUDIO SWITCHES AC CHARACTERISTICS**

|              |                               |                                                                                              |   |      |   |    |
|--------------|-------------------------------|----------------------------------------------------------------------------------------------|---|------|---|----|
| $THD_{AUD}$  | Audio THD                     | From 20 Hz to 20 kHz<br>$V_{IS} = 0.4\text{ V}_{RMS}$ , DC bias = 0V,<br>Load = $16\ \Omega$ | – | 0.01 | – | %  |
| $PSRR_{AUD}$ | Power Supply Ripple Rejection | From $V_{CC}$ onto AUDN / AUDP<br>$f = 217\text{ Hz}$ , $R_L = 16\ \Omega$                   | – | 90   | – | dB |

**ELECTRICAL CHARACTERISTICS**

Min and Max limits apply for  $T_A$  from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  (unless otherwise noted). Typical values are referenced to  $V_{CC} = 3.6\text{ V}$ ,  $T_A = +25^{\circ}\text{C}$  (unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

**SWITCHES TIMING CHARACTERISTICS**

|             |                         |                                                                                    |   |      |   |               |
|-------------|-------------------------|------------------------------------------------------------------------------------|---|------|---|---------------|
| $t_{PD}$    | Propagation Delay       | (Notes 6 and 7)                                                                    | – | 0.25 | – | ns            |
| $t_{ON}$    | Turn On Time            | $V_{IS} = 1\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 7\text{ pF}$<br>(fixture only) | – | 2.2  | – | $\mu\text{s}$ |
| $t_{OFF}$   | Turn Off Time           | $V_{IS} = 1\text{ V}$ , $R_L = 50\ \Omega$ , $C_L = 7\text{ pF}$<br>(fixture only) | – | 67   | – | ns            |
| $t_{b-b}$   | Bit-to-Bit Skew         | Within the same differential channel                                               | – | 5    | – | ps            |
| $t_{ch-ch}$ | Channel-to-Channel Skew | Maximum skew between all channels                                                  | – | 15   | – | ps            |

6. Specification guarantee by design

7. No other delays than the RC network formed by the load resistance and the load capacitance of the switch are added on the bus. For a 10 pF load, this delay is 5 ns which is much smaller than rise and fall time of typical driving systems. Propagation delays on the bus are determined by the driving circuit on the driving side and its interactions with the load of the driven side.

**TABLE OF GRAPHS**

| Symbol                        | Parameter                                        |               | Figure |
|-------------------------------|--------------------------------------------------|---------------|--------|
| $1080p_{EYE}$                 | MHL Video Eye Diagram at 3 Gbps (1080p)          |               | 4      |
| $720p_{EYE}$<br>$1080i_{EYE}$ | MHL Video Eye Diagram at 2.25 Gbps (720p, 1080i) |               | 5      |
| $USB2.0_{EYE}$                | USB 2.0 High Speed 480 Mbps Eye Diagram          |               | 6, 7   |
| $USB1.1_{EYE}$                | USB 1.1 Full Speed 12 Mbps Eye Diagram           |               | 8, 9   |
| $USB1.0_{EYE}$                | USB 1.0 Low Speed 1.5 Mbps Eye Diagram           |               | 10, 11 |
| $I_{CC}$                      | Product Supply Current                           | vs. $V_{CC}$  | 12     |
| $R_{ON}$                      | Data Path On Resistance                          | vs. $V_{IS}$  | 13     |
| $D_{IL}$                      | Data Switch Differential Insertion Loss          | vs. Frequency | 14     |
| $D_{ISO}$                     | Data Switch Differential Off Isolation           | vs. Frequency | 15     |
| $D_{CTK}$                     | Data Switch Differential Crosstalk               | vs. Frequency | 16     |
| $R_{ON}$                      | Audio Path On Resistance                         | vs. $V_{IS}$  | 17     |
| $THD_{AUD}$                   | Audio THD                                        | vs. Frequency | 18     |

TYPICAL OPERATING CHARACTERISTICS

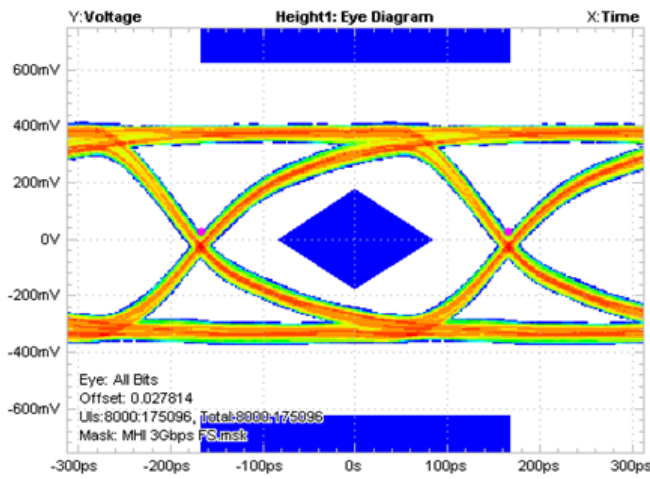


Figure 4. MHL Video Eye Diagram at 3 Gbps (1080p)

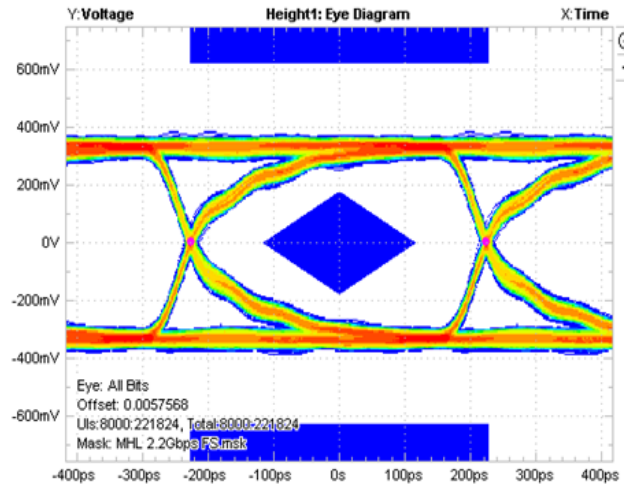


Figure 5. MHL Video Eye Diagram at 2.25 Gbps (720p, 1080i)

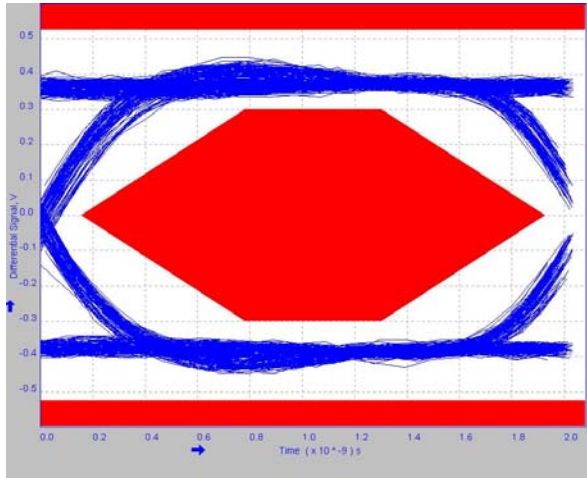


Figure 6. USB 2.0 High Speed Eye Diagram

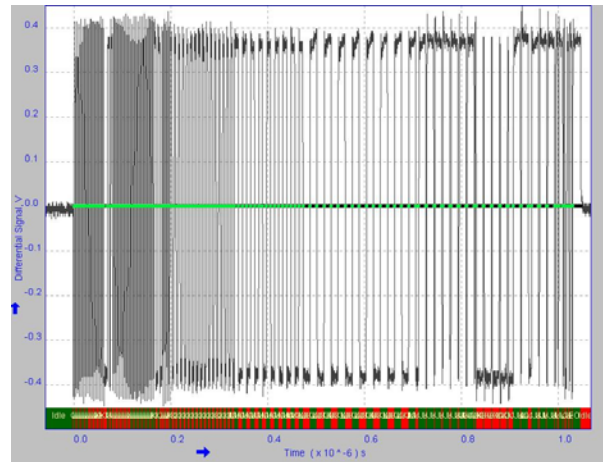


Figure 7. USB 2.0 High Speed Pattern

TYPICAL OPERATING CHARACTERISTICS

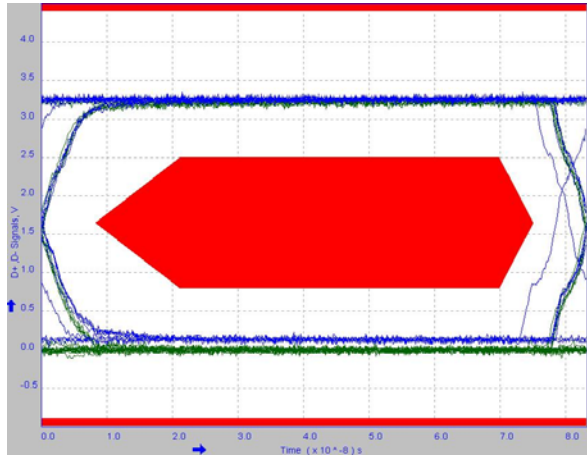


Figure 8. USB 1.1 Full Speed Eye Diagram

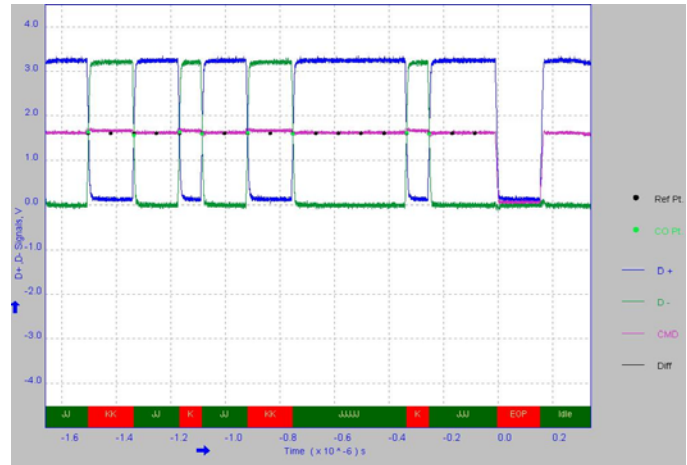


Figure 9. USB 1.0 Full Speed Pattern

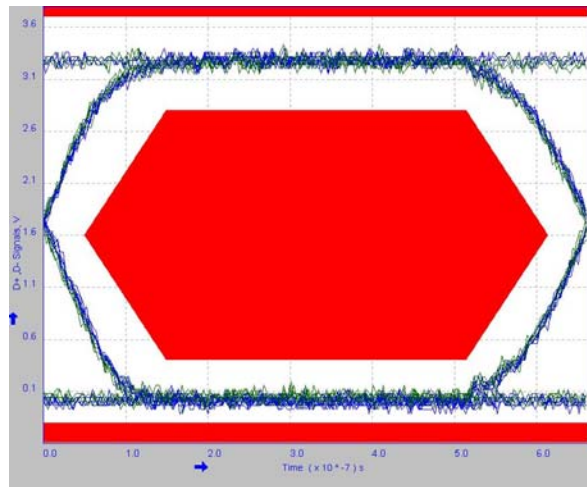


Figure 10. USB 1.0 Low Speed Eye Diagram

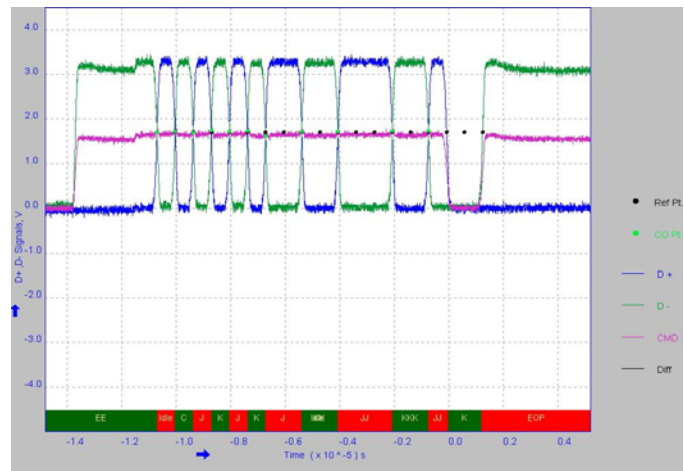


Figure 11. USB 1.0 Low Speed Pattern

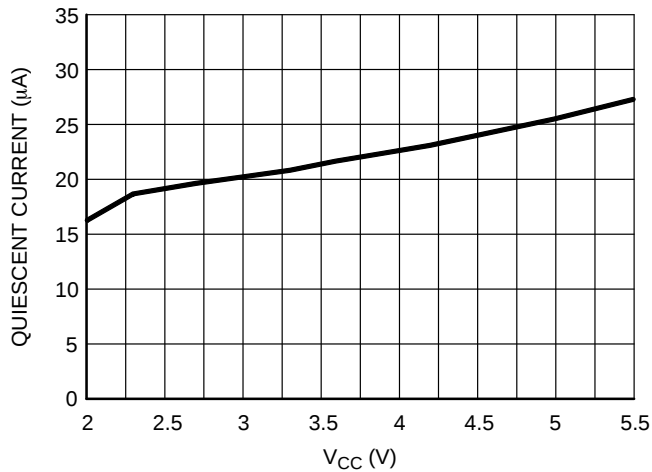


Figure 12. Product Supply Current

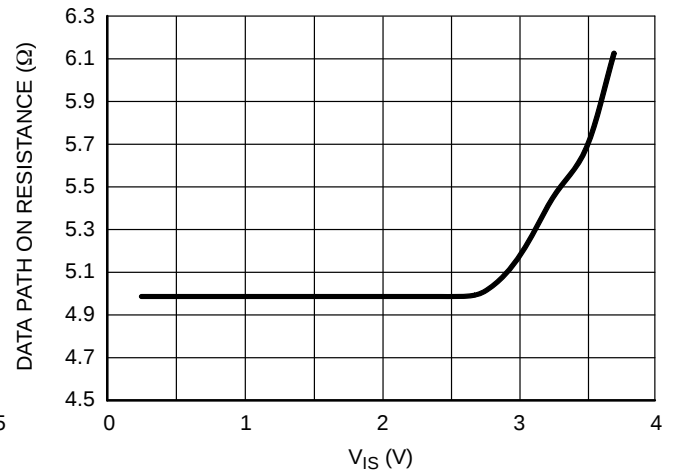


Figure 13. Data Path On Resistance

TYPICAL OPERATING CHARACTERISTICS

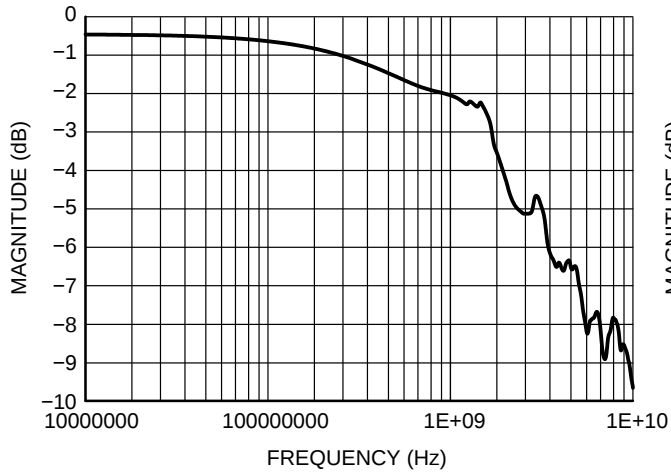


Figure 14. Data Switch Differential Insertion Loss

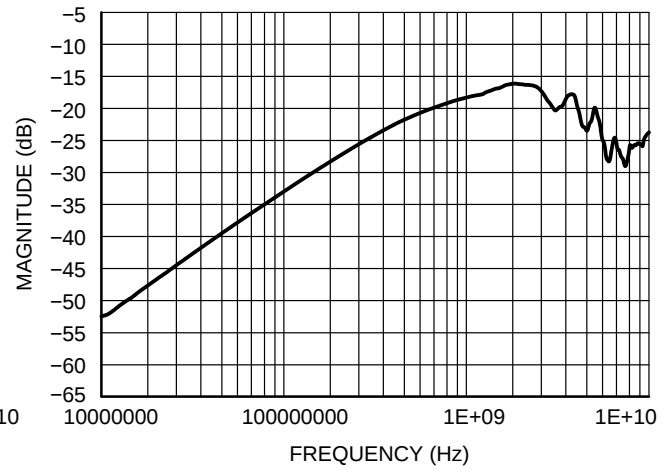


Figure 15. Data Switch Differential Off Isolation

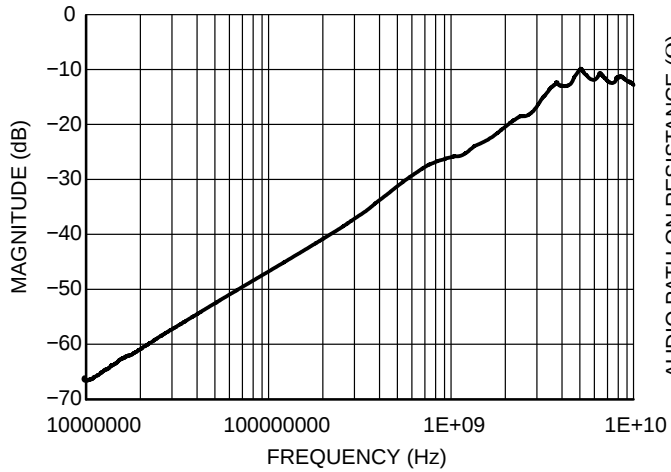


Figure 16. Data Switch Differential Crosstalk

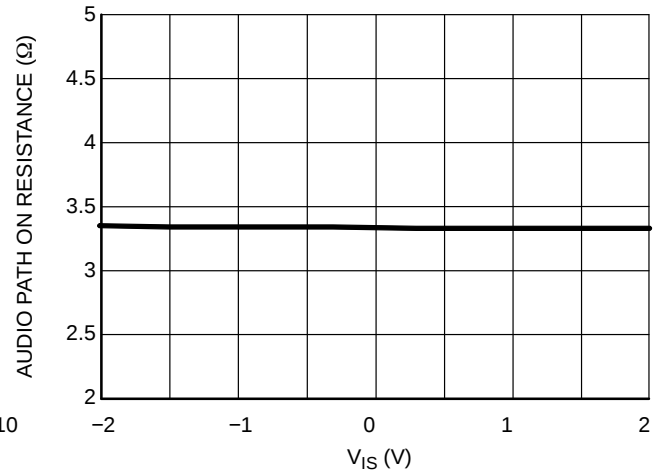


Figure 17. Audio Path On Resistance

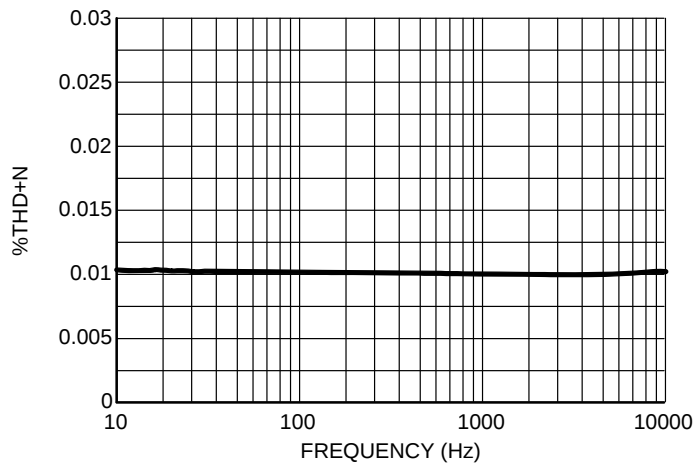
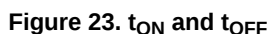


Figure 18. Audio THD

## 10



## DETAILED APPLICATION

The NCN1188 voltage range and high bandwidth performance permits switching between audio, video and data signals on a portable device. It allows D+ and D- data pins of a single USB connector to be used for many different functions as pictured by Figure 1:

- USB 2.0 data transfer with backward compatibility to USB 1.1 and USB 1.0
- MHL high definition video transfer up to 3 Gbps for 1080p resolutions
- Audio headset with negative voltage capability to connect true ground audio amplifier
- UART to address programming and testing in factory
- Any other analog or digital data sources within the recommended operating conditions

Figures 26 and 27 detail two design examples with different switching combinations using NCN1188.

In the first example shown in Figure 26, the device is directly supplied from a single Li-Ion battery, typically

from 3.0 V to 4.2 V. The NCN1188 switch connects a 5-pin micro-USB connector to a Communication Processor, an MHL Application Processor, and the Audio Management IC headphone amplifier. Each function is active pending on power management IC accessory detection to control IN1 and IN2. This decision is usually made on the D-, D+, and ID pins to detect and differentiate accessory types such as USB cable, USB to HDMI MHL cable and micro-USB stereo headset.

For solutions related to portable devices accessory detection, contact your ON Semiconductor Field Applications Engineer.

The USB 3.0 Micro-B receptacle may be considered a combination of the USB 2.0 Micro-B interface and USB 3.0 SuperSpeed contacts and maintains backward compatibility with USB 2.0 Micro-B plugs. As a consequence, the NCN1188's USB 2.0 capability is fully compatible to the USB 3.0 Micro-B receptacle, as well as USB 2.0 accessories.

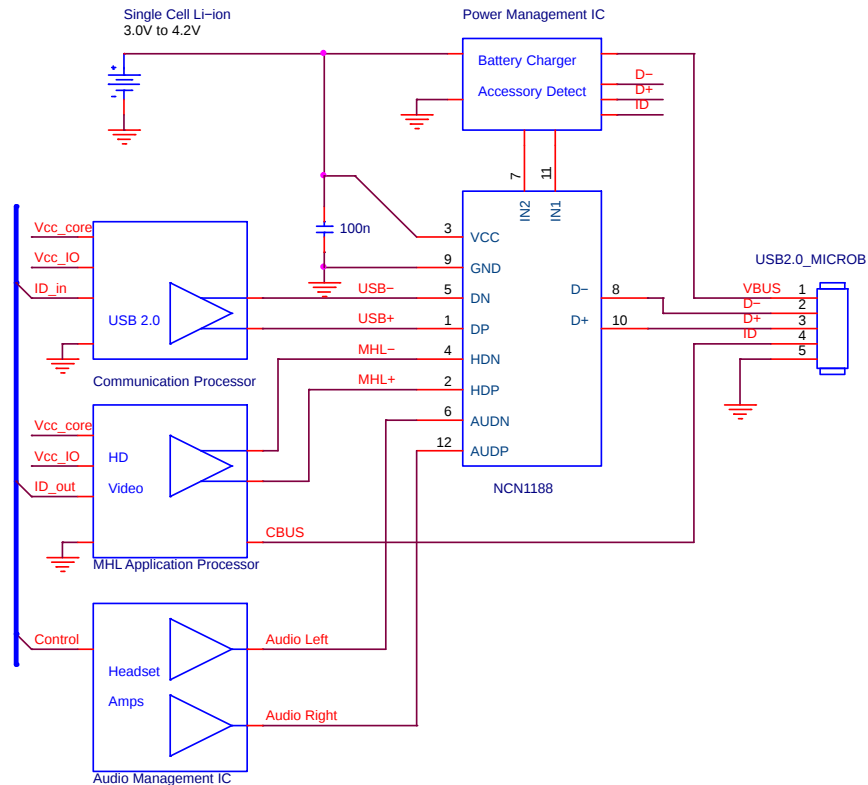
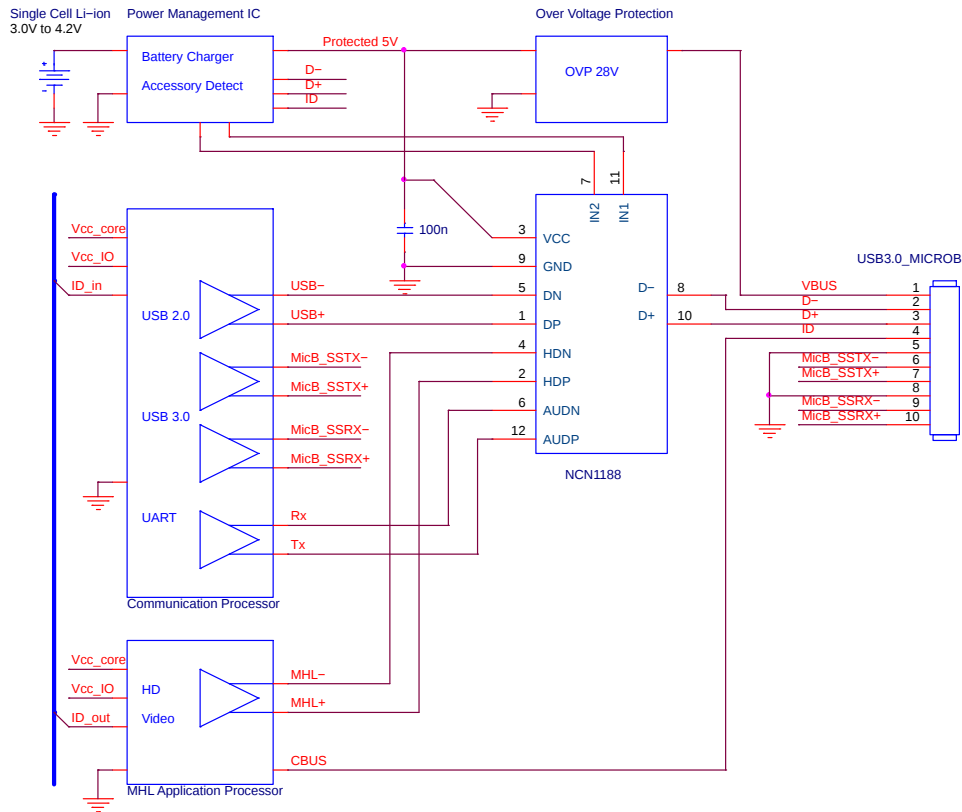


Figure 26. Schematic Example for USB 2.0, MHL, and Audio Combination; NCN1188 being supplied from battery

## NCN1188



**Figure 27. Schematic Example for USB 2.0, MHL, and UART Combination; NCN1188 Being Supplied by Protected VBUS 5 V**

In this second design proposal, as NCN1188 must be active only when VBUS accessories are connected (USB cable, UART cable and MHL cable), the device is supplied from a protected VBUS 5 V. This design arrangement limits the system's overall quiescent current and saves battery life. Figure 27 also pictures NCN1188 around a USB 3.0 Micro-B topology: USB 2.0, UART and MHL Video pairs remain multiplexed with D- and D+ while the two USB 3.0 differential pairs are directly connected to the main communication processor.

Pull-down resistors of 1 MΩ down to 100 kΩ can optionally be added on the D- and D+ I/Os for preventing eventual floating voltage situation on the NCN1188. This is not systematically necessary and has to be considered in regards to the application.

The flexibility of the NCN1188 offers many extra application and design combinations.

**PCB DESIGN PROCEDURE**

Implementing a high speed device requires careful design of signal traces to preserve signal integrity. The following electrical layout guidelines are basic rules to follow when designing boards capable of high speed transmission.

- The bypass capacitor must be placed as close as possible to the  $V_{CC}$  input pin for noise immunity.
- The PCB should be designed to comply with the characteristic impedance requirements of MHL and USB.
- Make the signal traces as short as possible to reduce losses through the PCB. Furthermore, all corresponding  $D+$  /  $D-$  line segment pairs should be the same length.
- The use of turns or bends to route these signals should be avoided when possible. Use  $45^\circ$  bends instead of  $90^\circ$  bends where bends are needed. The use of vias to route these signals should be avoided when possible.

# MECHANICAL CASE OUTLINE

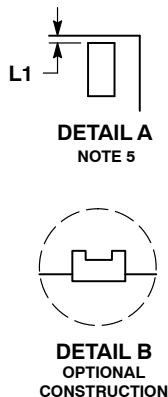
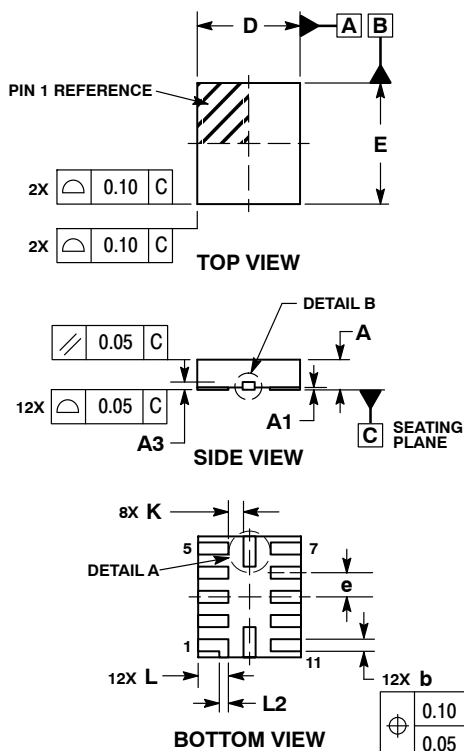
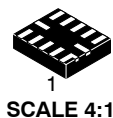
## PACKAGE DIMENSIONS

ON Semiconductor®

ON

UQFN12 1.7x2.0, 0.4P  
CASE 523AE-01  
ISSUE A

DATE 11 JUN 2007

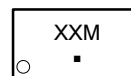


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 0.45        | 0.55 |
| A1  | 0.00        | 0.05 |
| A3  | 0.127 REF   |      |
| b   | 0.15        | 0.25 |
| D   | 1.70 BSC    |      |
| E   | 2.00 BSC    |      |
| e   | 0.40 BSC    |      |
| K   | 0.20        | ---- |
| L   | 0.45        | 0.55 |
| L1  | 0.00        | 0.03 |
| L2  | 0.15 REF    |      |

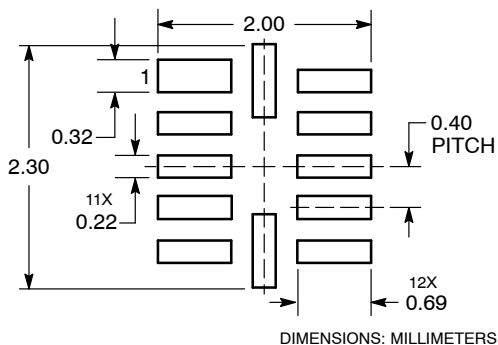
### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### MOUNTING FOOTPRINT SOLDERMASK DEFINED



|                         |                               |                                                                                                                                                                                  |
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