16-Ch/Dual 8-Ch High-Performance CMOS Analog Multiplexers

DESCRIPTION

The DG406 is a 16 channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. The DG407 selects one of eight differential inputs to a common differential output. Break-before-make switching action protects against momentary shorting of inputs.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

Applications for the DG406, DG407 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44 V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V, allowing operation with ± 20 V supplies. Additionally single (12 V) supply operation is allowed. An epitaxial layer prevents latchup.

For applications information please request documents 70601 and 70604.

FEATURES

- Low on-resistance - $R_{DS(on)}$: 50 Ω
- Low charge injection - Q: 15 pC
- Fast transition time - t_{TRANS}: 200 ns
- Low power: 0.2 mW
- Single supply capability
- 44 V supply max. rating
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free Available
RoHS* Available
HALOGEN FREE

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

BENEFITS

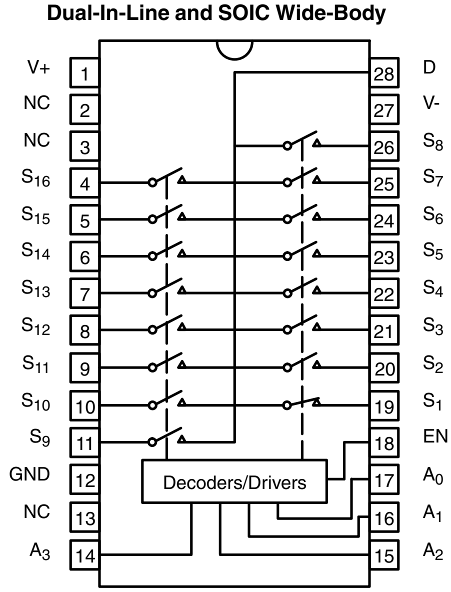
- Higher accuracy
- Reduced glitching
- Improved data throughput
- Reduced power consumption
- Increased ruggedness
- Wide supply ranges: ± 5 V to ± 20 V

APPLICATIONS

- Data acquisition systems
- Audio signal routing
- Medical instrumentation
- ATE systems
- Battery powered systems
- High-rel systems
- Single supply systems

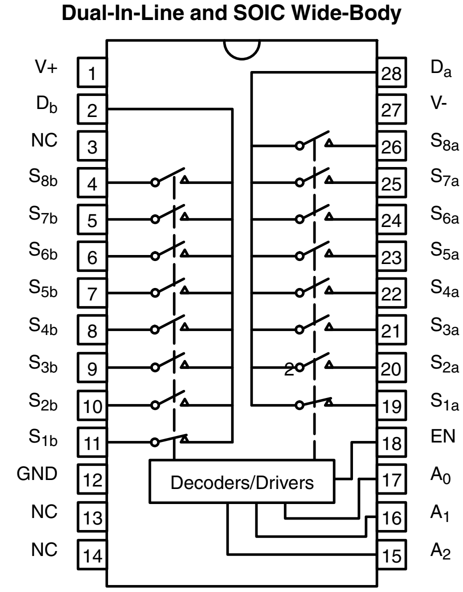
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406 Dual-In-Line and SOIC Wide-Body



Top View

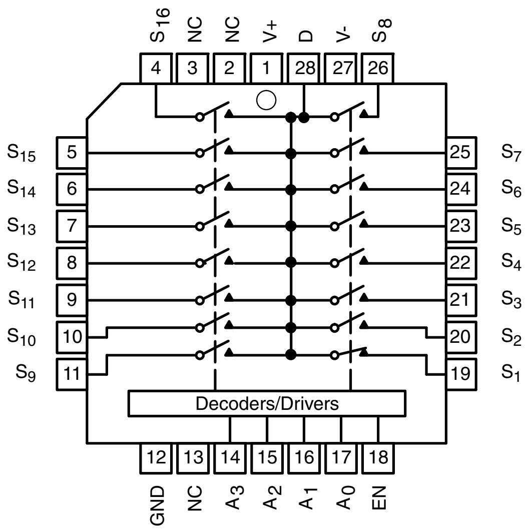
DG407 Dual-In-Line and SOIC Wide-Body



Top View

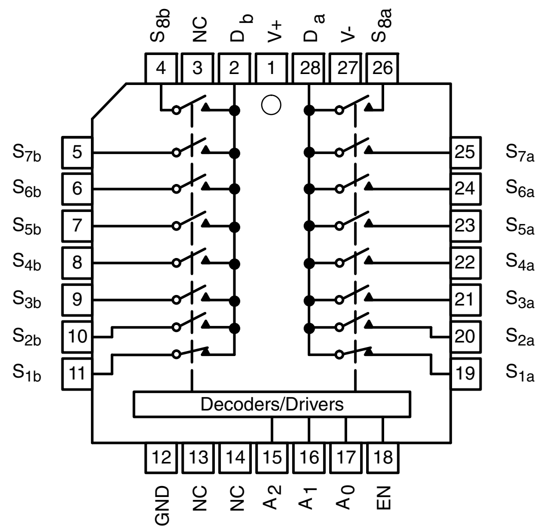
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG406 PLCC and LCC



Top View

DG407 PLCC and LCC



Top View

TRUTH TABLE (DG406)

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

TRUTH TABLE (DG407)

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Notes

- Logic “0” = $V_{AL} \leq 0.8$ V
- Logic “1” = $V_{AH} \geq 2.4$ V
- X = do not care

ORDERING INFORMATION (DG406)

TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	28-pin PLCC	DG406DN-T1-E3
	28-pin widebody SOIC	DG406DW-E3, DG406DW-T1-E3

ORDERING INFORMATION (DG407)

TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	28-pin PLCC	DG407DN-T1-E3
	28-pin widebody SOIC	DG407DW-E3, DG407DW-T1-E3

Note

- -T1 indicates tape and reel, -E3 indicates lead (Pb)-free and RoHS-compliant

ABSOLUTE MAXIMUM RATINGS			
PARAMETER		LIMIT	UNIT
Voltages referenced to V-	V+ to V - [f]	44	V
	GND to V-	-25	
Digital inputs [a], V_S, V_D		(V-) - 2 to (V+) + 2 V or 20 mA, whichever occurs first	
Current (any terminal)		30	mA
Peak current, S or D (pulsed at 1 ms, 10 % duty cycle max.)		100	
Storage temperature	(AK, AZ suffix)	-65 to +150	°C
	(DJ, DN suffix)	-65 to +125	
Power dissipation (package)[b]	28-pin plastic DIP [b]	625	mW
	28-pin plastic PLCC [c]	450	
	28-pin widebody SOIC	450	

Notes

a. Signals on SX, DX or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads soldered or welded to PC board
c. Derate 6 mW/°C above 75 °C
d. Derate 12 mW/°C above 75 °C
e. Derate 13.5 mW/°C above 75 °C
f. Also applies when V- = GND

SPECIFICATIONS [a]								
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 15 V, V- = -15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V [f]**		**TEMP. [b]**	**TYP. [c]**	**D SUFFIX -40 °C TO +85 °C MIN. [d]**	**MAX. [d]**	**UNIT**
Analog Switch								
Analog signal range [e]	V_{ANALOG}			Full	-	-15	15	V
Drain-source on-resistance	$R_{DS(on)}$	V_D = ± 10 V, I_S = -10 mA sequence each switch on		Room	50	-	100	Ω
				Full	50	-	125	
$R_{DS(on)}$ matching between channels [g]	$\Delta R_{DS(on)}$	V_D = ± 10 V		Room	5	-	-	%
Source off leakage current	$I_{S(off)}$	V_{EN} = 0 V, V_D = ± 10 V, V_S = ± 10 V		Room	0.01	-0.5	0.5	nA
				Full	0.01	-5	5	
Drain off leakage current	$I_{D(off)}$		DG406	Room	0.04	-1	1	
				Full	0.04	-40	40	
			DG407	Room	0.04	-1	1	
				Full	0.04	-20	20	
Drain on leakage current	$I_{D(on)}$	V_S = V_D = ± 10 sequence each switch on	DG406	Room	0.04	-1	1	
				Full	0.04	-40	40	
			DG407	Room	0.04	-1	1	
				Full	0.04	-20	20	
Digital Control								
Logic high input voltage	V_{INH}			Full	-	2.4	-	V
Logic low input voltage	V_{INL}			Full	-	-	0.8	
Logic high input current	I_{AH}	V_A = 2.4 V, 15 V		Full	-	-1	1	µA
Logic low input current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full	-	-1	1	
Logic input capacitance	C_{in}	f = 1 MHz		Room	7	-	-	pF
Dynamic Characteristics								
Transition time	t_{TRANS}	see figure 2		Room	200	-	350	ns
				Full	-	-	450	
Break-before-make interval	t_{OPEN}	see figure 4		Room	50	25	-	
				Full	-	10	-	
Enable turn-on time	$t_{ON(EN)}$	see figure 3		Room	150	-	200	
				Full	-	-	400	
Enable turn-off time	$t_{OFF(EN)}$			Room	70	-	150	
				Full	-	-	300	
Charge injection	Q	V_S = 0 V, C_L = 1 nF, R_S = 0 Ω		Room	15	-	-	pC
Off isolation [h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ, f = 100 kHz		Room	-69	-	-	dB
Source off capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	8	-	-	pF
Drain off capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V, f = 1 MHz		Room	130	-	-	
			DG407	Room	65	-	-	
Drain on capacitance	$C_{D(on)}$		DG406	Room	140	-	-	
			DG407	Room	70	-	-	
Power Supplies								
Positive supply current	I+	V_{EN} = V_A = 0 or 5 V		Room	13	-	30	µA
				Full	-	-	75	
Negative supply current	I-			Room	-0.01	-1	-	
				Full	-	-10	-	
Positive supply current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room	50	-	500	
				Full		-	700	
Negative supply current	I-			Room	-0.01	-20	-	
				Full	-0.01	-20	-	

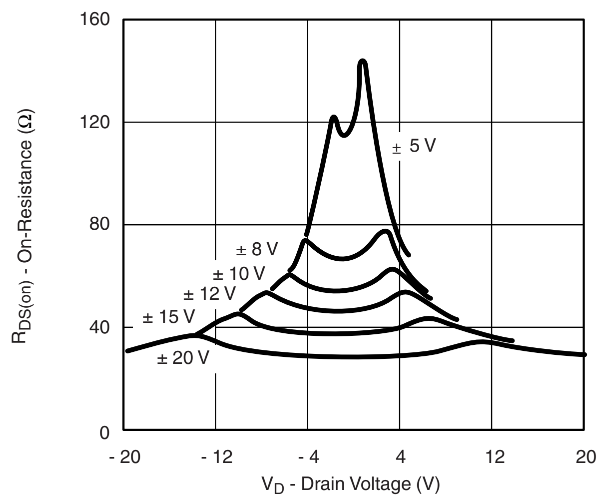
SPECIFICATIONS [a] (for single supply)								
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED $V+ = 12$ V, $V- = 0$ V $V_{AL} = 0.8$ V, $V_{AH} = 2.4$ V [f]		TEMP. [b]	TYP. [c]	D SUFFIX -40 °C TO +85 °C		UNIT
						MIN. [d]	MAX. [d]	
Analog Switch								
Analog signal range [e]	V_{ANALOG}			Full	-	0	12	V
Drain-source on-resistance	$R_{DS(on)}$	$V_D = 3$ V, 10 V, $I_S = -1$ mA sequence each switch on		Room	90	-	120	Ω
$R_{DS(on)}$ matching between channels [g]	$\Delta R_{DS(on)}$			Room	5	-	-	%
Source off leakage current	$I_{S(off)}$	$V_{EN} = 0$ V, $V_D = 10$ V or 0.5 V, $V_S = 0.5$ V or 10 V		Room	0.01	-	-	nA
Drain off leakage current	$I_{D(off)}$		DG406	Room	0.04	-	-	
			DG407	Room	0.04	-	-	
Drain on leakage current	$I_{D(on)}$	$V_S = V_D = \pm 10$ V sequence each switch on	DG406	Room	0.04	-	-	
			DG407	Room	0.04	-	-	
Dynamic Characteristics								
Switching time of Multiplexer	t_{OPEN}	$V_{S1} = 8$ V, $V_{S8} = 0$ V, $V_{IN} = 2.4$ V		Room	300	-	450	ns
Enable turn-on time	$t_{ON(EN)}$	$V_{INH} = 2.4$ V, $V_{INL} = 0$ V, $V_{S1} = 5$ V		Room	250	-	600	
Enable turn-off Time	$t_{OFF(EN)}$			Room	150	-	300	
Charge injection	Q	$C_L = 1$ nF, $V_S = 6$ V, $R_S = 0$ Ω		Room	20	-	-	pC
Power Supplies								
Positive supply current	I+	$V_{EN} = 0$ V or 5 V, $V_A = 0$ V or 5 V		Room	13	-	30	μA
				Full	-	-	75	
Negative supply current	I-			Room	-0.01	-20	-	
				Full	-0.01	-20	-	

Notes

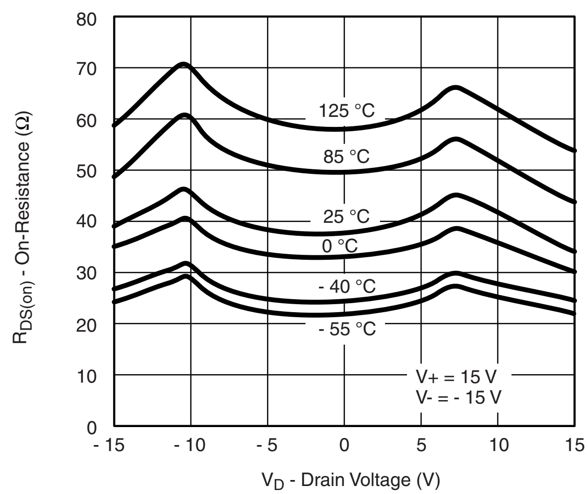
a. Refer to PROCESS OPTION FLOWCHART
b. Room = 25 °C, full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test
f. V_{IN} = input voltage to perform proper function
g. $\Delta R_{DS(on)} = R_{DS(on)}$ max. - $R_{DS(on)}$ min.
h. Worst case isolation occurs on Channel 4 due to proximity to the drain pin

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

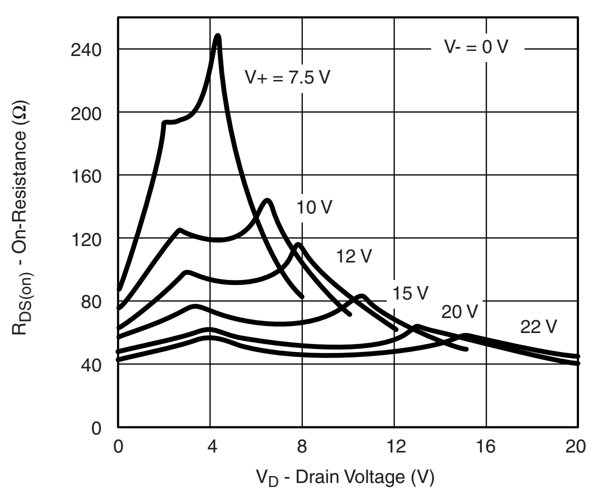
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



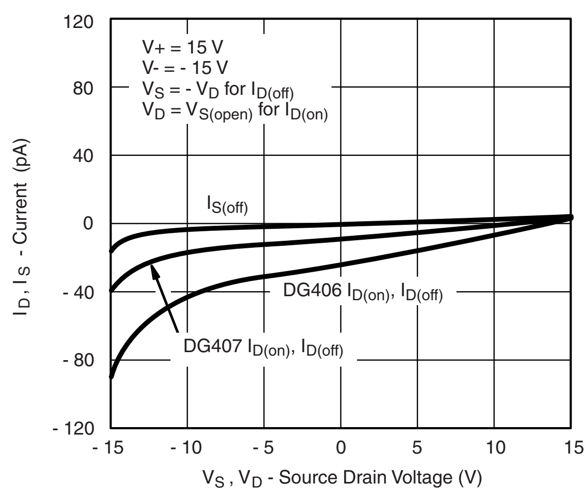
$R_{DS(on)}$ vs. V_D and Supply



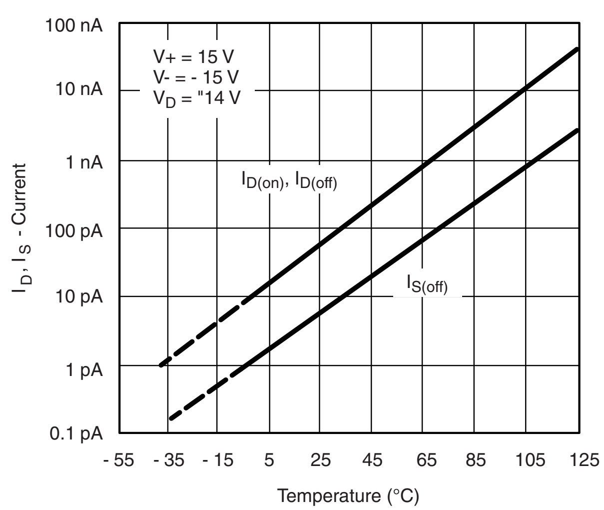
$R_{DS(on)}$ vs. V_D and Temperature



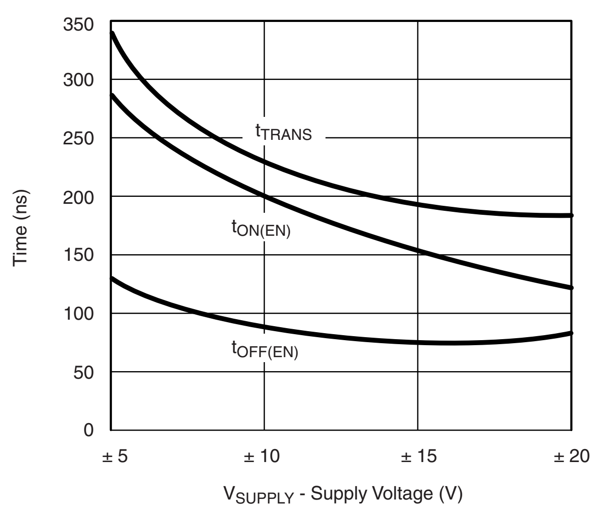
$R_{DS(on)}$ vs. V_D and Supply



I_D, I_S Leakage Currents vs. Analog Voltage

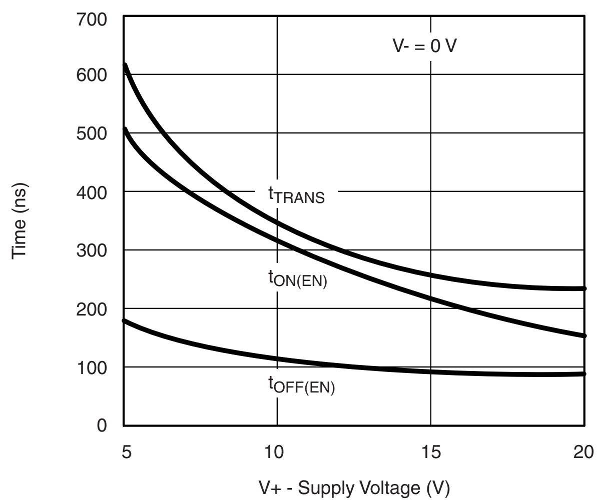


I_D, I_S Leakages vs. Temperature

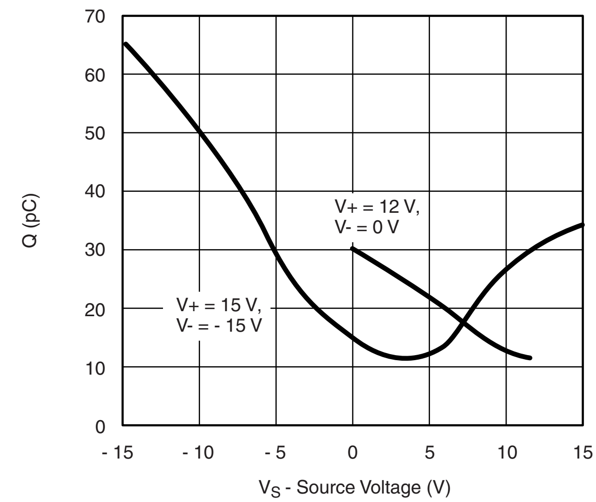


Switching Times vs. Bipolar Supplies

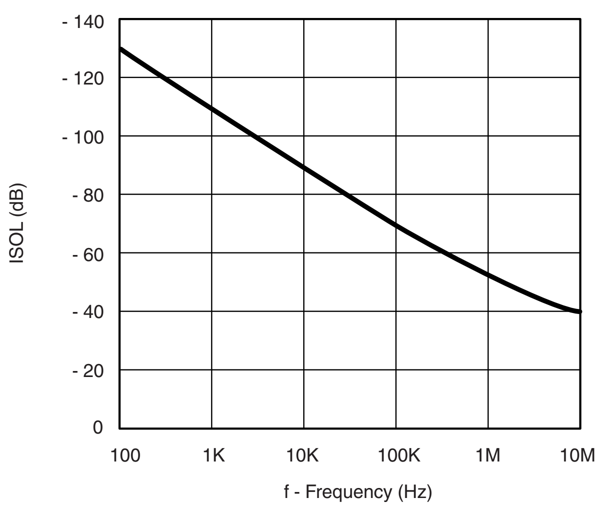
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



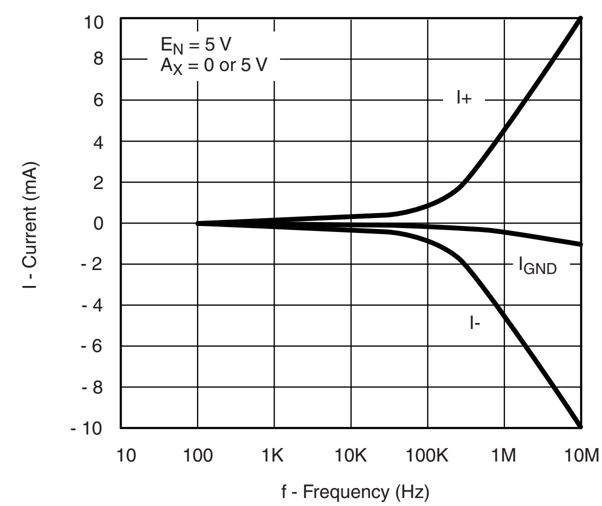
Switching Times vs. Single Supply



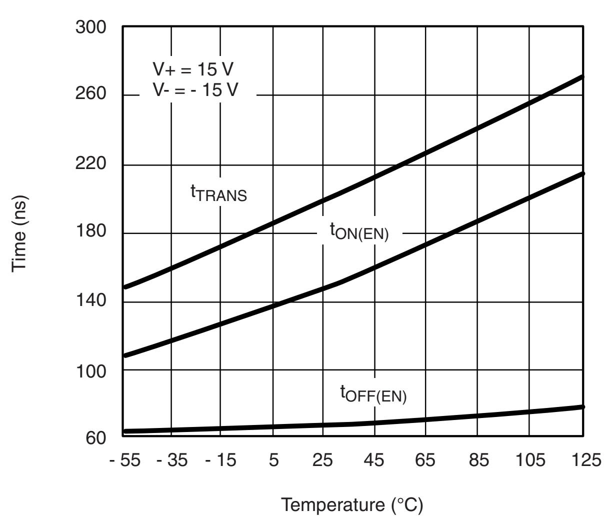
Charge Injection vs. Analog Voltage



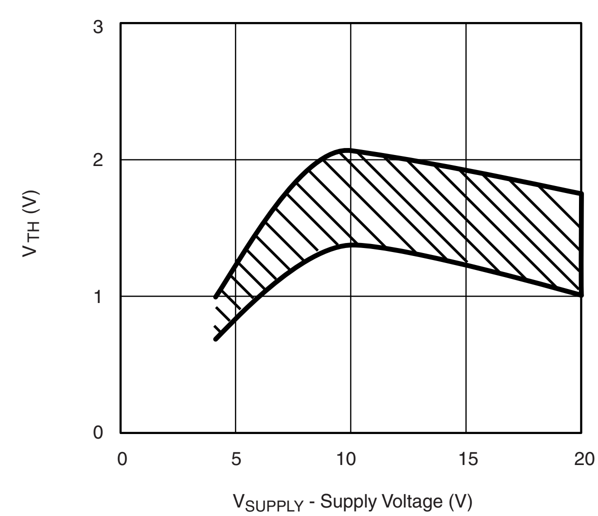
Off-Isolation vs. Frequency



Supply Currents vs. Switching Frequency



t_{ON}/t_{OFF} vs. Temperature



Switching Threshold vs. Supply Voltage

SCHEMATIC DIAGRAM (typical channel)

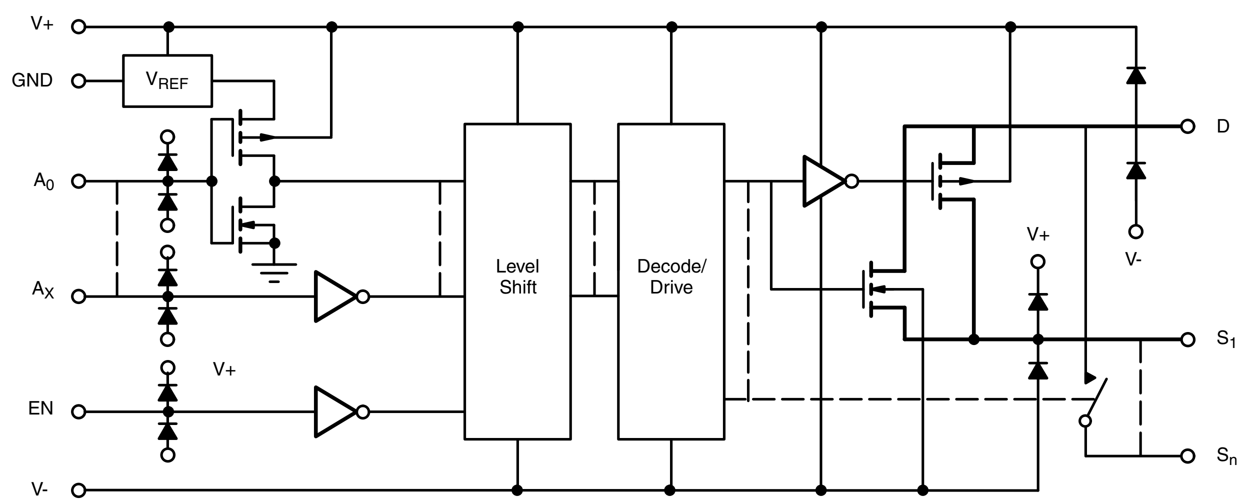
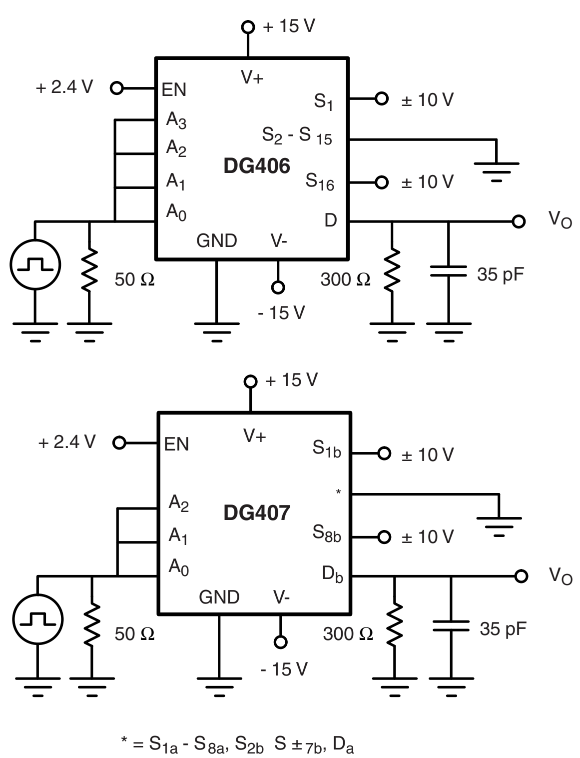


Fig. 1

TEST CIRCUITS



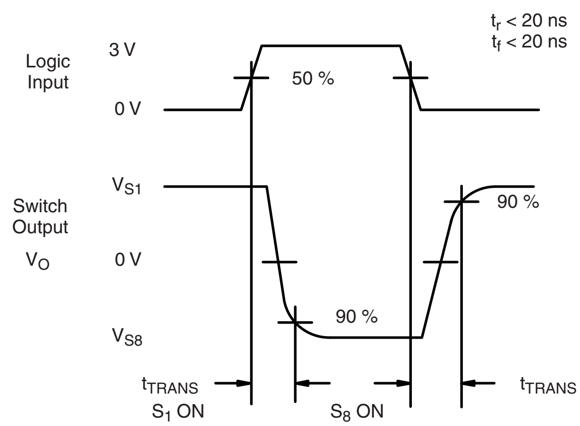


Fig. 2 - Transition Time

TEST CIRCUITS

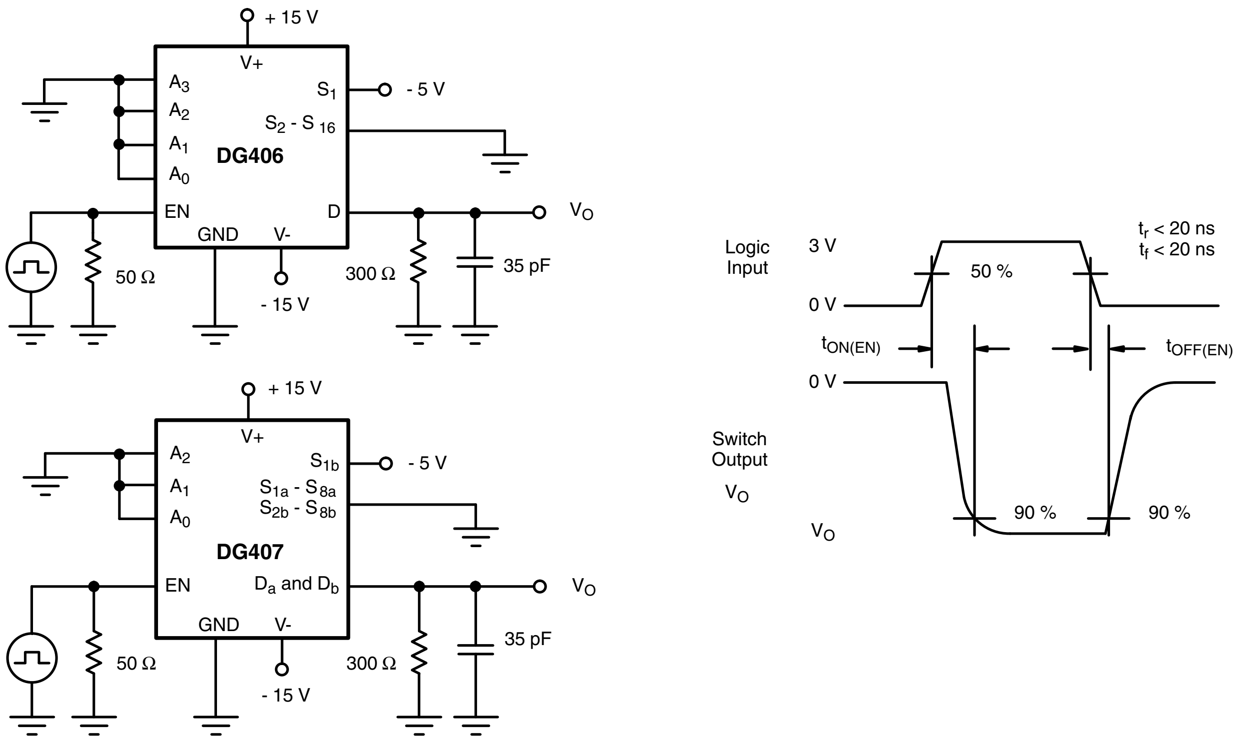


Fig. 3 - Enable Switching Time

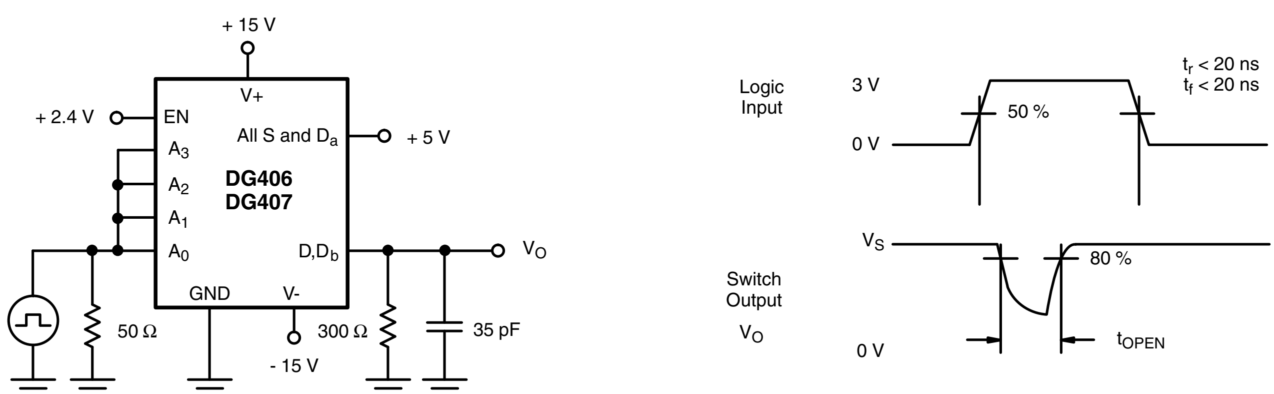


Fig. 4 - Break-Before-Make Interval

APPLICATIONS HINTS

Sampling speed is limited by two consecutive events: the transition time of the multiplexer, and the settling time of the sampled signal at the output.

t_{TRANS} is given on the data sheet. Settling time at the load depends on several parameters: $R_{DS(on)}$ of the multiplexer, source impedance, multiplexer and load capacitances, charge injection of the multiplexer and accuracy desired.

The settling time for the multiplexer alone can be derived from the model shown in figure 5. Assuming a low impedance signal source like that presented by an op amp or a buffer amplifier, the settling time of the RC network for a given accuracy is equal to $n\tau$:

% ACCURACY	# BITS	N
0.25	8	6
0.012	12	9
0.0017	15	11

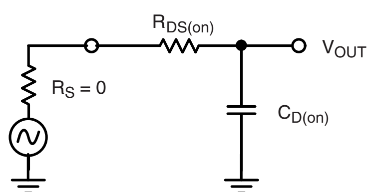


Fig. 5 - Simplified Model of One Multiplexer Channel

The maximum sampling frequency of the multiplexer is:

$$f_s = \frac{1}{N(t_{SETTLING} + t_{TRANS})} \quad (1)$$

where N = number of channels to scan
$t_{SETTLING} = n\tau = n \times R_{DS(on)} \times C_{D(on)}$

For the DG406 then, at room temp and for 12-bit accuracy, using the maximum limits:

$$f_s = \frac{1}{16(9 \times 100\ \Omega \times 10^{-12}F) + 300 \times 10^{-12}s} \quad (2)$$

or

$$f_s = 694\ kHz \quad (3)$$

From the sampling theorem, to properly recover the original signal, the sampling frequency should be more than twice the maximum component frequency of the original signal. This assumes perfect bandlimiting. In a real application sampling at three to four times the filter cutoff frequency is a good practice.

Therefore from equation 2 above:

$$f_c = \frac{1}{4} \times f_s = 173\ kHz \quad (4)$$

From this we can see that the DG406 can be used to sample 16 different signals whose maximum component frequency can be as high as 173 kHz. If for example, two channels are used to double sample the same incoming signal then its cutoff frequency can be doubled.

The block diagram shown in figure 6 illustrates a typical data acquisition front end suitable for low-level analog signals. Differential multiplexing of small signals is preferred since this method helps to reject any common mode noise. This is especially important when the sensors are located at a distance and it may eliminate the need for individual amplifiers. A low $R_{DS(on)}$, low leakage multiplexer like the DG407 helps to reduce measurement errors. The low power dissipation of the DG407 minimizes on-chip thermal gradients which can cause errors due to temperature mismatch along the parasitic thermocouple paths. Please refer to Application Note AN203 for additional information.

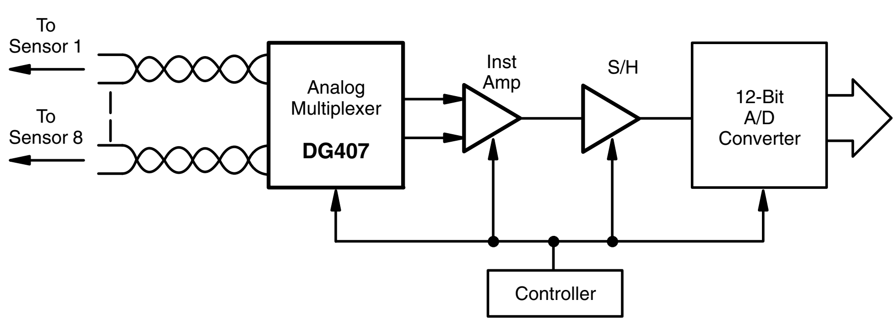
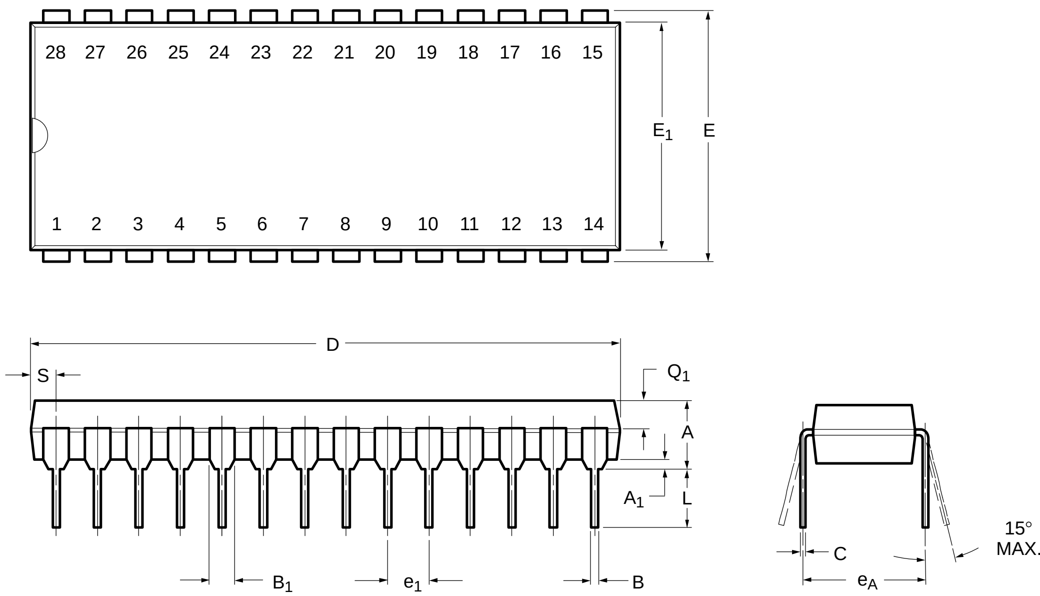


Fig. 6 - Measuring Low-Level Analog Signals is more accurate when using a Differential Multiplexing Technique

PRODUCT SUMMARY				
Part number	DG406	DG406	DG407	DG407
Status code	2	2	2	2
Configuration	16:1 x 1	16:1 x 1	8:1 x 2	8:1 x 2
Single supply min. (V)	5	5	5	5
Single supply max. (V)	44	44	44	44
Dual supply min. (V)	5	5	5	5
Dual supply max. (V)	22	22	22	22
On-resistance (Ω)	50	50	50	50
Charge injection (pC)	15	15	15	15
Source on capacitance (pF)	140	140	70	70
Source off capacitance (pF)	8	8	8	8
Leakage switch on typ. (nA)	0.04	0.04	0.04	0.04
Leakage switch off max. (nA)	0.5	0.5	0.5	0.5
-3 dB bandwidth (MHz)	-	-	-	-
Package	SO-28 (wide)	PLCC-28	SO-28 (wide)	PLCC-28
Functional circuit / applications	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare	Multi purpose, instrumentation, medical and healthcare
Interface	Parallel	Parallel	Parallel	Parallel
Single supply operation	Yes	Yes	Yes	Yes
Dual supply operation	Yes	Yes	Yes	Yes
Turn on time max. (ns)	350	350	350	350
Crosstalk and off isolation	-69	-69	-69	-69

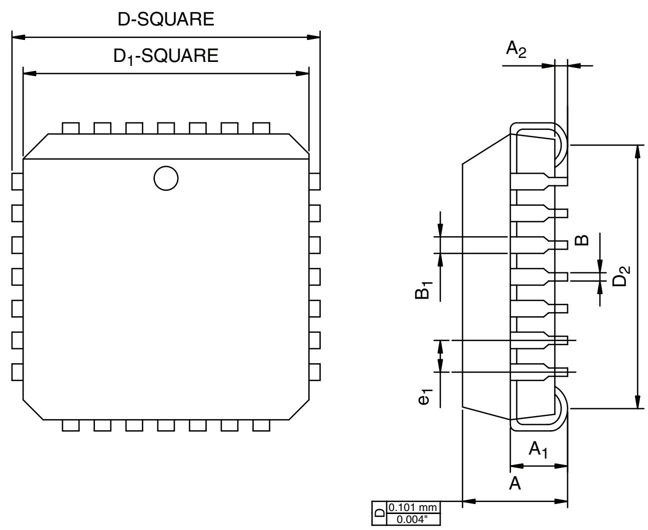
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?70061.

PDIP: 28-LEAD



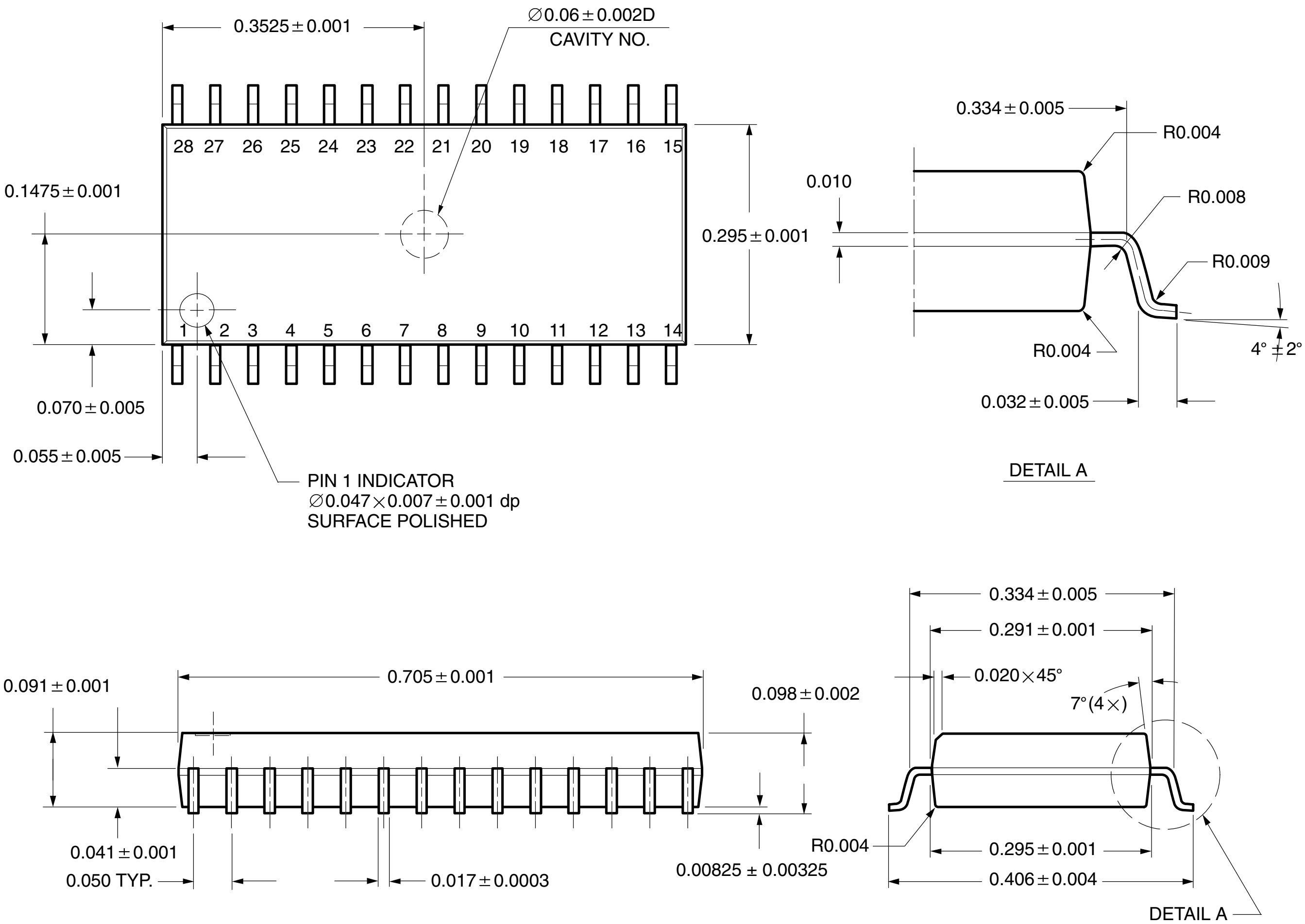
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.29	5.08	0.090	0.200
A_1	0.39	1.77	0.015	0.070
B	0.38	0.56	0.015	0.022
B_1	0.89	1.65	0.035	0.065
C	0.204	0.30	0.008	0.012
D	35.10	39.70	1.380	1.565
E	15.24	15.88	0.600	0.625
E_1	13.21	14.73	0.520	0.580
e_1	2.29	2.79	0.090	0.110
e_A	14.99	15.49	0.590	0.610
L	2.60	5.08	0.100	0.200
Q_1	0.95	2.345	0.0375	0.0925
S	0.995	2.665	0.0375	0.105
ECN: S-03946—Rev. F, 09-Jul-01 DWG: 5488				

PLCC: 28-LEAD



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.20	4.57	0.165	0.180
A_1	2.29	3.04	0.090	0.120
A_2	0.51	-	0.020	-
B	0.331	0.553	0.013	0.021
B_1	0.661	0.812	0.026	0.032
D	12.32	12.57	0.485	0.495
D_1	11.430	11.582	0.450	0.456
D_2	9.91	10.92	0.390	0.430
e_1	1.27 BSC		0.050 BSC	
ECN: T09-0766-Rev. D, 28-Sep-09 DWG: 5491				

SOIC (WIDE-BODY): 28-LEADS



All Dimensions In Inches

ECN: E11-2209-Rev. D, 01-Aug-11
DWG: 5850

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