Powered-off Protection, 1 Ω, 1.8 V to 5.5 V, SPDT Analog Switch (2:1 Multiplexer)

DESCRIPTION

The DG2012E is a high performance single-pole, double-throw (SPDT) analog switch designed for 1.8 V to 5.5 V operation with a single power rail.

Fabricated with high density CMOS technology, the device achieves low on resistance of 1 Ω at a 5 V power supply, low power consumption, and fast switching speeds.

The DG2012E can handle both analog and digital signals and permits signals with amplitudes of up to V+ to be transmitted in either direction. Its control logic inputs can go over V+ up to 5.5 V. It features break before make switching performance. Its -3 dB bandwidth is typically 160 MHz.

A powered-off protection circuit is built into the switch to prevent an abnormal current flow from COM pin to V+ during the power-down condition. Each output pin can withstand greater than 7 kV (human body model).

Operation temperature is specified from -40 °C to +85 °C. The DG2012E is available in SC-70-6L package.

FEATURES

Pb-free Available

RoHS* Available

- Low switch on-resistance (1 Ω)
- 1.65 V to 5.5 V single supply operation
- Isolation in powered-off mode
- Control logic inputs can go over V+
- Low charge injection (5 pC)
- Low total harmonic distortion
- Break before make switching
- Latch-up performance exceeds 300 mA per JESD 78
- ESD tested
  - 7000 V human body model (JS-001)
  - 1000 V charge device model (JS-002)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

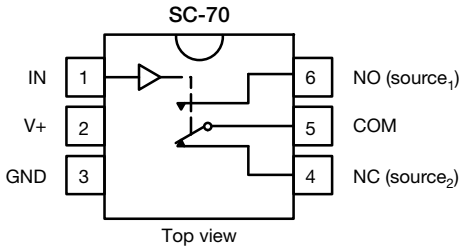
Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

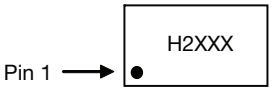
APPLICATIONS

- Smartphones and tablets
- Consumer and computing
- Portable instrumentation
- Medical equipment

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device marking: H2



Device marking: H2XXX
XXX = date / lot traceability code

TRUTH TABLE		
LOGIC	NC	NO
0	On	Off
1	Off	On

ORDERING INFORMATION		
TEMP. RANGE	PACKAGE	PART NUMBER
-40 °C to +85 °C	SC-70-6	DG2012EDL-T1-GE3

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ABSOLUTE MAXIMUM RATINGS

PARAMETER		LIMIT	UNIT
V+, COM, NC, NO, IN reference to GND		-0.3 to 6	V
Continuous current (NO, NC, and COM pins)		± 100	mA
Peak current (pulsed at 1 ms, 10 % duty cycle)		± 300	
Storage temperature (D suffix)		-65 to +150	°C
Power dissipation (packages) [a]	6-pin SO-70 [b]	250	mW
ESD / HBM	JS-001	7000	V
ESD / CDM	JS-002	1000	
Latch up	Per JESD78 with 1.5 x voltage clamp	300	mA

Notes
a. All leads welded or soldered to PC board
b. Derate 3.1 mW/°C above 70 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 5 V)

PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V [e]	TEMP. [a]	LIMITS -40 °C to +85 °C MIN. [b]	TYP. [c]	MAX. [b]	UNIT
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC} V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 4.5 V, V_{COM} = 0.5 V / 2.5 V, I_{NO}, I_{NC} = 10 mA	Room	-	1	1.6	Ω
			Full [d]	-		2	
R_{ON} flatness [d]	R_{ON} flatness	V+ = 4.5 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room	-	0.2	0.5	
R_{ON} match [d]	ΔR_{ON}		Room	-	-	0.3	
Switch off leakage current [f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5 V V_{NO}, V_{NC} = 0.5 V / 4.5 V, V_{COM} = 4.5 V / 0.5 V	Room	-5	-	5	nA
			Full	-20	-	20	
	$I_{COM(off)}$		Room	-5	-	5	
			Full [d]	-20	-	20	
Channel-on leakage current [f]	$I_{COM(on)}$	V+ = 5 V, V_{NO}, V_{NC} = V_{COM} = 0.5 V / 4.5 V	Room	-5	-	5	
			Full [d]	-20	-	20	
Power down leakage	$I_{COM(PD)}$	V+ = 0 V, V_{COM} = 4.5 V, V_{IN} = GND	Full [d]	-1	-	1	µA
Digital Control							
Input high voltage	V_{INH}		Full	2.4	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.8	
Input capacitance [d]	C_{IN}		Full	-	3	-	pF
Input current [f]	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time [d]	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF	Room	-	15	32	ns
			Full [d]	-	-	35	
Turn-off time [d]	t_{OFF}		Room	-	7	28	
			Full [d]	-	-	30	
Break-before-make time [d]	t_d		Room	1	5	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	8	-	pC
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk [d]	X_{TALK}		Room	-	-63	-	
N_O, N_C off capacitance [d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
Channel-on capacitance [d]	C_{ON}		Room	-	52	-	
Power Supply							
Power supply current	I+	V_{IN} = 0 V or V+	Full	-	0.0003	1	µA

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SPECIFICATIONS (V+ = 3 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 1.4 V [e]	**TEMP.** [a]	**LIMITS** -40 °C to 85 °C			**UNIT**
				MIN. [b]	**TYP.** [c]	**MAX.** [b]	
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC} V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0.2 V / 1.5 V, I_{NO} I_{NC} = 10 mA	Room	-	1.4	2.5	Ω
			Full [d]	-	-	3	
R_{ON} flatness [d]	R_{ON} flatness	V+ = 2.7 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room	-	0.6	0.9	
R_{ON} match [d]	ΔR_{ON}		Room	-	-	0.3	
Switch off leakage current [f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 1 V / 3 V, V_{COM} = 3 V / 1 V	Room	-5	-	5	nA
			Full	-15	-	15	
	$I_{COM(off)}$		Room	-5	-	5	
			Full [d]	-15	-	15	
Channel-on leakage current [f]	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V / 3 V	Room	-5	-	5	
			Full [d]	-15	-	15	
Digital Control							
Input high voltage	V_{INH}		Full	1.4	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.4	
Input capacitance [d]	C_{IN}		Full	-	3	-	pF
Input current [f]	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time [d]	t_{ON}	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF	Room	-	21	42	ns
			Full [d]	-	-	47	
Turn-off time [d]	t_{OFF}		Room	-	16	32	
			Full [d]	-	-	35	
Break-before-make time [d]	t_d		Room	1	7	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	6	-	pC
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk [d]	X_{TALK}		Room	-	-63	-	
Bandwidth [d]	BW		Room	-	160	-	MHz
N_O, N_C off capacitance [d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
Channel-on capacitance [d]	C_{ON}		Room	-	52	-	
Power Supply							
Power supply current	I+	V_{IN} = 0 V or V+	Full	-	0.00002	1	µA

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SPECIFICATIONS (V+ = 2 V)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V+ = 2 V, ± 10 %, V_{IN} = 0.4 V or 1.6 V [e]	**TEMP.** [a]	**LIMITS** -40 °C to +85 °C			**UNIT**
				MIN. [b]	**TYP.** [c]	**MAX.** [b]	
Analog Switch							
Analog signal range [d]	V_{NO}, V_{NC}, V_{COM}		Full	0	-	V+	V
On-resistance	R_{ON}	V+ = 1.8 V, V_{COM} = 0.2 V / 0.9 V, I_{NO}, I_{NC} = 10 mA	Room	-	5	10	Ω
			Full [d]	-	-	15	
R_{ON} flatness [d]	R_{ON} flatness	V+ = 1.8 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room	-	6	9	
R_{ON} match [d]	ΔR_{ON}		Room	-	-	0.3	
Switch off leakage current [f]	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 2.2 V, V_{NO}, V_{NC} = 0.5 V / 1.5 V, V_{COM} = 1.5 V / 0.5 V	Room	-0.5	-	0.5	nA
			Full	-5	-	5	
	$I_{COM(off)}$		Room	-0.5	-	0.5	
			Full [d]	-5	-	5	
Channel-on leakage current [f]	$I_{COM(on)}$	V+ = 2.2 V, V_{NO}, V_{NC} = V_{COM} = 0.5 V / 1.5 V	Room	-0.5	-	0.5	
			Full [d]	-5	-	5	
Digital Control							
Input high voltage	V_{INH}		Full	1.6	-	-	V
Input low voltage	V_{INL}		Full	-	-	0.4	
Input capacitance [d]	C_{IN}		Full	-	3	-	pF
Input current [f]	I_{INL} or I_{INH}	V_{IN} = 0 V or V+	Full	-1	-	1	µA
Dynamic Characteristics							
Turn-on time [d]	t_{ON}	V_{NO} or V_{NC} = 1.5 V, R_L = 300 Ω, C_L = 35 pF	Room	-	37	57	ns
			Full [d]	-	-	60	
Turn-off time [d]	t_{OFF}		Room	-	26	44	
			Full [d]	-	-	45	
Break-before-make time [d]	t_d		Room	1	17	-	
Charge injection [d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω	Room	-	21	-	pC
Off-isolation [d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	-	-63	-	dB
Crosstalk [d]	X_{TALK}		Room	-	-63	-	
N_O, N_C off capacitance [d]	$C_{NO(off)}$ $C_{NC(off)}$	V_{IN} = 0 V or V+, f = 1 MHz	Room	-	16	-	pF
Channel-on capacitance [d]	C_{ON}		Room	-	51	-	
Power Supply							
Power supply current	I+	V_{IN} = 0 V or V+	Full	-	0.00001	1	µA

Notes

a. Room = 25 °C, full = as determined by the operating suffix
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
c. Typical values are for design aid only, not guaranteed nor subject to production testing
d. Guarantee by design, nor subjected to production test
e. V_{IN} = input voltage to perform proper function
f. Guaranteed by 5 V leakage testing, not production tested

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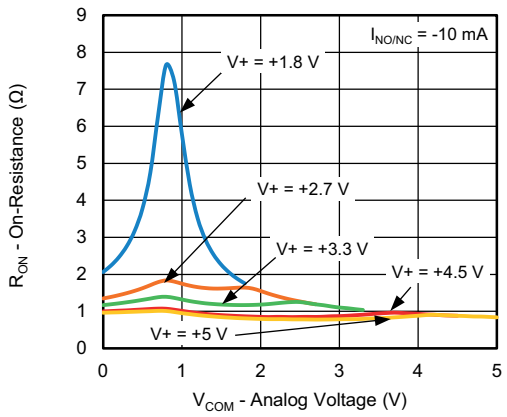
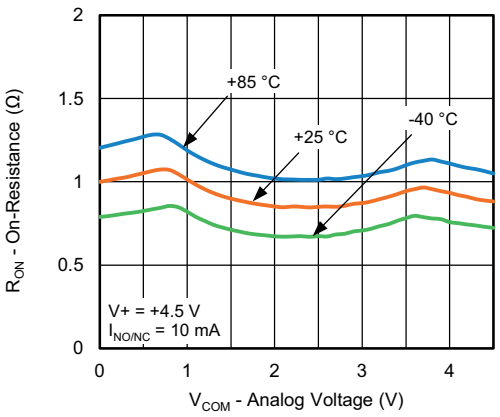
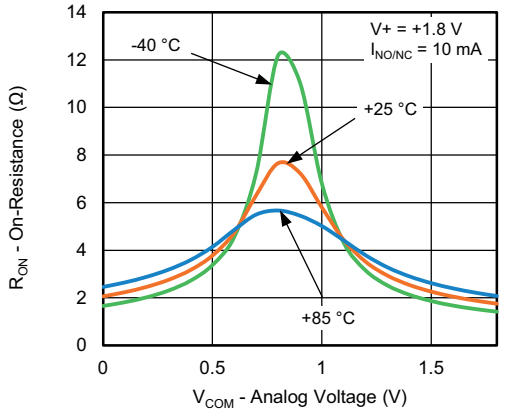
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



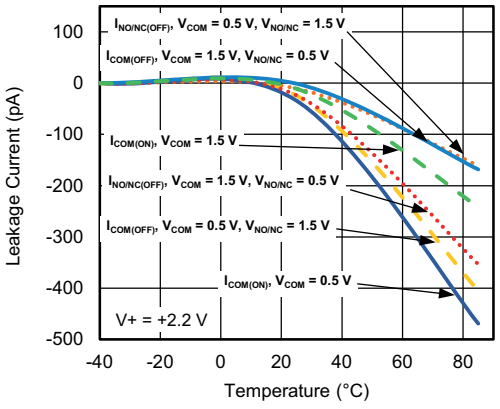
R_{ON} vs. V_{COM} and Supply Voltage



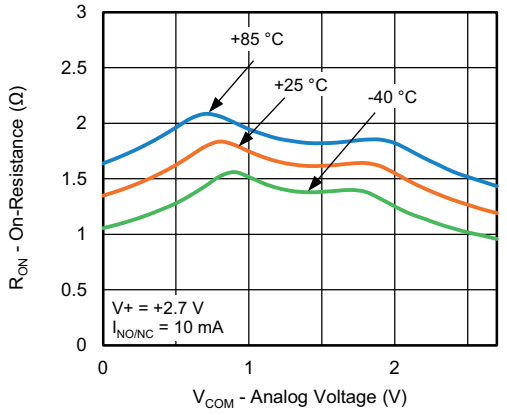
R_{ON} vs. V_{COM} and Temperature



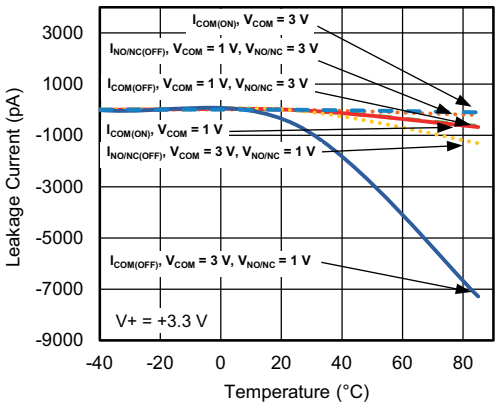
R_{ON} vs. V_{COM} and Temperature



Leakage Current vs. Temperature



R_{ON} vs. V_{COM} and Temperature



Leakage Current vs. Temperature

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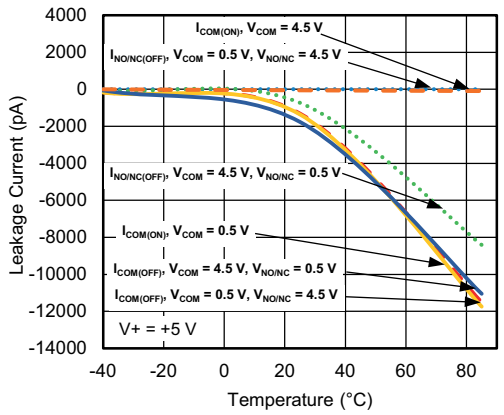
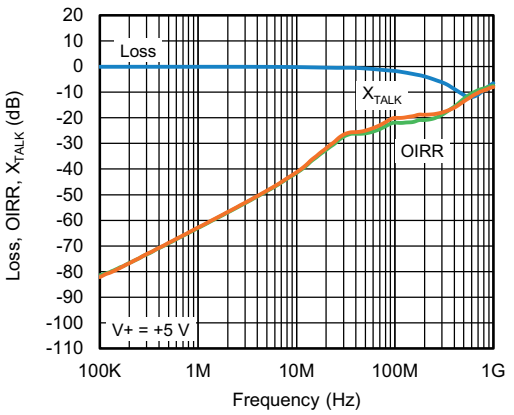
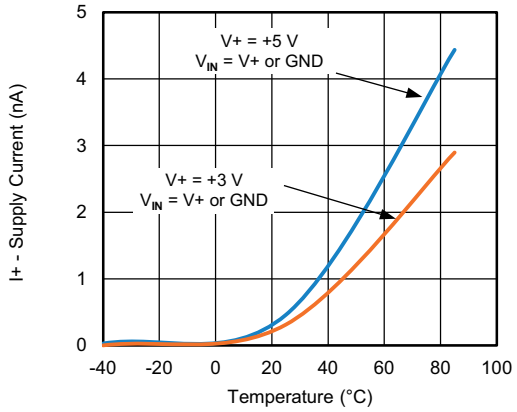


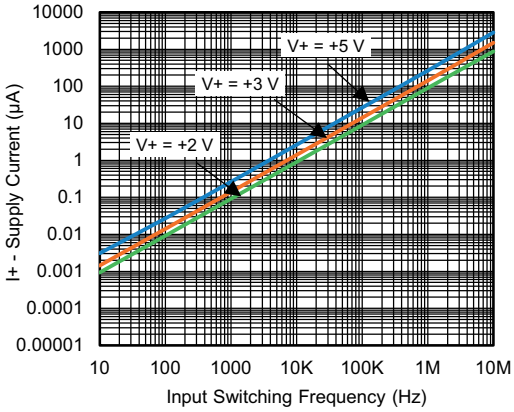
Leakage Current vs. Temperature



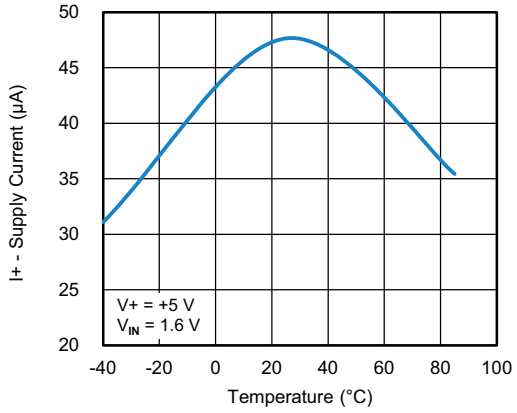
Insertion Loss, Off-Isolation Crosstalk vs. Frequency



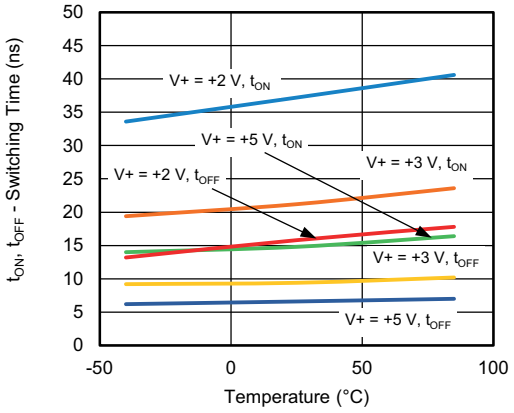
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency



Supply Current vs. Temperature



Switching Time vs. Temperature and Supply Voltage

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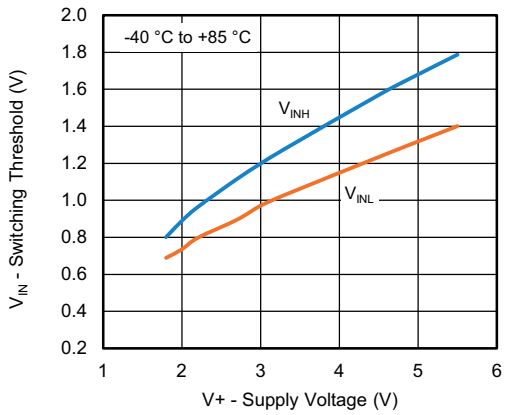
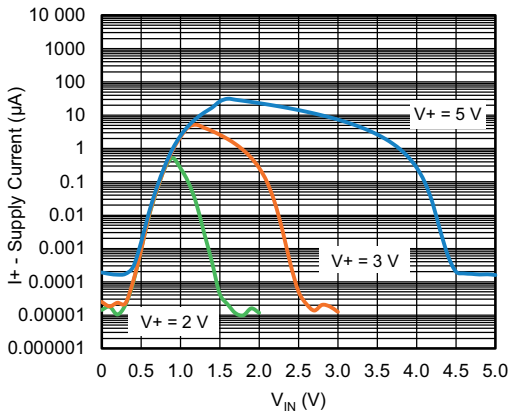
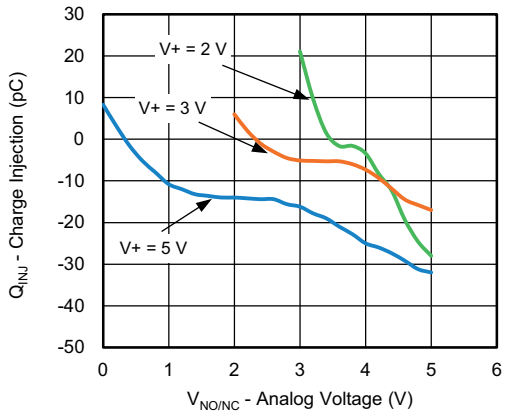


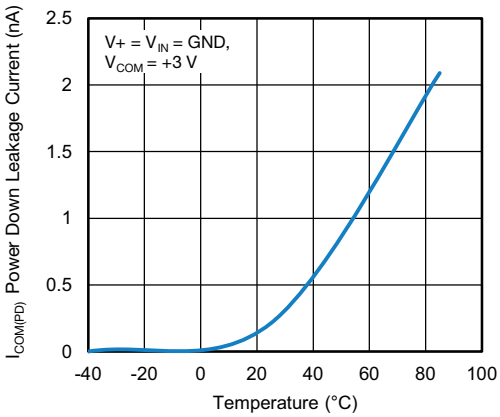
Switching Threshold vs. Supply Voltage



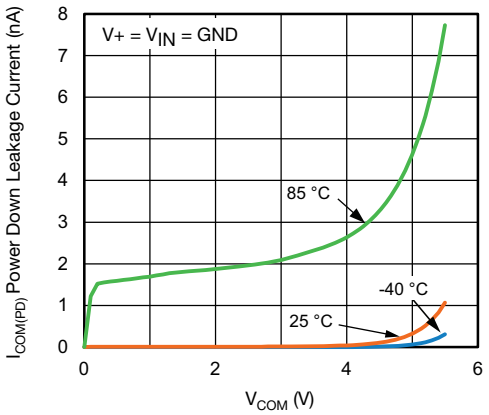
Supply Current vs. Enable Input Voltage



Charge Injection vs. Analog Voltage



Power Down Leakage Current vs. Temperature



Power Down Leakage Current vs. V_{COM}

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TEST CIRCUITS

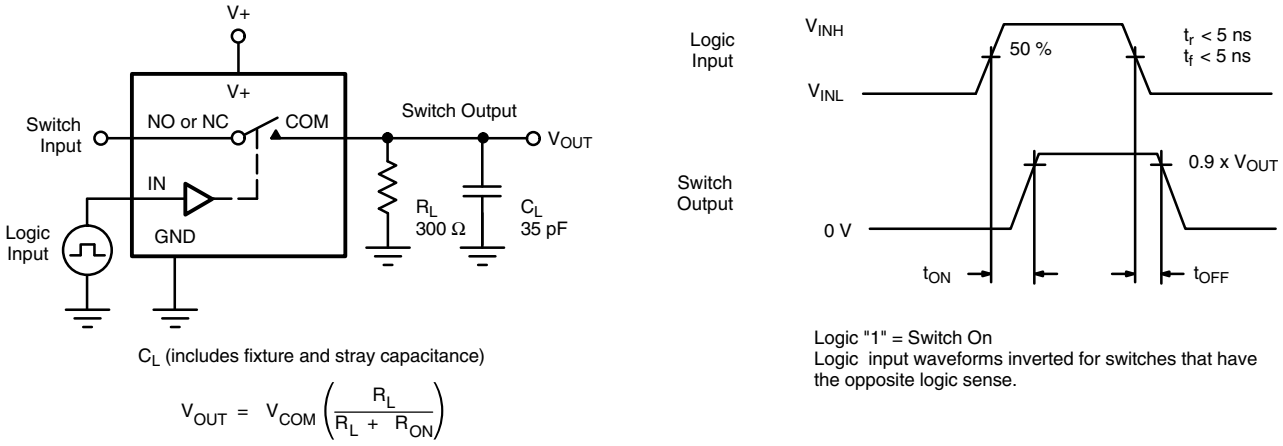

Fig. 1 - Switching Time

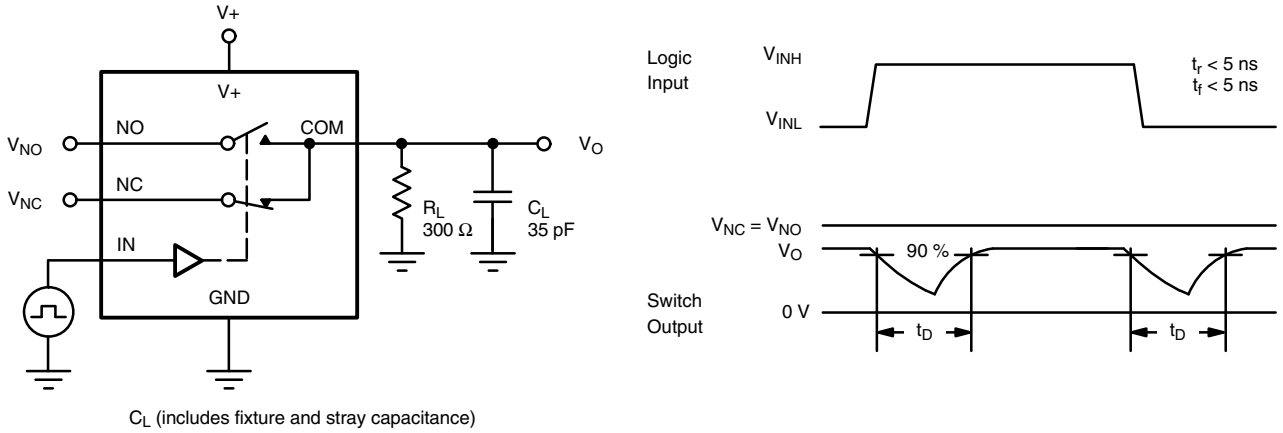

Fig. 2 - Break-Before-Make Interval

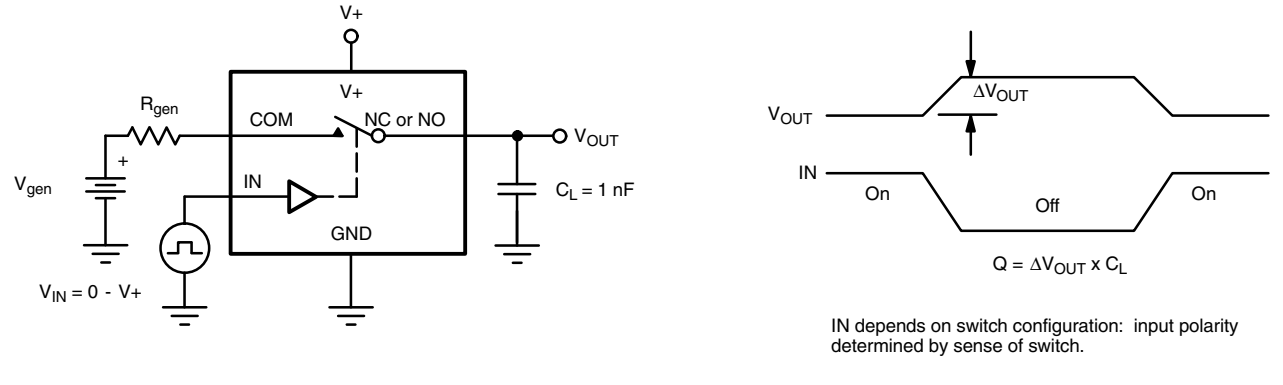

Fig. 3 - Charge Injection

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TEST CIRCUITS

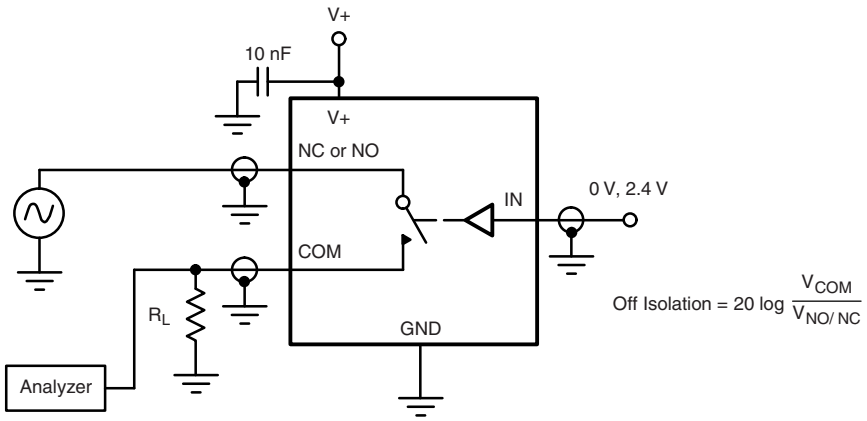

Fig. 4 - Off-Isolation

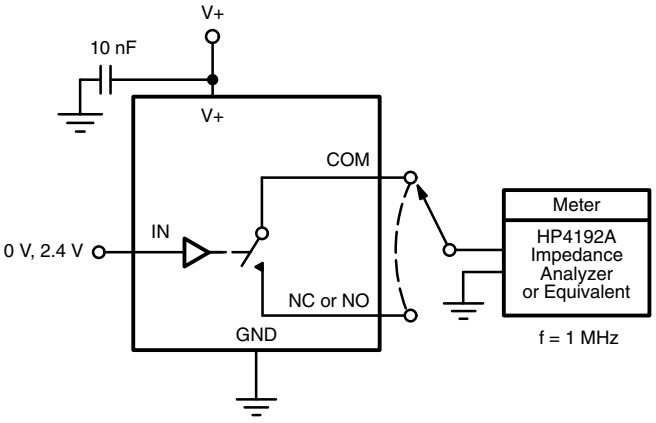

Fig. 5 - Channel Off / On Capacitance

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