TMUXHS221LV USB 2.0 480Mbps 2:1 or 1:2 Multiplexer or Demultiplexer Switch

1 Features

- Compatible to USB 2.0 and eUSB2 LS, FS, and HS physical layers
- Switch that supports differential signals up to 3Gbps
- Analog switch that can support most CMOS signals up to 3.3 V
- Data pins are 5 V tolerant
- Low RON of 3 Ω at $V_{I/O}$ = 0 V
- High –3 dB BW of 3.3 GHz
- Excellent for USB 2.0 or eUSB2 HS signals at 240 MHz:
  - Insertion loss = –0.4 dB
  - Return loss = –22 dB
  - Off isolation or cross talk = –32 dB
- Minimal vertical and horizontal USB 2.0 HS eye attenuation
- 1.8 V supply voltage
- 1.2 or 1.8 V control logic inputs
- Extended industrial temperature range of –40 to 125°C
- Small 10-pin 1.8 mm × 1.4 mm, UQFN package
- Pin-to-pin and BOM-to-BOM with multiple sources

2 Applications

- PC and notebooks
- Gaming, TV, home theater, and entertainment
- Data center and enterprise computing
- Medical applications
- Test and measurements
- Factory automation and control
- Mobile phones and tablets

3 Description

The TMUXHS221LV is a high-speed bidirectional 2:1 or 1:2 multiplexer or demultiplexer optimized for USB 2.0 and eUSB2 LS, FS, and HS signaling. The TMUXHS221LV is an analog passive switch that works for many high-speed interfaces with data rates up to 3Gbps. The TMUXHS221LV supports either differential or single-ended CMOS signaling with a voltage range of −0.3 to 3.6 V.

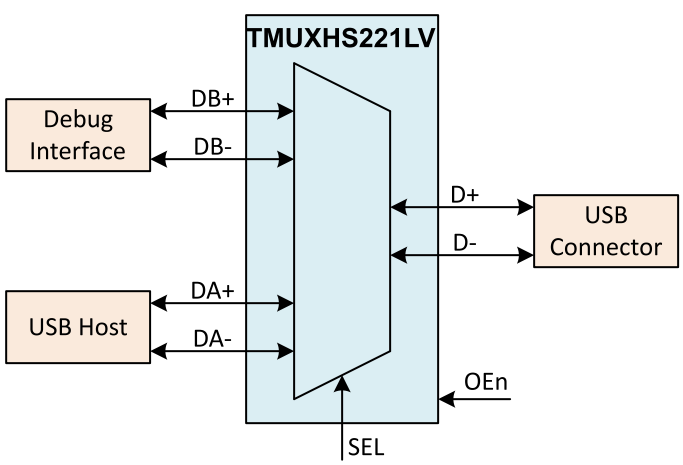
The ideal high-speed performance of the TMUXHS221LV results in minimal attenuation to the USB 2.0 or eUSB2 HS signal eye diagrams with very low channel ON resistance, high bandwidth, low reflection, and low added jitter. The device is optimized for ideal high frequency response so that passing USB 2.0 HS electrical compliance becomes easier. The data-paths of the device are also matched for best intra-pair skew performance.

The TMUXHS221LV has an extended temperature range that suits many rugged applications including industrial and high reliability use cases.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMUXHS221LV	NKG (UQFN, 10)	1.8 mm × 1.4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Application Use Case

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4 Revision History

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Pin Configuration and Functions

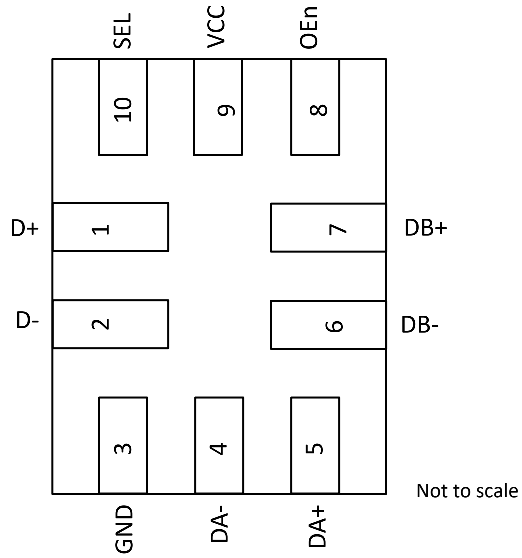


Figure 5-1. TMUXHS221LV NKG Package, 10-Pin UQFN (Top View)

Table 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
D+	1	I/O	Data signals Common Port, positive
D-	2	I/O	Data signals Common Port, negative
DA+	5	I/O	Data signals Port A, positive
DA-	4	I/O	Data signals Port A, negative
DB+	7	I/O	Data signals Port B, positive
DB-	6	I/O	Data signals Port B, negative
SEL	10	IN	Switch control configuration signal as provided in Table 7-1.
OEn	8	IN	
VCC	9	P	1.8 V power supply
GND	3	G	Ground

(1) IN = input, I/O = input or output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
$V_{CC\text{-}ABSMAX}$	Supply voltage		–0.5	2.4	V
$V_{I/O\text{-}ABSMAX}$	Voltage	Data pins	–0.5	5.5	V
$V_{IN\text{-}ABSMAX}$	Voltage	Control pins	–0.5	4	V
$I_{I/O\text{-}ABSMAX}$	ON-state switch current	Data pins		100	mA
$T_{J\text{-}ABSMAX}$	Junction temperature		–40	125	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±5000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
VCC	Supply voltage	DC plus AC power should not exceed these limits	1.62	1.8	1.98	V
VCC_{RAMP}	Supply voltage ramp time		0.1		100	ms
$V_{I/O}$	Voltage range for data signals ($V_{I/O}$)	D, DA, DB	-0.3		3.6	V
V_{IN}	Voltage range for control signals (V_{IN})	OEn, SEL	-0.3		3.6	V
T_J	Junction temperature				125	°C
T_A	Operating free-air/ambient temperature		-40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TMUXHS221LV	UNIT
		NKG (UQFN)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance - High K	225.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	147.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	147.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Device active current	OEn = L		10	17	µA
I_{STDN}	Device shutdown current	OEn = H		0.5	3	µA
C_{ON}	Output ON capacitance to GND	OEn = L		1.4		pF
R_{ON}	Channel ON resistance	$V_{I/O}$ = 0 V , I_O = –8 mA		3	5.4	Ω
		$V_{I/O}$ = 2.4 V, I_O = –8 mA		3.9	8	Ω
$R_{ON,FLAT}$	Channel ON resistance flatness defined as difference of R_{ON} over input voltage range	$V_{I/O}$ = 0 V and $V_{I/O}$ = 2.4 V; I_O = –8 mA		1		Ω
ΔR_{ON}	On-resistance match between pairs for the same channel at same $V_{I/O}$, VCC and $T_{A,}$	$V_{I/O}$ = 0 V; I_O = –8 mA		0.2		Ω
		$V_{I/O}$ = 2.4 V; I_O = –8 mA		0.2		Ω
V_{IH}	Input high voltage, control pins (OEn, SEL)		0.9		3.6	V
V_{IL}	Input low voltage, control pins (OEn, SEL)		-0.3		0.25	
$I_{IH,IN}$	Input high current, control pins (OEn, SEL)	V_{IN} = 3.6 V			8	µA
$I_{IL,IN}$	Input low current, control pins (OEn, SEL)	V_{IN} = 0 V			0.2	µA
$I_{I/O,H}$	Input high current, data pins (Dx, DAx, DBx)	$V_{I/O}$ = 3.6 V			5	µA
$I_{I/O,L}$	Input low current, data pins (Dx, DAx, DBx)	$V_{I/O}$ = 0 V			0.2	µA
$I_{HIZ,I/O}$	Leakage current through turned off switch	OEn = H; $V_{I/O}$ = 3.6 V			8	µA
$I_{OFF,IN}$	Failsafe leakage current for control pins (IN)	VCC = 0 V, V_{IN} = 1.98 V			12	µA
$I_{OFF,I/O}$	Failsafe leakage current for data pins (I/O)	VCC = 0 V, $V_{I/O}$ = 3.6 V			12	µA

6.6 High-Speed Performance Parameters

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
BW	–3-dB bandwidth	Relative to DC		3.3		GHz
I_L	Differential insertion loss	f = 10 MHz		-0.3		dB
		f = 240 MHz		-0.4		
R_L	Differential return loss	f = 10 MHz		-32		dB
		f = 240 MHz		-22		
O_{IRR}	Differential OFF isolation (D to DA/DB)	f = 10 MHz		-60		dB
		f = 240 MHz		-32		
XT	Single-Ended cross-talk (in between D+ and D- or DA+ and DA- or DB+ and DB-)	f = 10 MHz		-60		dB
		f = 240 MHz		-41		dB
XT_diff	Differential cross-talk (DA to DB or DB to DA)	f = 10 MHz		-64		dB
		f = 240 MHz		-32		dB

6.7 Switching Characteristics

over operating free-air temperature and supply voltage range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay			60	80	ps
t_{SW}	Switching time CTRL-to-Switch ON (SEL toggles in between H, L)	R_L = 50 Ω, C_L = 10 pF			1.5	µs
t_{OFF}	Time required for device ON-to-OFF transition (OEn = L to H)	R_L = 50 Ω, C_L = 10 pF			0.5	µs
t_{ON}	Time required for device OFF-to-ON transition (OEn = H to L)	R_L = 50 Ω, C_L = 10 pF			32	µs
t_{SK_INTRA}	Intra-pair output skew between positive and negative for same differential channel	For Dx to DAx or DBx channels		3	10	ps
t_{SK_INTER}	Inter-pair output skew between channels	For Dx to DAx or DBx channels		1	10	ps

6.8 Typical Characteristics – S-Parameters

Figure 6-1 and Figure 6-2 show differential insertion loss and return loss for a typical TMUXHS221LV channel, respectively. The excellent high-speed performance at 240 MHz results in minimal attenuation to the USB 2.0 or eUSB2 HS signal eye diagrams. Figure 6-3 shows differential crosstalk for a typical TMUXHS221LV channel. Note, the measurements provided are performed in TI evaluation board with board and equipment parasitics calibrated out.

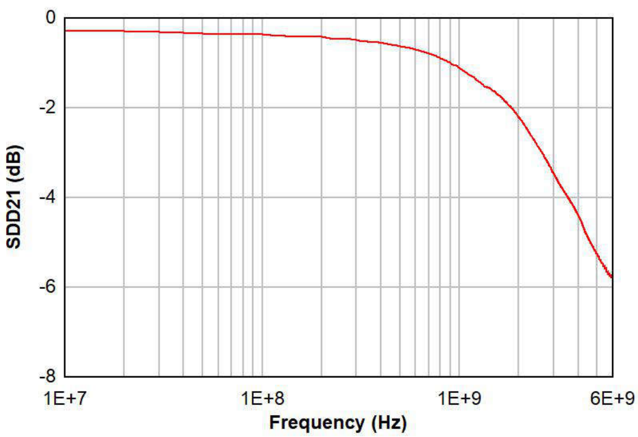


Figure 6-1. Typical Differential Insertion Loss vs Frequency

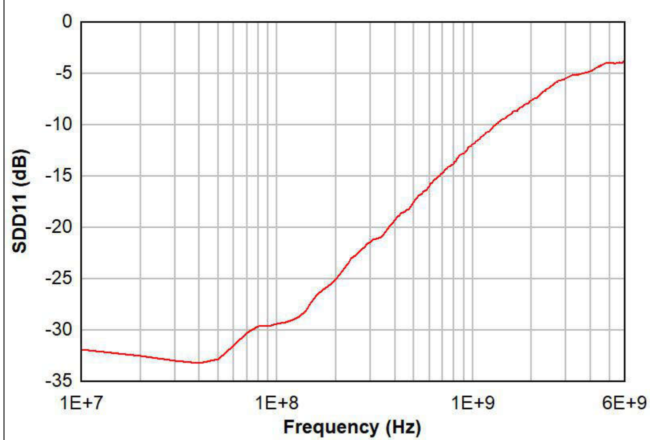


Figure 6-2. Typical Differential Return Loss vs Frequency

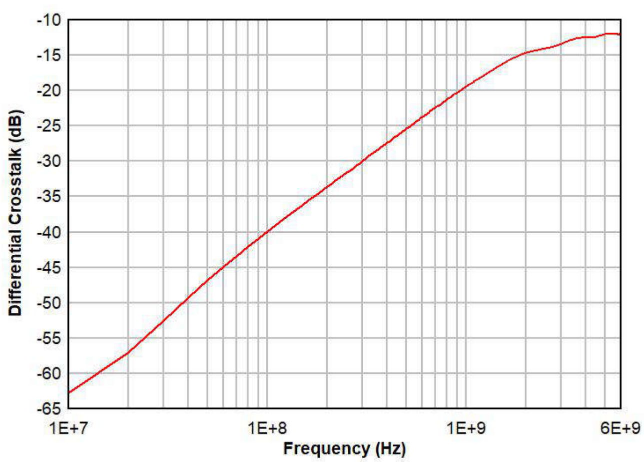


Figure 6-3. Typical Differential Crosstalk vs Frequency

6.9 Typical Characteristics – R_{ON}

Figure 6-4, Figure 6-5, and Figure 6-6 show switch ON resistance R_{ON} versus common mode voltage VCM, supply voltage VCC, and ambient temperature respectively. All curves are at nominal PVT conditions unless specified.

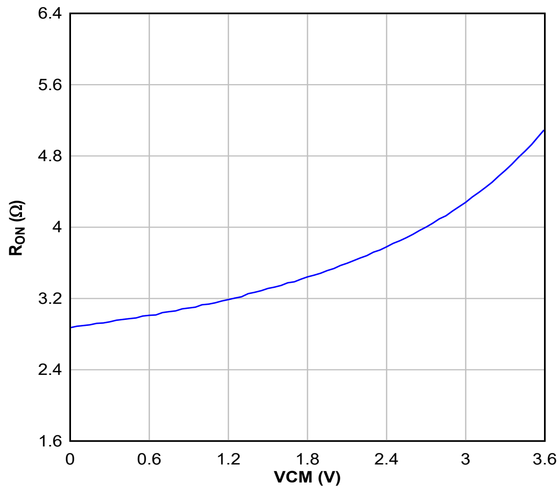


Figure 6-4. R_{ON} vs Common Mode Voltage VCM

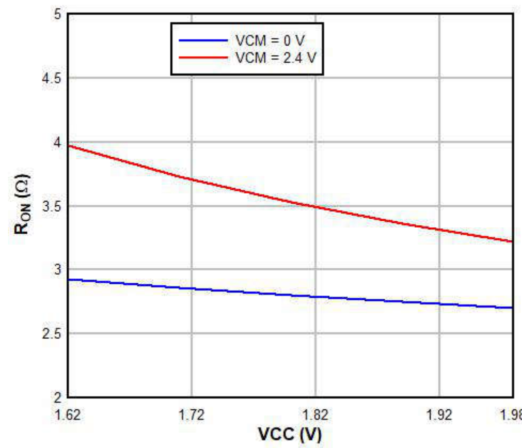


Figure 6-5. R_{ON} vs Supply Voltage VCC

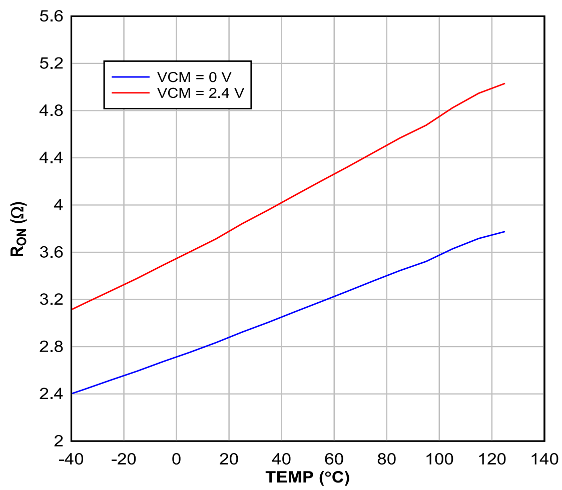


Figure 6-6. R_{ON} vs Ambient Temperature

6.10 Typical Characteristics – Eye Diagrams

Figure 6-7 and Figure 6-8 show a side-by-side comparison of 480Mbps USB 2.0 HS signals through calibration traces (without the device) and a typical TMUXHS221LV channel. The attenuation of the vertical and horizontal eye opening through the device is minimal. Also, the mux device adds a negligible amount of jitter to the signals.

Figure 6-7. Through Calibration Traces at 480Mbps

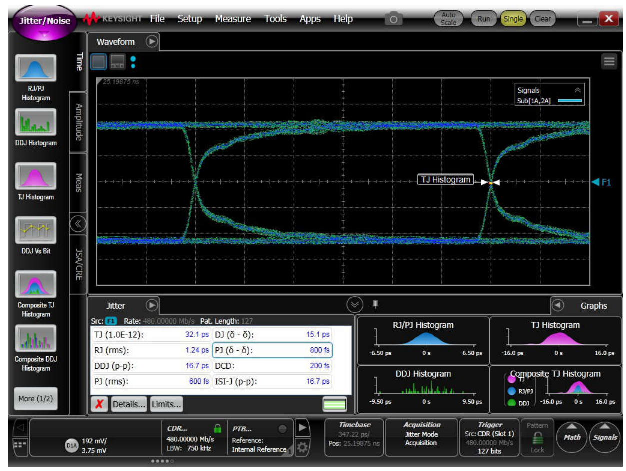


Figure 6-8. Through a Typical TMUXHS221LV Channel at 480Mbps

Figure 6-9 and Figure 6-10 show a side-by-side eye diagram comparison at 3Gbps signals through calibration traces (without the device) and a typical TMUXHS221LV channel. Attenuation of the vertical and horizontal eye opening through the device is minimal. The mux device adds only a small amount of jitter at 3Gbps.

Figure 6-9. Through Calibration Traces at 3Gbps

Figure 6-10. Through a Typical TMUXHS221LV Channel at 3Gbps

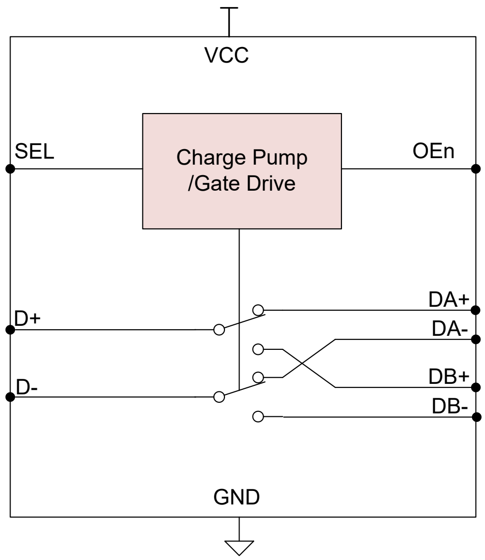
7 Detailed Description

7.1 Overview

The TMUXHS221LV is an analog passive mux with 2:1 or 1:2 multiplexer or demultiplexer that can work for any low-speed, high-speed, differential or single-ended signals. The signals must be within the allowable voltage range of −0.3 to 3.6 V. The device is optimized for eUSB2 and USB 2.0 LS, FS, and HS signaling.

The dynamic characteristics of the device allow high-speed switching with minimal attenuation to the signal eye diagram and little added jitter. While the device is recommended for the interfaces up to 3Gbps, actual data rates where the device can be used highly depends on the electrical channels. For low loss channels where adequate margin is maintained, the device can potentially be used for higher data rates.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Enable and Power Savings

The TMUXHS221LV has two power modes: active, or normal, operating mode and standby, or shutdown mode. During standby mode, the device consumes very little current to achieve ultra low power in systems where saving power is critical. To enter standby mode, OEn must be pulled high.

7.3.2 Data Line Biasing

The TMUXHS221LV does not contain any internal biasing. All channels of the device must be externally biased from either of the two sides to avoid floating channels.

7.4 Device Functional Modes

Table 7-1. Mux Configuration Control Logic for TMUXHS221LV[1]

SEL	OEn	Mux Configuration
L	L	D to DA
H	L	D to DB
X	H	All channels are disabled and Hi-Z

(1) The TMUXHS221LV can tolerate polarity inversions. Ensure that the polarity consistency is maintained for all signals. However the device cannot change polarity from input to output.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUXHS221LV is an analog high-speed mux/demux that can be used for routing differential as well as single ended CMOS signals through it. The device can be used for many high speed and low speed interfaces up to 3Gbps including the following:

- Universal Serial Bus (USB) 2.0 HS, FS, and LS
- Embedded Universal Serial Bus (eUSB) 2.0 HS, FS, and LS
- Inter-Integrated Circuit (I^2C) Bus
- System Management Bus (SMBus™)
- Universal Asynchronous Receiver-Transmitter (UART™)
- Debug interface signals
- Mipi® Camera Serial Interface (CSI-2), Display Serial Interface (DSI)
- PCIe® clock
- DisplayPort™ Auxiliary and Hot Plug Detect Signals
- Universal Serial Bus Type C Sideband Use (USB-C™ SBU) signals
- Low Voltage Differential Signaling (LVDS)

An available GPIO pin of a controller or hard tie to voltage level H or L can easily control the mux or demux selection pin (SEL) of the device as an application requires.

Many interfaces require AC coupling the capacitors between the transmitter and receiver. The 0201 or 0402 capacitors are the preferred option, but other capacitors may be used depending on interface speed and signal integrity needs. If AC coupling capacitors are used on both sides of the TMUXHS221LV, then ensure the device is biased from either side, as there is no internal biasing to the device.

8.2 Typical Applications

8.2.1 Routing Debug Signals to USB Port

Many electronic end-equipment such as PCs, media players, point of sales registers, printers, cameras, headphones, smartphones, tablets, and so forth use USB ports (such as USB Type-A, USB Type-B, or USB Type-C™) for in-field or factory debug interface. In such use cases debug signals are routed to USB 2.0 pins of a USB port through a mux or demux device. TMUXHS221LV is a good fit for such use cases with its flexible data handling capability. TMUXHS221LV can handle virtually any debug interface signals as long as they are limited to −0.3 V (minimum) to 3.6 V (maximum). The device also provides very low attenuation to both USB 2.0 and debug signals with its very low channel ON resistance, high bandwidth, and low reflection.

Figure 8-1 shows a system implementation where USB 2.0 signals are multiplexed with debug interface signals into DP/DM wires of a USB port.

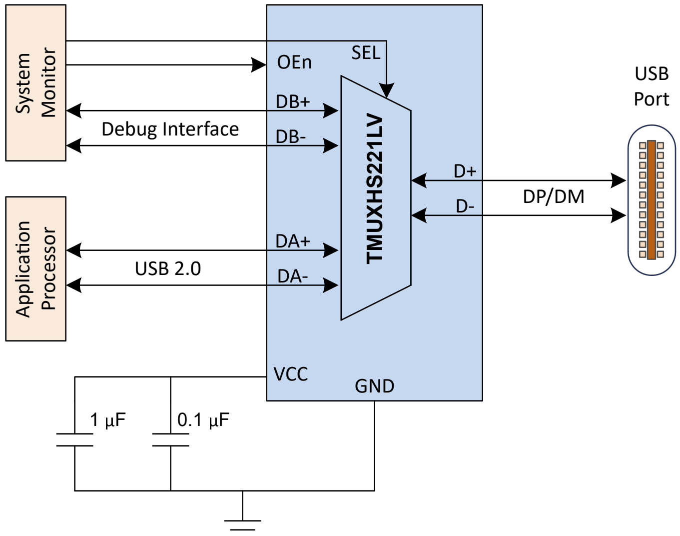


Figure 8-1. Routing Debug Signals to USB Port

8.2.1.1 Design Requirements

Table 8-1 provides various parameters and their expected values to implement the routing debug signals into the USB port. Note that the recommendation is for illustration purpose only.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
DA+, DA-, DB+, and DB−	Direct connect to processors, −0.3 – 3.6 V
SEL/OEn pin maximum voltage for low	0.4 V
SEL/OEn pin minimum voltage for high	1.4 V
Decoupling capacitor for VCC	0.1 µF and 1 µF

8.2.1.2 Detailed Design Procedure

Signal integrity is important because as a passive switch, the device provides no signal conditioning capability.

- Determine the loss profile between circuits that are to be muxed or demuxed.
- Provide clean impedance and electrical length matched board traces.
- Provide a control signal for the SEL and OEn pins.
- Provide good ground connection to the board ground plane.
- See the application schematics for the recommended decoupling capacitors from VCC pins to ground.

8.2.1.3 Application Curves

Figure 8-2 and Figure 8-3 show eye diagrams for USB 2.0 signals through calibration traces (without device) and TMUXHS221LV channel. A combination of very low channel ON resistance, high bandwidth, very low reflection (return loss), and low added jitter from the device allows 480Mbps USB 2.0 HS signals to remain unattenuated. Many system platforms struggle to pass USB 2.0 compliance due to high loss. TMUXHS221LV allows insertion of an analog mux device in the signal path without creating any additional signal integrity issues.

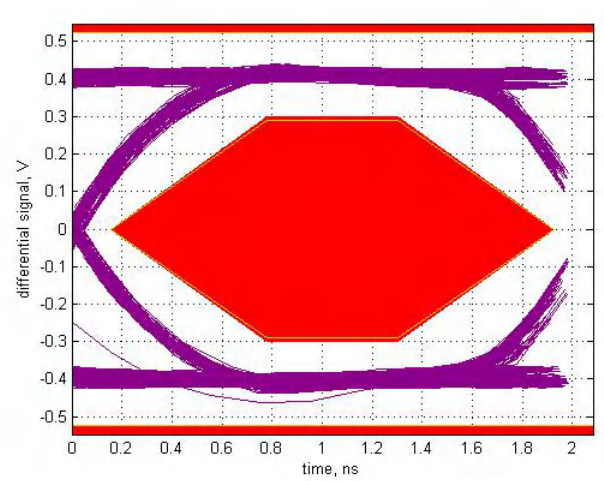


Figure 8-2. USB 2.0 HS Compliance Eye in TI Evaluation Board – Through Calibration Traces

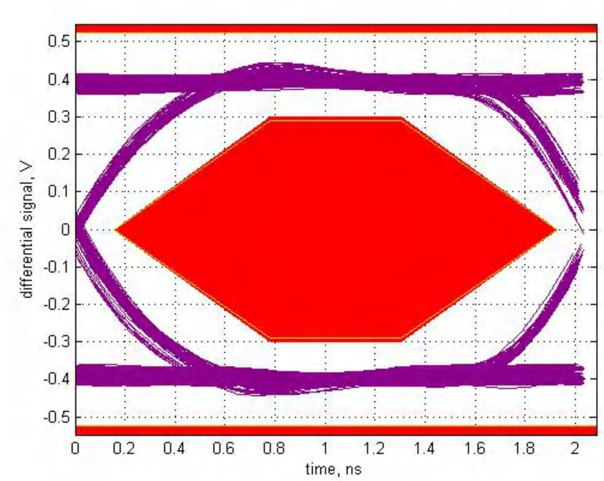


Figure 8-3. USB 2.0 HS Compliance Eye in TI Evaluation Board – Through TMUXHS221LV Channel

8.2.2 Systems Examples

8.2.2.1 PCIe Clock Muxing

Figure 8-4 shows an application where TMUXHS221LV is used to switch the PCIe clock. The device is measured in a TI evaluation board with an available clock source to show an added jitter less than 10 fs for all NOISE_FOLD and PCIe 5.0 CK filter versions, which is well below PCIe 5.0 clock specifications.

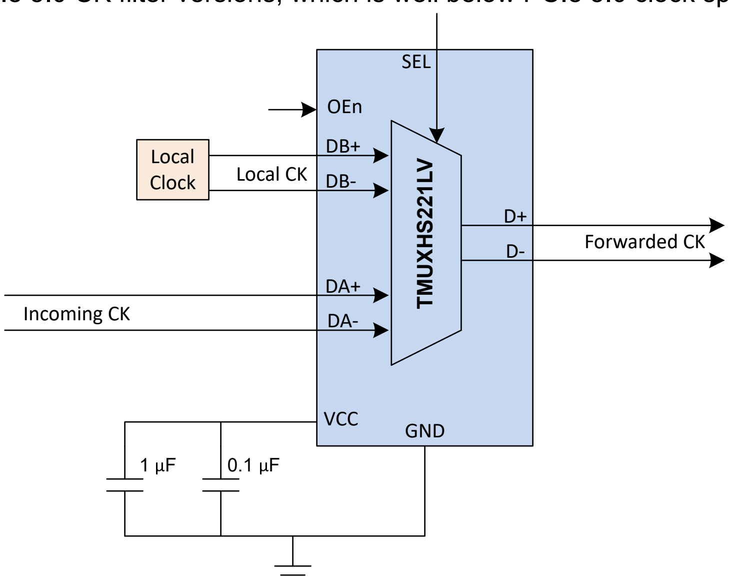


Figure 8-4. PCIe Clock Muxing

8.2.2.2 USB-C SBU Muxing

Figure 8-5 shows an application block diagram that implements SBU cross-muxing in a USB Type-C interface for implementing DisplayPort (DP) Alternate mode using the TMUXHS221LV. Note that the device has adequate bandwidth to support fast Auxiliary (AUX) signals. It is also capable of handling asymmetric biasing for DP AUX signals.

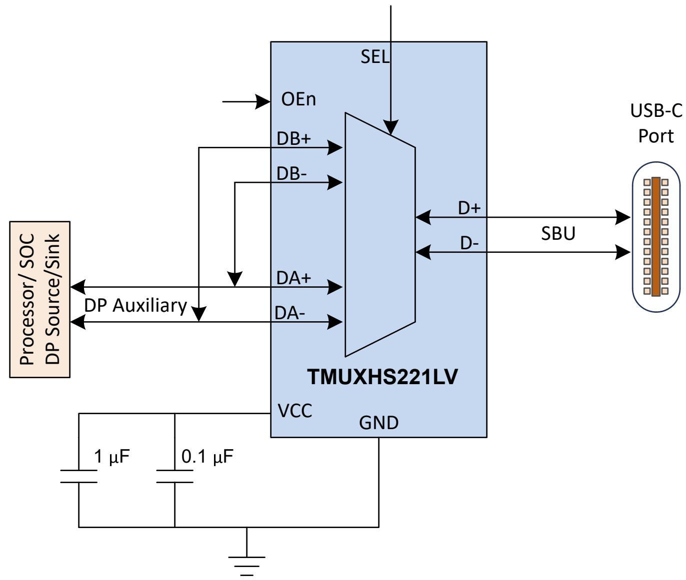


Figure 8-5. USB Type-C SBU Signals Muxing

8.2.2.3 Switching USB Port

Figure 8-6 shows an application block diagram where TMUXHS221LV is used to switch the USB port in between a hand-held portable device and its connected dock.

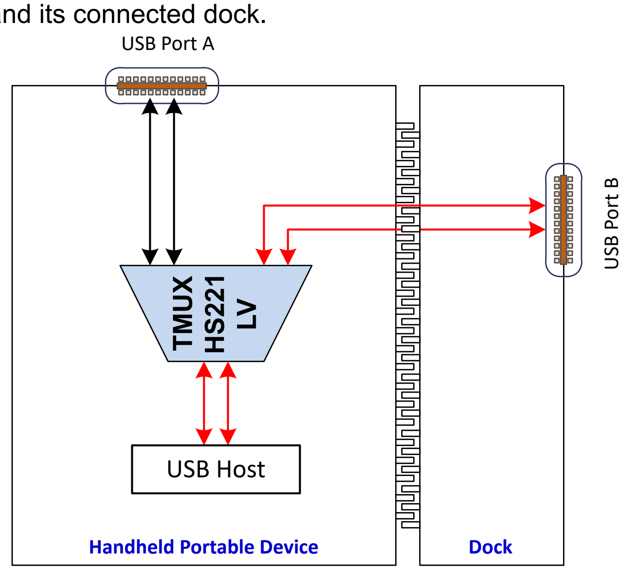


Figure 8-6. Switching USB Port

8.3 Power Supply Recommendations

The TMUXHS221LV does not require a power supply sequence. However, TI recommends to enable the device after VCC is stable and within specification. TI also recommends to place ample decoupling capacitors at the device VCC near the pin.

8.4 Layout

8.4.1 Layout Guidelines

A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In the layout, the impedance of D+ and D– traces should match the cable characteristic differential impedance for optimal performance. The high-speed D+/D– traces should always be matched and must be no more than 4 inches, otherwise the eye diagram performance may be degraded.

- Place supply bypass capacitors as close to the VCC pin as possible.
- Avoid placing the bypass capacitors near the D+/D–traces.
- Route the high-speed USB signals using a minimum of vias and corners which will reduce signal reflections and impedance changes. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. When a via must be used, increase the clearance size around it to minimize its capacitance.
- Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
- When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
- Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices, or ICs that use or duplicate clock signals.
- Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.
- Route all high-speed USB signal traces over continuous planes (VCC or GND) with no interruptions.
- Avoid crossing over anti-etch, commonly found with plane split.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* application note.

8.4.2 Layout Example

Figure 8-7 shows a TMUXHS221LV layout example.

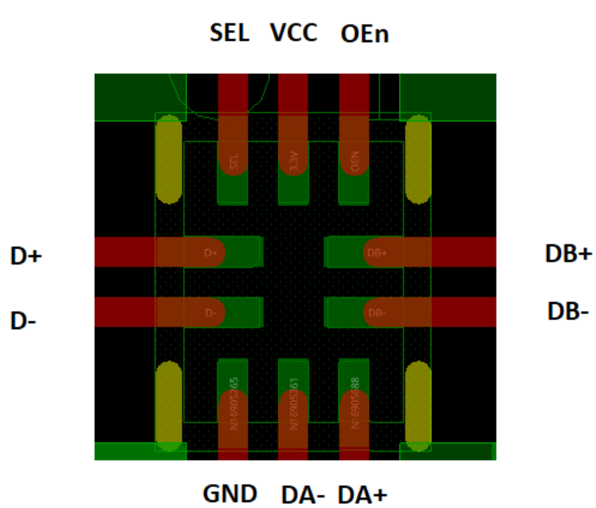


Figure 8-7. TMUXHS221LV Layout Example

9 Device and Documentation Support

9.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs* application note

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUXHS221LVNKGR	ACTIVE	UQFN	NKG	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21L	Samples
TMUXHS221LVNKGT	ACTIVE	UQFN	NKG	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	21L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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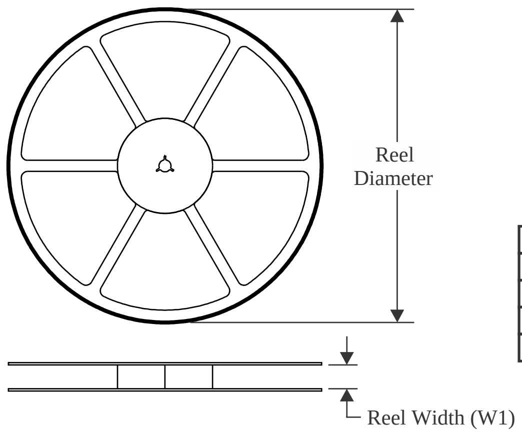
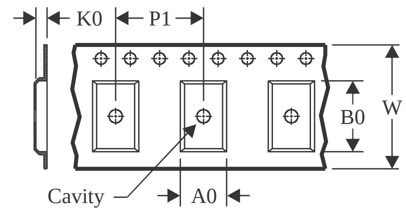
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

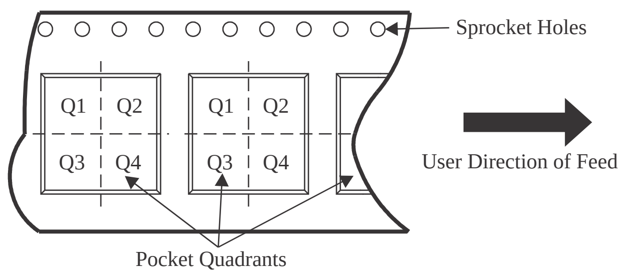


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

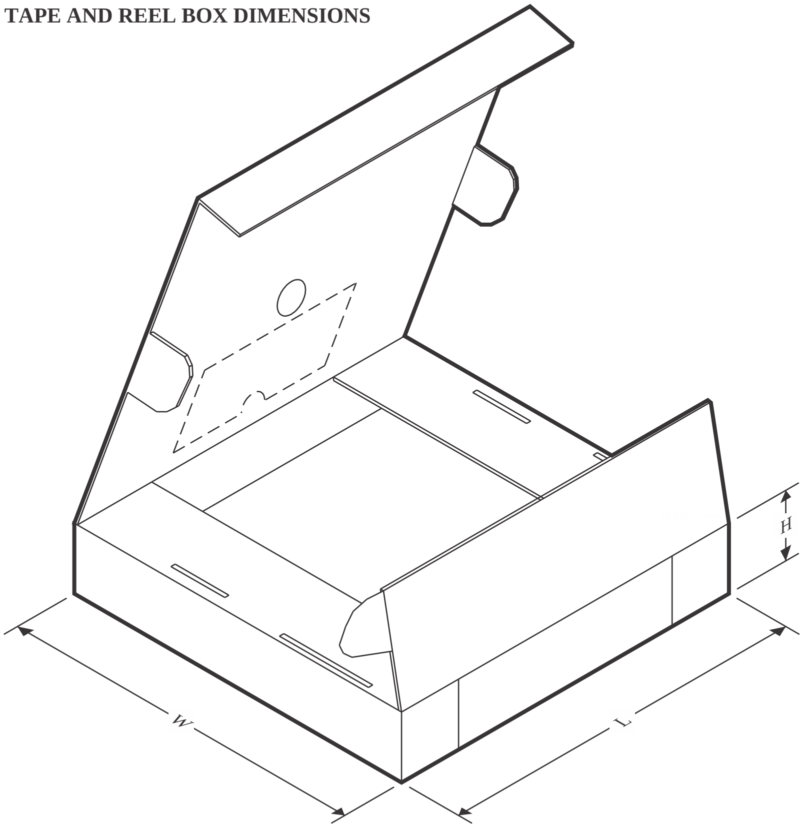
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUXHS221LVNKGR	UQFN	NKG	10	3000	180.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1
TMUXHS221LVNKGT	UQFN	NKG	10	250	180.0	8.4	1.7	2.1	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



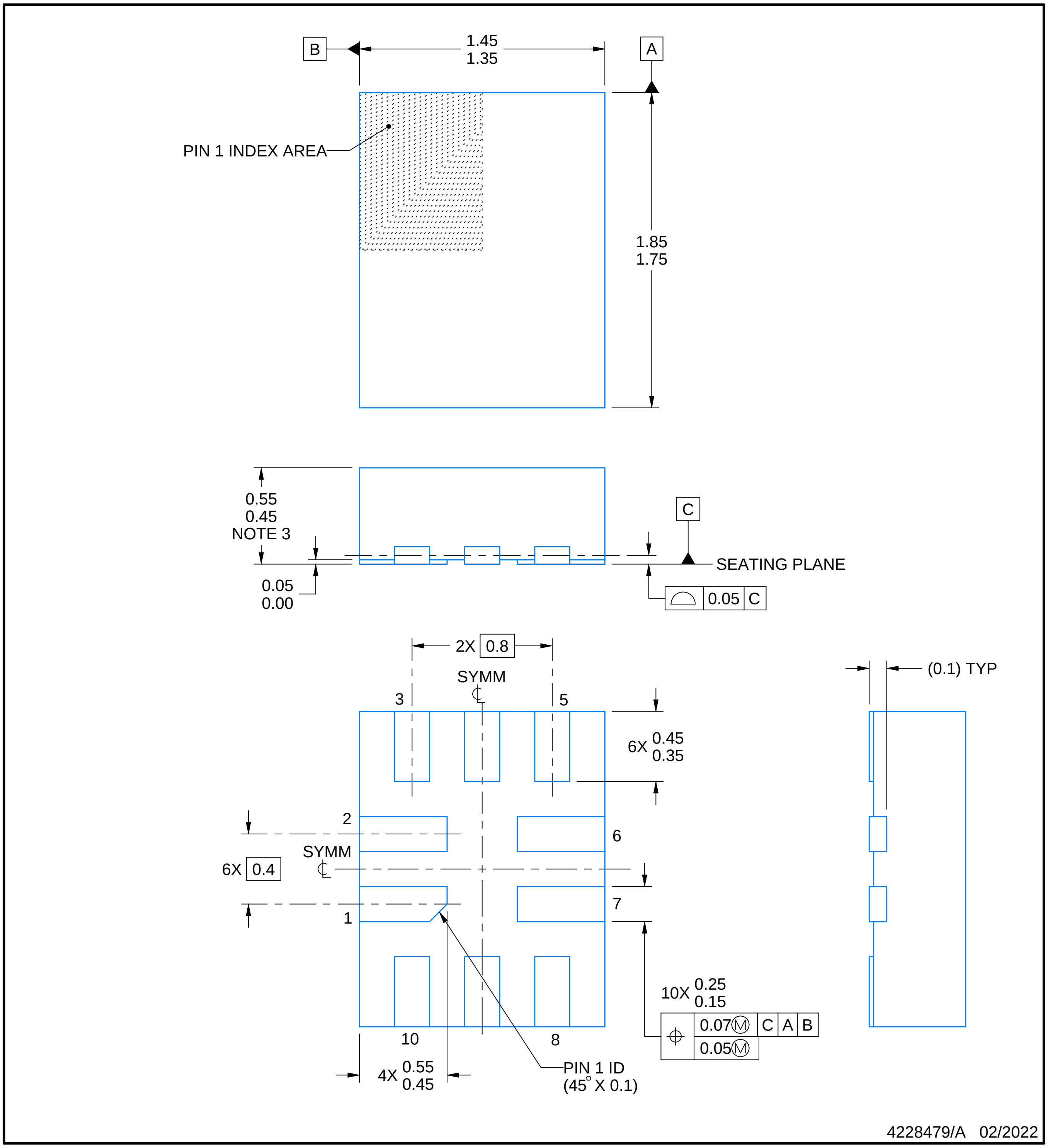
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUXHS221LVNKGR	UQFN	NKG	10	3000	210.0	185.0	35.0
TMUXHS221LVNKGT	UQFN	NKG	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

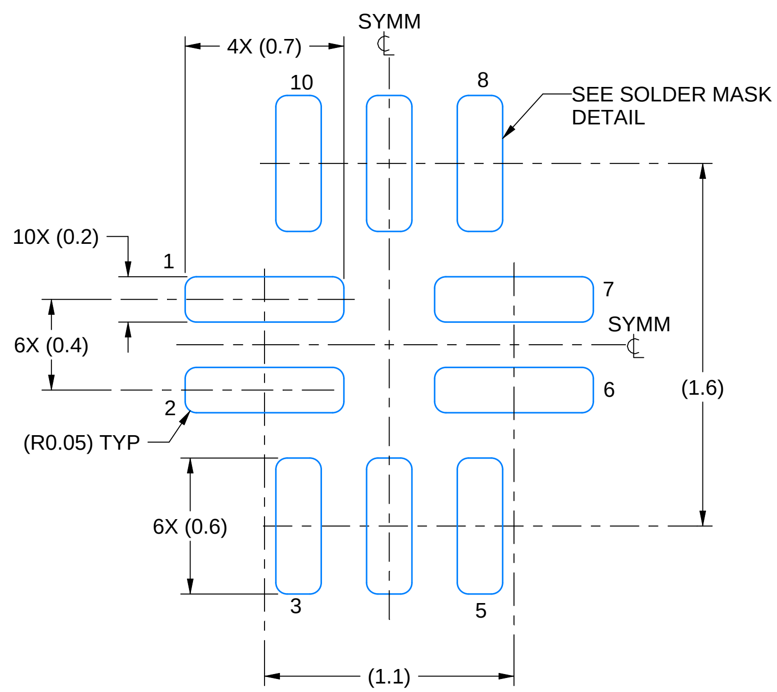
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

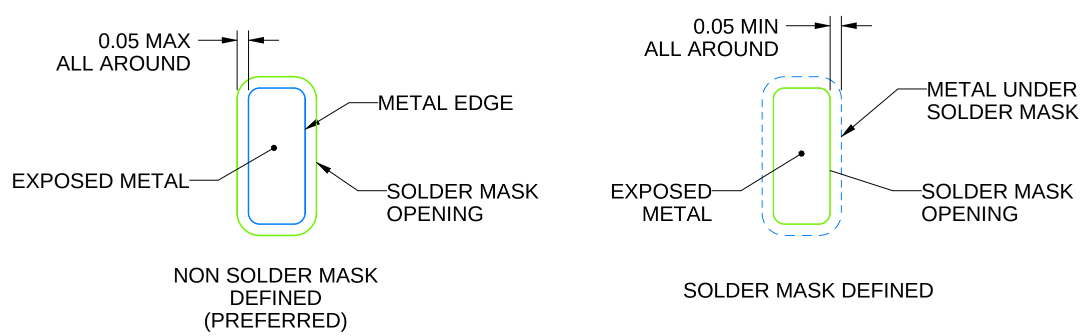


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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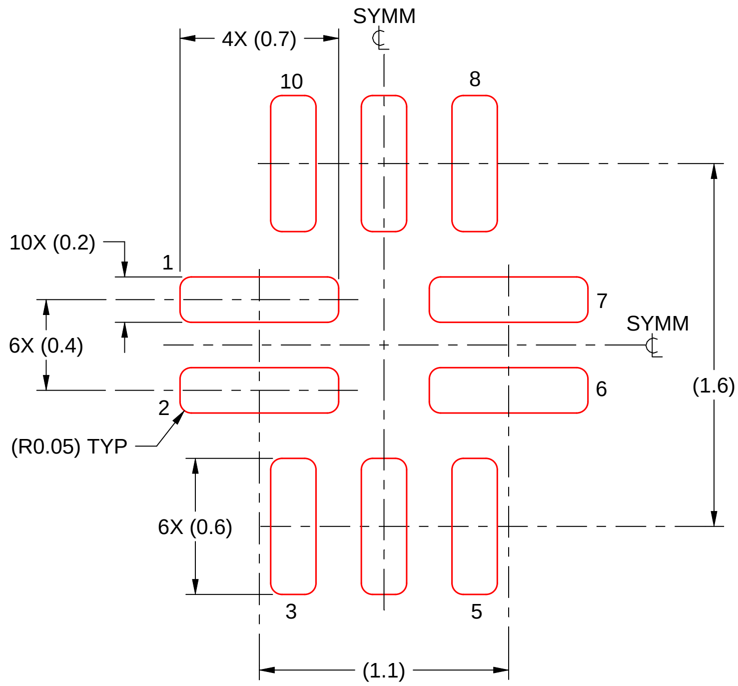
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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