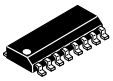
Analog Multiplexer/ Demultiplexer

High−Performance Silicon−Gate CMOS

MC74LVX4051, MC74LVX4052, MC74LVX4053, MC74LVXT4051, MC74LVXT4052, MC74LVXT4053

QFN16
MN SUFFIX
CASE 485AW

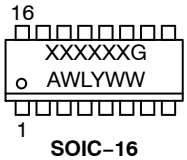


SOIC−16
D SUFFIX
CASE 751B

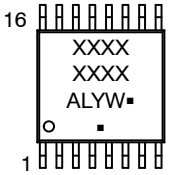
TSSOP−16
DT SUFFIX
CASE 948F

MARKING DIAGRAMS

QFN16



SOIC−16



TSSOP−16

XXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

These devices utilize silicon−gate CMOS technology to achieve fast propagation delays, low ON resistances, and low leakage currents. This analog multiplexer/demultiplexer controls analog voltages that may vary across the complete power supply range (from V_{CC} to V_{EE}).

The devices are similar in pinout to the LVX805n, the HC405nA, and the metal−gate MC1405nB. The Channel−Select inputs determine which one of the Analog Inputs/Outputs is to be connected, by means of an analog switch, to the Common Output/Input. When the Enable pin is HIGH, all analog switches are turned off.

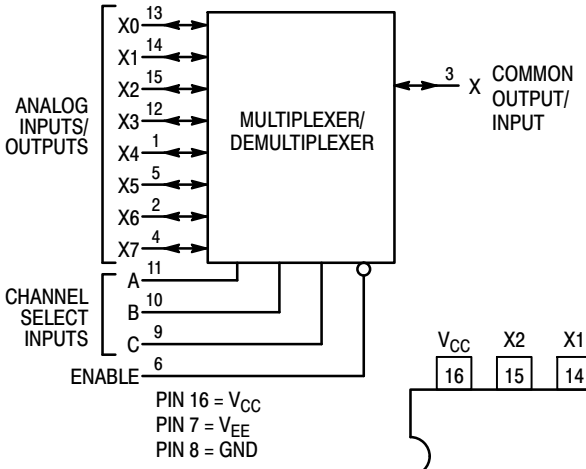
The Channel−Select and Enable inputs are compatible with standard CMOS outputs. These inputs are overvoltage tolerant (OVT) for level translation from 6.0 V down to 3.0 V.

This device has been designed so the ON resistance (R_{ON}) is more linear over input voltage than the R_{ON} of metal−gate CMOS analog switches and High−Speed CMOS analog switches.

Features

- Fast Switching and Propagation Speeds
- Low Crosstalk Between Switches
- Analog Power Supply Range ($V_{CC} - V_{EE}$) = −3.0 V to +3.0 V
- Digital (Control) Power Supply Range (V_{CC} − GND) = 2.5 to 6.0 V
- Improved Linearity and Lower ON Resistance Than Metal−Gate, HSL, or VHC Counterparts
- Low Noise
- Designed to Operate on a Single Supply with V_{EE} = GND, or Using Split Supplies up to ±3.0 V
- Break−Before−Make Circuitry
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM
4051
Single−Pole, 8−Position Plus Common Off

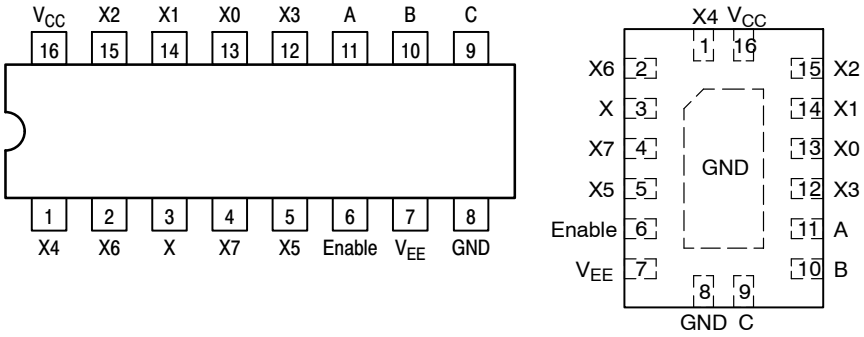


FUNCTION TABLE − 4051

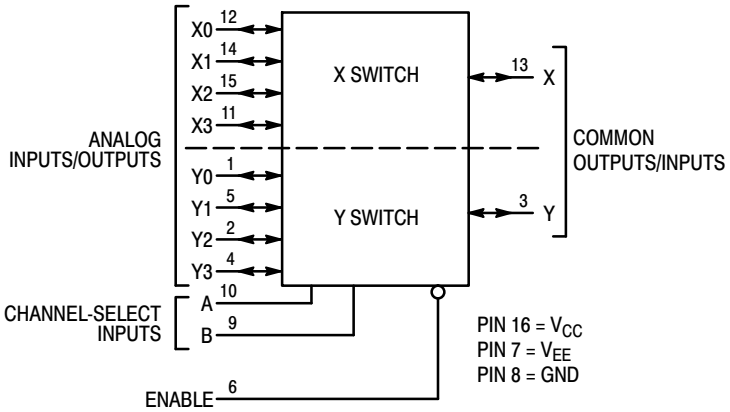
Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

X = Don't Care

Pinouts: 4051 (Top View)



LOGIC DIAGRAM
4052
Double−Pole, 4−Position Plus Common Off

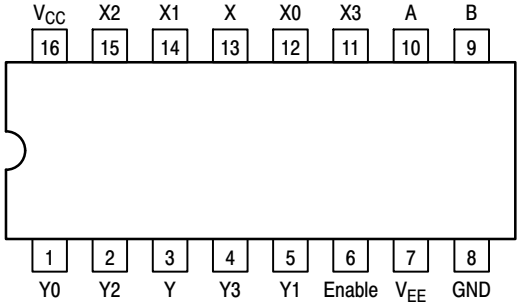


FUNCTION TABLE − 4052

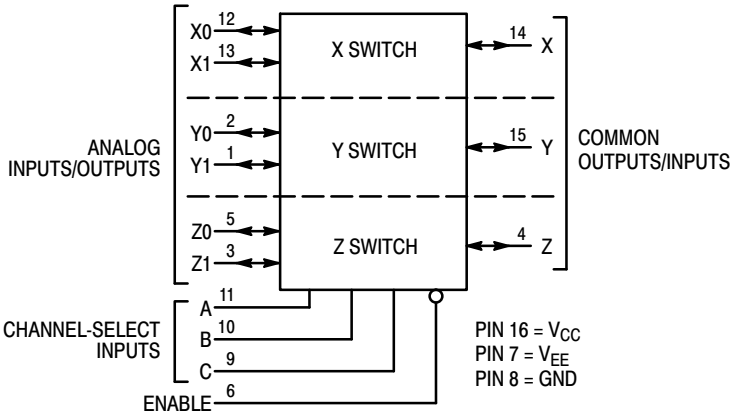
Control Inputs			
	Select		
Enable	B	A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

Pinout: 4052 (Top View)



LOGIC DIAGRAM
4053
Triple Single−Pole, Double−Position Plus Common Off



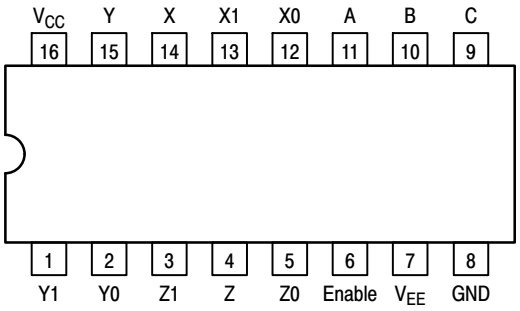
NOTE: This device allows independent control of each switch. Channel−Select Input A controls the X−Switch, Input B controls the Y−Switch and Input C controls the Z−Switch

FUNCTION TABLE − 4053

Control Inputs						
Enable	Select C	Select B	Select A	ON Channels		
L	L	L	L	Z0	Y0	X0
L	L	L	H	Z0	Y0	X1
L	L	H	L	Z0	Y1	X0
L	L	H	H	Z0	Y1	X1
L	H	L	L	Z1	Y0	X0
L	H	L	H	Z1	Y0	X1
L	H	H	L	Z1	Y1	X0
L	H	H	H	Z1	Y1	X1
H	X	X	X	NONE		

X = Don't Care

Pinout: 4053 (Top View)



MAXIMUM RATINGS (Voltages referenced to GND unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{CC}	Positive DC Supply Voltage		−0.5 to +6.5	V
$V_{CC} - V_{EE}$	DC Supply Voltage		−0.5 to +6.5	V
V_{IS}	Analog Input Voltage		V_{EE}−0.5 to V_{CC}+0.5	V
V_{IN}	Digital Input Voltage	(Referenced to V_{EE})	−0.5 to +6.5	V
I	DC Current, into or out of any pin		±50	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		+260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 30% to 35%	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 2000 > 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to GND unless otherwise specified)

Symbol	Parameter		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		2.5	6.0	V
V_{EE}	Negative DC Supply Voltage		−3.5	GND	V
$V_{CC} - V_{EE}$	DC Supply Voltage		2.5	6.0	V
V_{IS}	Analog Input Voltage		V_{EE}	V_{CC}	V
V_{IN}	Digital Input Voltage	(Note 3) (Referenced to V_{EE})	0	6.0	V
T_A	Operating Temperature Range		−55	+125	°C
t_r, t_f	Input Transition Rise or Fall Time (Channel Select or Enable Inputs)	V_{CC} = 3.0 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
MC74LVX							
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs		2.5 3.0 4.5 6.0	1.90 2.10 3.15 4.2	1.90 2.10 3.15 4.2	1.90 2.10 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs		2.5 3.0 4.5 6.0	0.6 0.9 1.35 1.8	0.6 0.9 1.35 1.8	0.6 0.9 1.35 1.8	V
I_{IN}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{IN} = 6.0 or GND	0 V to 6.0 V	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND	6.0	4.0	40	80	μA
MC74LVXT							
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs		3.0 4.5 5.5	2.0 2.0 2.0	2.0 3.15 4.2	2.0 3.15 4.2	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs		3.0 4.5 6.0	0.9 1.35 1.8	0.9 1.35 1.8	0.9 1.35 1.8	V
I_{IN}	Maximum Input Leakage Current, Channel–Select or Enable Inputs	V_{IN} = 6.0 or GND	0 V to 6.0 V	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	Channel Select, Enable and V_{IS} = V_{CC} or GND	6.0	4.0	40	80	μA

DC ELECTRICAL CHARACTERISTICS – Analog Section

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit			Unit
					–55 to 25°C	≤85°C	≤125°C	
R_{ON}	Maximum “ON” Resistance	V_{IN} = V_{IL} or V_{IH} V_{IS} = ½ (V_{CC} + V_{EE}) $\|I_S\|$ = 2.0 mA (Figure 1)	3.0 4.5 3.0	0 0 –3.0	86 37 26	108 46 33	120 55 37	Ω
ΔR_{ON}	Maximum Difference in “ON” Resistance Between Any Two Channels in the Same Package	V_{IN} = V_{IL} or V_{IH} V_{IS} = ½ (V_{CC} + V_{EE}) $\|I_S\|$ = 2.0 mA	3.0 4.5 3.0	0 0 –3.0	15 13 10	20 18 15	20 18 15	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or V_{EE}; Switch Off (Figure 2)	5.5 +3.0	0 –3.0	0.1 0.1	0.5 0.5	1.0 1.0	μA
	Maximum Off–Channel Leakage Current, Common Channel	V_{in} = V_{IL} or V_{IH}; V_{IO} = V_{CC} or V_{EE}; Switch Off (Figure 3)	5.5 +3.0	0 –3.0	0.2 0.2	2.0 2.0	4.0 4.0	
I_{on}	Maximum On–Channel Leakage Current, Channel–to–Channel	V_{in} = V_{IL} or V_{IH}; Switch–to–Switch = V_{CC} or V_{EE}; (Figure 4)	5.5 +3.0	0 –3.0	0.2 0.2	2.0 2.0	4.0 4.0	μA

AC CHARACTERISTICS (Input t_r = t_f = 3 ns)

Symbol	Parameter	Test Conditions	V_{CC} V	V_{EE} V	Guaranteed Limit				Unit
					–55 to 25°C		≤85°C	≤125°C	
					Min	Typ*			
t_{BBM}	Minimum Break–Before–Make Time	V_{IN} = V_{IL} or V_{IH} V_{IS} = V_{CC} R_L = 300 Ω, C_L = 35 pF (Figures 9 and 10)	3.0 4.5 3.0	0.0 0.0 — 3.0	1.0 1.0 1.0	6.5 5.0 3.5	– – –	– – –	ns

*Typical Characteristics are at 25°C.

AC CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 3 ns)

Symbol	Parameter	V_{CC} V	V_{EE} V	Guaranteed Limit							Unit
				−55 to 25°C			≤85°C		≤125°C		
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Channel−Select to Analog Output (Figures 11 and 12)	2.5 3.0 4.5 3.0	0 0 0 −3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Enable to Analog Output (Figures 13 and 14)	2.5 3.0 4.5 3.0	0 0 0 −3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Enable to Analog Output (Figures 13 and 14)	2.5 3.0 4.5 3.0	0 0 0 −3.0			40 28 23 23		45 30 25 25		50 35 30 28	ns

			Typical @ 25°C, V_{CC} = 5.0 V, V_{EE} = 0 V	
C_{PD}	Power Dissipation Capacitance (Figure 15) (Note 4)		45	pF
C_{IN}	Maximum Input Capacitance, Channel−Select or Enable Inputs		10	pF
$C_{I/O}$	Maximum Capacitance (All Switches Off)	Analog I/O	10	pF
		Common O/I	10	
		Feedthrough	1.0	

4. Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

ADDITIONAL APPLICATION CHARACTERISTICS (GND = 0 V)

Symbol	Parameter	Condition	V_{CC} V	V_{EE} V	Typ 25°C	Unit
BW	Maximum On−Channel Bandwidth or Minimum Frequency Response	(Figure 5)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 −3.0	80 80 80 80	MHz
V_{ISO}	Off−Channel Feedthrough Isolation	(Figure 6)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 −3.0	−70 −70 −70 −70	dB
V_{ONL}	Maximum Feedthrough On Loss	(Figure 7)	3.0 4.5 6.0 3.0	0.0 0.0 0.0 −3.0	−2 −2 −2 −2	dB
Q	Charge Injection	(Figure 8)	5.0 3.0	0.0 −3.0	9.0 12	pC
THD	Total Harmonic Distortion + Noise	f_{IS} = 1 MHz, R_L = 10 KΩ, C_L = 50 pF, V_{IS} = 5.0 V_{PP} sine wave + DC Bias V_{IS} = 6.0 V_{PP} sine wave + DC Bias (Figure 16)	 6.0 3.0	 0.0 −3.0	 0.10 0.05	%

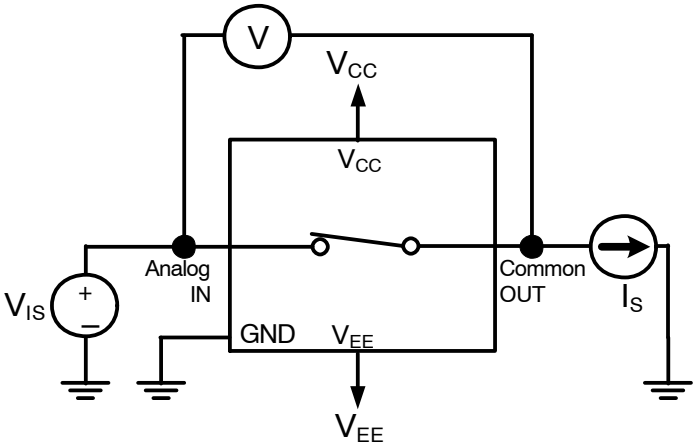


Figure 1. On Resistance

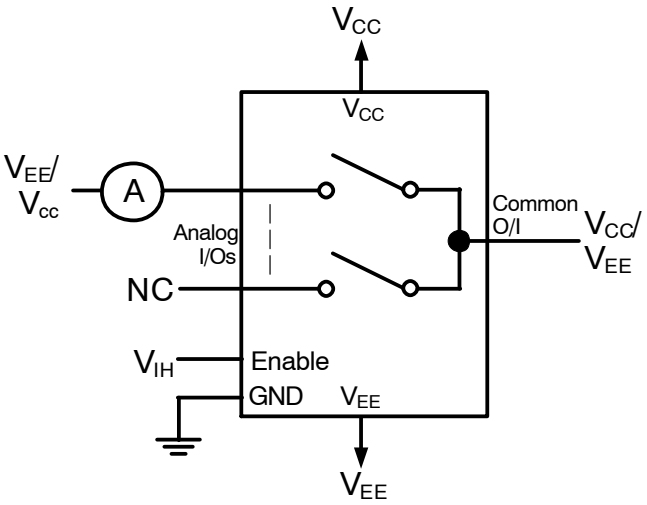


Figure 2. Off Channel Leakage, Any One Channel

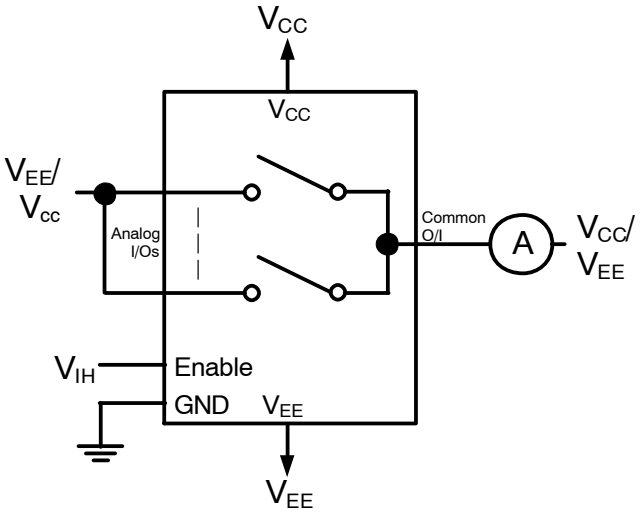


Figure 3. Off Channel Leakage, Common Channel

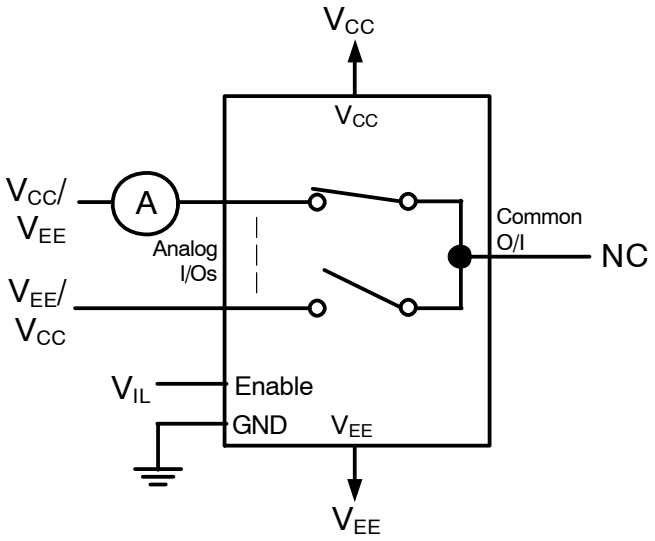
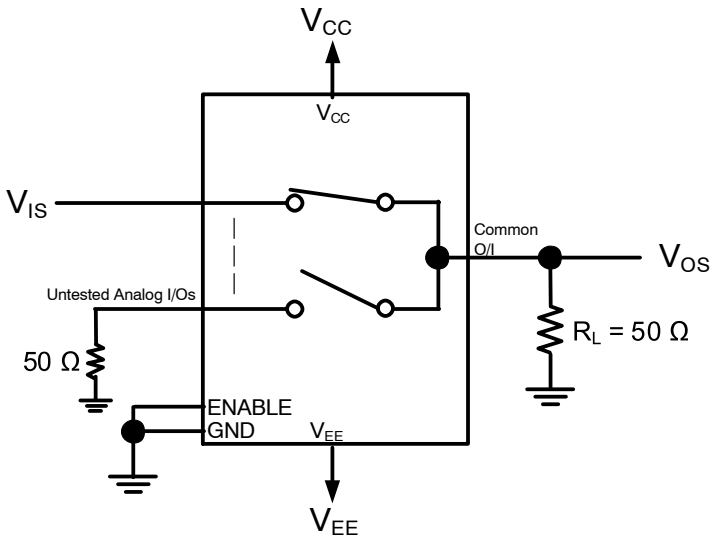
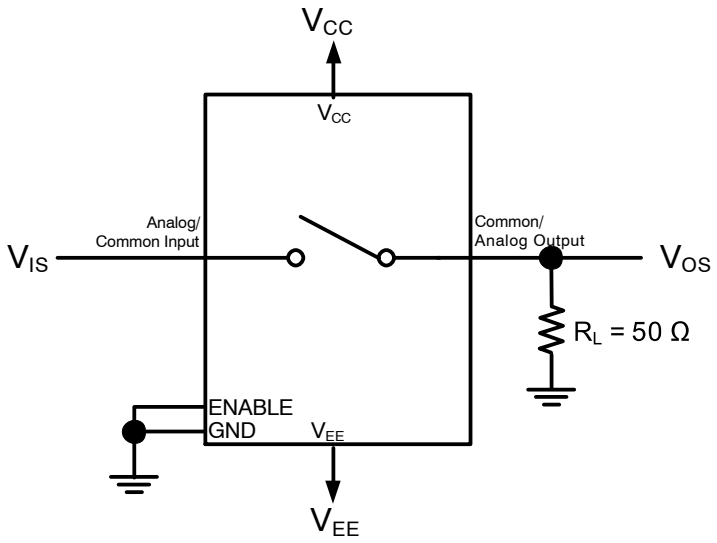


Figure 4. On Channel Leakage



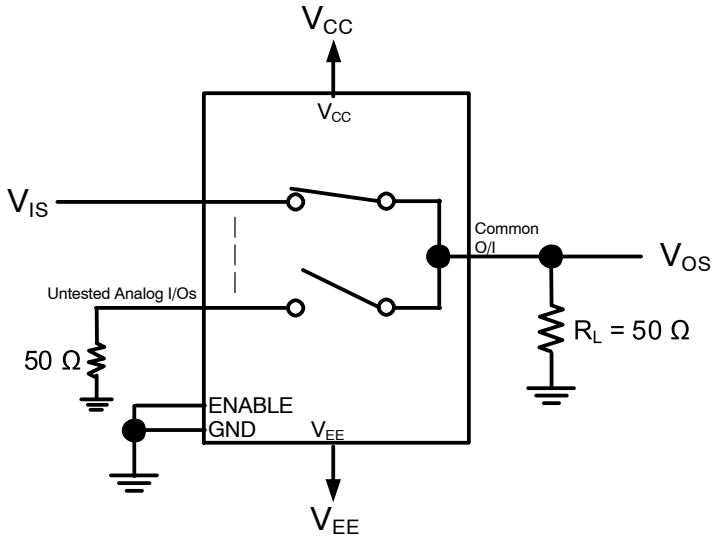
DC Bias = $(V_{CC} + V_{EE})/2$
V_{IS} = sine wave + DC Bias
(1) Adjust V_{IS} Amplitude for 0 dBm at V_{OS}
(2) Increase f_{IS} until V_{OS} at −3 dB of step 1

Figure 5. Bandwidth



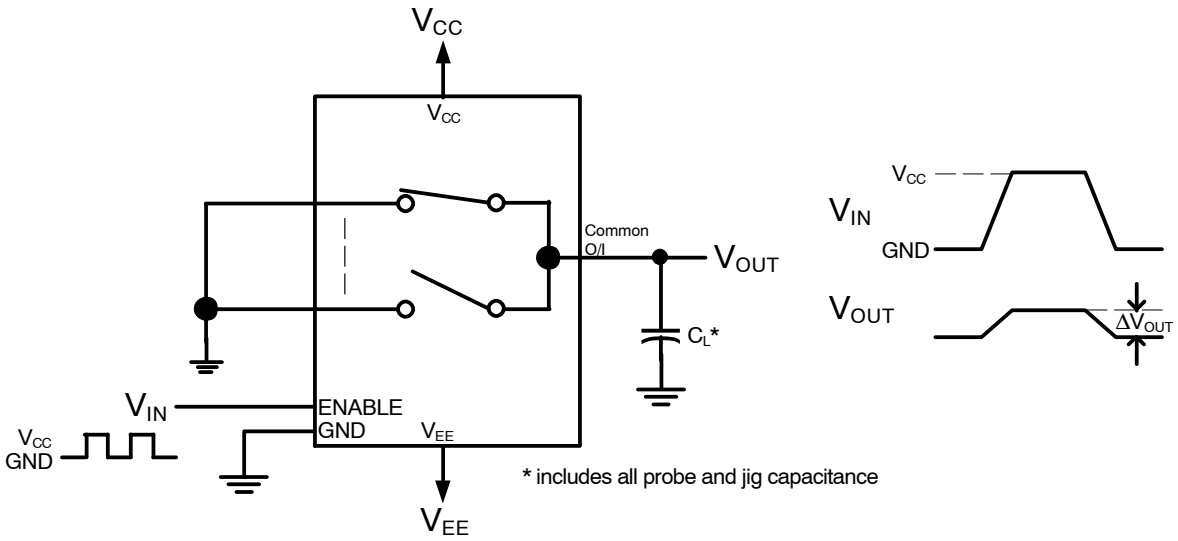
f = 1 MHz
DC Bias = $(V_{CC} + V_{EE})/2$
V_{IS} = sine wave + DC Bias
(1) Adjust V_{IS} Amplitude to 10 dBm
(2) V_{ISO}(dB) = 20 log (V_{OS}/V_{IS})

Figure 6. Common/Off Channel Feedthrough Isolation



f_{IS} = 1 kHz
DC Bias = $(V_{CC} + V_{EE})/2$
V_{IS} = sine wave + DC Bias
(1) Adjust V_{IS} Amplitude to 0 dBm
(2) V_{ONL}(dB) = 20 log (V_{OS}/V_{IS})

Figure 7. On Channel Feedthrough On Loss



f_{IN} = 1 kHz, input $t_R = t_F$ = 3 ns
C_L = 1000 pF
$Q = C_L \times \Delta V_{OUT}$

Figure 8. Charge Injection

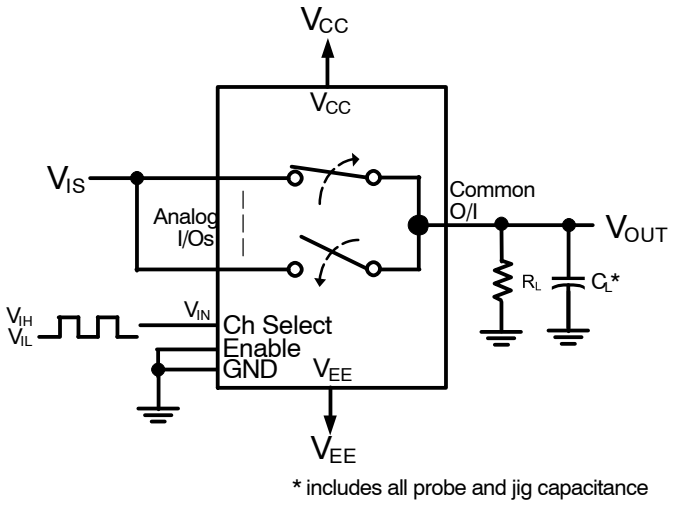


Figure 9. Break−Before−Make

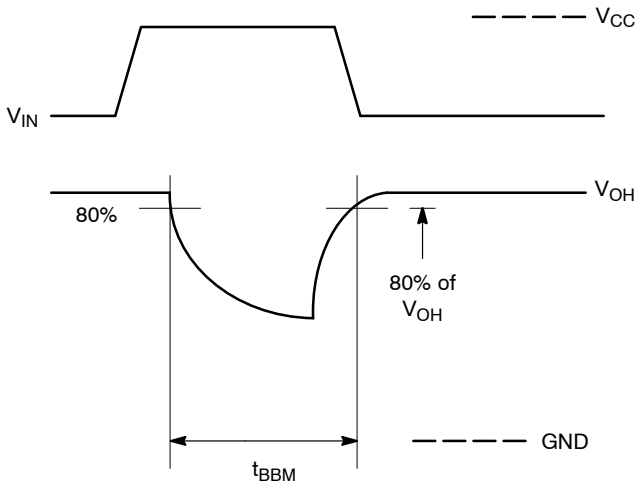


Figure 10. Break−Before−Make Time

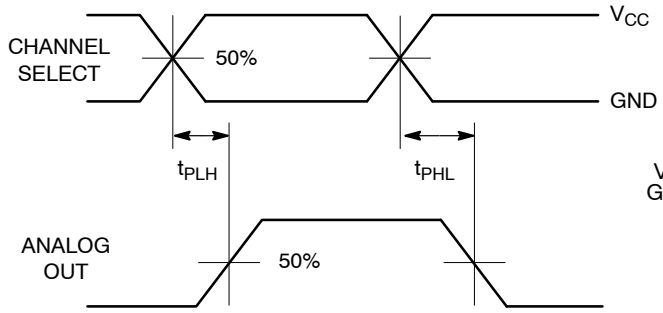


Figure 11. Propagation Delays, Channel Select to Analog Out

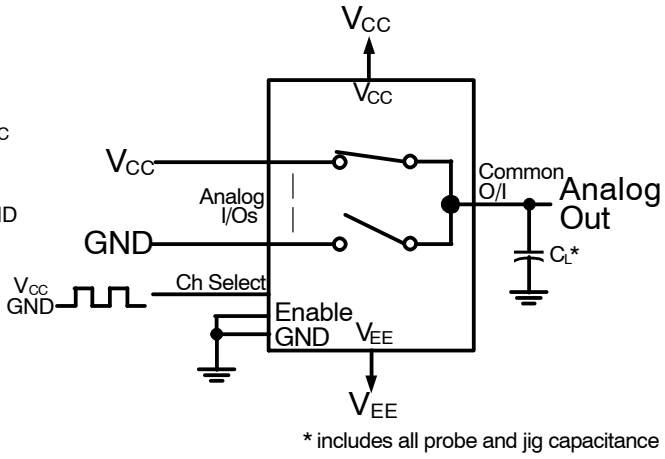


Figure 12. Propagation Delay, Select to Analog Out

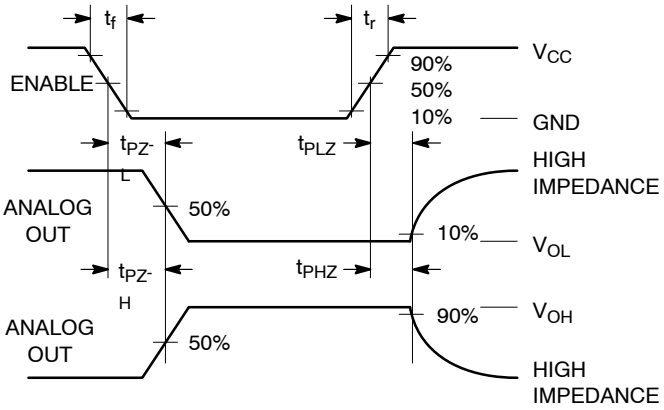


Figure 13. Propagation Delays, Enable to Analog Out

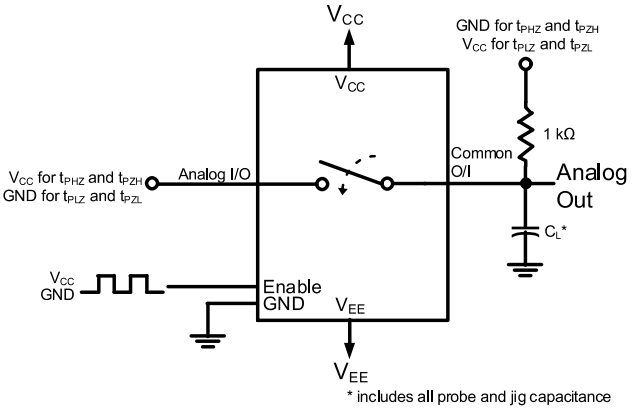


Figure 14. Propagation Delay, Enable to Analog Out

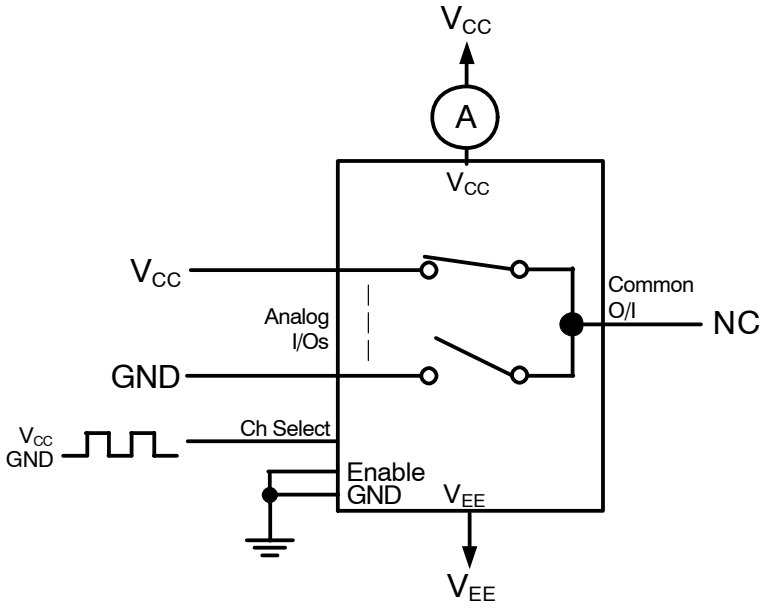
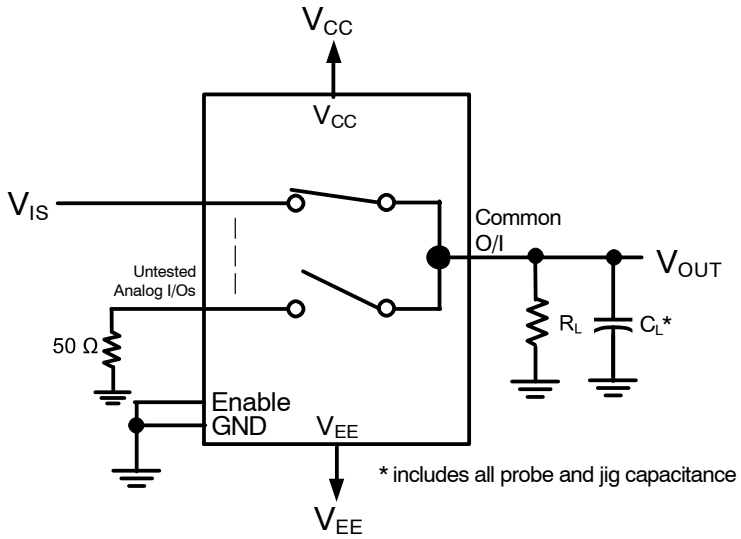


Figure 15. Power Dissipation Capacitance



DC Bias = $(V_{CC} + V_{EE})/2$

Figure 16. Total Harmonic Distortion

APPLICATIONS INFORMATION

The Channel Select and Enable control pins should be at V_{CC} or GND logic levels. V_{CC} being recognized as a logic high and GND being recognized as a logic low. In this example:

$$V_{CC} = +5\ V = \text{logic high}$$
$$GND = 0\ V = \text{logic low}$$

The maximum analog voltage swing is determined by the supply voltages V_{CC} and V_{EE}. The positive peak analog voltage should not exceed V_{CC}. Similarly, the negative peak analog voltage should not go below V_{EE}. In this example, the difference between V_{CC} and V_{EE} is five volts. Therefore, using the configuration of Figure 18, a maximum analog signal of five volts peak−to−peak can be controlled. Unused analog inputs/outputs may be left floating (i.e., not connected). However, tying unused analog inputs and outputs to V_{CC} or GND through a low value resistor helps minimize crosstalk and feedthrough noise that may be picked up by an unused switch.

Although used here, balanced supplies are not a requirement. The only constraints on the power supplies are that:

$$V_{EE} - GND = 0 \text{ to } -3.5 \text{ volts}$$
$$V_{CC} - GND = 2.5 \text{ to } 6 \text{ volts}$$
$$V_{CC} - V_{EE} = 2.5 \text{ to } 6 \text{ volts}$$
$$\text{and } V_{EE} \leq GND$$

When voltage transients above V_{CC} and/or below V_{EE} are anticipated on the analog channels, external Germanium or Schottky diodes (D_x) are recommended as shown in Figure 19. These diodes should be able to absorb the maximum anticipated current surges during clipping.

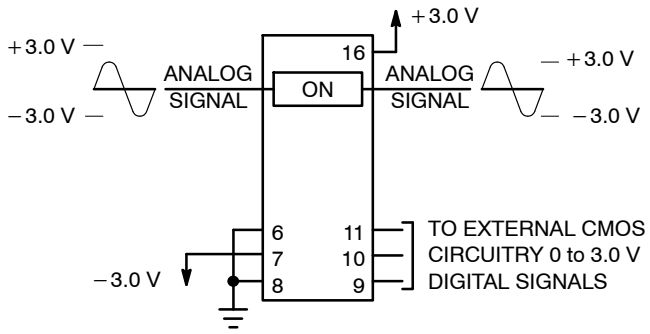


Figure 17. Application Example

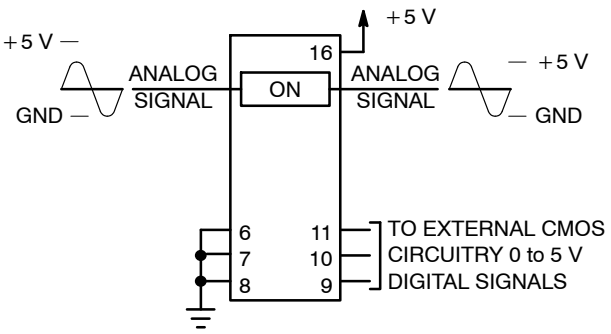


Figure 18. Application Example

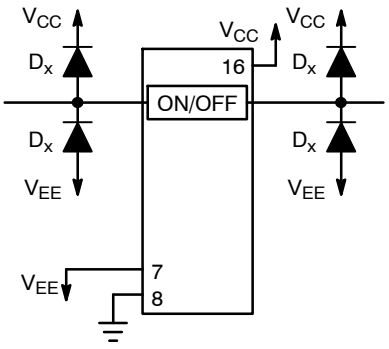


Figure 19. External Germanium or Schottky Clipping Diodes

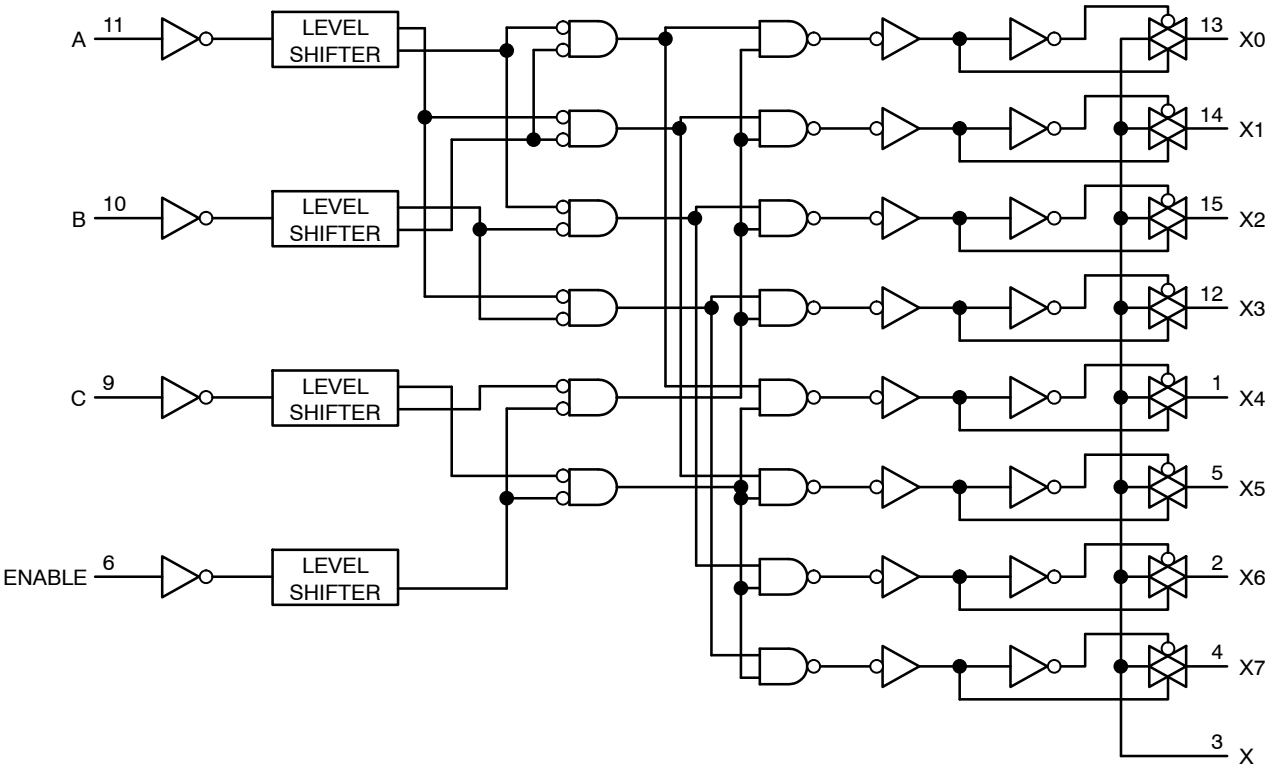


Figure 20. Function Diagram, 4051

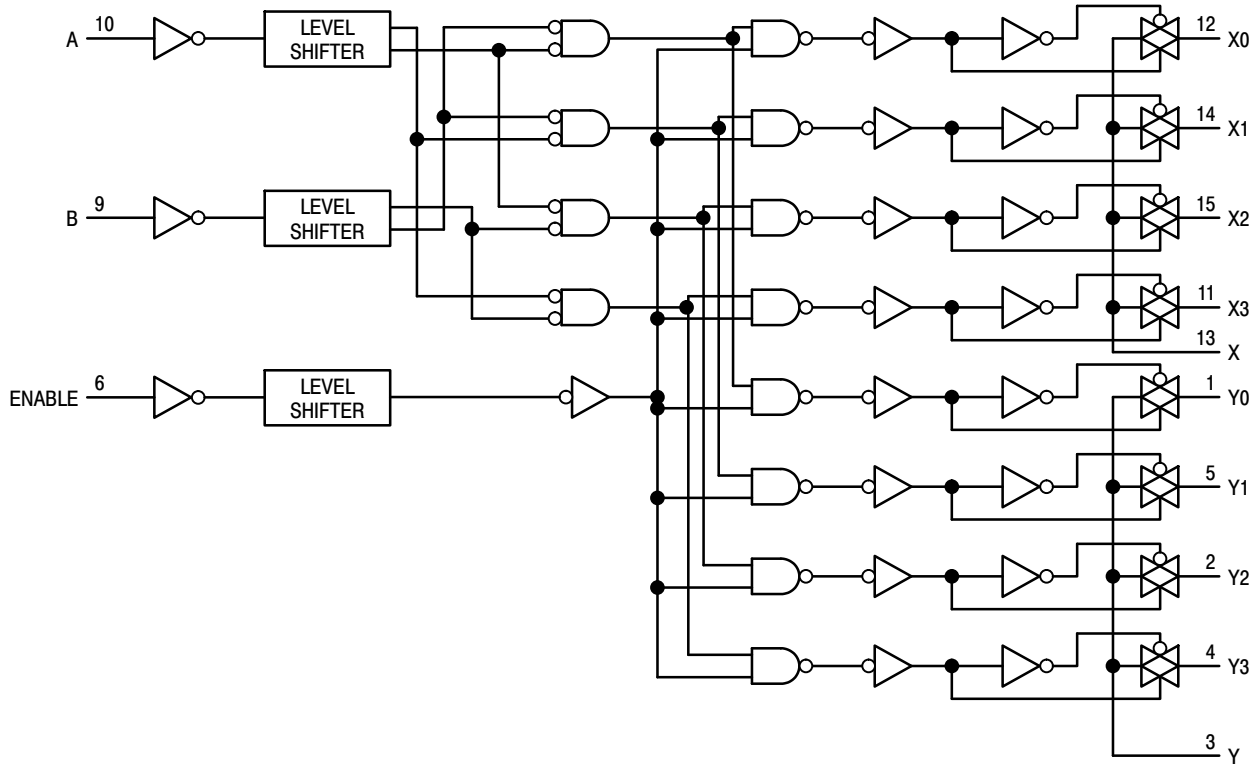


Figure 21. Function Diagram, 4052

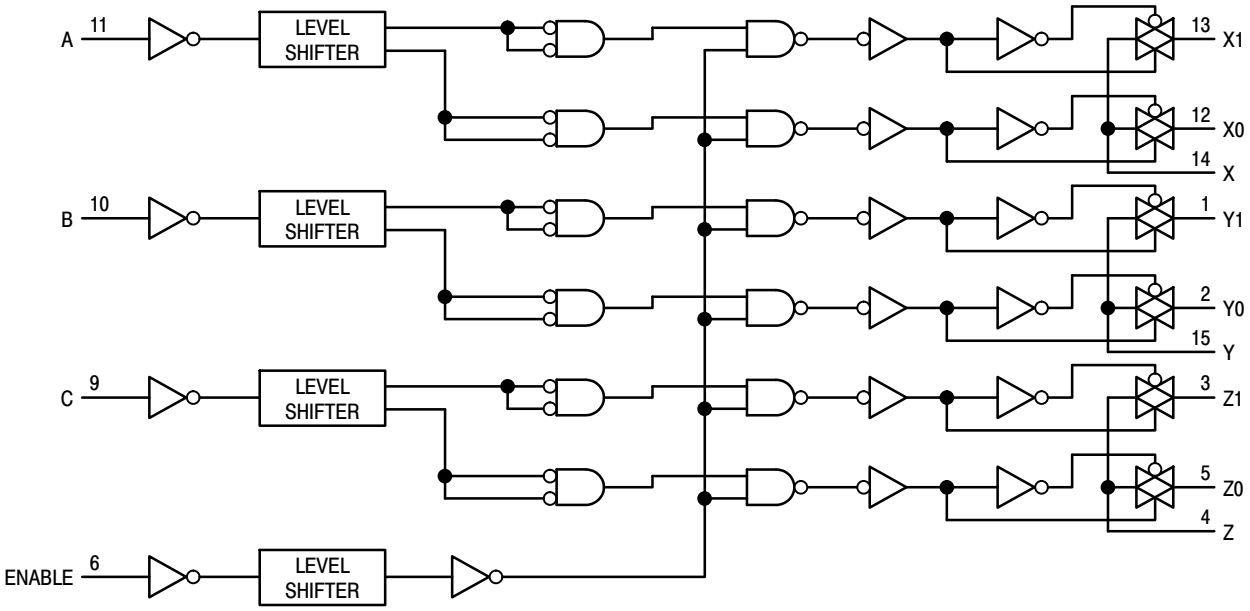


Figure 22. Function Diagram, 4053

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74LVX4051DG	LVX4051G	SOIC−16	48 Units / Rail
MC74LVX4051DR2G	LVX4051G	SOIC−16	2500 / Tape & Reel
MC74LVX4051DTG	LVX 4051	TSSOP−16	96 Units / Rail
MC74LVX4051DTR2G	LVX 4051	TSSOP−16	2500 / Tape & Reel
MC74LVX4051MNTWG	4051	QFN−16	3000 / Tape & Reel (8mm pitch carrier tape)
MC74LVX4052DG	LVX4052G	SOIC−16	48 Units / Rail
MC74LVX4052DR2G	LVX4052G	SOIC−16	2500 / Tape & Reel
MC74LVX4052DTR2G	LVX 4052	TSSOP−16	2500 / Tape & Reel
MC74LVX4052DTR2G−Q*	LVX 4052	TSSOP−16	2500 / Tape & Reel
MC74LVX4053DG	LVX4053G	SOIC−16	48 Units / Rail
MC74LVX4053DTG	LVX 4053	TSSOP−16	96 Units / Rail
MC74LVXT4051DR2G	LVXT4051G	SOIC−16	2500 / Tape & Reel
MC74LVXT4051DTR2G	LVXT 4051	TSSOP−16	2500 / Tape & Reel
MC74LVXT4052DR2G	LVX4052G	SOIC−16	2500 / Tape & Reel
MC74LVXT4052DTG	LVX 4052	TSSOP−16	96 Units / Rail
MC74LVXT4052DTR2G	LVX 4052	TSSOP−16	2500 / Tape & Reel
MC74LVXT4053DR2G	LVX4053G	SOIC−16	2500 / Tape & Reel
MC74LVXT4053DTG	LVX 4053	TSSOP−16	96 Units / Rail
MC74LVXT4053DTR2G	LVX 4053	TSSOP−16	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

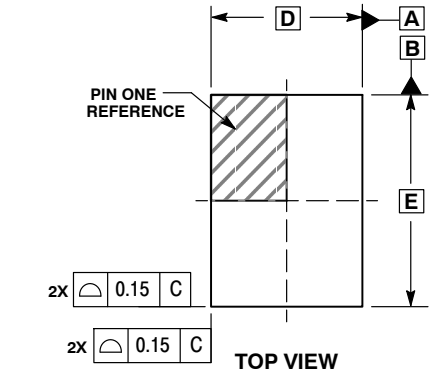
*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

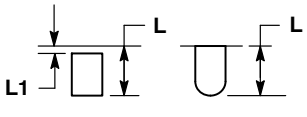
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

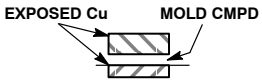
QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

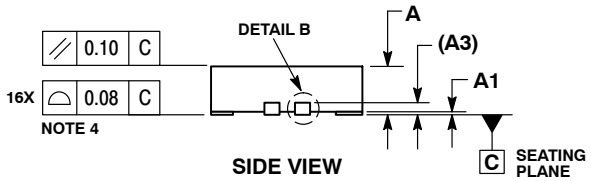
DATE 11 DEC 2008

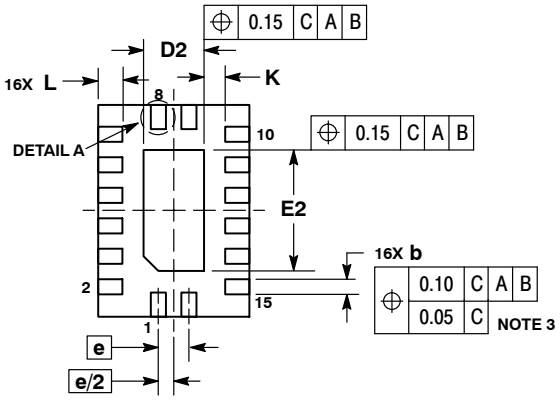
SCALE 2:1











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

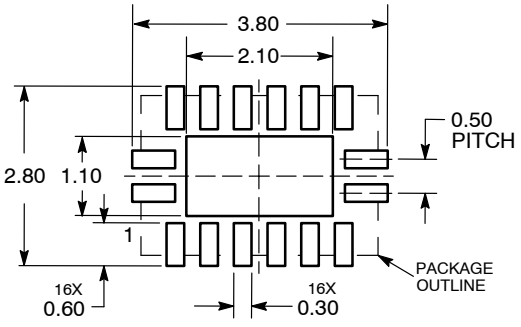
GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*

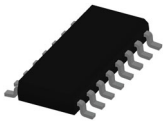


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON36347E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**QFN16, 2.5X3.5, 0.5P**	**PAGE 1 OF 1**

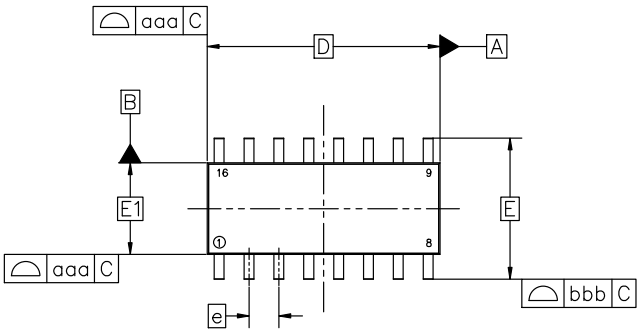
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



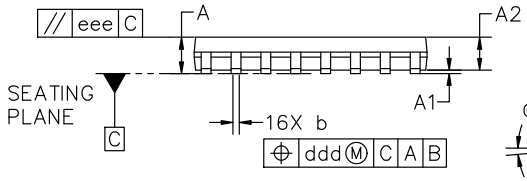
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

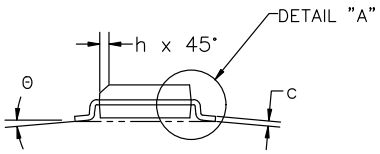
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

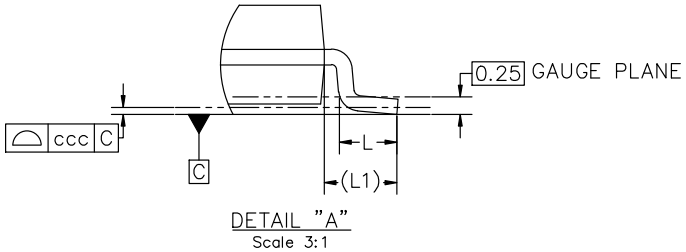


SIDE VIEW

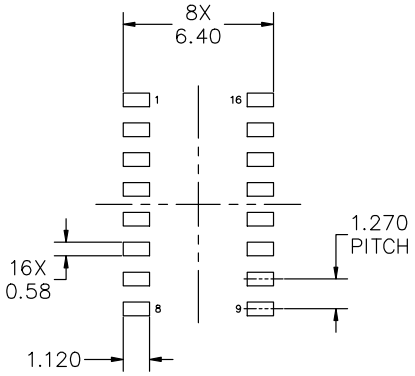


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

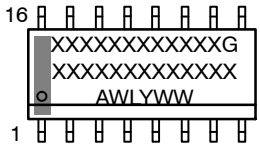
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

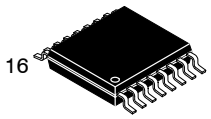
STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

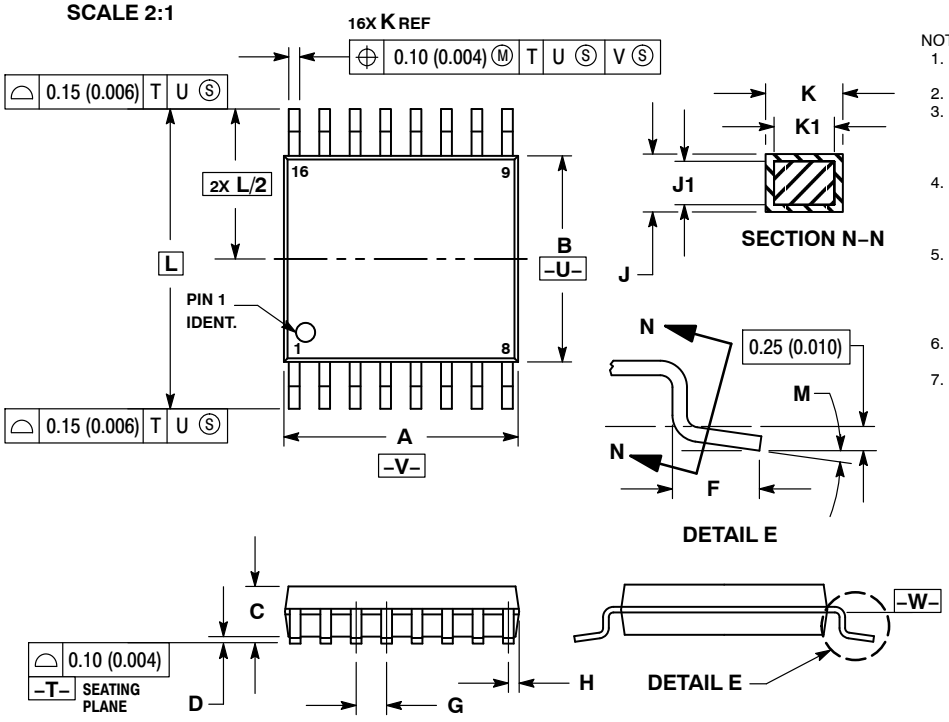
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



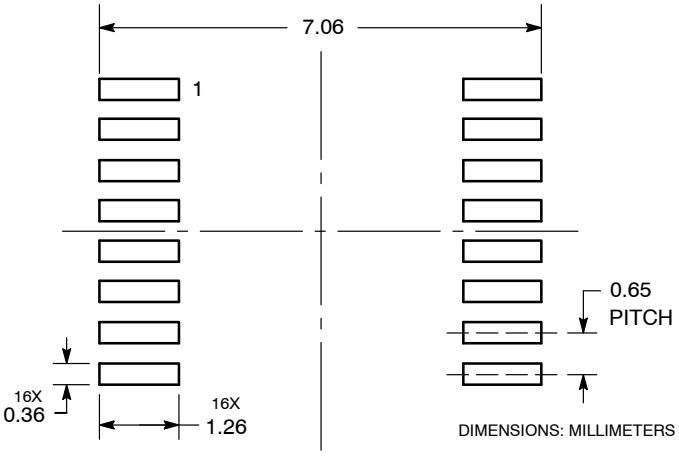
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

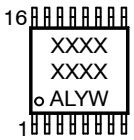
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70247A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales