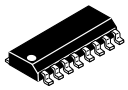
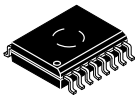
Analog Multiplexers/ Demultiplexers with Injection Current Effect Control

Automotive Customized

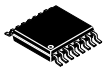
MC74HC4851A, MC74HC4852A, MC74HCT4851A, MC74HCT4852A



SOIC−16
D SUFFIX
CASE 751B



SOIC−16 WIDE
DW SUFFIX
CASE 751G



TSSOP−16
DT SUFFIX
CASE 948F

QFN16
MN SUFFIX
CASE 485AW

These devices are pin compatible to standard HC405x and MC1405xB analog mux/demux devices, but feature injection current effect control. This makes them especially suited for usage in automotive applications where voltages in excess of normal logic voltage are common.

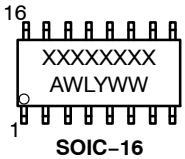
The injection current effect control allows signals at disabled analog input channels to exceed the supply voltage range without affecting the signal of the enabled analog channel. This eliminates the need for external diode/resistor networks typically used to keep the analog channel signals within the supply voltage range.

The devices utilize low power silicon gate CMOS technology. The Channel Select and Enable inputs are compatible with standard CMOS outputs.

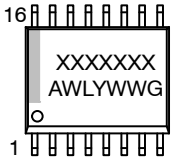
Features

- Injection Current Cross−Coupling Less than 1 mV/mA (See Figure 10)
- Pin Compatible to HC405X and MC1405XB Devices
- Power Supply Range 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- In Compliance With the Requirements of JEDEC Standard No. 7 A
- Chip Complexity: 154 FETs or 36 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

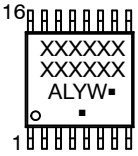
MARKING DIAGRAMS



SOIC−16



SOIC−16 WIDE



TSSOP−16

QFN16*

*V4851 marking used for NLV74HC4851AMN1TWG

XXXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

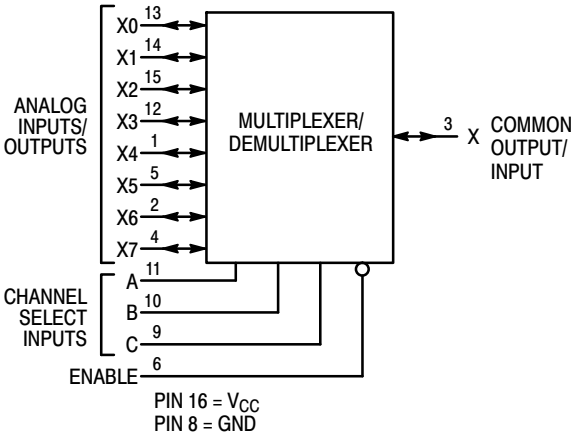


Figure 1. 4851A Logic Diagram
Single−Pole, 8−Position Plus Common Off

FUNCTION TABLE − 4851A

Control Inputs				
	Select			
Enable	C	B	A	ON Channels
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	X	X	X	NONE

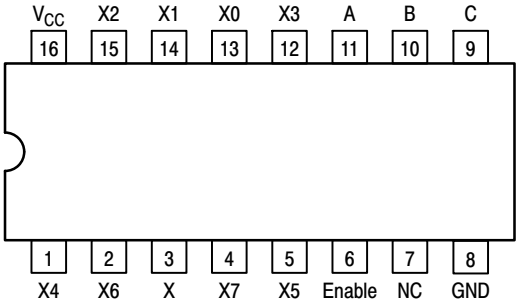


Figure 2. 4851A 16−Lead Pinout (Top View)

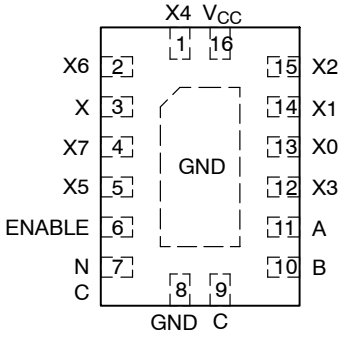


Figure 3. 4851A QFN Pinout

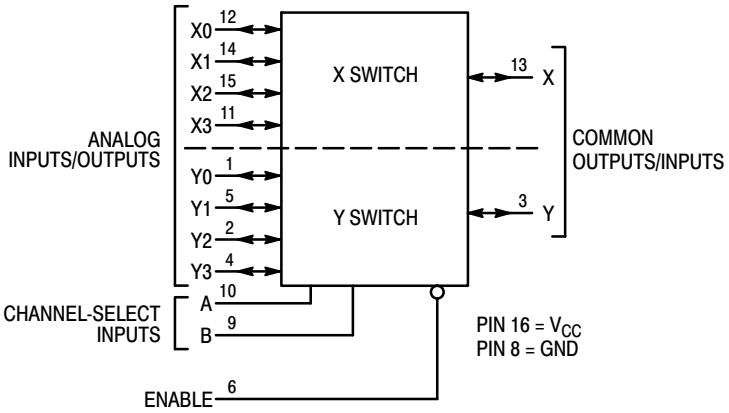


Figure 4. 4852A Logic Diagram
Double−Pole, 4−Position Plus Common Off

FUNCTION TABLE − 4852A

Control Inputs			
	Select		
Enable	B	A	ON Channels
L	L	L	Y0 X0
L	L	H	Y1 X1
L	H	L	Y2 X2
L	H	H	Y3 X3
H	X	X	NONE

X = Don't Care

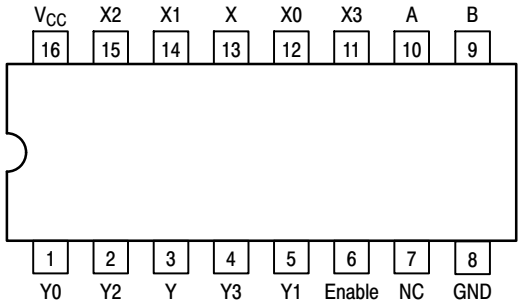


Figure 5. 4852A 16−Lead Pinout (Top View)

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Current, per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±50	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{IN}	DC Input Voltage − Any Pin (Referenced to GND)		0	V_{CC}	V
V_{IO*}	Static or Dynamic Voltage Across Switch		0	1.2	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns
MC74HCT					
V_{CC}	DC Supply Voltage (Referenced to GND)		4.5	5.5	V
V_{IN}	DC Input Voltage − Any Pin (Referenced to GND)		0	V_{CC}	V
V_{IO*}	Static or Dynamic Voltage Across Switch		0	1.2	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 4.5 V	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or VCC). Unused outputs must be left open.

DC CHARACTERISTICS – Digital Section (MC74HC4851A, MC74HC4852A)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	1.50 2.10 3.15 4.20	V
V_{IL}	Maximum Low–Level Input Voltage, Channel–Select or Enable Inputs	R_{on} = Per Spec	2.0 3.0 4.5 6.0	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	0.50 0.90 1.35 1.80	V
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)}$ = V_{CC} or GND $V_{in(analog)}$ = GND	6.0	2	20	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DC CHARACTERISTICS – Analog Section (MC74HC4851A, MC74HC4852A)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				–55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} to GND (Note 4); I_S ≤ 2.0 mA (Note 5)	2.0 3.0 4.5 6.0	1700 1100 550 400	1750 1200 650 500	1800 1300 750 600	Ω
ΔR_{on}	Delta “ON” Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC}/2 (Note 4); I_S ≤ 2.0 mA (Note 5)	2.0 3.0 4.5 6.0	300 160 80 60	400 200 100 80	500 240 120 100	Ω
I_{off}	Maximum Off–Channel Leakage Current, Any One Channel Common Channel	V_{in} = V_{CC} or GND	6.0	±0.1 ±0.1	±0.1 ±0.1	±0.1 ±0.1	μA
I_{on}	Maximum On–Channel Leakage Channel–to–Channel	V_{in} = V_{CC} or GND	6.0	±0.1	±0.1	±0.1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. V_{IS} is the input voltage of an analog I/O pin.
5. I_S is the currebnt flowing in or out of analog I/O pin.

AC CHARACTERISTICS (MC74HC4851A, MC74HC4852A) (C_L = 50 pF)

Symbol	Parameter	V_{CC}	–55 to 25°C	≤85°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	2.0 3.0 4.5 6.0	160 80 40 30	180 90 45 35	200 100 50 40	ns
t_{PHL}, $t_{PHZ,PZH}$ t_{PLH}, $t_{PLZ,PZL}$	Maximum Propagation Delay, Enable or Channel–Select to Analog Output	2.0 3.0 4.5 6.0	260 160 80 78	280 180 90 80	300 200 100 80	ns
C_{in}	Maximum Input Capacitance Digital Pins (All Switches Off) Any Single Analog Pin (All Switches Off) Common Analog Pin		10 35 40	10 35 40	10 35 40	pF
C_{PD}	Power Dissipation Capacitance Typical	5.0	20			pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

INJECTION CURRENT COUPLING SPECIFICATIONS (MC74HC4851A, MC74HC4852A) (V_{CC} = 5 V, T_A = −55°C to +125°C)

Symbol	Parameter	Condition	Typ	Max	Unit
$V\Delta_{out}$	Maximum Shift of Output Voltage of Enabled Analog Channel	I_{in}* ≤ 1 mA, R_S ≤ 3,9 kΩ I_{in}* ≤ 10 mA, R_S ≤ 3,9 kΩ I_{in}* ≤ 1 mA, R_S ≤ 20 kΩ I_{in}* ≤ 10 mA, R_S ≤ 20 kΩ	0.1 1.0 0.5 5.0	1.0 5.0 2.0 20	mV

*I_{in} = Total current injected into all disabled channels.

DC CHARACTERISTICS – Digital Section (MC74HCT4851A, MC74HCT4852A)

Symbol	Parameter	Condition	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
V_{IH}	Minimum High−Level Input Voltage, Channel−Select or Enable Inputs	R_{on} = Per Spec	4.5 to 5.5	2.0	2.0	2.0	V
V_{IL}	Maximum Low−Level Input Voltage, Channel−Select or Enable Inputs	R_{on} = Per Spec	4.5 to 5.5	0.8	0.8	0.8	V
I_{in}	Maximum Input Leakage Current on Digital Pins (Enable/A/B/C)	V_{in} = V_{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in(digital)}$ = V_{CC} or GND $V_{in(analog)}$ = GND	5.5	2.0	20	40	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DC CHARACTERISTICS – Analog Section (MC74HCT4851A, MC74HCT4852A)

Symbol	Parameter	Condition	V_{CC}	Guaranteed Limit			Unit
				−55 to 25°C	≤85°C	≤125°C	
R_{on}	Maximum “ON” Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC} to GND (Note 4); I_S ≤ 2.0 mA (Note 5)	4.5 5.5	550 400	650 500	750 600	Ω
ΔR_{on}	Delta “ON” Resistance	V_{in} = V_{IL} or V_{IH}; V_{IS} = V_{CC}/2 (Note 4); I_S ≤ 2.0 mA (Note 5)	4.5 5.5	80 60	100 80	120 100	Ω
I_{off}	Maximum Off−Channel Leakage Current, Any One Channel Common Channel	V_{in} = V_{CC} or GND	5.5	±0.1 ±0.1	±0.1 ±0.1	±0.1 ±0.1	μA
I_{on}	Maximum On−Channel Leakage Channel−to−Channel	V_{in} = V_{CC} or GND	5.5	±0.1	±0.1	±0.1	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC CHARACTERISTICS (MC74HCT4851A, MC74HCT4852A) (C_L = 50 pF)

Symbol	Parameter	V_{CC}	−55 to 25°C	≤85°C	≤125°C	Unit
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Analog Input to Analog Output	5.0	40	45	50	ns
t_{PHL}, $t_{PHZ,PZH}$ t_{PLH}, $t_{PLZ,PZL}$	Maximum Propagation Delay, Enable or Channel−Select to Analog Output	5.0	80	90	100	ns
C_{in}	Maximum Input Capacitance — Digital Pins (All Switches Off) — Any Single Analog Pin (All Switches Off) — Common Analog Pin		10 35 40	10 35 40	10 35 40	pF
C_{PD}	Power Dissipation Capacitance — Typical	5.0	20			pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

INJECTION CURRENT COUPLING SPECIFICATIONS (MC74HCT4851A, MC74HCT4852A) (V_{CC} = 5 V, T_A = −55°C to +125°C)

Symbol	Parameter	Condition	Typ	Max	Unit
$V\Delta_{out}$	Maximum Shift of Output Voltage of Enabled Analog Channel	I_{in}* ≤ 1 mA, R_S ≤ 3,9 kΩ I_{in}* ≤ 10 mA, R_S ≤ 3,9 kΩ I_{in}* ≤ 1 mA, R_S ≤ 20 kΩ I_{in}* ≤ 10 mA, R_S ≤ 20 kΩ	0.1 1.0 0.5 5.0	1.0 5.0 2.0 20	mV

*I_{in} = Total current injected into all disabled channels.

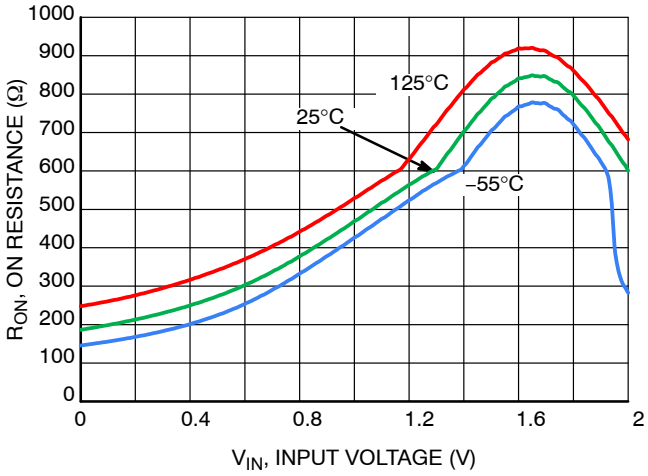


Figure 6. Typical On Resistance V_{CC} = 2 V

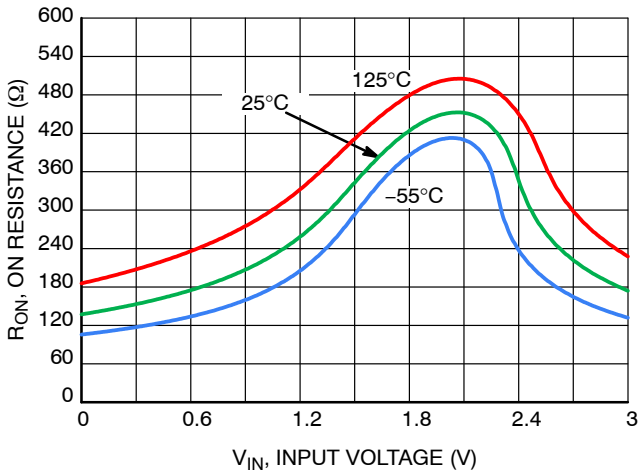


Figure 7. Typical On Resistance V_{CC} = 3 V

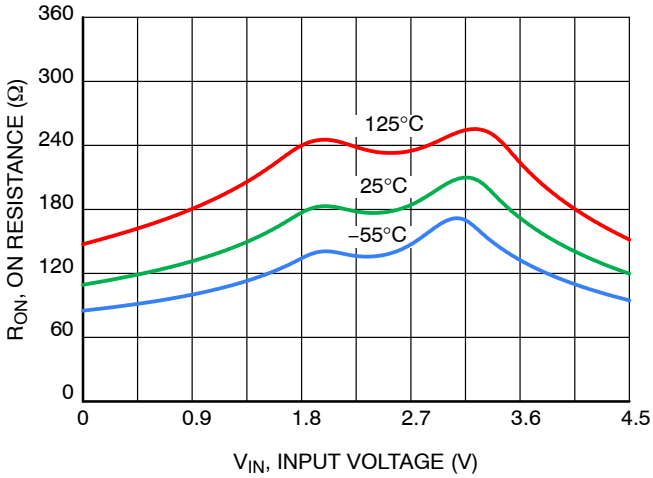


Figure 8. Typical On Resistance V_{CC} = 4.5 V

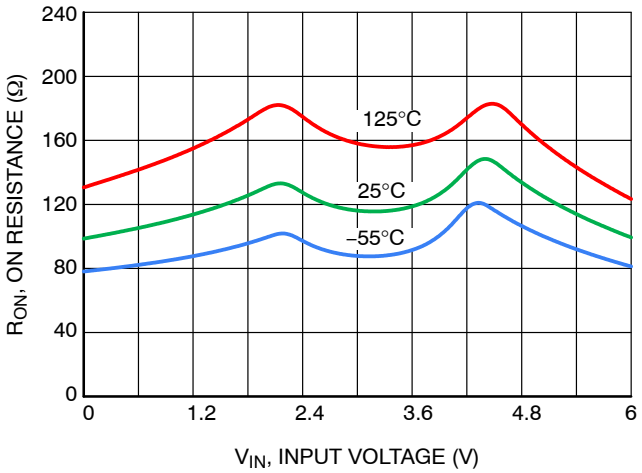


Figure 9. Typical On Resistance V_{CC} = 6 V

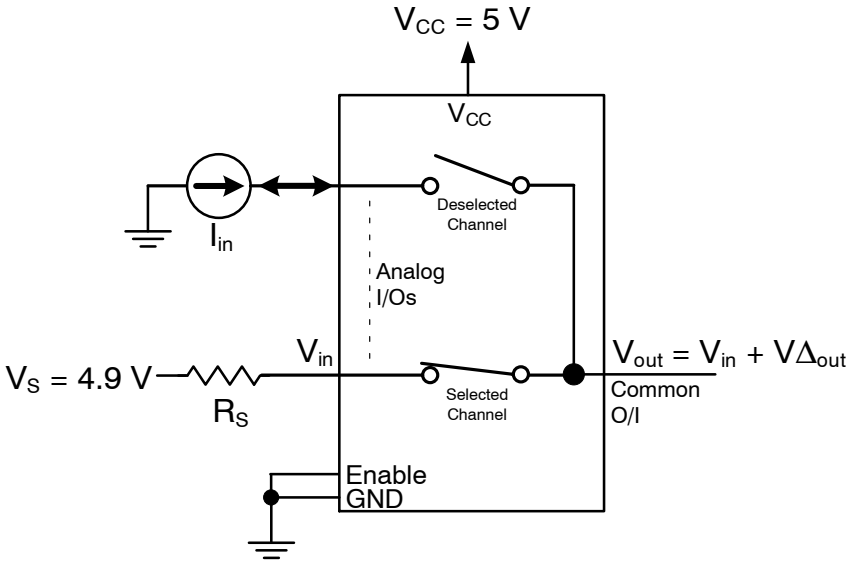


Figure 10. Injection Current Coupling Specification

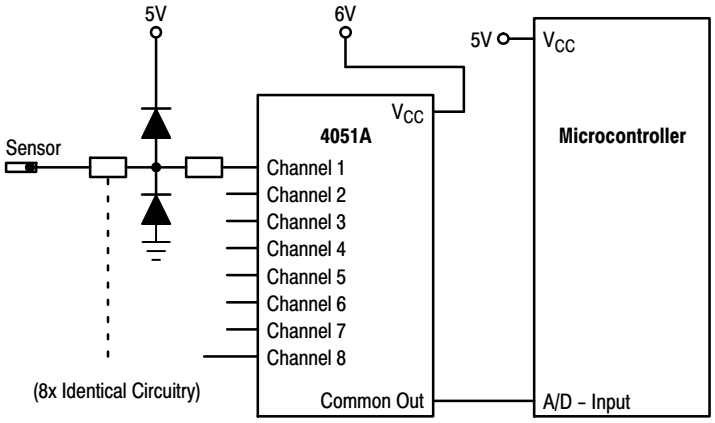


Figure 11. Actual Technology
Requires 32 passive components and one extra 6 V regulator
to suppress injection current into a standard 4051 multiplexer

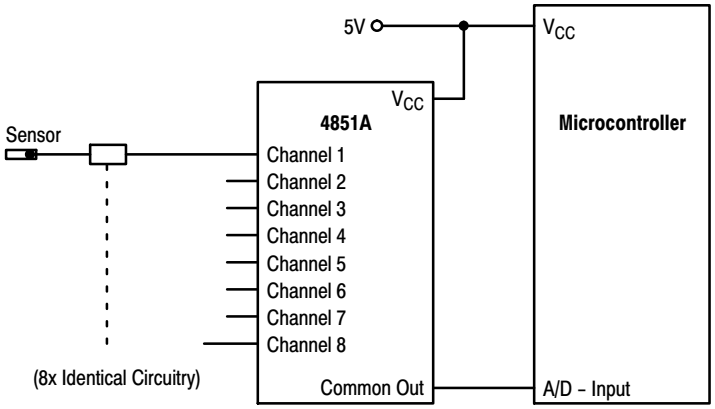


Figure 12. 4851A Solution
Solution by applying the 4851A multiplexer

TEST SETUPS

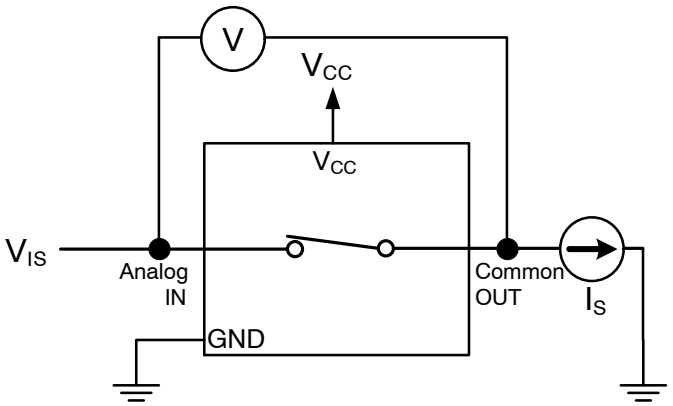


Figure 13. On Resistance

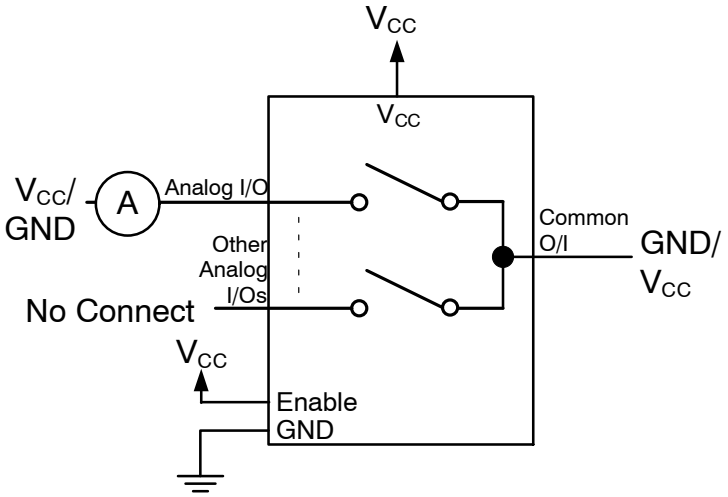


Figure 14. Maximum Off Channel Leakage Current, Any One Channel

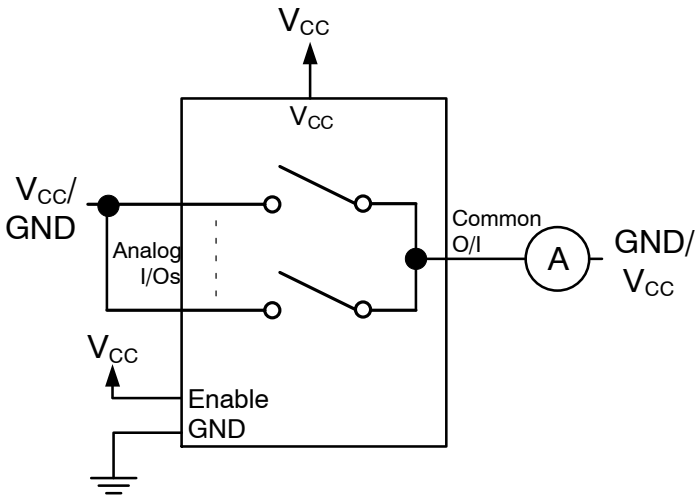


Figure 15. Maximum Off Channel Leakage Current, Common Channel

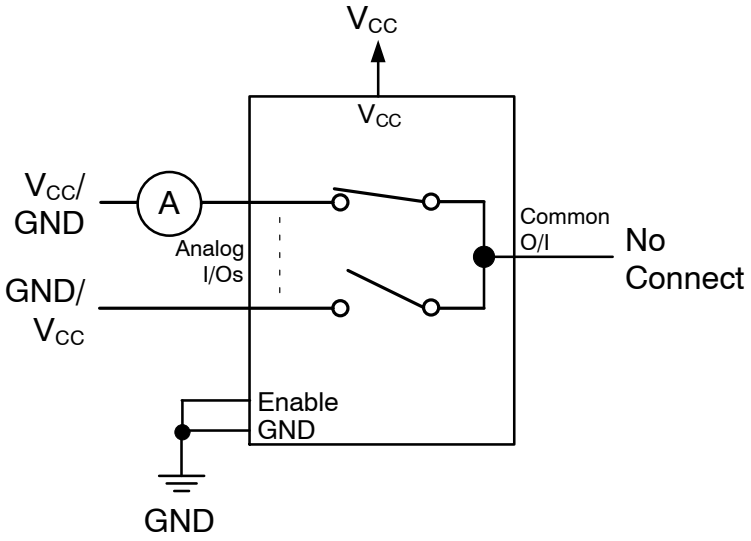
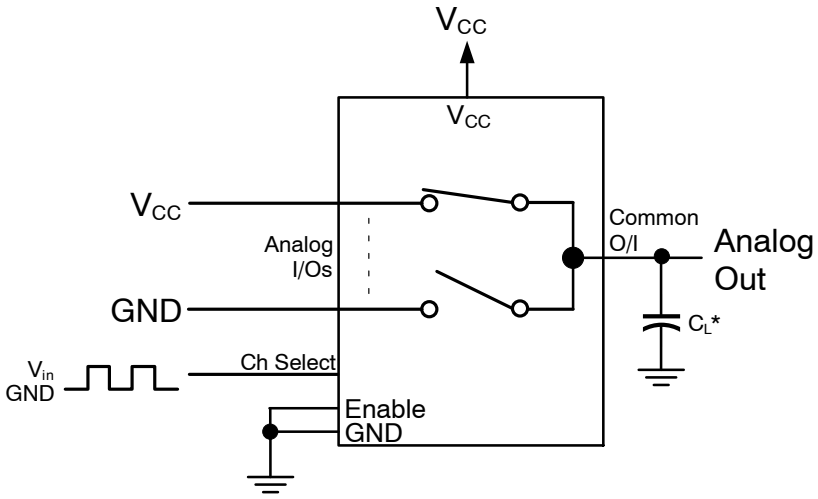
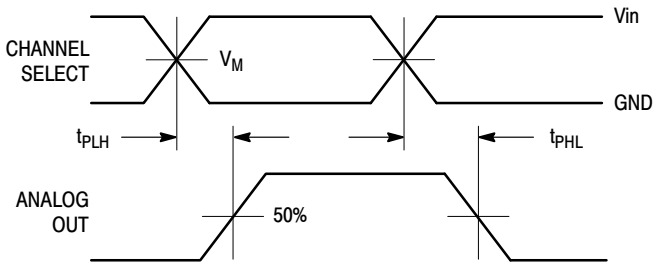


Figure 16. Maximum On Channel Leakage Current, Channel to Channel

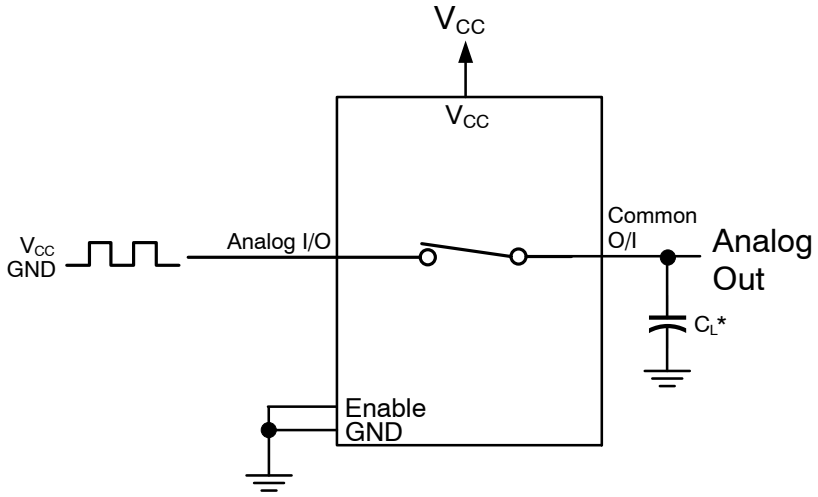


*Includes all probe and jig capacitance.



Vin = Vcc for HC, 3 V for HCT
V_M = 50% x V_{CC} for HC, 1.3 V for HCT

Figure 17. Propagation Delay, Channel Select to Analog Out



*Includes all probe and jig capacitance.

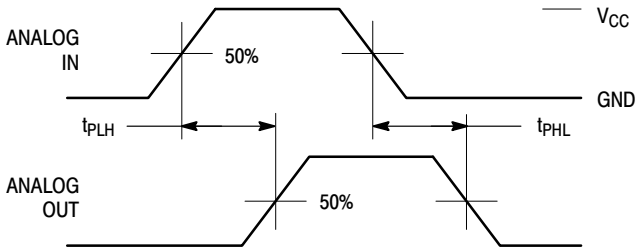
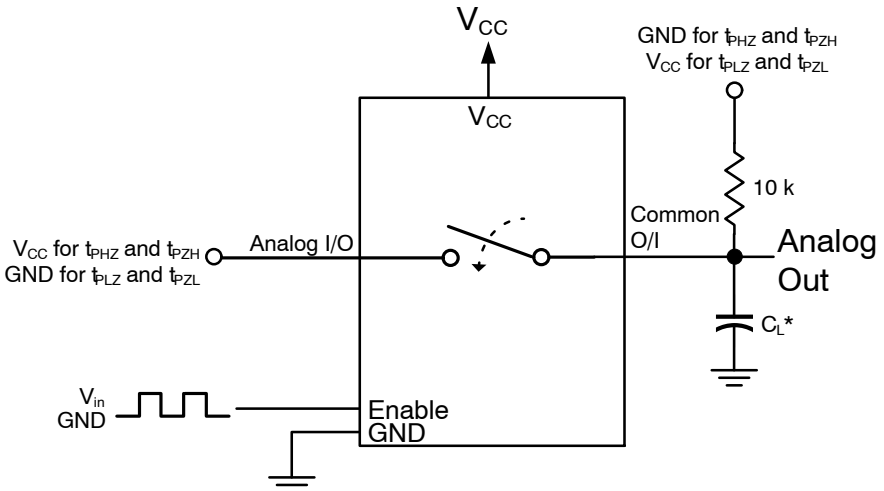
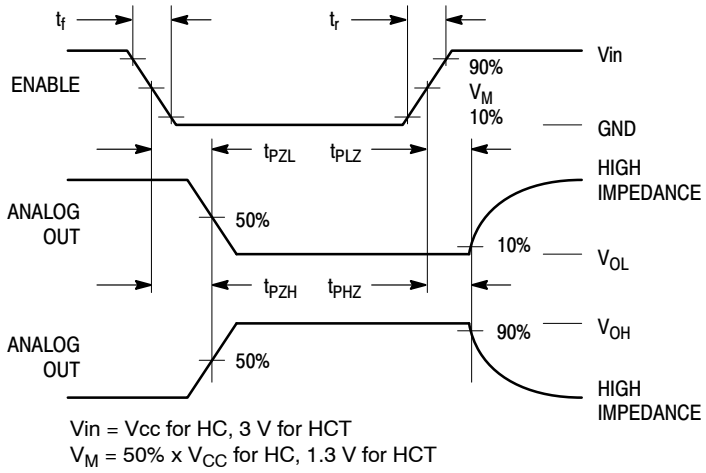


Figure 18. Propagation Delay, Analog In to Analog Out



*Includes all probe and jig capacitance.



Vin = Vcc for HC, 3 V for HCT
V_M = 50% x V_{CC} for HC, 1.3 V for HCT

Figure 19. Propagation Delay, Enable to Analog Out

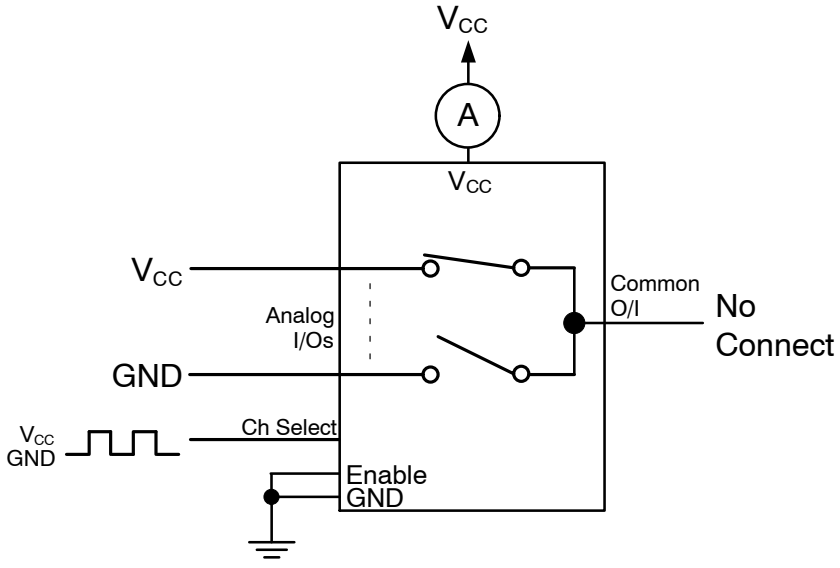


Figure 20. Power Dissipation Capacitance

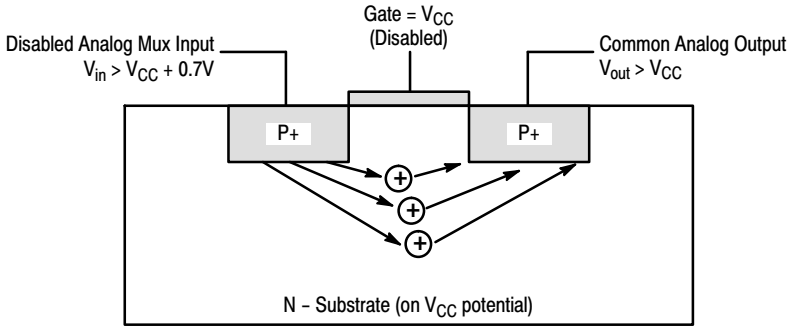


Figure 21. Diagram of Bipolar Coupling Mechanism
Appears if V_{in} exceeds V_{CC}, driving injection current into the substrate

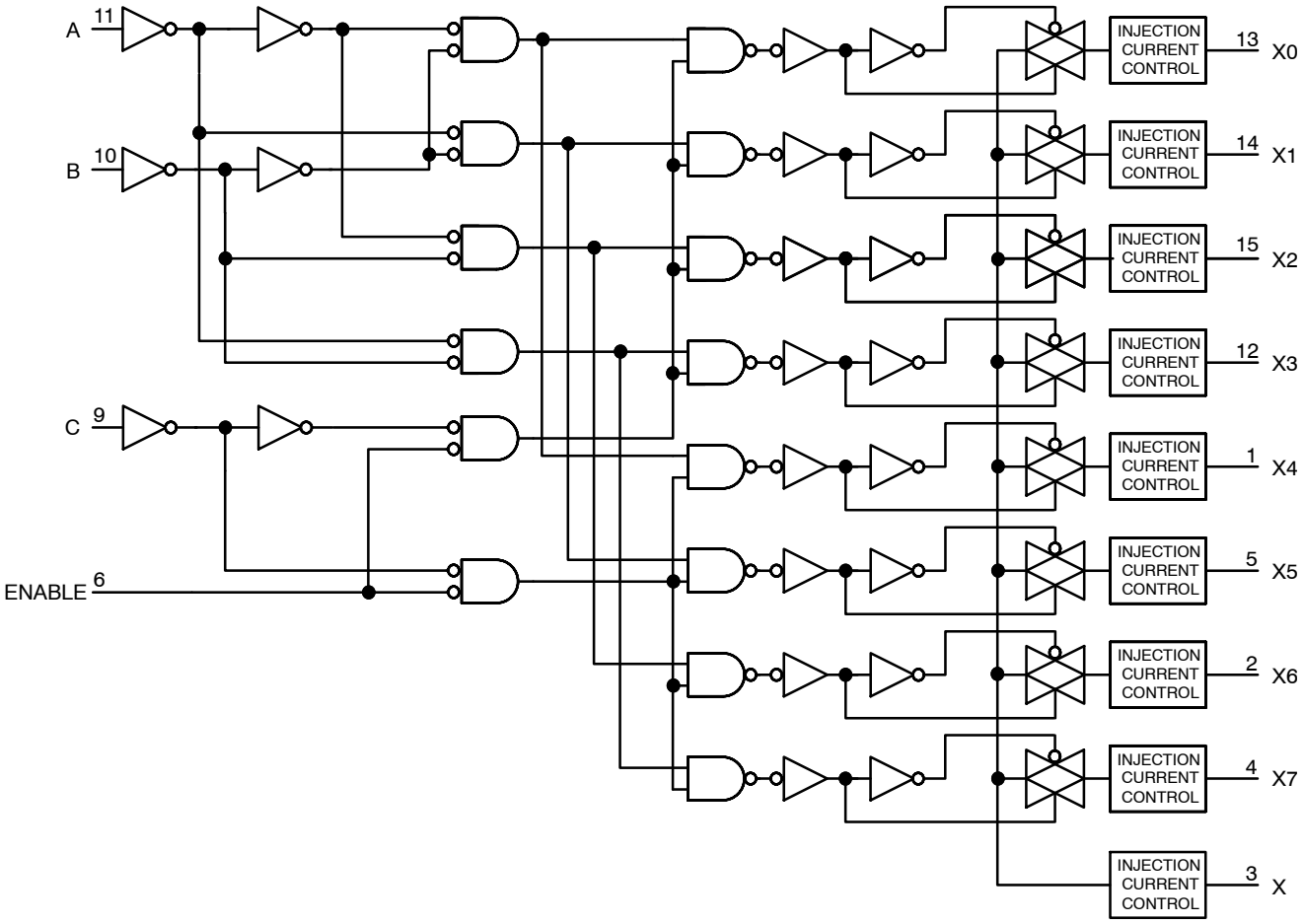


Figure 22. Function Diagram, 4851A

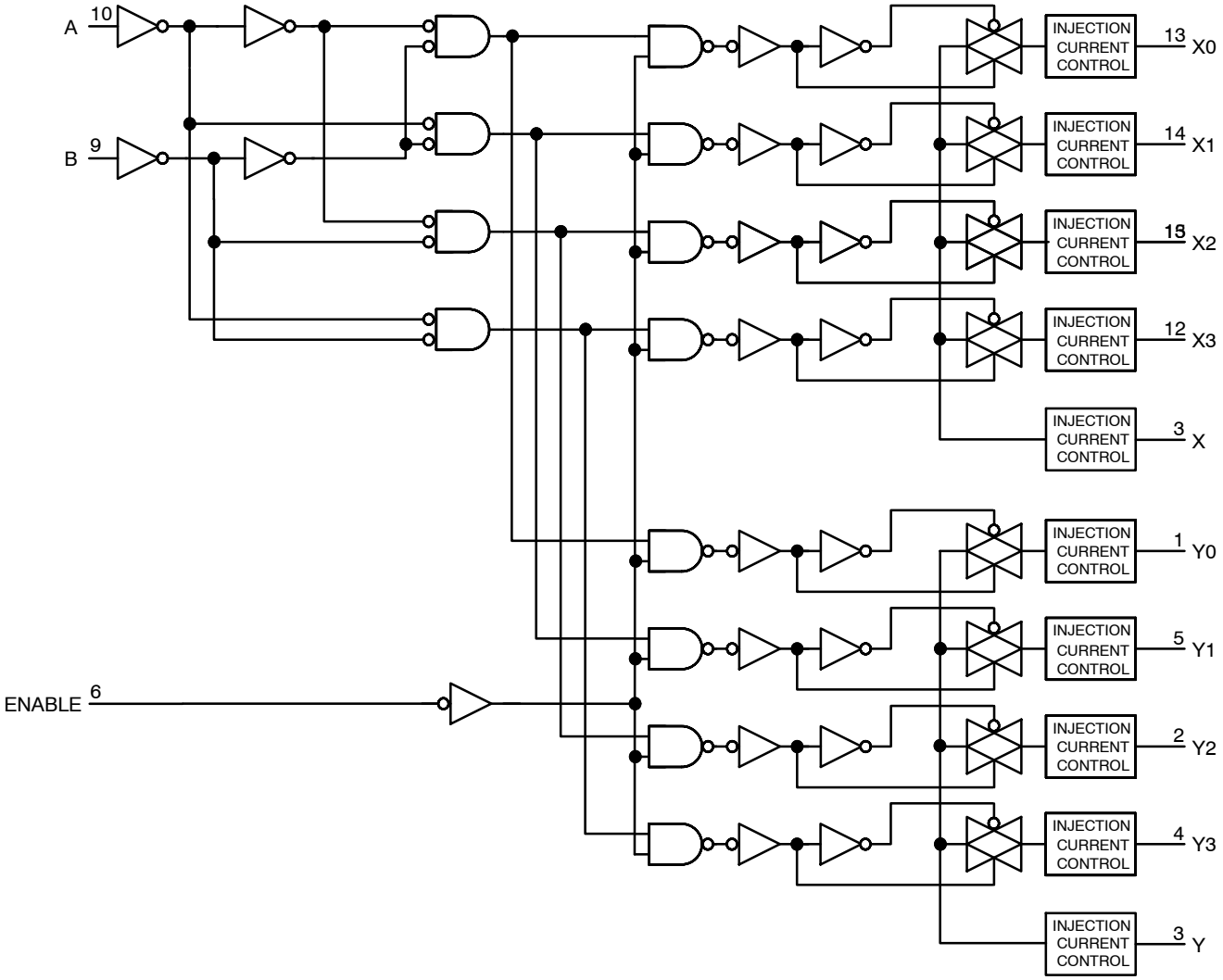


Figure 23. Function Diagram, 4852A

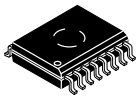
ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC4851ADG	HC4851AG	SOIC−16	55 Units / Rail
MC74HC4851ADR2G	HC4851AG	SOIC−16	2500 / Tape & Reel
MC74HC4851ADR2G−Q*	HC4851AG	SOIC−16	2500 / Tape & Reel
MC74HC4851ADTR2G	HC48 51A	TSSOP−16	2500 / Tape & Reel
MC74HC4851ADTR2G−Q*	HC48 51A	TSSOP−16	2500 / Tape & Reel
MC74HC4851AMN1TWG−Q*	4851	QFN−16	3000 / Tape & Reel
MC74HC4852ADR2G	HC4852AG	SOIC−16	2500 / Tape & Reel
MC74HC4852ADR2G−Q*	HC4852AG	SOIC−16	2500 / Tape & Reel
MC74HC4852ADTR2G	HC48 52A	TSSOP−16	2500 / Tape & Reel
MC74HC4852ADTR2G−Q*	HC48 52A	TSSOP−16	2500 / Tape & Reel
MC74HCT4851ADR2G	HCT4851AG	SOIC−16	2500 / Tape & Reel
MC74HCT4851ADTR2G	HCT4 851A	TSSOP−16	2500 / Tape & Reel
MC74HCT4851ADTR2G−Q*	HCT4 851A	TSSOP−16	2500 / Tape & Reel
MC74HCT4852ADR2G	HCT4852AG	SOIC−16	2500 / Tape & Reel
MC74HCT4852ADTR2G	HCT4 852A	TSSOP−16	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

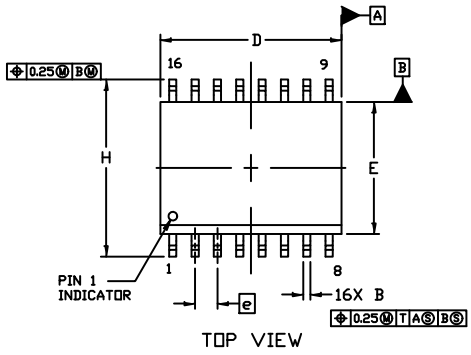


1

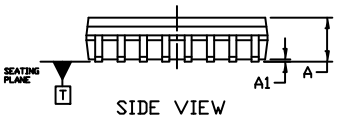
SCALE 1:1

SOIC−16 WB
CASE 751G
ISSUE E

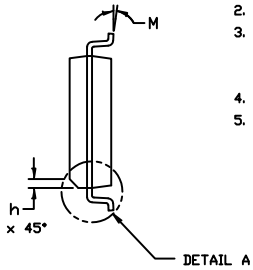
DATE 08 OCT 2021



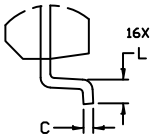
TOP VIEW



SIDE VIEW



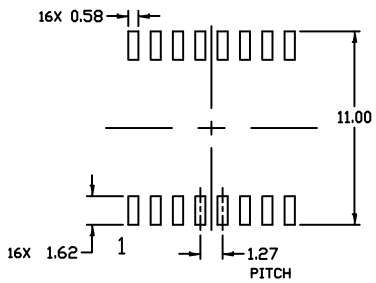
END VIEW



DETAIL A
2X SCALE

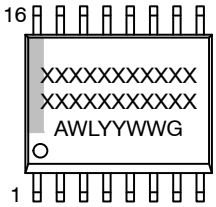
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

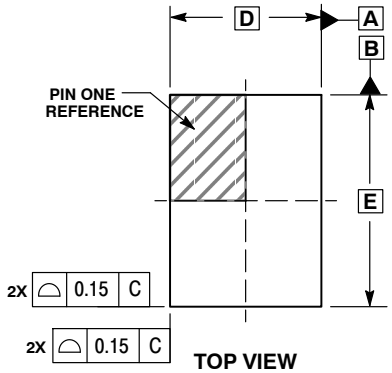
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

PACKAGE DIMENSIONS

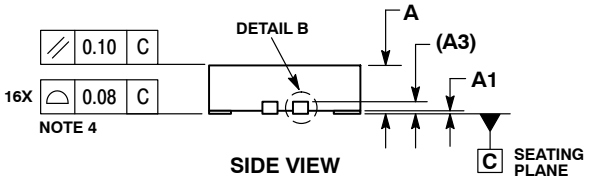
SCALE 2:1

QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

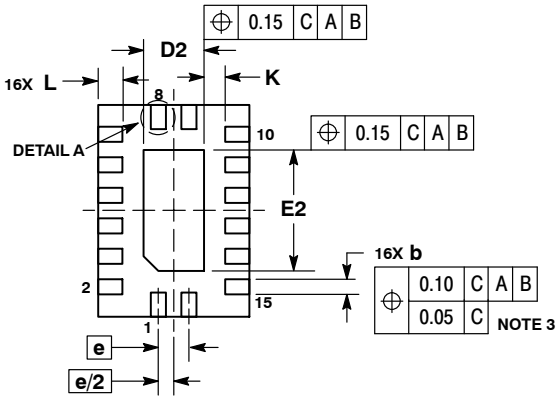
DATE 11 DEC 2008



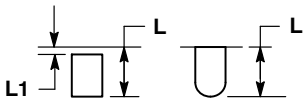
TOP VIEW



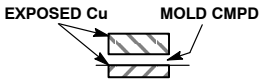
SIDE VIEW



BOTTOM VIEW



DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

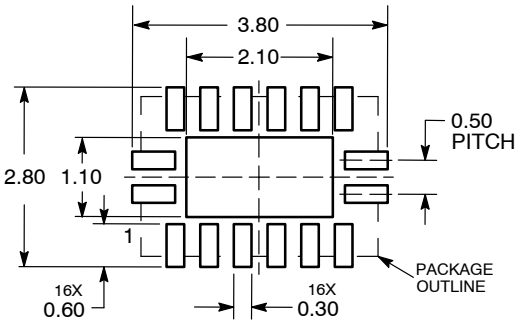
GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

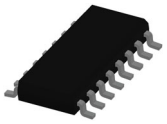
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

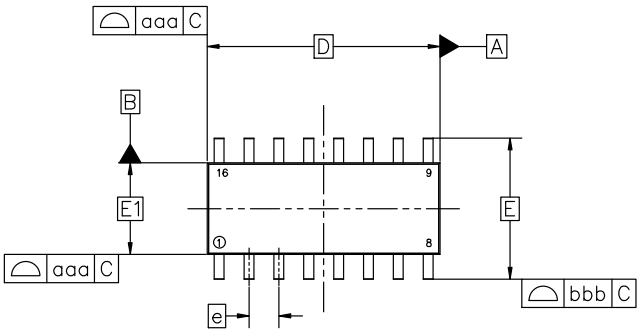
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



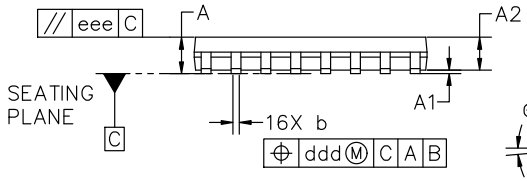
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

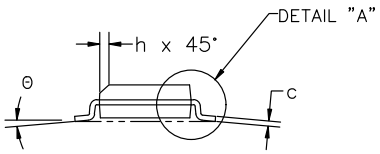
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

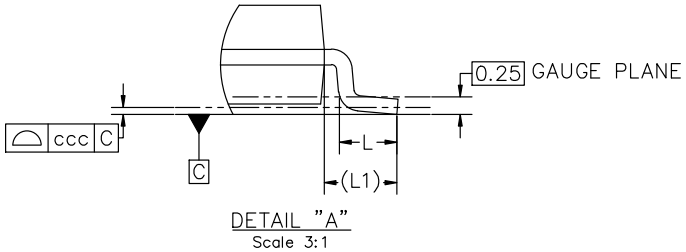


SIDE VIEW

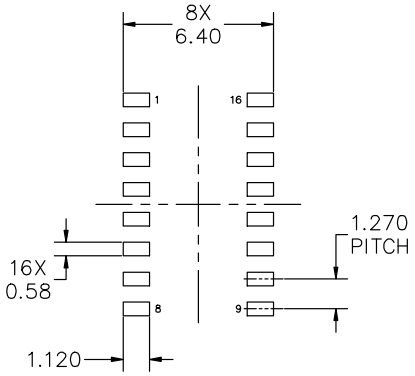


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

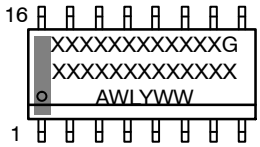
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

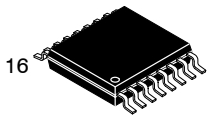
STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

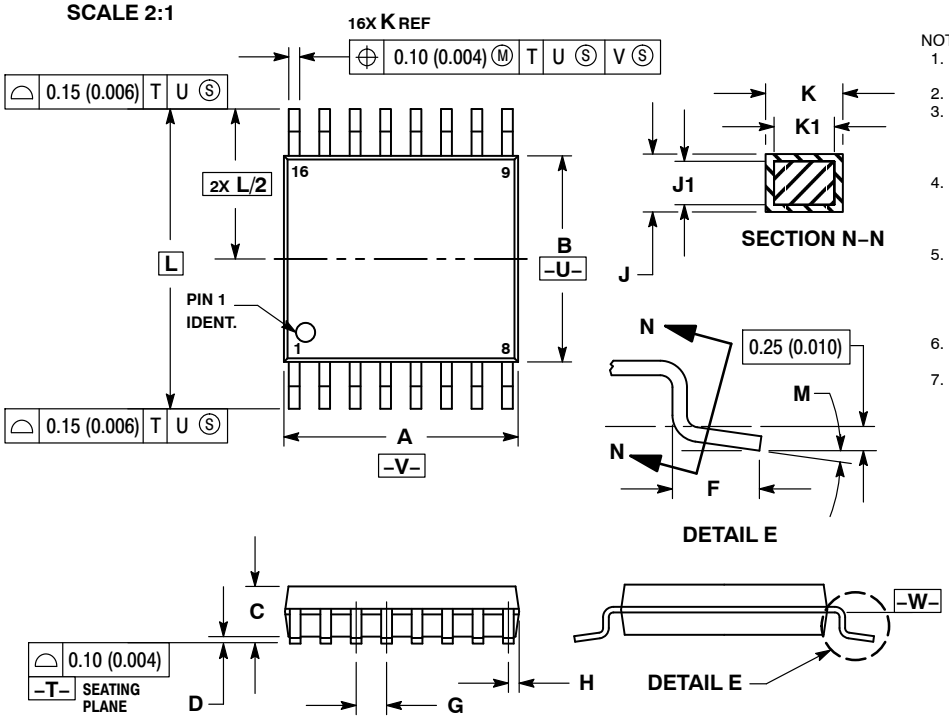
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



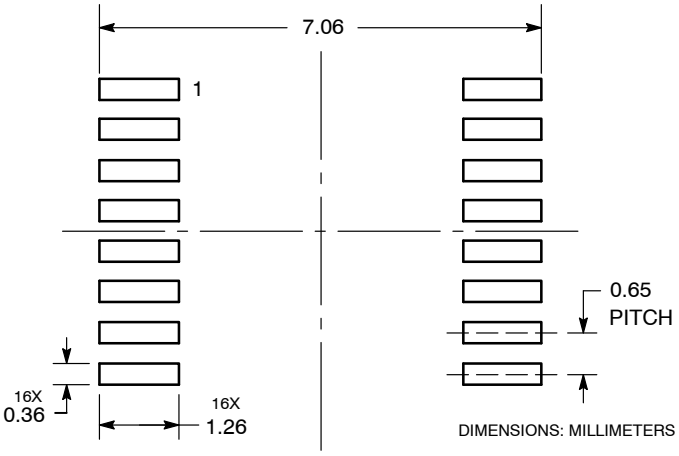
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

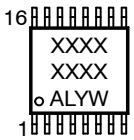
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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