HV2825/HV2925/HV2926

Single 5V Bias, Low Harmonic Distortion, 64-Channel, High-Voltage Analog Switch

Features

- 64-Channel High-Voltage Analog Switch
- Only +5V Bias Supply Required
- 3.3V and 5V CMOS Input Logic Level
- Asymmetric Switch Topology for Small Size
- 66 MHz Data Shift Clock Frequency
- Dual SPI for Fast ON/OFF Control
- Low Parasitic Capacitance
- Low Harmonic Distortion
- DC to 50 MHz Analog Small-Signal Frequency
- 200 kHz to 50 MHz Large-Signal Frequency
- -70 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Integrated Bleed Resistors (SWS and SWT Pins in HV2925, SWT Pin in HV2926)

Application

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Module

General Description

The HV2825/HV2925/HV2926 are low harmonic distortion, low charge injection, 64-channel, high-voltage switches for multiplexers/demultiplexers, without high-voltage bias supplies. They are intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

The devices require no high voltage bias supplies but only a +5V low voltage source (V_{DD}). All of the analog switches in the devices can pass ±100V high voltage pulses from SWS to SWT with a typical 6Ω R_{ON} and 50 MHz bandwidth for small signals. Since the devices have low-voltage biased switches, they cannot pass high-voltage DC signals.

In the HV2825/HV2925/HV2926, an asymmetric switch topology is used to reduce the die size. The piezoelectric transducers are connected to SWT pins and the pulsed signals are applied to SWS pins.

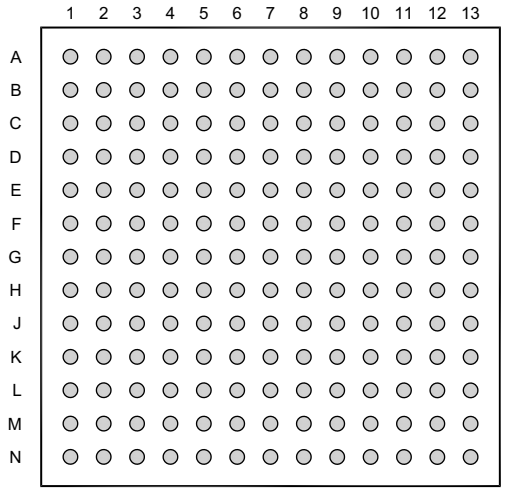
The HV2925 has bleed resistors in both SWS and SWT pins. HV2926 has bleed resistors only in SWT pins. HV2825 does not have bleed resistors. The bleed resistor removes potential charge built up in capacitive load of the analog switches as well as capacitive load in piezoelectric transducers.

The HV2825/HV2925/HV2926 have dual SPI (Serial to Parallel Interface) logic inputs to control two sets of 32 switches independently for a higher speed on switch ON/OFF control. The ON/OFF states of each 32 switches are programmed individually through the corresponding SPI. Users can also program HV2825/HV2925/HV2926 as 64-channel switches by connecting two SPI in daisy-chain configuration to reduce the control logic signals from FPGA.

The HV2825/HV2925/HV2926 are available in 169-ball 11 x 11 x 1.50 mm LFBGA package.

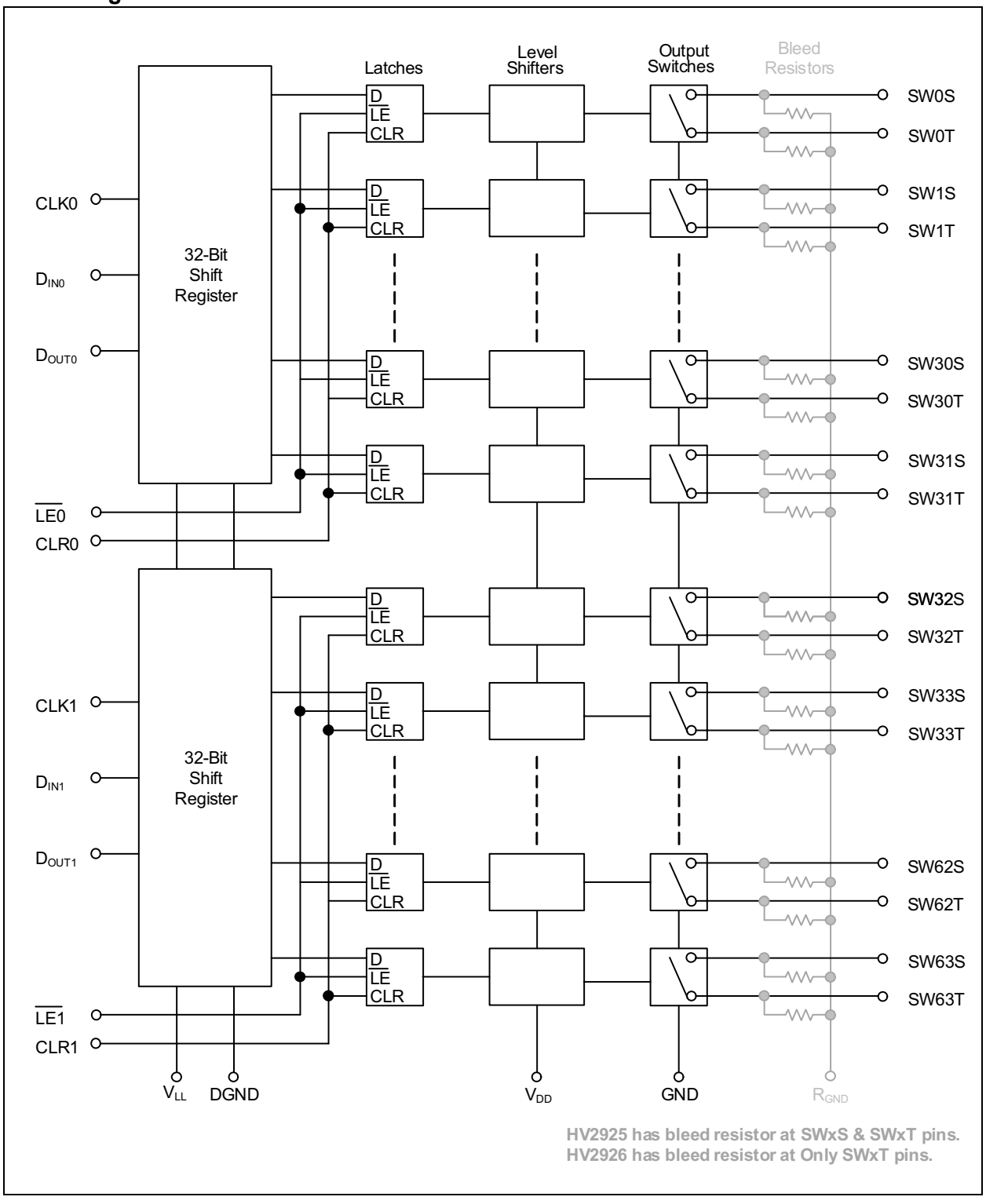
Package Type

11 x 11 x 1.50 mm LFBGA (Top View*)



* See Table 2-1 for pin information.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input Supply (V_{LL}, V_{DD}) ..... -0.5V to 6.6V
Logic Level Pins ..... -0.5V to (V_{LL} +0.3)V
Switch Pins (SWSx) ..... -110V to +110V
Switch Pins (SWTx, switch ON) ..... -110V to +110V
Switch Pins (SWTx, switch OFF) ..... -2V to +2V
Peak Analog Signal Current/Channel (IPK) 2.9A
Operating Junction Temperature ..... -40°C to +125°C
Storage Temperature ..... -65°C to +150°C
HBM ESD Rating (Low Voltage Pins) ..... 2 kV

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{LL}	3	—	5.5	V	Note 1
Positive Supply Voltage	V_{DD}	4.5	—	6.3	V	
High-Level Input Voltage	V_{IH}	0.9 V_{LL}	—	V_{LL}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1 V_{LL}	V	
Analog Signal Voltage SWS Pin Peak-to-Peak	V_{SWS}	-100	—	100	V	

Note 1: Specification is obtained by characterization and is not 100% tested.
2: V_{SWS} and V_{SWT} must be within V_{DD} and GND or floating during power-up/down transition.
3: Rise and fall times of power supplies, V_{LL} and V_{DD}, should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = +5V, V_{LL} = +5V, T_{AMB} = +25°C; **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Small-Signal Switch On-Resistance	R_{ONS}	—	6	**9**	Ω	I_{SIG} = 5 mA
		—	6	**9**	Ω	I_{SIG} = 200 mA
Small-Signal Switch On-Resistance Matching	ΔR_{ONS}	—	—	**20**	%	I_{SIG} = 5 mA
Large-Signal Switch On-Resistance	R_{ONL}	—	7	—	Ω	V_{SIG} = 90V, R_{LOAD} = 80Ω **(Note 1)**
Value of Output Bleed Resistor	R_{INT}	20	35	50	kΩ	Output switch to RGND, I_{RINT} = 20 µA
Switch-Off Leakage per SWT Pin	I_{SOL}	—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse
		—	—	**3**	µA	V_{SIG} = -100V, 100 µs pulse, **(Note 1)**

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, V_{DD} = +5V, V_{LL} = +5V, T_{AMB} = +25°C; **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
HV2825						
Switch-Off Bias per SWS Pin	I_{SOB}	—	—	**5**	µA	V_{SIG} = +100V, 500 µs pulse
		—	—	**3**	mA	V_{SIG} = -100V, 100 µs pulse **(Note 1)**
Switch-Off Bias per SWT Pin		—	—	**3**	µA	V_{SIG} = +300 mV, -300 mV
HV2925						
Switch-Off Bias per SWS Pin	I_{SOB}	—	—	**5**	µA	V_{SIG} = +100V, 500 µs pulse **(Note 2)**
		—	—	**3**	mA	V_{SIG} = -100V, 100 µs pulse **(Note 2)**
Switch-Off Bias of all SWT Pin		—	—	**20**	µA	V_{SIG} = +300 mV, -300 mV
HV2926						
Switch-Off Bias per SWS Pin	I_{SOB}	—	—	**5**	µA	V_{SIG} = +100V, 500 µs pulse
		—	—	**3**	mA	V_{SIG} = -100V, 100 µs pulse **(Note 1)**
Switch-Off Bias of all SWT Pins		—	—	**20**	µA	V_{SIG} = +300 mV, -300 mV
DC Offset Switch OFF	V_{OS}	—	1	**10**	mV	R_{LOAD} = 25 kΩ (HV2825), 50 kΩ (HV2926), no load (HV2925)
DC Offset Switch ON		—	1	**10**	mV	
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	**20**	µA	All switches OFF
		—	—	**20**	µA	All switches ON, V_{SW} = 1V
Quiescent V_{LL} Supply Current	I_{LLQ}	—	—	**20**	µA	All logic inputs are GND.
Switch Output Peak Current	I_{SW}	**2.1**	2.9	—	A	V_{SIG} duty cycle < 0.1% **(Note 1)**
Output Switching Frequency	f_{SW}	—	—	**50**	kHz	Duty cycle = 50% **(Note 1)**
Average V_{DD} Supply Current	I_{DD}	—	14	**20**	mA	All output switches are turning ON and OFF at 50 kHz with no load
Average V_{LL} Supply Current	I_{LL}	—	2.7	**5**	mA	f_{CLK} = 5.0 MHz
Data Out Source Current	I_{SOR}	**10**	—	—	mA	V_{OUT} = V_{LL} - 0.7V
Data Out Sink Current	I_{SINK}	**10**	—	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	—	8	—	pF	**Note 2**

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{DD} = +5V, V_{LL} = +5V, T_{AMB} = +25°C; **Boldface** specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Setup Time Before $\overline{LE}$ rises	t_{SD}	**25**	—	—	ns	**Note 1**
Time Width of $\overline{LE}$	t_{WLE}	**12**	—	—	ns	**Note 1**
Clock Delay Time to Data Out	t_{DO}	—	—	**13.5**	ns	
Time Width of CLR	t_{WCLR}	**55**	—	—	ns	**Note 1**
Setup Time Data to Clock	t_{SU}	**1.5**	—	—	ns	**Note 1**
Hold Time Data from clock	t_H	**1.5**	—	—	ns	**Note 1**
Clock Frequency	f_{CLK}	—	—	**66**	MHz	50% duty cycle, $f_{DIN} = (1/2)f_{CLK}$, C_{DOUT} = 20 pF **(Note 1)**
Clock Rise and Fall Times	t_R, t_F	—	—	**50**	ns	
Turn ON Time	t_{ON}	—	—	**5**	µs	V_{SIG} = 5V, R_{LOAD} = 550Ω
Turn OFF Time	t_{OFF}	—	—	**5**		
Input Large-Signal Pulse Width	t_{PW}	—	—	**2.5**	µs	V_{PULSE} = 0V to ±100V, **(Note 1)**
Maximum V_{SIG} Slew Rate	dv/dt	—	—	20	V/ns	**Note 1**
Analog Small-Signal Frequency	f_{BWS}	—	50	—	MHz	**Note 1**
OFF Isolation SWS to SWT	K_O	—	-65	—	dB	f = 5.0 MHz, 10Vp-p, 1.0 kΩ//15 pF load, **(Note 1)**
		—	-70	—		f = 5.0 MHz, 10Vp-p, 50Ω load, **(Note 1)**
OFF Isolation SWT to SWS		—	-65	—	dB	f = 5.0 MHz, 2Vp-p, 1.0 kΩ//15 pF load, **(Note 1)**
		—	-70	—		f = 5.0 MHz, 2Vp-p, 50Ω load, **(Note 1)**
Switch Crosstalk	K_{CR}	—	-75	—	dB	f = 5.0 MHz, 50Ω load, **(Note 1)**
OFF Capacitance SWT to GND	$C_{SG(OFF)}$	—	5	—	pF	V_{SIG} = 50 mV @ 1 MHz, no load **(Note 1)**
OFF Capacitance SWS to GND		—	15	—		
ON Capacitance SWT to GND	$C_{SG(ON)}$	—	16	—	pF	V_{SIG} = 50 mV @ 1 MHz, no load **(Note 1)**
ON Capacitance SWS to GND		—	16	—		
Output Voltage Spike at SWT	$+V_{SPK}$	—	—	40	mV	R_{LOAD} = 50Ω, **(Note 1)**
	$-V_{SPK}$	-10	—	—		
Output Voltage Spike at SWS	$+V_{SPK}$	—	—	40	mV	R_{LOAD} = 50Ω, **(Note 1)**
	$-V_{SPK}$	-10	—	—		
Charge Injection at SWT	QC	—	50	—	pC	**Note 1**
Charge Injection at SWS		—	100	—	pC	**Note 1**
Second Harmonic Distortion	HD2	—	-65	—	dBc	V_{SIG} = 1.5 V_{PP} @ 5 MHz, 50Ω load **(Note 1)**
		—	-70	—	dBc	V_{SIG} = 1.5 V_{PP} @ 5 MHz, 1 kΩ//15 pF load **(Note 1)**

Note 1: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATION

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Range						
Operating Temperature Range	T_A	0	—	+70	°C	
Storage Temperature Range	T_S	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, LFBGA	θ_{JA}	—	+18	—	°C/W	

TABLE 1-1: TRUTH TABLE(SPI0)

D0	D1	...	D15	D16	...	D31	$D_{IN}0$	$\overline{LE0}$	CLR0	SW0	SW1	...	SW15	SW16	...	SW31
L	—		—	—		—	X	L	L	OFF	—		—	—		—
H	—		—	—		—	X	L	L	ON	—		—	—		—
—	L		—	—		—	X	L	L	—	OFF		—	—		—
—	H		—	—		—	X	L	L	—	ON		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		L	—		—	X	L	L	—	—		OFF	—		—
—	—	...	H	—	...	—	X	L	L	—	—	...	ON	—	...	—
—	—		—	L		—	X	L	L	—	—		—	OFF		—
—	—		—	H		—	X	L	L	—	—		—	ON		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		L	X	L	L	—	—		—	—		OFF
—	—		—	—		H	X	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	X	H	ALL SWITCHES (SW0~SW31) OFF						

Note 1: The 32 switches operate independently.

2: Serial data are clocked in on the L to H transition of the CLK0.

3: All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE0}$. When $\overline{LE0}$ is low the shift registers' data flow through the latch.

4: DOUT0 is high when data in Register 31 is high.

5: Shift register clocking has no effect on the switch states if $\overline{LE0}$ is high.

6: The CLR0 clear input overrides all the inputs.

TABLE 1-2: TRUTH TABLE(SPI1)

D32	D33	...	D47	D48	...	D63	$D_{IN}1$	$\overline{LE1}$	CLR1	SW32	SW33	...	SW47	SW48	...	SW63
L	—		—	—		—	X	L	L	OFF	—		—	—		—
H	—		—	—		—	X	L	L	ON	—		—	—		—
—	L		—	—		—	X	L	L	—	OFF		—	—		—
—	H		—	—		—	X	L	L	—	ON		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		L	—		—	X	L	L	—	—		OFF	—		—
—	—	...	H	—	...	—	X	L	L	—	—	...	ON	—	...	—
—	—		—	L		—	X	L	L	—	—		—	OFF		—
—	—		—	H		—	X	L	L	—	—		—	ON		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		—	X	L	L	—	—		—	—		—
—	—		—	—		L	X	L	L	—	—		—	—		OFF
—	—		—	—		H	X	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	X	H	ALL SWITCHES (SW32~SW63) OFF						

Note 1: The 32 switches operate independently.

2: Serial data are clocked in on the L to H transition of the CLK1.

3: All 32 switches go to a state retaining their latched condition at the rising edge of $\overline{LE1}$. When $\overline{LE1}$ is low the shift registers' data flow through the latch.

4: DOUT1 is high when data in Register 63 is high.

5: Shift register clocking has no effect on the switch states if $\overline{LE1}$ is high.

6: The CLR1 clear input overrides all the inputs.

2.0 PIN DESCRIPTION

This section details the pin description for the 169-Ball LFBGA package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	SW13T	SW13S	SW14T	SW15T	SW46T	SW47T	VDD0	SW48T	SW49T	SW16T	SW17T	SW18S	SW18T	A
B	SW12T	SW12S	SW14S	SW15S	SW46S	SW47S	VDD1	SW48S	SW49S	SW16S	SW17S	SW19S	SW19T	B
C	SW11T	SW11S	SW43T	SW43S	SW45T	SW45S	NC/ RGND0	SW50S	SW50T	SW52S	SW52T	SW20S	SW20T	C
D	SW10T	SW10S	SW42T	SW42S	SW44T	SW44S	NC/ RGND1	SW51S	SW51T	SW53S	SW53T	SW21S	SW21T	D
E	SW9T	SW9S	SW41T	SW41S	GND0	GND0	GND1	GND1	GND1	SW54S	SW54T	SW22S	SW22T	E
F	SW8T	SW8S	SW40T	SW40S	GND0	CLR0	DIN0	DOUT0	GND1	SW55S	SW55T	SW23S	SW23T	F
G	SW7T	SW7S	SW39T	SW39S	VLL0	CLR1	DIN1	DOUT1	VLL1	SW56S	SW56T	SW24S	SW24T	G
H	SW6T	SW6S	SW38T	SW38S	DGND0	LEb0	CLK0	CLK1	DGND1	SW57S	SW57T	SW25S	SW25T	H
J	SW5T	SW5S	SW37T	SW37S	GND0	GND0	LEb1	GND1	GND1	SW58S	SW58T	SW26S	SW26T	J
K	SW4T	SW4S	SW36T	SW36S	SW32S	GND0	GND0	GND1	SW63S	SW59S	SW59T	SW27S	SW27T	K
L	SW3T	SW3S	SW35T	SW35S	SW32T	GND0	GND1	GND1	SW63T	SW60S	SW60T	SW28S	SW28T	L
M	SW2T	SW2S	SW0S	SW34S	SW33S	VDD1	NC/ RGND1	VDD1	SW62S	SW61S	SW31S	SW29S	SW29T	M
N	SW1T	SW1S	SW0T	SW34T	SW33T	VDD0	NC/ RGND0	VDD0	SW62T	SW61T	SW31T	SW30S	SW30T	N
	1	2	3	4	5	6	7	8	9	10	11	12	13	

FIGURE 2-1: *Pin Map of HV2825/HV2925/HV2926 – Top View.*

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2825	HV2925/ HV2926	
A1	SW13T	SW13T	Analog Switch 13 SWT Terminal; Connect to a Piezoelectric Element.
A2	SW13S	SW13S	Analog Switch 13 SWS Terminal.
A3	SW14T	SW14T	Analog Switch 14 SWT Terminal; Connect to a Piezoelectric Element.
A4	SW15T	SW15T	Analog Switch 15 SWT Terminal; Connect to a Piezoelectric Element.
A5	SW46T	SW46T	Analog Switch 46 SWT Terminal; Connect to a Piezoelectric Element.
A6	SW47T	SW47T	Analog Switch 47 SWT Terminal; Connect to a Piezoelectric Element.
A7	V_{DD0}	V_{DD0}	Positive Supply Voltage.
A8	SW48T	SW48T	Analog Switch 48 SWT Terminal; Connect to a Piezoelectric Element.
A9	SW49T	SW49T	Analog Switch 49 SWT Terminal; Connect to a Piezoelectric Element.
A10	SW16T	SW16T	Analog Switch 16 SWT Terminal; Connect to a Piezoelectric Element.
A11	SW17T	SW17T	Analog Switch 17 SWT Terminal; Connect to a Piezoelectric Element.
A12	SW18S	SW18S	Analog Switch 18 SWS Terminal.
A13	SW18T	SW18T	Analog Switch 18 SWT Terminal; Connect to a Piezoelectric Element.
B1	SW12T	SW12T	Analog Switch 12 SWT Terminal; Connect to a Piezoelectric Element
B2	SW12S	SW12S	Analog Switch 12 SWS Terminal.
B3	SW14S	SW14S	Analog Switch 14 SWS Terminal.
B4	SW15S	SW15S	Analog Switch 15 SWS Terminal.
B5	SW46S	SW46S	Analog Switch 46 SWS Terminal.
B6	SW47S	SW47S	Analog Switch 47 SWS Terminal.
B7	V_{DD1}	V_{DD1}	Positive Supply Voltage.
B8	SW48S	SW48S	Analog Switch 48 SWS Terminal.
B9	SW49S	SW49S	Analog Switch 49 SWS Terminal.
B10	SW16S	SW16S	Analog Switch 16 SWS Terminal.
B11	SW17S	SW17S	Analog Switch 17 SWS Terminal.
B12	SW19S	SW19S	Analog Switch 19 SWS Terminal.
B13	SW19T	SW19T	Analog Switch 19 SWT Terminal; Connect to a Piezoelectric Element.
C1	SW11T	SW11T	Analog Switch 11 SWT Terminal; Connect to a Piezoelectric Element.
C2	SW11S	SW11S	Analog Switch 11 SWS Terminal.
C3	SW43T	SW43T	Analog Switch 43 SWT Terminal; Connect to a Piezoelectric Element.
C4	SW43S	SW43S	Analog Switch 43 SWS Terminal.
C5	SW45T	SW45T	Analog Switch 45 SWT Terminal; Connect to a Piezoelectric Element.
C6	SW45S	SW45S	Analog Switch 45 SWS Terminal.
C7	NC	RGND0	No Connection/Ground for Bleed Resistor.
C8	SW50S	SW50S	Analog Switch 50 SWS Terminal.
C9	SW50T	SW50T	Analog Switch 50 SWT Terminal; Connect to a Piezoelectric Element.
C10	SW52S	SW52S	Analog Switch 52 SWS Terminal.
C11	SW52T	SW52T	Analog Switch 52 SWT Terminal; Connect to a Piezoelectric Element.
C12	SW20S	SW20S	Analog Switch 20 SWS Terminal.
C13	SW20T	SW20T	Analog Switch 20 SWT Terminal; Connect to a Piezoelectric Element.
D1	SW10T	SW10T	Analog Switch 10 SWT Terminal; Connect to a Piezoelectric Element.
D2	SW10S	SW10S	Analog Switch 10 SWS Terminal.
D3	SW42T	SW42T	Analog Switch 42 SWT Terminal; Connect to a Piezoelectric Element.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2825	HV2925/ HV2926	
D4	SW42S	SW42S	Analog Switch 42 SWS Terminal.
D5	SW44T	SW44T	Analog Switch 44 SWT Terminal; Connect to a Piezoelectric Element.
D6	SW44S	SW44S	Analog Switch 44 SWS Terminal.
D7	NC	RGND1	No Connection/Ground for Bleed Resistor.
D8	SW51S	SW51S	Analog Switch 51 SWS Terminal.
D9	SW51T	SW51T	Analog Switch 51 SWT Terminal; Connect to a Piezoelectric Element.
D10	SW53S	SW53S	Analog Switch 53 SWS Terminal.
D11	SW53T	SW53T	Analog Switch 53 SWT Terminal; Connect to a Piezoelectric Element.
D12	SW21S	SW21S	Analog Switch 21 SWS Terminal.
D13	SW21T	SW21T	Analog Switch 21 SWT Terminal; Connect to a Piezoelectric Element.
E1	SW9T	SW9T	Analog Switch 9 SWT Terminal; Connect to a Piezoelectric Element.
E2	SW9S	SW9S	Analog Switch 9 SWS Terminal.
E3	SW41T	SW41T	Analog Switch 41 SWT Terminal; Connect to a Piezoelectric Element.
E4	SW41S	SW41S	Analog Switch 41 SWS Terminal.
E5~E6	GND0	GND0	Ground
E7~E9	GND1	GND1	Ground
E10	SW54S	SW54S	Analog Switch 54 SWS Terminal.
E11	SW54T	SW54T	Analog Switch 54 SWT Terminal; Connect to a Piezoelectric Element.
E12	SW22S	SW22S	Analog Switch 22 SWS Terminal.
E13	SW22T	SW22T	Analog Switch 22 SWT Terminal; Connect to a Piezoelectric Element.
F1	SW8T	SW8T	Analog Switch 8 SWT Terminal; Connect to a Piezoelectric Element.
F2	SW8S	SW8S	Analog Switch 8 SWS Terminal.
F3	SW40T	SW40T	Analog Switch 40 SWT Terminal; Connect to a Piezoelectric Element.
F4	SW40S	SW40S	Analog Switch 40 SWS Terminal.
F5	GND0	GND0	Ground
F6	CLR0	CLR0	Latch Clear Logic Input.
F7	D_{IN0}	D_{IN0}	Data In Logic Input.
F8	D_{OUT0}	D_{OUT0}	Data Out Logic Output.
F9	GND1	GND1	Ground
F10	SW55S	SW55S	Analog Switch 55 SWS Terminal.
F11	SW55T	SW55T	Analog Switch 55 SWT Terminal; Connect to a Piezoelectric Element.
F12	SW23S	SW23S	Analog Switch 23 SWS Terminal.
F13	SW23T	SW23T	Analog Switch 23 SWT Terminal; Connect to a Piezoelectric Element.
G1	SW7T	SW7T	Analog Switch 7 SWT Terminal; Connect to a Piezoelectric Element.
G2	SW7S	SW7S	Analog Switch 7 SWS Terminal.
G3	SW39T	SW39T	Analog Switch 39 SWT Terminal; Connect to a Piezoelectric Element.
G4	SW39S	SW39S	Analog Switch 39 SWS Terminal.
G5	V_{LL0}	V_{LL0}	Logic Supply Voltage.
G6	CLR1	CLR1	Latch Clear Logic Input.
G7	D_{IN1}	D_{IN1}	Data In Logic Input.
G8	D_{OUT1}	D_{OUT1}	Data Out Logic Input.
G9	V_{LL1}	V_{LL1}	Logic Supply Voltage.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2825	HV2925/ HV2926	
G10	SW56S	SW56S	Analog Switch 56 SWS Terminal.
G11	SW56T	SW56T	Analog Switch 56 SWT Terminal; Connect to a Piezoelectric Element.
G12	SW24S	SW24S	Analog Switch 24 SWS Terminal.
G13	SW24T	SW24T	Analog Switch 24 SWT Terminal; Connect to a Piezoelectric Element.
H1	SW6T	SW6T	Analog Switch 6 SWT Terminal; Connect to a Piezoelectric Element.
H2	SW6S	SW6S	Analog Switch 6 SWS Terminal.
H3	SW38T	SW38T	Analog Switch 38 SWT Terminal; Connect to a Piezoelectric Element.
H4	SW38S	SW38S	Analog Switch 38 SWS Terminal.
H5	DGND0	DGND0	Digital Ground For Logic Circuitry.
H6	$\overline{LE0}$	$\overline{LE0}$	Latch Enable Logic Input, Low Active.
H7	CLK0	CLK0	Clock Logic Input For Shift Register.
H8	CLK1	CLK1	Clock Logic Input For Shift Register.
H9	DGND1	DGND1	Digital Ground For Logic Circuitry.
H10	SW57S	SW57S	Analog Switch 57 SWS Terminal.
H11	SW57T	SW57T	Analog Switch 57 SWT Terminal; Connect to a Piezoelectric Element.
H12	SW25S	SW25S	Analog Switch 25 SWS Terminal.
H13	SW25T	SW25T	Analog Switch 25 SWT Terminal; Connect to a Piezoelectric Element.
J1	SW5T	SW5T	Analog Switch 5 SWT Terminal; Connect to a Piezoelectric Element.
J2	SW5S	SW5S	Analog Switch 5 SWS Terminal.
J3	SW37T	SW37T	Analog Switch 37 SWT Terminal; Connect to a Piezoelectric Element.
J4	SW37S	SW37S	Analog Switch 37 SWS Terminal.
J5~J6	GND0	GND0	Ground.
E7	$\overline{LE1}$	$\overline{LE1}$	Latch Enable Logic Input, Low Active.
J8~J9	GND1	GND1	Ground.
J10	SW58S	SW58S	Analog Switch 58 SWS Terminal.
J11	SW58T	SW58T	Analog Switch 58 SWT Terminal; Connect to a Piezoelectric Element.
J12	SW26S	SW26S	Analog Switch 26 SWS Terminal.
J13	SW26T	SW26T	Analog Switch 26 SWT Terminal; Connect to a Piezoelectric Element.
K1	SW4T	SW4T	Analog Switch 4 SWT Terminal; Connect to a Piezoelectric Element.
K2	SW4S	SW4S	Analog Switch 4 SWS Terminal.
K3	SW36T	SW36T	Analog Switch 36 SWT Terminal; Connect to a Piezoelectric Element.
K4	SW36S	SW36S	Analog Switch 36 SWS Terminal.
K5	SW32S	SW32S	Analog Switch 32 SWS Terminal.
K6~K7	GND0	GND0	Ground.
K8	GND1	GND1	Ground.
K9	SW63S	SW63S	Analog Switch 63 SWS Terminal.
K10	SW59S	SW59S	Analog Switch 59 SWS Terminal.
K11	SW59T	SW59T	Analog Switch 59 SWT Terminal; Connect to a Piezoelectric Element.
K12	SW27S	SW27S	Analog Switch 27 SWS Terminal.
K13	SW27T	SW27T	Analog Switch 27 SWT Terminal; Connect to a Piezoelectric Element.
L1	SW3T	SW3T	Analog Switch 3 SWT Terminal; Connect to a Piezoelectric Element.
L2	SW3S	SW3S	Analog Switch 3 SWS Terminal.

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Symbol		Description
	HV2825	HV2925/ HV2926	
L3	SW35T	SW35T	Analog Switch 35 SWT Terminal; Connect to a Piezoelectric Element.
L4	SW35S	SW35S	Analog Switch 35 SWS Terminal.
L5	SW32T	SW32T	Analog Switch 32 SWT Terminal; Connect to a Piezoelectric Element.
L6	GND0	GND0	Ground.
L7~L8	GND1	GND1	Ground.
L9	SW63T	SW63T	Analog Switch 63 SWT Terminal; Connect to a Piezoelectric Element.
L10	SW60S	SW60S	Analog Switch 60 SWS Terminal.
L11	SW60T	SW60T	Analog Switch 60 SWT Terminal; Connect to a Piezoelectric Element.
L12	SW28S	SW28S	Analog Switch 28 SWS Terminal.
L13	SW28T	SW28T	Analog Switch 28 SWT Terminal; Connect to a Piezoelectric Element.
M1	SW2T	SW2T	Analog Switch 2 SWT Terminal; Connect to a Piezoelectric Element.
M2	SW2S	SW2S	Analog Switch 2 SWS Terminal.
M3	SW0S	SW0S	Analog Switch 0 SWS Terminal.
M4	SW34S	SW34S	Analog Switch 34 SWS Terminal.
M5	SW33S	SW33S	Analog Switch 33 SWS Terminal.
M6	V_{DD1}	V_{DD1}	Positive Supply Voltage.
M7	NC	RGND1	No Connection/Ground for Bleed Resistor.
M8	V_{DD1}	V_{DD1}	Positive Supply Voltage.
M9	SW62S	SW62S	Analog Switch 62 SWS Terminal.
M10	SW61S	SW61S	Analog Switch 61 SWS Terminal.
M11	SW31S	SW31S	Analog Switch 31 SWS Terminal.
M12	SW29S	SW29S	Analog Switch 29 SWS Terminal.
M13	SW29T	SW29T	Analog Switch 29 SWT Terminal; Connect to a Piezoelectric Element.
N1	SW1T	SW1T	Analog Switch 1 SWT Terminal; Connect to a Piezoelectric Element.
N2	SW1S	SW1S	Analog Switch 1 SWS Terminal.
N3	SW0T	SW0T	Analog Switch 0 SWT Terminal; Connect to a Piezoelectric Element.
N4	SW34T	SW34T	Analog Switch 34 SWT Terminal; Connect to a Piezoelectric Element.
N5	SW33T	SW33T	Analog Switch 33 SWT Terminal; Connect to a Piezoelectric Element.
N6	V_{DD0}	V_{DD0}	Positive Supply Voltage.
N7	NC	RGND0	No Connection/Ground for Bleed Resistor.
N8	V_{DD0}	V_{DD0}	Positive Supply Voltage.
N9	SW62T	SW62T	Analog Switch 62 SWT Terminal; Connect to a Piezoelectric Element.
N10	SW61T	SW61T	Analog Switch 61 SWT Terminal; Connect to a Piezoelectric Element.
N11	SW31T	SW31T	Analog Switch 31 SWT Terminal; Connect to a Piezoelectric Element.
N12	SW30S	SW30S	Analog Switch 30 SWS Terminal.
N13	SW30T	SW30T	Analog Switch 30 SWT Terminal; Connect to a Piezoelectric Element.

3.0 TEST CIRCUIT EXAMPLES

This section details a few example of test circuits.

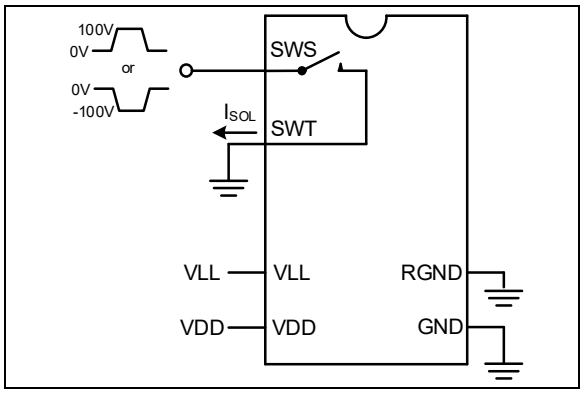


FIGURE 3-1: *Switch-Off Leakage SWT.*

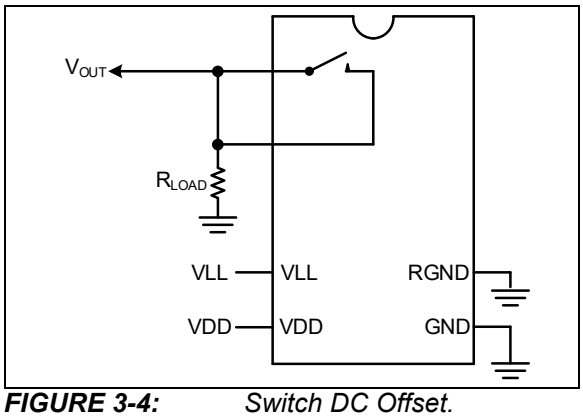


FIGURE 3-4: *Switch DC Offset.*

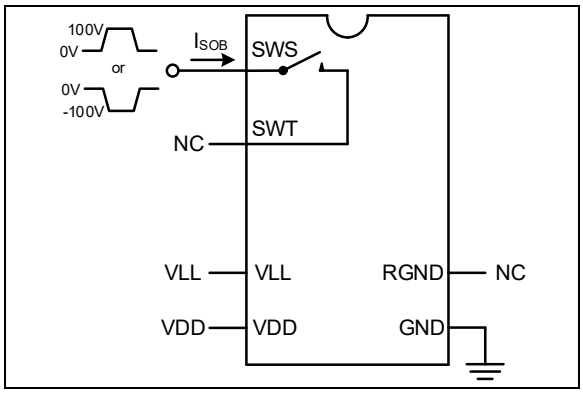


FIGURE 3-2: *Switch-Off Bias SWS.*

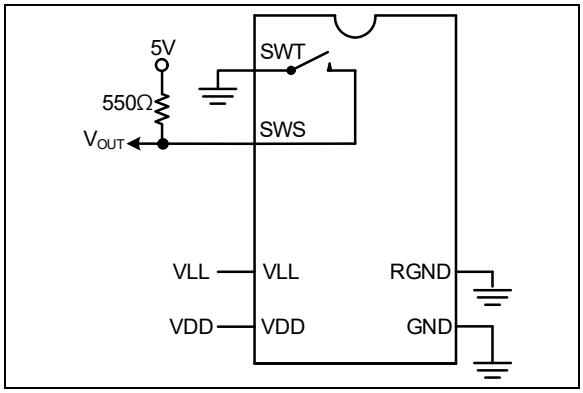


FIGURE 3-5: *T_{ON}/T_{OFF} Test Circuit.*

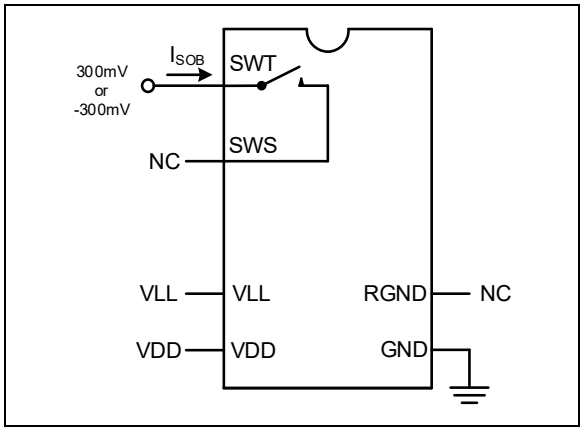


FIGURE 3-3: *Switch-Off Bias SWT.*

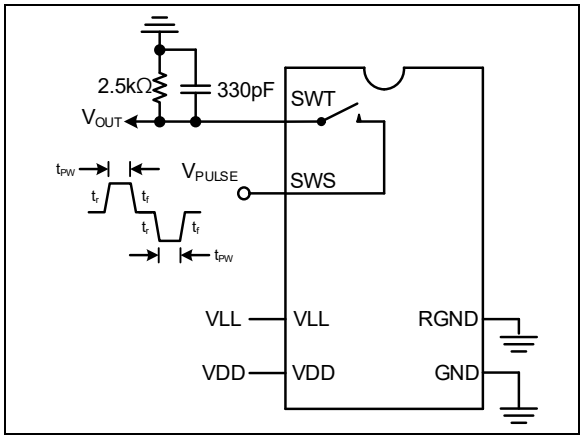


FIGURE 3-6: *Tx Pulse Width.*

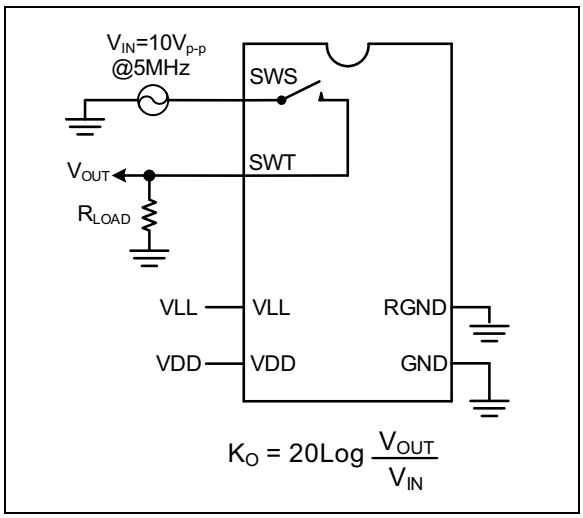


FIGURE 3-7: *Off Isolation SWS to SWT.*

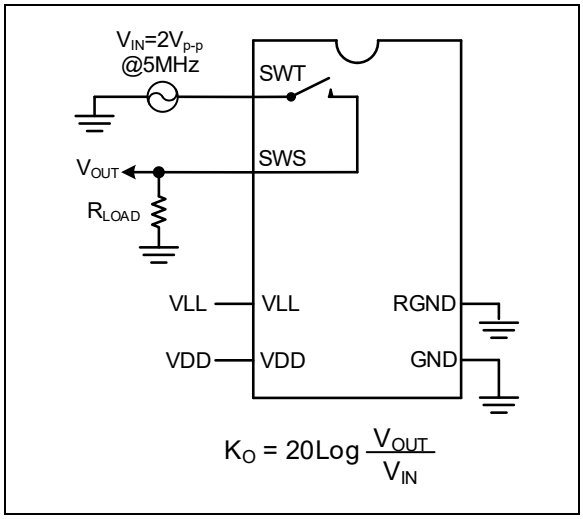


FIGURE 3-8: *Off Isolation SWT to SWS.*

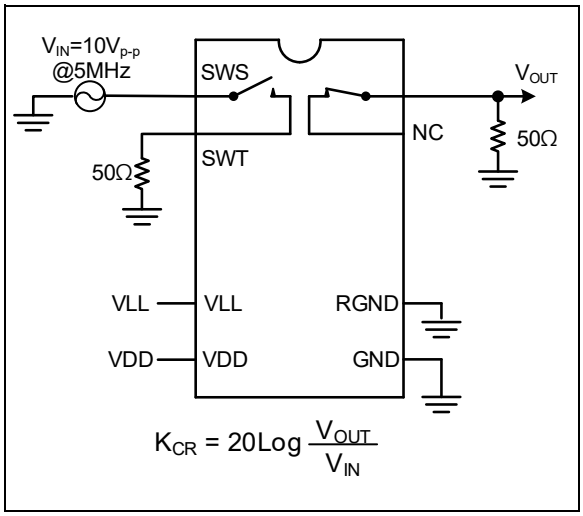


FIGURE 3-9: *Switch Crosstalk.*

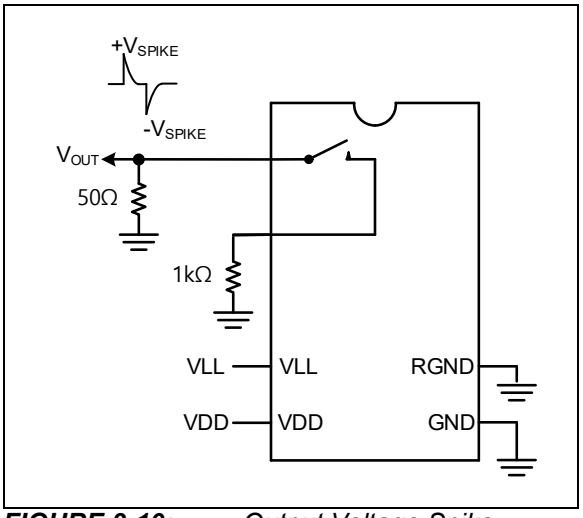


FIGURE 3-10: *Output Voltage Spike.*

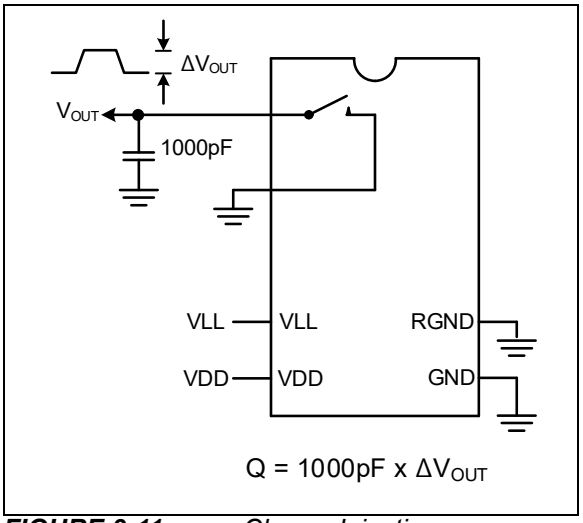


FIGURE 3-11: *Charge Injection.*

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: V_{DD} = +5V, V_{LL} = +5V, T_A = +25°C.

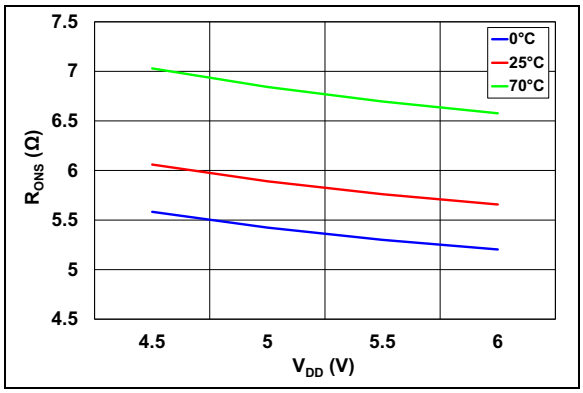


FIGURE 4-1: *R_{ONS} at 5 mA vs. V_{DD}.*

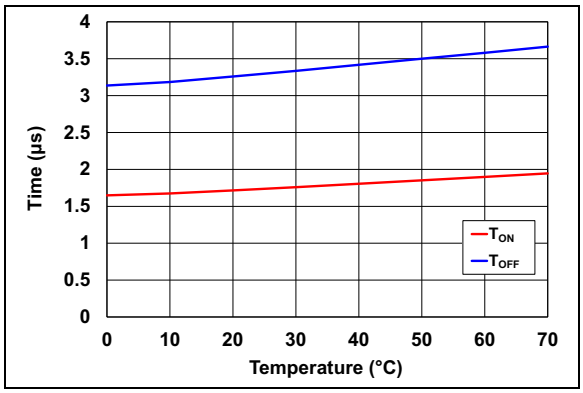


FIGURE 4-4: *T_{ON}/T_{OFF} vs. Temperature.*

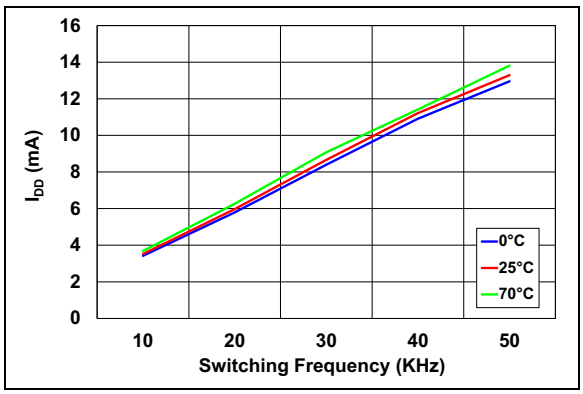


FIGURE 4-2: *I_{DD} vs. Switching Frequency.*

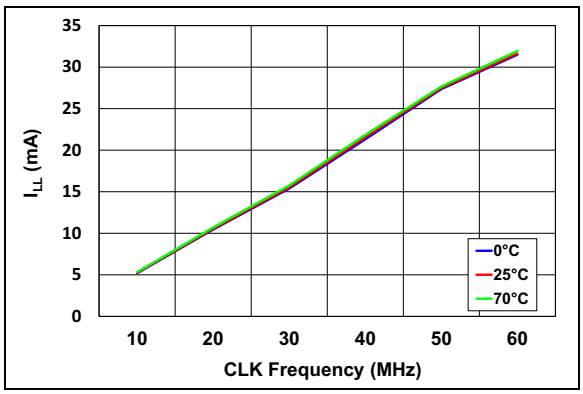


FIGURE 4-5: *I_{LL} vs. CLK Frequency.*

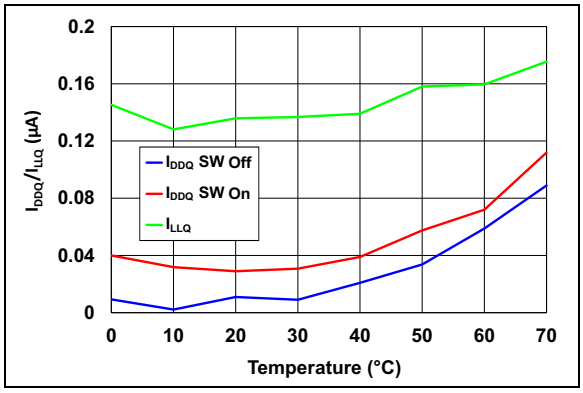


FIGURE 4-3: *I_{DDQ}/I_{LLQ} vs. Temperature.*

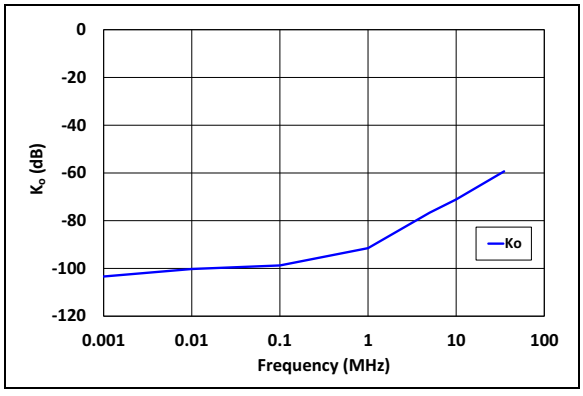


FIGURE 4-6: *K_O, SWS to SWT vs. Frequency with 50Ω Load.*

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

As it is depicted in the Block Diagram, two independent sets of the shifted registers are controlled by two SPI independently. After the SPI, two sets of 32-bit shift registers with latches deliver and store ON/OFF configuration bits of the switches. The bit information is level-shifted and buffered to drive the output switches connected with SWS and SWT pins. The different configurations of the bleed resistors allow users to dissipate the charge built up at the switches based on what they need to fit their applications.

5.2 Logic Input Timing

Figure 5-1 is the logic input timing diagram to show the control waveforms. Table 1-1 is the truth table of SPI0 control logic for details. The truth table of SPI1 control logic is identical as that in SPI0 (see Table 1-2). The data is shifted into the shift registers on the rising edge (low to high transition) of the clock. The switch configuration bit of SW31 or SW63 is shifted in first and the configuration bit of SW0 or SW32 is shifted in last. The timing waveforms are indicated in Figure 5-2. To avoid the configuration bits changing the status of the analog switches during programming, the latch enable bar inputs ($\overline{LE0}$ and $\overline{LE1}$) should remain high while the two 32-bit data-in signals are shifted into the two sets of 32-bit registers. After the valid 32-bit data complete shifting into the registers, the high to low transition of the $\overline{LE0}$ and $\overline{LE1}$ signals transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE0}$ high again allows all the latches to keep the current state while new data can now be shifted into the shift registers without upsetting the latches. It is recommended to change all the latch states at the same time through this method to avoid possible clock-feedthrough noise.

When the CLR0 input is set high, all 32 latches are cleared of the data. Consequently, all the high-voltage switches are set to an off state. However, the CLR0 signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR0 signal. Hence, after the CLR0 input is set low, the shift register would still retain the previous data. The operation of SPI1 logic inputs is identical to SPI0.

5.3 Multiple Devices Connection

HV2825/HV2925/HV2926 has two sets of SPI (SPI0 and SPI1) consisting of Data-In pins (DIN0 and DIN1), Clock pins (CLK0 and CLK1), Data-Out pins (DOUT0 and DOUT1), Latch-Enable-bar pins ($\overline{LE0}$ and $\overline{LE1}$), and Clear pins (CLR0 and CLR1) for programming switch ON/OFF states individually. The SPI0 controls 32 switches from SW0 to SW31 and SPI1 controls 32 switches from SW32 to SW63.

For higher speed control, users can apply two SPI in parallel and then only 32 clocks are required to program 64 switches. They can also use HV2825/HV2925/HV2926 in one SPI configuration by daisy-chaining SPI0 and SPI1. In the daisy chain, DOUT0 is connected to DIN1. The two CLK, $\overline{LE}$ and CLR pins are tied together. DIN0 becomes the data input for 64-bit shift registers and DOUT1 becomes the data output. Figure 5-3 illustrates the daisy chain connection of two HV2825/HV2925/HV2926 in single SPI and dual SPI operations. The digital circuits are supplied by V_{LL}. The serial clock frequency is up to 66 MHz.

5.4 Power-up/Down Sequence

The recommended power-up sequence of HV2825/HV2925/HV2926 is V_{LL} to power up first, then V_{DD} follows. The power-down sequence is in reverse order of power-up sequence. During the power-up or power-down period, all the analog switch inputs should stay within V_{DD} and GND range, no matter if connected with other components or floating without any connection.

5.5 Layout Considerations

HV2825/HV2925/HV2926 devices have two separate ground connections. DGND is the ground connection for digital circuitry, and GND is the ground connection for substrate and analog switches. DGND pins and GND pins will be shorted on the boards to reduce ground bounces caused by the routing resistance when the rush current passes through it. V_{LL} and V_{DD} require decoupling capacitors located close to the supply pins of the devices. Ceramic capacitors are preferred to provide low ESR and ESL for decoupling. If V_{LL} is too noisy, a ferrite bead may be needed to filter out the noise before connecting the V_{LL} to the local decoupling capacitors.

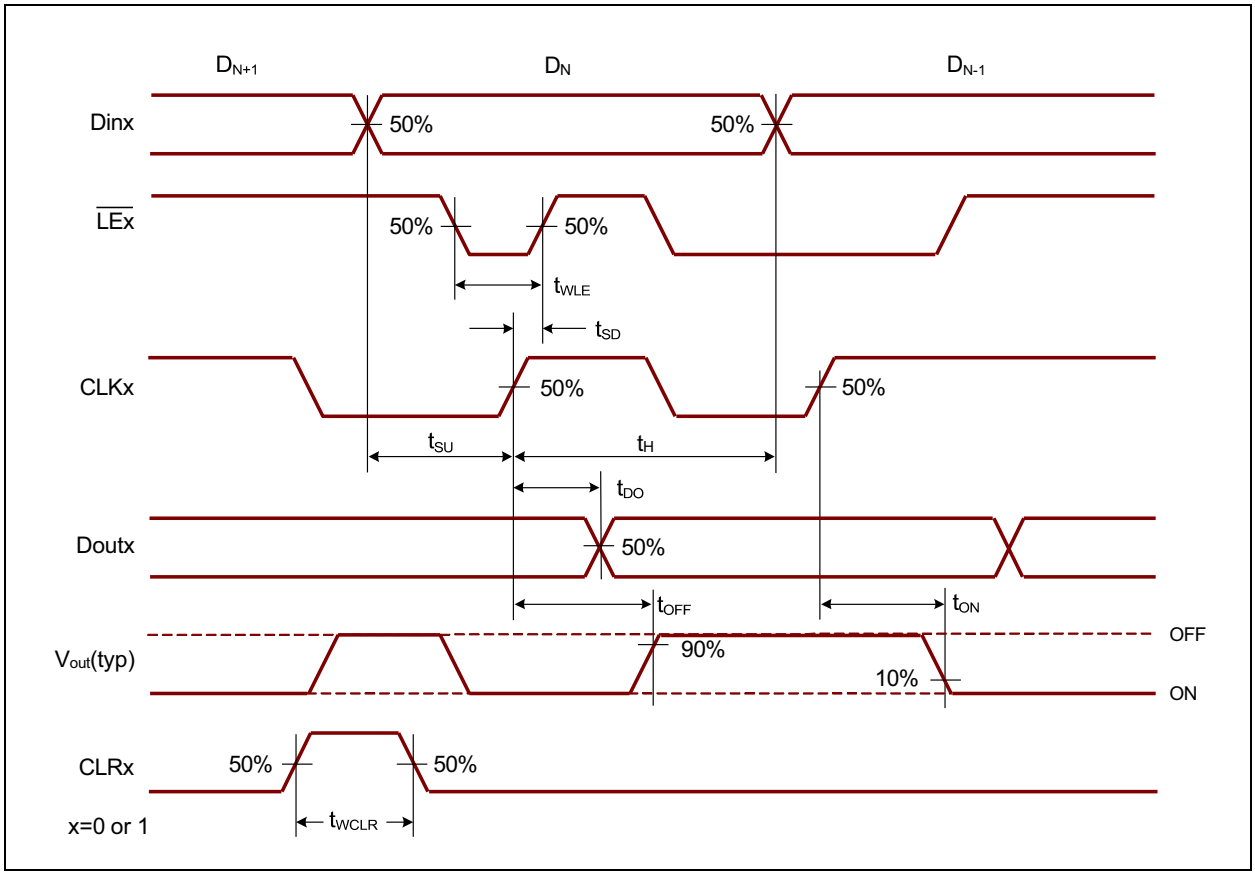


FIGURE 5-1: *Logic Input Timing Waveforms.*

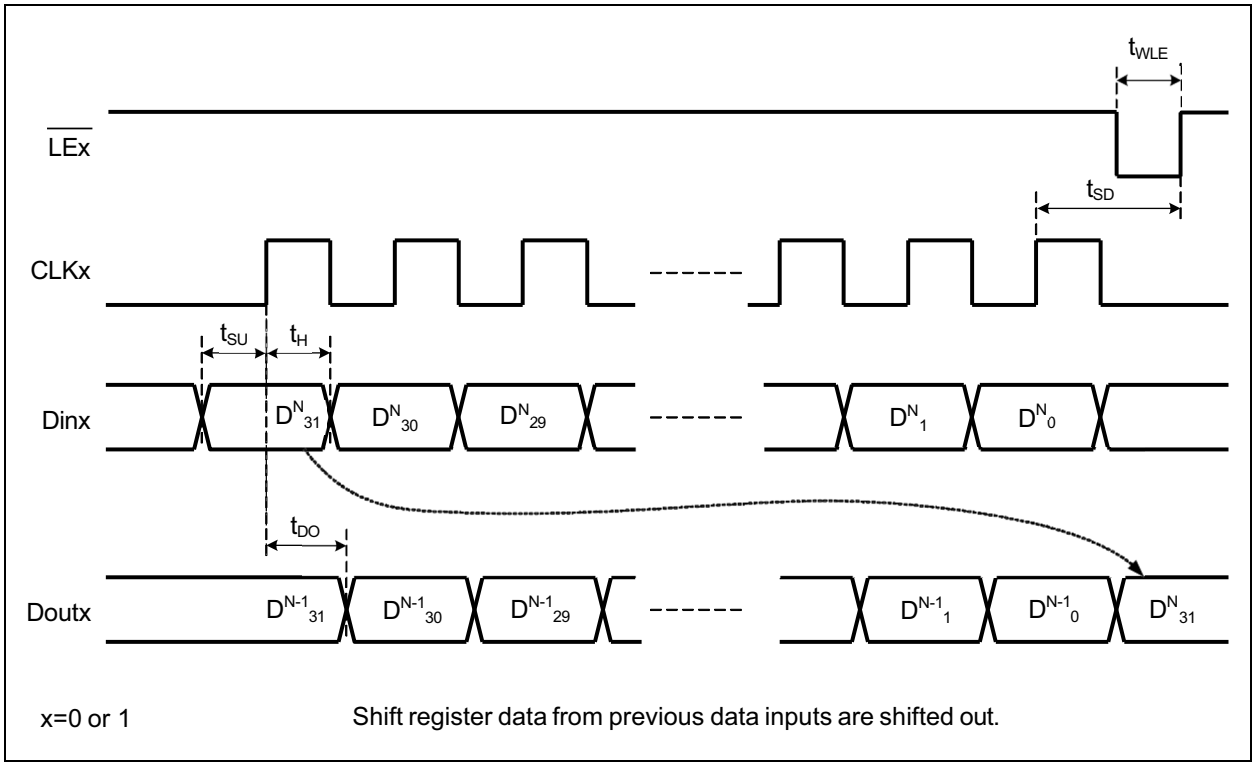
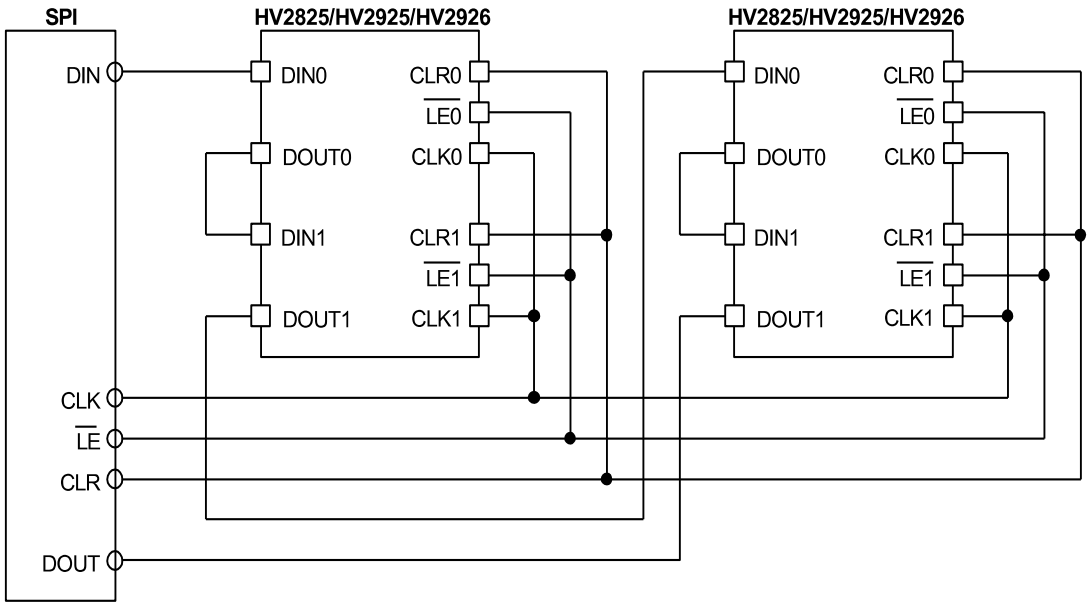


FIGURE 5-2: *Latch Enable Timing Diagram.*

Daisy Chain in Single SPI



Daisy Chain in Dual SPI

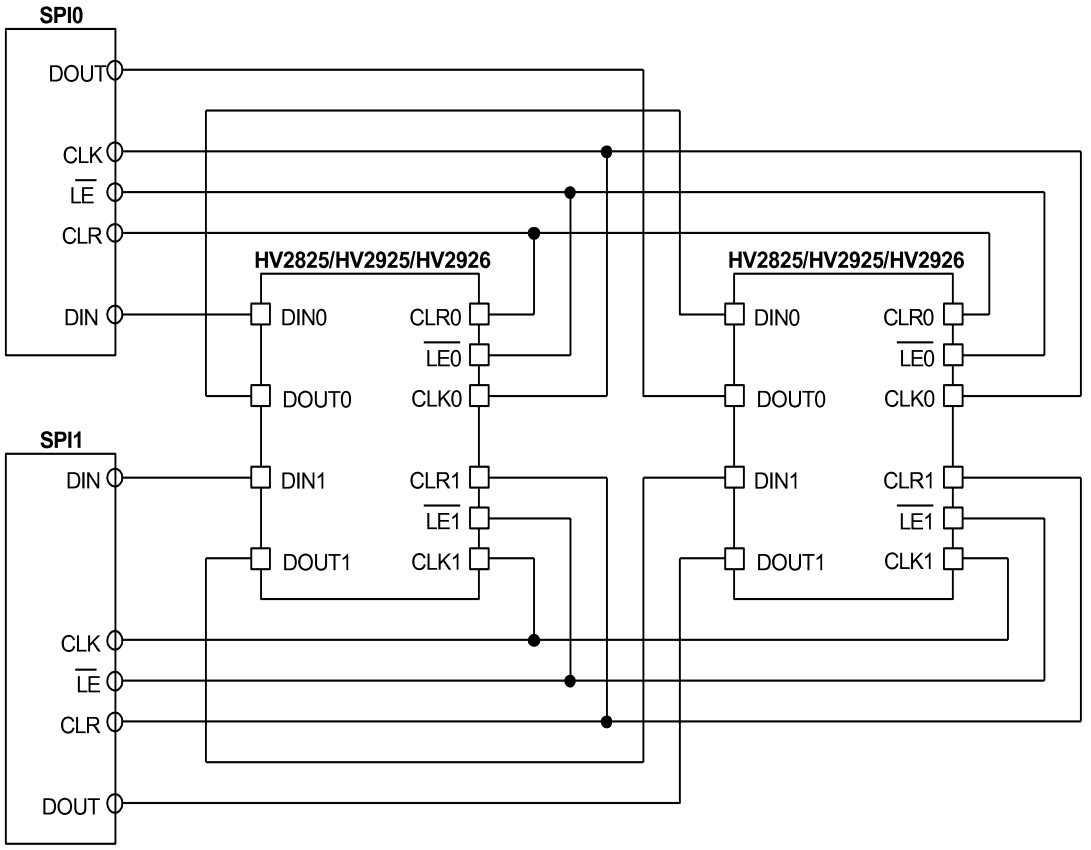
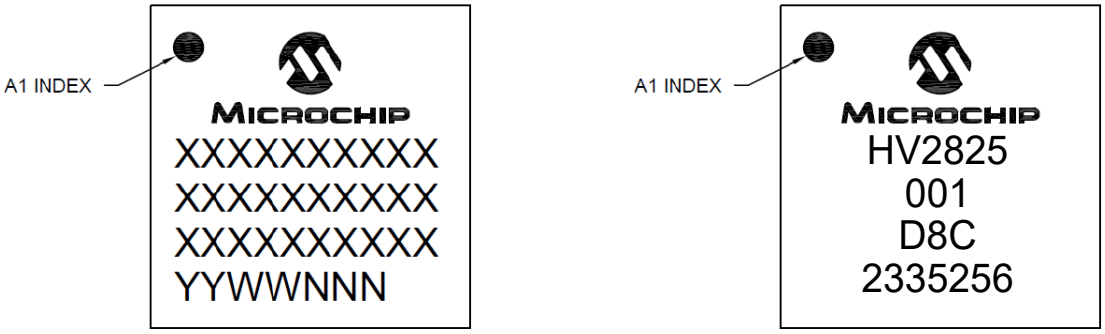


FIGURE 5-3: *Daisy Chain Connection in Single and Dual Configurations.*

6.0 PACKAGING INFORMATION

6.1 Package Marking Information

169-Lead LFBGA (11 x 11 x 1.50 mm) Example



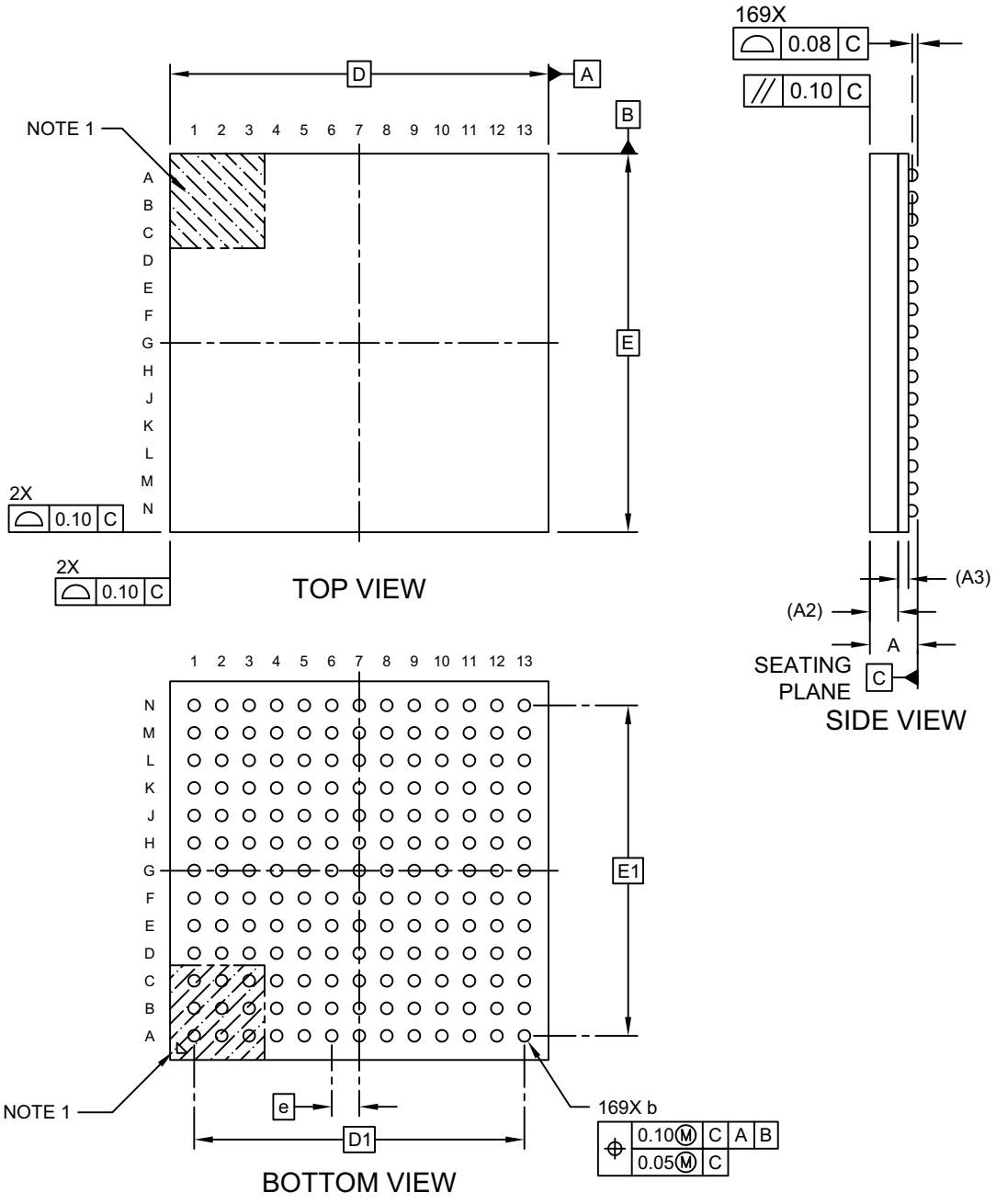
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

169-Ball Low Profile Fine-Pitch Ball Grid Array (D8C) - 11×11×1.50 mm Body [LFBGA]

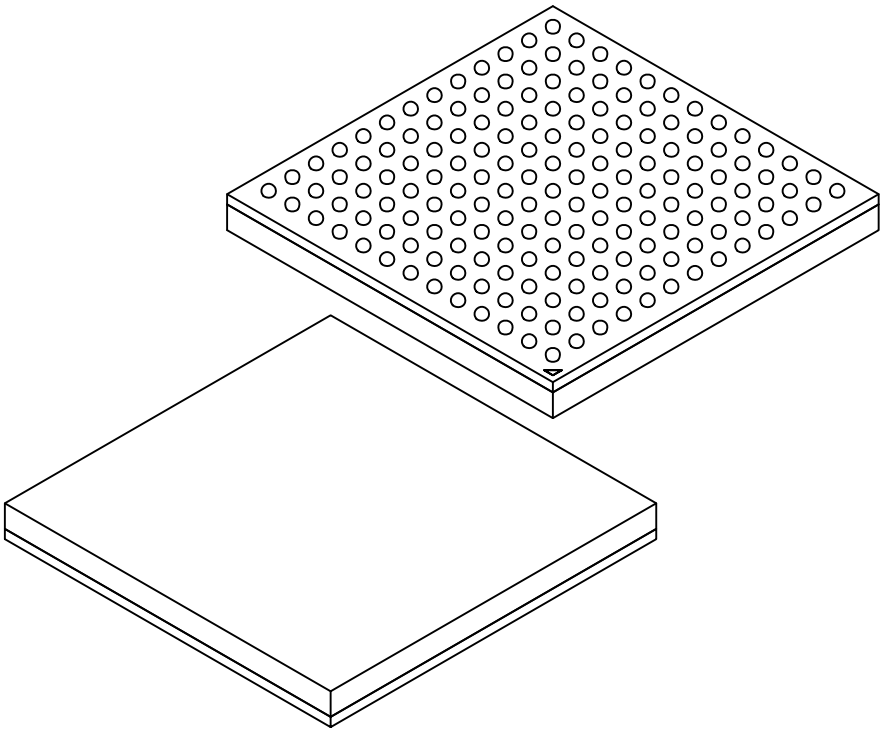
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25535 Rev C Sheet 1 of 2

169-Ball Low Profile Fine-Pitch Ball Grid Array (D8C) - 11×11×1.50 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		169	
Pitch	e		0.80 BSC	
Overall Height	A	1.31	1.39	1.50
Mold Thickness	A2		0.86 REF	
Substrate Thickness	A3		0.26 REF	
Overall Length	D		11.00 BSC	
Ball Array Length	D1		9.60 BSC	
Overall Width	E		11.00 BSC	
Ball Array Width	E1		9.60 BSC	
Ball Diameter	b	0.32	–	0.42

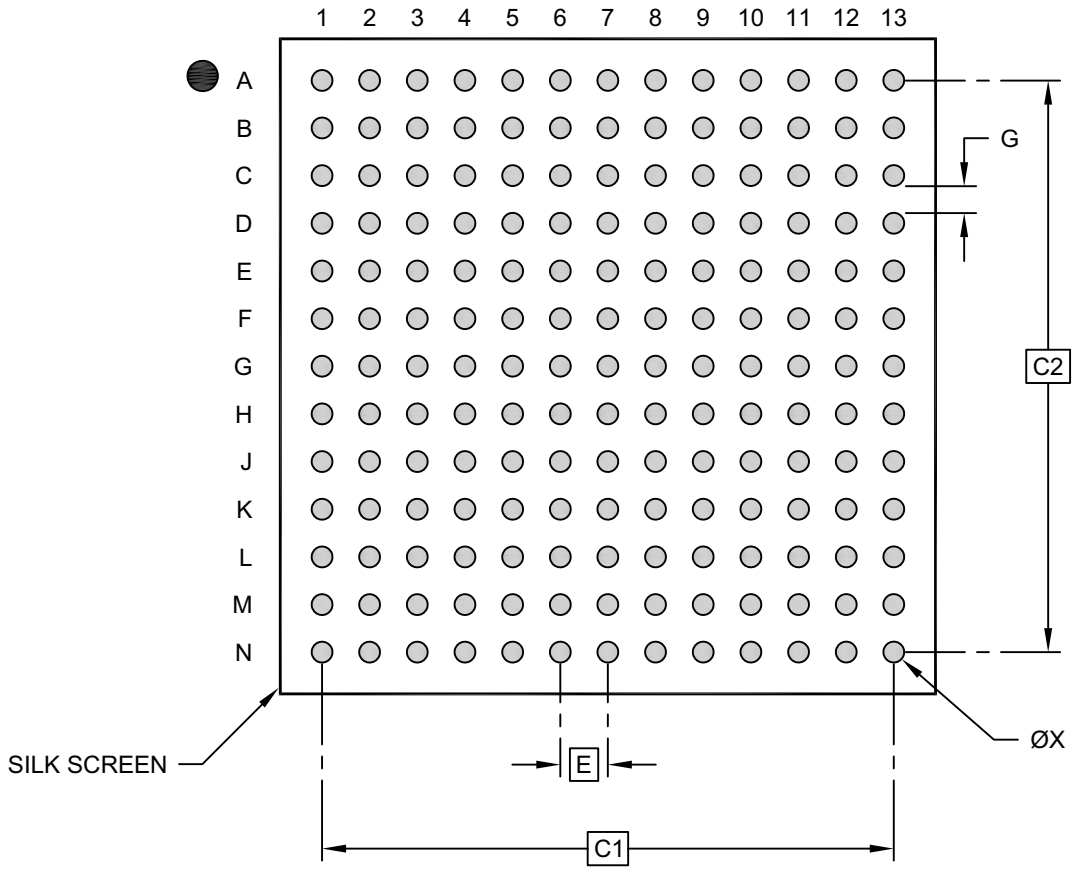
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25535 Rev C Sheet 2 of 2

169-Ball Low Profile Fine-Pitch Ball Grid Array (D8C) - 11×11×1.50 mm Body [LFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		9.60 BSC	
Contact Pad Spacing	C2		9.60 BSC	
Contact Pad Width (X169)	X			0.35
Contact Pad to Contact Pad	G	0.45		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-27535 Rev C

APPENDIX A: REVISION HISTORY

Revision A (December 2023)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	/XXX
Device	Package

Device:	HV2825:	Single 5V Bias, Low Harmonic Distortion, 64-Channel High-Voltage Analog Switch
	HV2925:	Single 5V Bias, Low Harmonic Distortion, 64-Channel High-Voltage Analog Switch with Bleed Resistor
	HV2926:	Single 5V Bias, Low Harmonic Distortion, 64-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch
Package:	D8C =	Low Profile Fine Pitch Ball Grid Array – 11x11x1.50 mm (LFBGA), 169-Ball

Examples:

a) HV2825/D8C: Single 5V Bias, Low Harmonic Distortion, 64-Channel High-Voltage Analog Switch, low Profile Fine Pitch Ball Grid Array (LFBGA), 169-Ball Package

b) HV2925/D8C: Single 5V Bias, Low Harmonic Distortion, 64-Channel High-Voltage Analog Switch with Bleed Resistor, Low Profile Fine Pitch Ball Grid Array (LFBGA), 169-Ball Package

c) HV2926/D8C: Single 5V Bias, Low Harmonic Distortion, 64-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch, Low Profile Fine Pitch Ball Grid Array (LFBGA), 169-Ball Package

NOTES:

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