ON Semiconductor®

FSFM260N / FSFM261N / FSFM300N Green-Mode ON Semiconductor Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET
- Advanced Burst-Mode Operation Consumes Under 1W at 240V_{AC} and 0.5W Load
- Precision Fixed Operating Frequency: 67kHz
- Internal Startup Circuit
- Over-Voltage Protection (OVP)
- Overload Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Abnormal Over-Current Protection (AOCP)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO) with Hysteresis
- Low Operating Current: 2.5mA
- Built-in Soft-Start: 15ms

Applications

- Power Supply for LCD TV and Monitor, VCR, SVR, STB, DVD, and DVD Recorder
- Adapter

Description

The FSFM260/261/300 is an integrated Pulse Width Modulator (PWM) and SenseFET specifically designed for high-performance offline Switch Mode Power Supplies (SMPS) with minimal external components.

This device is an integrated high-voltage power-switching regulator that combines an avalanche-rugged SenseFET with a current-mode PWM control block. The PWM controller includes an integrated fixed-frequency oscillator, under-voltage lockout, leading-edge blanking (LEB), optimized gate driver, internal soft-start, temperature-compensated precise-current sources for a loop compensation, and self-protection circuitry. Compared with discrete MOSFET and PWM controller solutions, it can reduce total cost, component count, size, and weight while simultaneously increasing efficiency, productivity, and system reliability. This device is a basic platform for cost-effective designs of flyback converters.

May-2024, Rev. 3
Publication Order Number:
FSFM260N/D

Ordering Information

Product Number	PKG.(5)	Operating Temp.	Current Limit	$R_{DS(ON)}$ Max.	Maximum Output Power(1)				Replaces Devices
					230V_{AC}±15%(2)		85-265V_{AC}		
					Adapter(3)	Open Frame(4)	Adapter(3)	Open Frame(4)	
FSFM260N	8-DIP	-25 to +85°C	1.5A	2.6Ω	23W	35W	17W	26W	FSDM0465RS FSQ0465RS
FSFM261N	8-DIP	-25 to +85°C	1.5A	2.7Ω	23W	35W	17W	26W	
FSFM300N	8-DIP	-25 to +85°C	1.6A	2.2Ω	26W	40W	20W	30W	

Notes:

1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open-frame design at 50°C ambient.
5. Eco status for all the FSFM260N, FSFM261N and FSFM300NS is RoHS.

Application Diagram

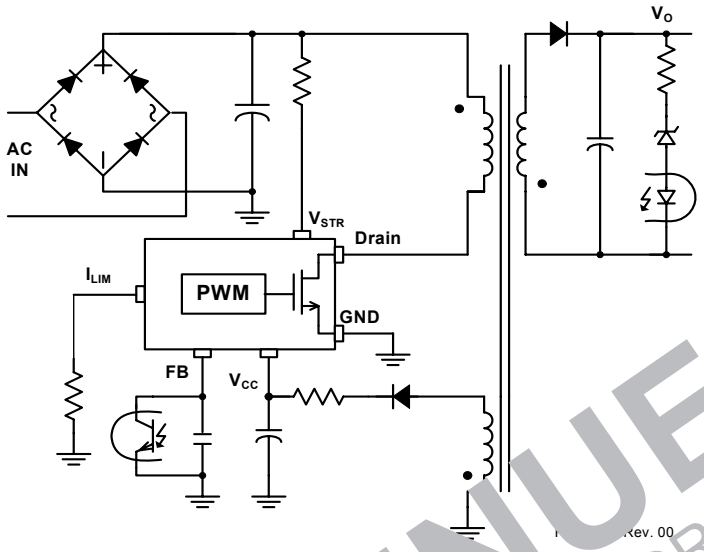


Figure 1. Typical Flyback Application

Internal Block Diagram

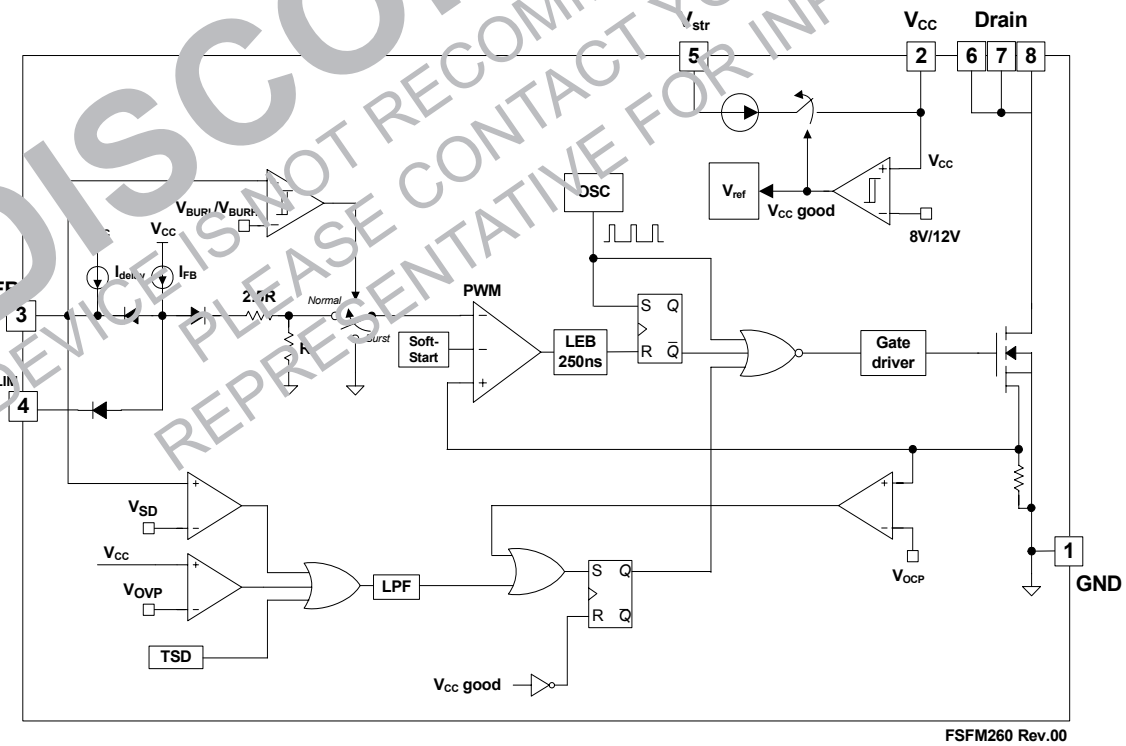
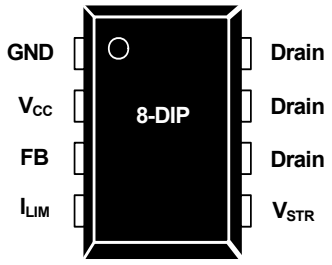


Figure 2. Internal Block Diagram

Pin Configuration



FSFM260 Rev.1.0.0

Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	**Ground**. This pin is the control ground and the SenseFET source.
2	V_{CC}	**Power Supply**. This pin is the positive supply input, providing internal operating current for both startup and steady-state operation.
3	FB	**Feedback**. This pin is internally connected to the inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 6V, the overload protection triggers, which shuts down the FPS.
4	I_{LIM}	**Peak Current Limit**. Adjusts the peak current limit of the SenseFET. The feedback 0.9mA current source is converted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the peak current limit.
5	V_{STR}	**Startup**. This pin is connected directly, or through a resistor, to the high-voltage DC link. At startup, the internal high-voltage current source supplies internal bias and charges the external capacitor connected to the V_{CC} pin. Once V_{CC} reaches 12V, the internal current source is disabled. It is not recommended to connect V_{STR} and drain together.
6, 7, 8	Drain	**SenseFET Drain**. High-voltage power SenseFET drain connection.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C, unless otherwise specified.

Symbol	Parameter		Min.	Max.	Unit
V_{STR}	V_{STR} Pin Voltage		650		V
$V_{DS}1$	Drain Pin Voltage of FSFM260N and FSFM300N		650		V
$V_{DS}2$	Drain Pin Voltage of FSFM261N		700		V
V_{CC}	Supply Voltage			21	V
V_{FB}	Feedback Voltage Range(6)		-0.3		V
I_{DM}	Drain Current Pulsed			9.6	A
I_D	Continuous Drain Current of FSFM260 and FSFM261(7)	T_C = 25°C		2.2	A
		T_C = 100°C		1.4	
	Continuous Drain Current of FSFM300(7)	T_C = 25°C		2.8	
		T_C = 100°C		1.7	
E_{AS}	Single Pulsed Avalanche Energy(8)	FSFM260 and FSFM261		120	mJ
		FSFM300		90	
P_D	Total Power Dissipation (T_C=25°C)			1.5	W
T_J	Operating Junction Temperature		Internally Limited		°C
T_A	Operating Ambient Temperature		-25	+85	°C
T_{STG}	Storage Temperature		-55	+150	°C
ESD	Electrostatic Discharge Capability Human Body Model, JESD22-A114		2.0		kV
	Electrostatic Discharge Capability Charged Device Model, JESD22-C110		2.0		

Notes:

6. V_{FB} is internally clamped and its maximum clamping current capability is 100μA.
7. Repetitive rating: pulse width limited by maximum junction temperature.
8. L=14mH, starting T_J=25°C.

Thermal Impedance

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Package	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance(9)	8-DIP	80	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance(10)		20	°C/W
Ψ_{JT}	Junction-to-Top Thermal Resistance(11)		35	°C/W

Notes:

9. Free standing with no heat-sink under natural convection.
10. Infinite cooling condition - refer to the SEMI G30-88.
11. Measured on the package top surface.

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SenseFET Section						
$BV_{DSS}1$	Drain Source Breakdown Voltage of FSFM260 and FSFM300	V_{CC} = 0V, I_D = 250μA	650			V
$BV_{DSS}2$	Drain Source Breakdown Voltage of FSFM261	V_{CC} = 0V, I_D = 250μA	700			V
I_{DSS1}	Zero Gate Voltage Drain Current1	V_{DS} = 650V, V_{GS} = 0V, T_C = 25°C			250	μA
I_{DSS2}	Zero Gate Voltage Drain Current2	V_{DS} = 520V, V_{GS} = 0V, T_C = 125°C			250	μA
$R_{DS(ON)}$	Static Drain Source on Resistance of FSFM260[12]	V_{GS} = 10V, I_D = 2.5A			2.60	Ω
	Static Drain Source on Resistance of FSFM261[12]			2.30	2.70	Ω
	Static Drain Source on Resistance of FSFM300[12]			1.76	2.20	Ω
C_{OSS}	Output Capacitance of FSFM260/261	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		60		pF
$t_{d(on)}$	Turn-On Delay Time of FSFM260/261	V_{DD} = 325V, I_D = 5A		12		ns
t_r	Rise Time of FSFM260/261			20		
$t_{d(off)}$	Turn-Off Delay Time of FSFM260/261			30		
t_f	Fall Time of FSFM260/261			16		
C_{OSS}	Output Capacitance of FSFM300	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		75		pF
$t_{d(on)}$	Turn-On Delay Time of FSFM300	V_{DD} = 325V, I_D = 5A		14		ns
t_r	Rise Time of FSFM300			26		
$t_{d(off)}$	Turn-Off Delay Time of FSFM300			32		
t_f	Fall Time of FSFM300			25		
Control Section						
f_{OSC}	Switching Frequency	V_{FB} = 3V	61	67	73	kHz
Δf_{OSC}	Switching Frequency Stability	13V ≤ V_{CC} ≤ 18V	0	1	3	%
Δf_{OSC}	Switching Frequency Variation[13]	-25°C ≤ T_A ≤ 85°C	0	±5	±10	%
I_{FB}	Feedback Source Current	V_{FB} = GND	0.7	0.9	1.1	mA
D_{MAX}	Maximum Duty Cycle		71	77	83	%
D_{MIN}	Minimum Duty Cycle				0	%
V_{START}	UVLO Threshold Voltage	V_{FB} = GND	11	12	13	V
V_{STOP}			7	8	9	V
$t_{S/S}$	Internal Soft-Start Time	V_{FB} = 3V	10	15	20	ms
Burst Mode Section						
V_{BURH}	Burst Mode Voltages	V_{CC} = 14V		0.50		V
V_{BURL}				0.35		V

Electrical Characteristics (Continued)

T_A = 25°C unless otherwise specified.

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
Protection Section							
V_{SD}	Shutdown Feedback Voltage		$V_{FB} \geq 5.5V$	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5V	3.5	5.0	6.5	µA
t_{LEB}	Leading Edge Blanking Time[13]			200			ns
I_{LIMIT}	Peak Current Limit	FSFM260/ FSFM261	T_J = 25°C, di/dt = 200mA/µs	1.32	1.50	1.68	A
		FSFM300		1.41		1.79	
V_{OVP}	Over-Voltage Protection			18.	19.0	20.5	V
T_{SD}	Thermal Shutdown Temperature[13]			125	140		°C
Total Device Section							
I_{OP}	Operating Supply Current		V_{FB} = GND, V = 14		3	5	mA
I_{START}	Start Current		V_{CC} = 10V before V_{CC} reach V_{STA} T)	150	200	250	µA
I_{CH}	Startup Charging Current		V = V, V_{S} min. 50V	0.70	0.8	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage		at I_{S} IN= START		24		V

Notes:

12. Pulse test: pulse width ≤ 300µs, duty ≤
13. Guaranteed by design; not teste roduction.

Typical Performance Characteristics

Graphs are normalized at T_A= 25°C.

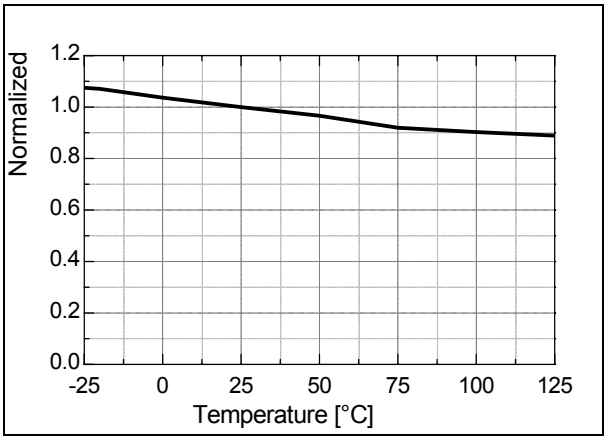


Figure 4. Operating Supply Current (I_{OP}) vs. T_A

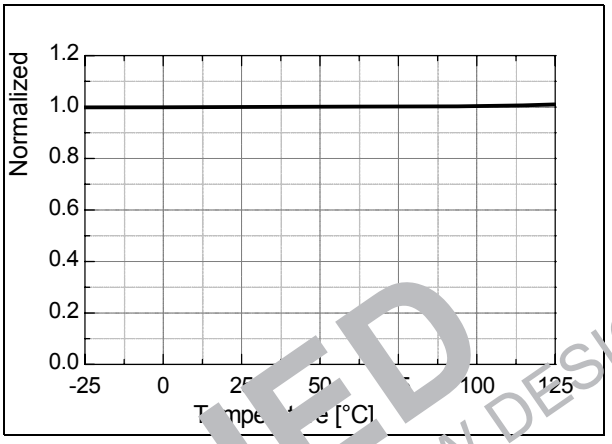


Figure 5. UVLO Start Threshold Voltage (V_{START}) vs. T_A

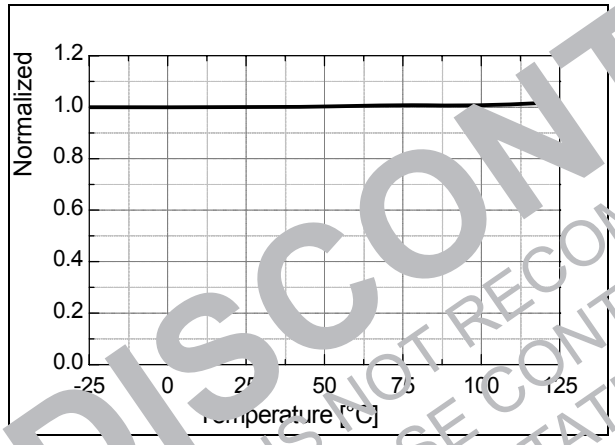


Figure 6. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

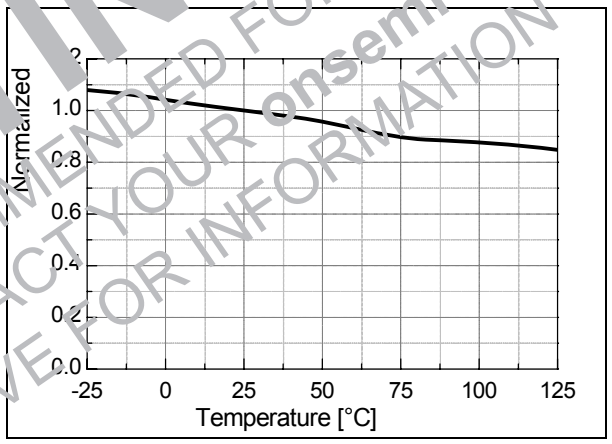


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

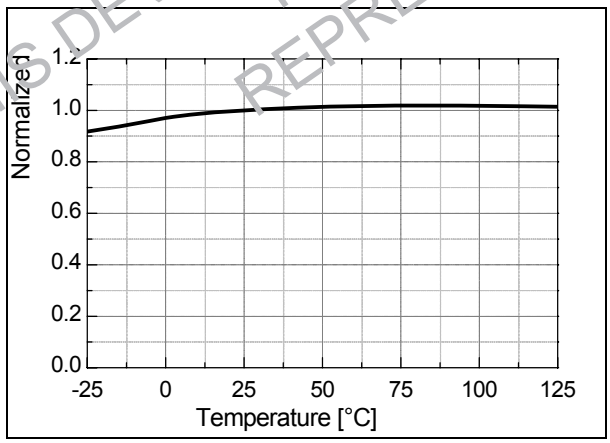


Figure 8. Switching Frequency (f_{OSC}) vs. T_A

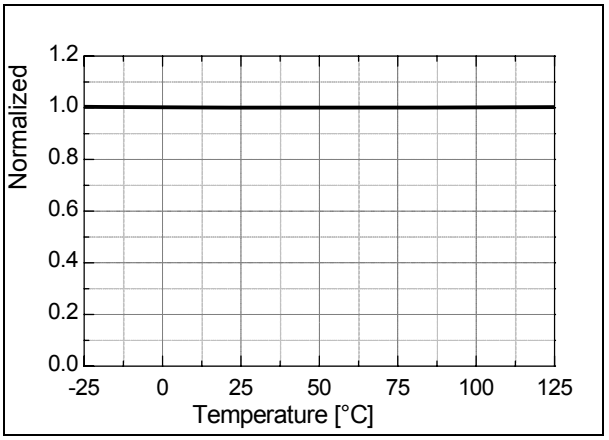


Figure 9. Maximum Duty Cycle (D_{MAX}) vs. T_A

Typical Performance Characteristics (Continued)

Graphs are normalized at T_A= 25°C.

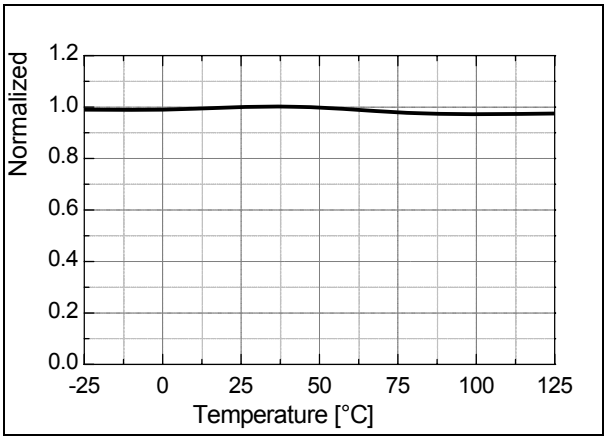


Figure 10. Over-Voltage Protection (V_{OVP}) vs. T_A

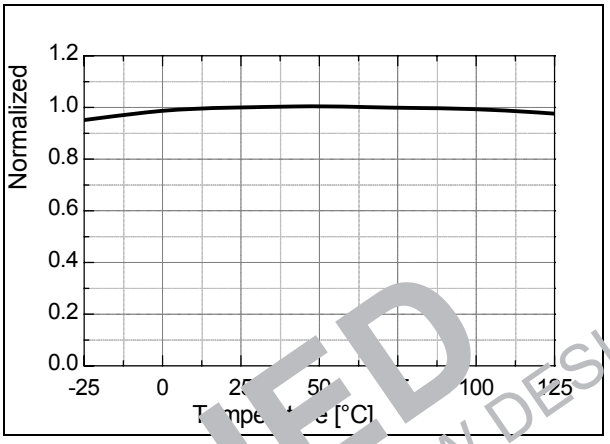


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

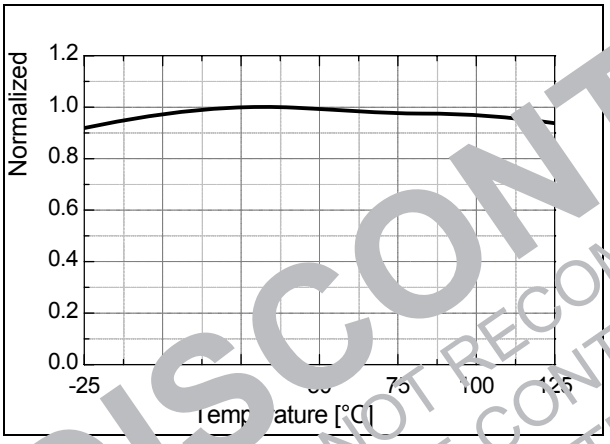


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

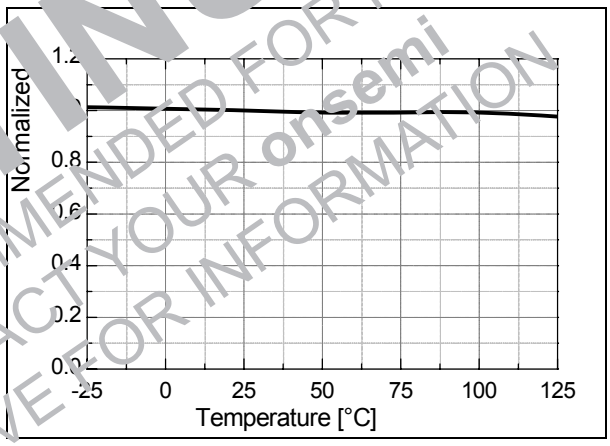


Figure 13. Burst-Mode HIGH Threshold Voltage (V_{BURH}) vs. T_A

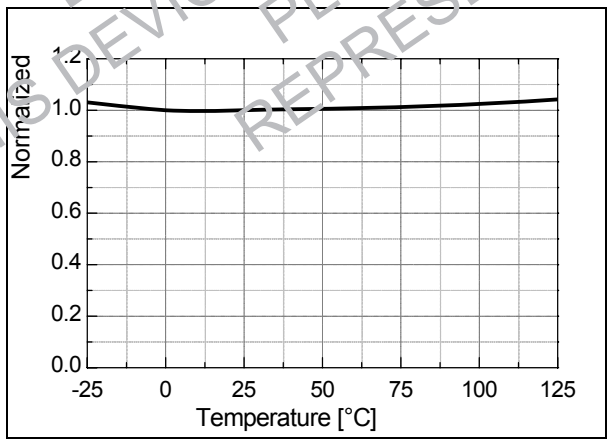


Figure 14. Burst-Mode LOW Threshold Voltage (V_{BURL}) vs. T_A

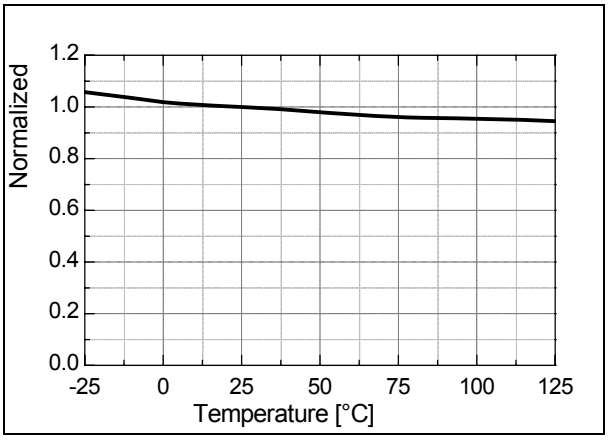


Figure 15. Peak Current Limit (I_{LIMIT}) vs. T_A

Functional Description

1. Startup: In previous generations of ON Semiconductor Power Switches (FPS™), the V_{CC} pin had an external startup resistor to the DC input voltage line. In this generation, the startup resistor is replaced by an internal high-voltage current source. At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_{vcc}) connected to the V_{CC} pin, as illustrated in Figure 16. When V_{CC} reaches 12V, the FSFM260/261/300 begins switching and the internal high-voltage current source is disabled. Then, the FSFM260/261/300 continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8V.

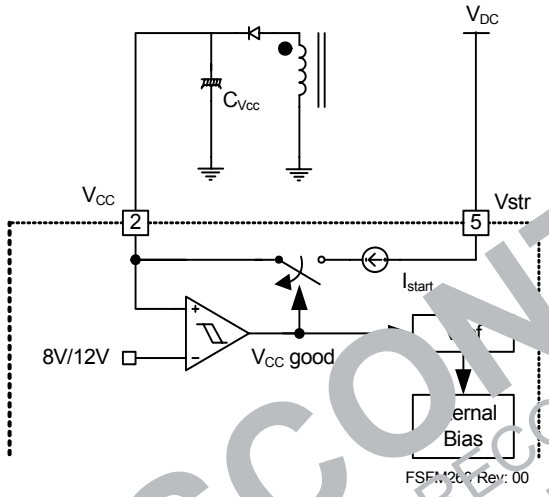


Figure 16. Internal Startup Circuit

2. Feedback Control: FSFM260/261/300 employs current-mode control, as shown in Figure 17. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5V, the opto coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically occurs when the input voltage is increased or the output load is decreased.

2.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the SenseFET is determined by the inverting input of the PWM comparator (V_{FB}*), as shown in Figure 17. When the current through the opto-transistor is zero and the current limit pin (#4) is left floating, the feedback current source (I_{FB}) of 0.9mA flows only through the internal resistor (R+2.5R=2.8k). In this case, the cathode voltage of diode D2 and the peak drain current have maximum values of 2.5V and 1.5A, respectively. The pulse-by-pulse current limit can be adjusted using a resistor to GND on the current limit pin (#4). The current limit level using an external resistor (R_{LIM}) is given by:

$$I_{LIM}=\frac{R_{LIM}\cdot I_{LIM\_SPEC}}{2.8k\Omega+R_{LIM}} \quad (1)$$

$$\Rightarrow R_{LIM}=\frac{I_{LIM}\cdot 2.8k\Omega}{I_{LIM\_SPEC}-I_{LIM}} \quad (2)$$

where, I_{LIM} is the desired drain current limit.

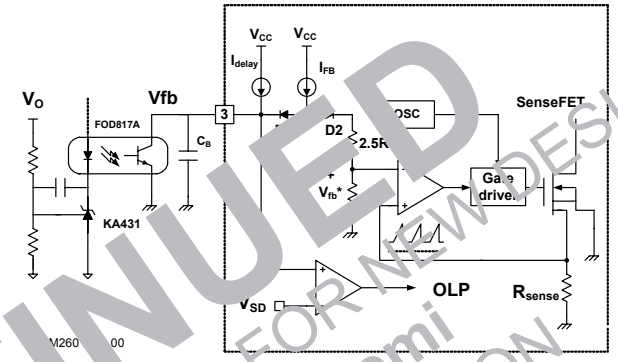


Figure 17. Pulse Width Modulation (PWM) Circuit

2.2 Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, a high-current spike occurs through the SenseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{SENSE} resistor would lead to incorrect feedback operation in the current-mode PWM control. To counter this effect, the FSFM260/261/300 employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SenseFET is turned on.

2.3 Constant Power Limit Circuit: Due to the circuit delay of FPS, the pulse-by-pulse limit current increases a little bit when the input voltage increases. This means unwanted excessive power is delivered to the secondary side. To compensate, the auxiliary power compensation network in Figure 18 can be used. R_{LIM} can adjust pulse-by-pulse current by absorbing internal current source (I_{FB}: typical value is 0.9mA) depending on the ratio between resistors. With the suggested compensation circuit, additional current from I_{FB} is absorbed more proportionally to the input voltage (V_{DC}) and achieves constant power in wide input range. Choose R_{LIM} for proper current to the application, then check the pulse-by-pulse current difference between minimum and maximum input voltage. To eliminate the difference (to gain constant power), R_y can be calculated by:

$$R_y \cong \frac{I_{lim\_spec}\times V_{dc}\times \frac{N_a}{N_p}}{I_{fb}\times \Delta I_{lim\_comp}} \quad (3)$$

where, I_{lim_spec} is the limit current stated on the specification; N_a and N_p are the number of turns for V_{CC} and primary side, respectively; I_{fb} is the internal current source at feedback pin with a typical value of 0.9mA; and ΔI_{lim_comp} is the current difference that must be eliminated. In case of capacitor in the circuit 1μF, 100V is good choice for all applications.

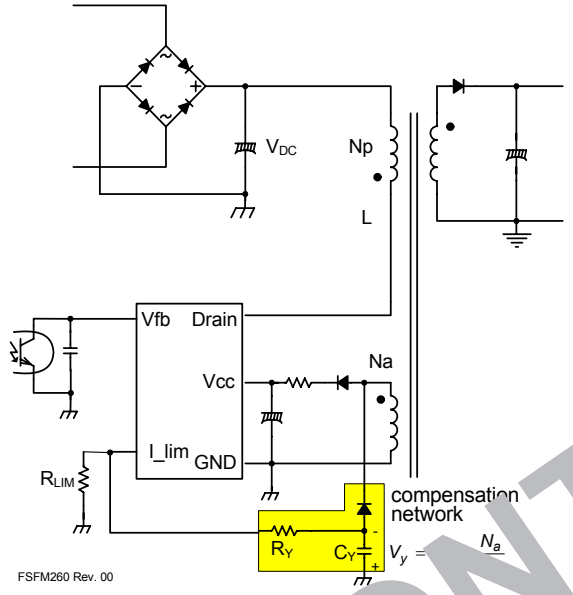


Figure 18. Constant Pow Limit rcu

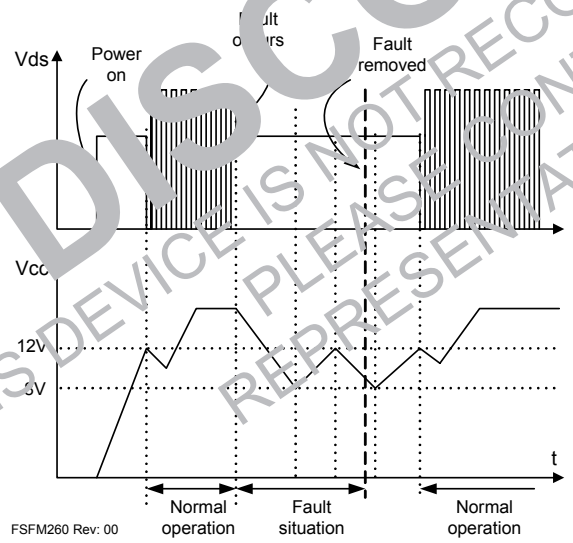


Figure 19. Auto Restart Operation

3. Protection Circuit: The FSFM260/261/300 has several self protective functions, such as overload protection (OLP), over-voltage protection (OVP), and thermal shutdown (TSD). Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost. Once the fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage, 8V, the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the Vstr pin. When V_{CC} reaches the UVLO start voltage, 12V, the FSFM260/261/300 resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated (*see Figure 19*).

3.1 Overload Protection (OLP): Overload is defined as the load current exceeding a pr level due to an unexpected event. In this situa n, the protection circuit should be activated to prot t the SMPS. However, even when the SMPS is in th normal op ati n, the overload protection circuit an be activated during the load transition. To avo th unesired operation, the overload pro tion c uit designed to be activated after a s ecifi time to dete mine whether it is a tra t si ation an overload situation. Because of e p se lse current limit capability, the maximum p k current through the Sense-FET is limited and, the fore the maximum input power is restricted with a given input voltage. If the output consumes beyond this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.5V, D1 is blocked and the 5μA current source starts to charge C_B slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 6V, when the switching operation is terminated, as shown in Figure 20. The delay time for shutdown is the time required to charge C_B from 2.5V to 6.0V with 5μA. In general, a 10 ~ 50ms delay time is typical for most applications.

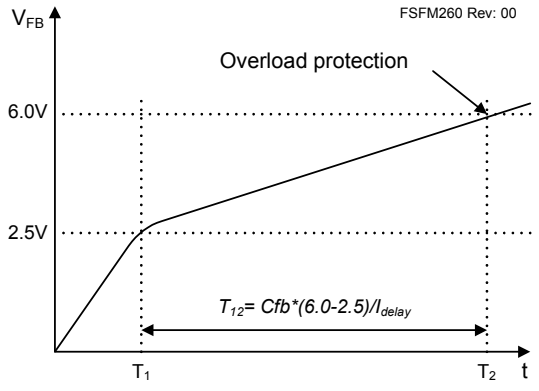


Figure 20. Overload Protection

3.2 Over-Voltage Protection (OVP): If the secondary side feedback circuit malfunctions or a solder defect causes an open in the feedback path, the current through the opto-coupler transistor becomes almost zero. Then, V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection is activated. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection is activated, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an over-voltage protection (OVP) circuit is employed. In general, V_{CC} is proportional to the output voltage and the FSFM260/261/300 uses V_{CC} instead of directly monitoring the output voltage. If V_{CC} exceeds 19V, an OVP circuit is activated, terminating the switching operation. To avoid undesired activation of OVP during normal operation, V_{CC} should be designed below 19V.

3.3 Thermal Shutdown (TSD): The SenseFET and the control IC are built in one package. This allows for the control IC to detect the heat generation from the SenseFET. When the temperature exceeds approximately 140°C, the thermal shutdown is activated.

3.4 Abnormal Over-Current Protection (AOCP). When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FPS has overload protection, it is not enough to protect the FPS in those abnormal cases, since severe current stress is imposed on the SenseFET until OLP triggers. The IC has an internal AOCP circuit shown in Figure 21. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

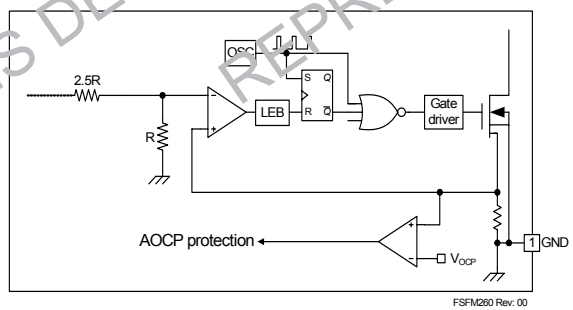


Figure 21. Abnormal Over-Current Protection

4. Soft-Start: The FSFM260/261/300 has an internal soft- start circuit that increases PWM comparator inverting input voltage, together with the SenseFET current, slowly after it starts up. The typical soft-start time is 15ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased to smoothly establish the required output voltage. It also helps prevent transformer saturation and reduce the stress on the secondary diode during startup.

5. Burst Operation: To minimize power dissipation in standby mode, the FSFM260/261/300 enters burst mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 22, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (350mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (500mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power SenseFET, thereby reducing switching loss in standby mode.

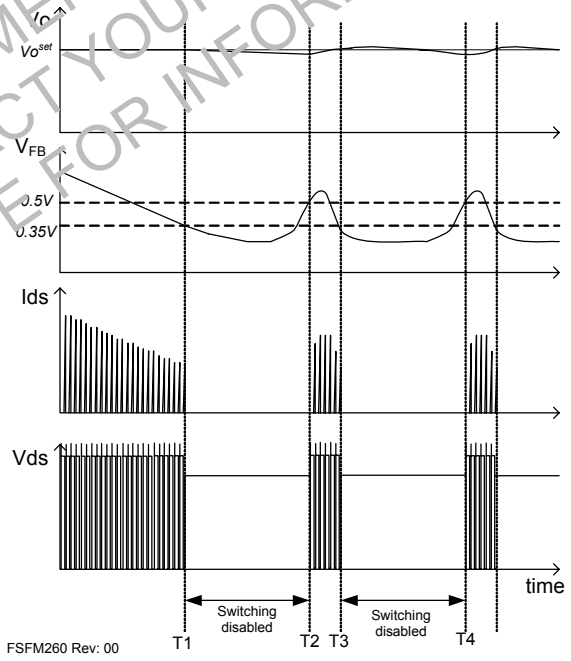


Figure 22. Waveforms of Burst Operation

PCB Layout Guide

Due to the combined scheme, FPS shows better noise immunity than conventional PWM controller and MOSFET discrete solutions. Furthermore, internal drain current sense eliminates noise generation caused by a sensing resistor. There are some recommendations for PCB layout to enhance noise immunity and suppress the noise inevitable in power-handling components.

There are typically two grounds in the conventional SMPS: power ground and signal ground. The power ground is the ground for primary input voltage and power, while the signal ground is ground for PWM controller. In FPS, those two grounds share the same pin, GND. Normally the separate grounds do not share the same trace and meet only at one point, the GND pin. More, wider patterns for both grounds are good for large currents by decreasing resistance.

Capacitors at the V_{CC} and FB pins should be as close as possible to the corresponding pins to avoid noise from the switching device. Sometimes Mylar® or ceramic capacitors with electrolytic for V_{CC} is better for smooth operation. The ground of these capacitors needs to connect to the signal ground not the power ground.

The cathode of the snubber diode should be close to the drain pin to minimize stray inductance. The capacitor between primary and secondary should be directly connected to the power ground or DC line to maximize surge immunity.

Because the voltage range of feedback line is small, it is affected by the noise of the drain pin. Those traces should not draw across or close to the drain line.

In FSFM2[illegible]0/2[illegible]0, drain pins are the heat radiation pins, so wide PCB pattern is recommended to decrease the package temperature. Drain pins are also high voltage switching pins; however, too wide PCB pattern may deteriorate EMI immunity.

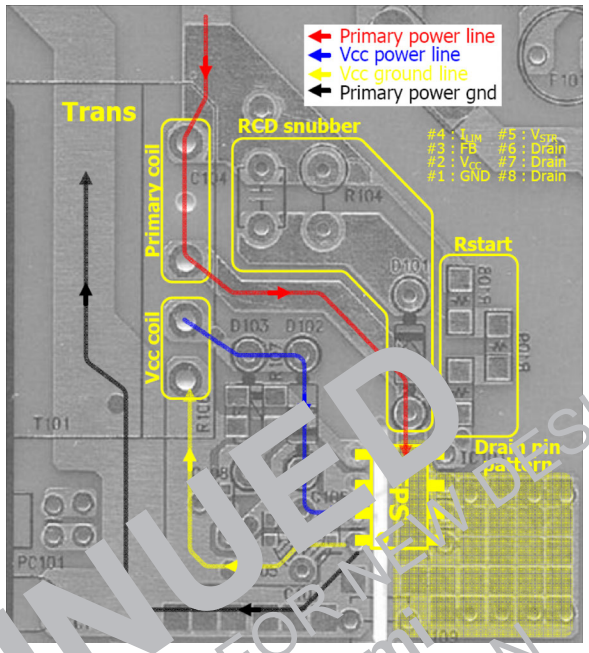


Figure 23. Recommended PCB Layout

Mylar® is a registered trademark of DuPont Teijin Films.

Typical Application Circuit

Application	FPS™ Device	Input Voltage Range	Rated Output Power	Output Voltage (Maximum Current)
LCD Monitor Power Supply	FSFM300N	85-265V_{AC}	30W	5.0V (2.0A) 14V (1.4A)

Features

- Average efficiency of 25%, 50%, 75%, and 100% load conditions is higher than 80% at universal input
- Low standby mode power consumption (<1W at 230V_{AC} input and 0.5W load)
- Enhanced system reliability through various protection functions
- Internal soft-start (15ms)

Key Design Notes

- The delay time for overload protection is designed to be about 23ms with C105 of 33nF. If faster/slower triggering of OLP is required, C105 can be changed to a smaller/larger value (e.g. 10nF for 7ms, 47nF for 50ms).
- The SMD-type 100nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improve surge immunity.

1. Schematic

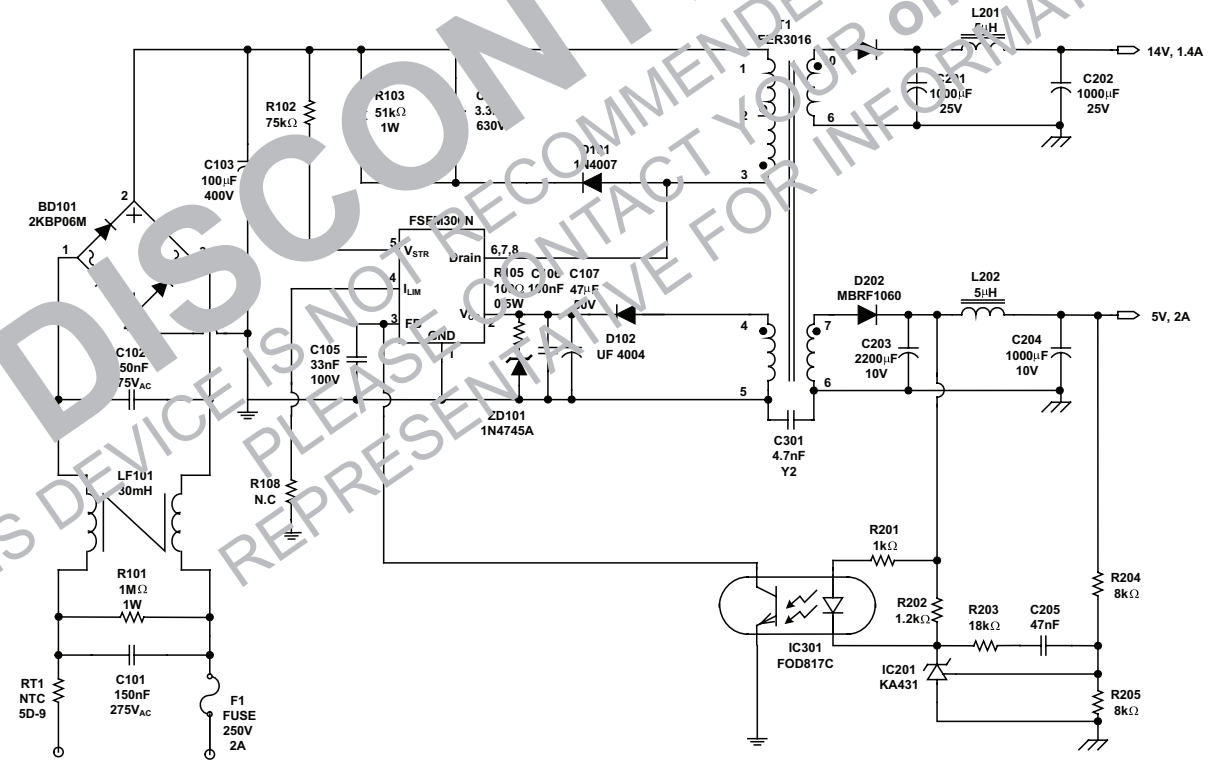


Figure 24. Demonstration Circuit of FSFM300N

2. Transformer

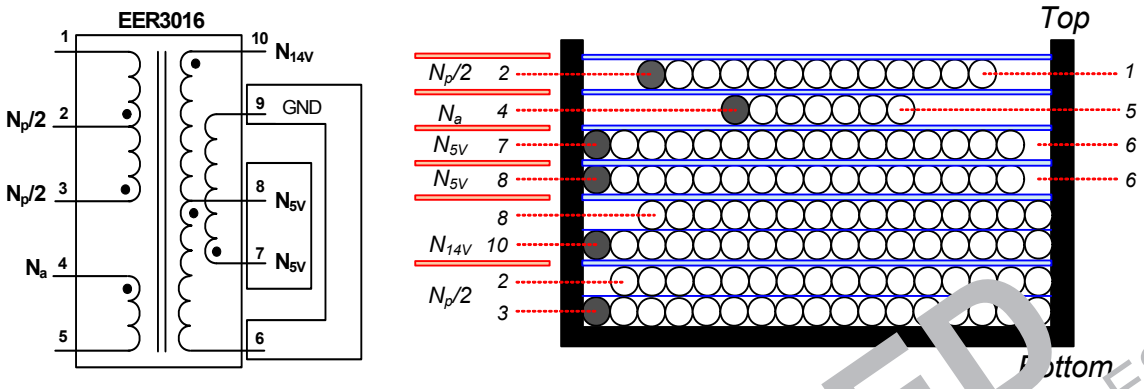


Figure 25. Transformer Schematic Diagra

3. Winding Specification

Position	No	Pin (s→f)	Wire	Turns	Winding Method
Bottom	$N_p/2$	3 → 2	0.2 × 1	30	Two-Layer Solenoid Winding
	Insulation: Polyester Tape t = .25m, Three Layers				
	N_{14V}	10	× 2(TIW)	5	Solenoid Winding
	Insulation: Polyeste Tape t = .02 mm, Three Layers				
	N_{5V}	8 → 6	0.4 × 3(TIW)	3	Solenoid Winding
	Insulation: Polyeste Tape t = 0.025mm, Three Layers				
	N_{5V}	7 → 6	0.4 × 3(TIW)	3	Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, Three Layers				
		7 → 6	0.15 × 1	7	Center Solenoid Winding
	Insulation: Polyester Tape t = 0.025mm, Three Layers				
	$N_p/2$	2 → 1	0.25 × 1	19	Center Solenoid Winding
Top	Insulation: Polyester Tape t = 0.025mm, Two Layers				

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1 - 3	1.2mH ± 10%	67kHz, 1V
Leakage	1 - 3	15μH Maximum	Short all other pins

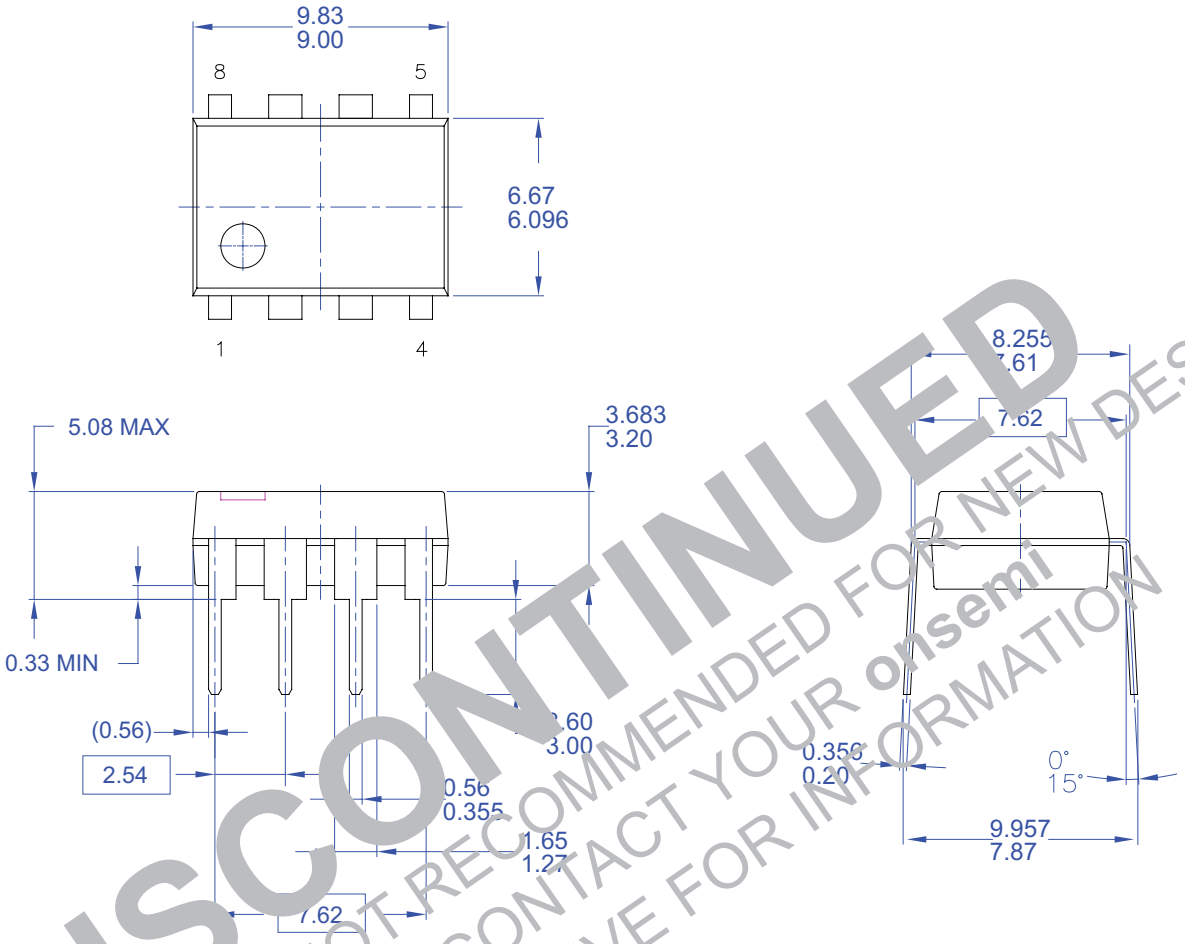
5. Core & Bobbin

- Core: EER3016 (Ae=109.7mm^2)
- Bobbin: EER3016

6. Evaluation Board Part List

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R101	1MΩ	1W	L201	5μH	5A Rating
R102	75kΩ	1/2W	L202	5μH	5A Rating
R103	51kΩ	1W	**Diode**		
R105	100Ω	1/4W	D101	IN4007	1A, 1000V General-Purpose Rectifier
R108	10kΩ	1/4W	D102	UF4004	1A, 400V Ultrafast Rectifier
R201	1kΩ	1/4W	ZD101	1N4745A	16V Zener Diode (optional)
R202	1.2kΩ	1/4W	D201	MBRF10H10	10A 100V Schottky Rectifier
R203	18kΩ	1/4W	D202	MBRF10	10A 60V Schottky Rectifier
R204	8kΩ	1/4W	**IC**		
R205	8kΩ	1/4W	IC101	FSF 00N	FPS™
Capacitor			IC201	A 1 (TL431)	Voltage Reference
C101	150nF/275V_{AC}	Box Capacitor	IC2 2	FOD817A	Opto-Coupler
C102	150nF/275V_{AC}	Box Capacitor	**Fuse**		
C103	100μF/400V	Electrolytic Capacitor	Fuse	2A/250V	
C104	3.3nF/630V	Film Ca	**NTC**		
C105	33nF/50V	Ceramic Capacitor	RT101	5D-9	
C106	100nF/50V	SMD (1206)	**Bridge Diode**		
C107	47μF/50	Electrolytic Capacitor	BD101	2KBP06M2N257	Bridge Diode
C201	1 0μF/25	Low-ESR Electrolytic Capacitor	**Line Filter**		
C202	1000uF/ V	Low-ESR Electrolytic Capacitor	LF101	34mH	
C203	2200μF/10V	Low-ESR Electrolytic Capacitor	**Transformer**		
C204	1000μF/10V	Low-ESR Electrolytic Capacitor	T1	EER3016	Ae=109.7mm^2
C205	47nF/50V	Ceramic Capacitor			
C301	4.7nF/1kV	Ceramic Capacitor			

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994
E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 26. 8-Lead Dual Inline Package (DIP)

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