

2 Channel Digital Isolator

DESCRIPTION

The CDIS 18012x15411x is a 2 channel digital isolator series that provides capacitive isolation between the primary and secondary sides of the device.

The digital isolator requires two supplies, one for the primary side and one for the secondary side.

The CDIS digital isolator ensures fast time to market and low development costs.

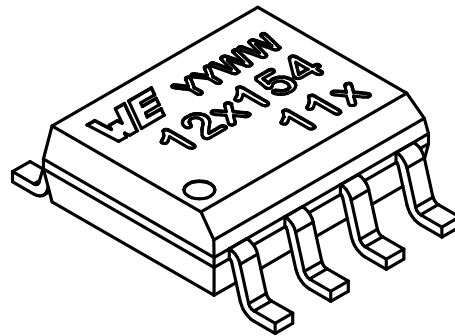
The digital isolator is available in an SOIC-8NB package (4.9 x 3.9 x 1.5)mm.

FEATURES

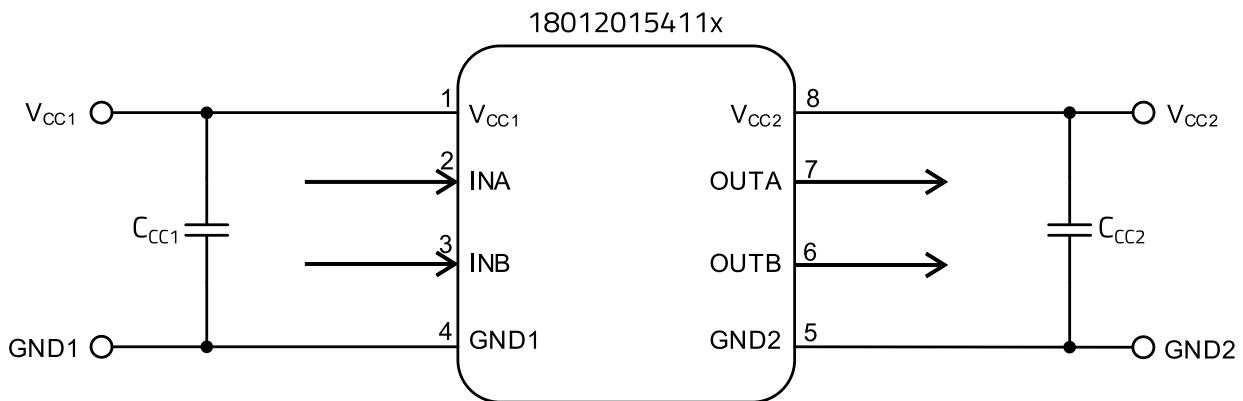
- Available channel configurations: 2/0 and 1/1
- Default channel output status: high or low
- Low propagation delay: 12ns typ.
- Input voltage range: 2.375V to 5.5V
- Data rate up to 150Mbps
- CMTI: $\pm 150\text{kV}/\mu\text{s}$ typ.
- Isolation: $3.75\text{kV}_{\text{RMS}}$ for 60s
- Ambient temperature range: -40°C to 125°C
- RoHS and REACH compliant
- UL1577 certified
- IEC 60747-17 pending

TYPICAL APPLICATIONS

- Communication bus isolation
- Motor control
- Battery management systems
- Solar inverters
- Test and measurement systems
- Programmable logic controller (PLC) interfaces



TYPICAL CIRCUIT DIAGRAM



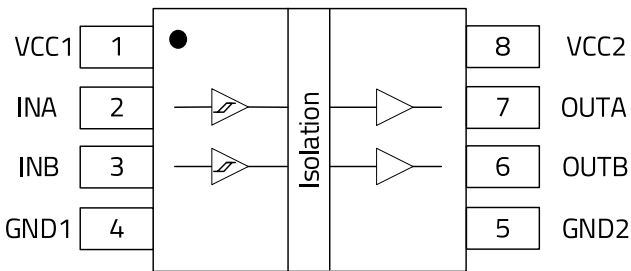
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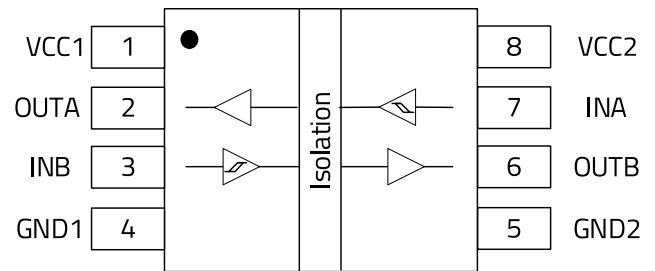


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1 PINOUT



18012015411(H/L)



18012115411(H/L)

Figure 1: Pinout.

Table 1: Marking description.

MARKING	DESCRIPTION
WE	Würth Elektronik eiSos GmbH & Co. KG
YYWW	Year and calendar week
12x15411x	Order code

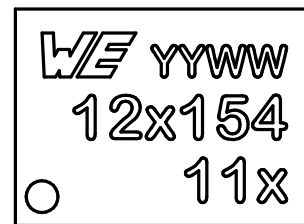


Figure 2: Marking.

Table 2: Pin description.

SYMBOL	NUMBER	TYPE	DESCRIPTION
VCC1	1	Power	Primary side supply pin.
INA/OUTA	2	I/O	Digital input/output A.
INB	3	I/O	Digital input B.
GND1	4	Power	Primary side ground connection.
GND2	5	Power	Secondary side ground connection.
OUTB	6	I/O	Digital output B.
INA/OUTA	7	I/O	Digital input/output A.
VCC2	8	Power	Secondary side supply pin.

18012x15411x

Digital Isolator

WPME-CDIS - Capacitive Digital Isolator Standard



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2 ORDERING INFORMATION

Table 3: Ordering information.

ORDER CODE	SPECIFICATIONS	PACKAGE	PACKAGING UNIT
18012015411H	2 forward, 0 reverse, default high	SOIC-8NB	13" Reel (2500 pieces)
18012015411L	2 forward, 0 reverse, default low		
18012115411H	1 forward, 1 reverse, default high		
18012115411L	1 forward, 1 reverse, default low		

3 SALES INFORMATION

SALES CONTACT
Würth Elektronik eiSos GmbH & Co. KG EMC and Inductive Solutions Max-Eyth-Str. 1 74638 Waldenburg Germany Tel. +49 (0) 7942 945 0 www.we-online.com/digitalisolators Technical support: powermodules@we-online.com

4 ABSOLUTE MAXIMUM RATINGS

Caution:

Exceeding the listed absolute maximum ratings may affect the device negatively and may cause permanent damage.

Table 4: Absolute maximum ratings.

SYMBOL	PARAMETER	LIMIT		UNIT
		MIN ⁽¹⁾	MAX ⁽¹⁾	
VCC1, VCC2	Supply voltage pins	-0.5	7	V
INX, OUTX	Voltage at INX, OUTX, SEL pins	-0.5	$V_{CCX} + 0.5^{(2)}$	V
I_{OUTX}	Channel output current	-20	20	mA
$T_{storage}$	Assembled, non-operating storage temperature	-65	150	°C
V_{ESD}	ESD voltage (HBM) ⁽⁴⁾	-6	6	kV
V_{ESD}	ESD voltage (CDM) ⁽⁴⁾	-2	2	kV

5 OPERATING CONDITIONS

Operating conditions are conditions under which the device is intended to be functional. All values are either referenced to GND1 or GND2.

MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C.

Table 5: Operating conditions.

SYMBOL	PARAMETER	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT
VCC1, VCC2	Supply voltage	2.375	—	5.5	V
V_{INX_H}	Logic input high threshold	2.0	—	—	V
V_{INX_L}	Logic input low threshold	—	—	0.8	V
I_{OH}	High-level channel output current $V_{CCO} = 5V$	-4	—	—	mA
	High-level channel output current $V_{CCO} = 3.3V$	-2	—	—	mA
	High-level channel output current $V_{CCO} = 2.5V$	-1	—	—	mA
I_{OL}	Low-level channel output current $V_{CCO} = 5V$	—	—	4	mA
	Low-level channel output current $V_{CCO} = 3.3V$	—	—	2	mA
	Low-level channel output current $V_{CCO} = 2.5V$	—	—	1	mA
DR	Data rate	0	—	150	Mbps
PW	Signal pulse width	5	—	—	ns
T_a	Ambient temperature range	-40	—	125	°C

6 ELECTRICAL SPECIFICATIONS

Caution:

MIN and MAX limits are valid for the recommended ambient temperature range of -40°C to 125°C . Typical values represent statistically the utmost probable values at the following conditions: $V_{CC} = 5\text{V}$, 3.3V or 2.5V , $T_A = 25^{\circ}\text{C}$, unless otherwise noted.

Table 6: Electrical specifications part 1.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT
Supply Characteristics						
V_{CCX_UVLO}	Supply undervoltage lockout falling threshold		1.88	2.10	2.325	V
	Undervoltage lockout rising threshold		1.95	2.24	2.375	V
	Undervoltage lockout hysteresis		70	140	250	mV
Channel Characteristics						
I_{IH}	High-level input leakage current	$V_{INX} = V_{CCI}$	—	—	20	μA
I_{IL}	Low-level input leakage current	$V_{INX} = 0\text{V}$	-20	—	—	μA
V_{OH}	High-level output voltage	$V_{INX} = V_{CCI}$	—	$V_{INX} - 0.2$	—	V
V_{OL}	Low-level output voltage	$V = 0\text{V}$	—	0.2	—	V
CMTI	Common-mode transient immunity	$V_{INX} = V_{CCI}$ or 0V , $V_{CM} = 1200\text{V}$	—	150	—	$\text{kV}/\mu\text{s}$
Timing Characteristics						
t_r	Output signal rise time	10% to 90% of V_{OUTX}	—	2.5	4.0	ns
t_f	Output signal fall time	90% to 10% of V_{OUTX}	—	2.5	4.0	ns
t_{PLH} , t_{PHL}	Propagation delay time	50% of V_{INX} to 50% of V_{OUTX}	5	12	15	ns
PWD	Pulse width distortion $ t_{PLH} - t_{PHL} $		—	0.2	4.5	ns
$t_{SK(C-C)}$	Channel-to-channel output skew time		—	0.4	2.5	ns
$t_{SK(P-P)}$	Part-to-part output skew time		—	2.0	4.5	ns

Parameters indicated in electrical specifications part 1 are applicable across all part numbers with all input/output conditions unless otherwise specified.

Table 7: Electrical specifications part 2.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT
18012015411x V_{CC1} = 5V and V_{CC2} = 5V						
I _{CC1}	Primary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	0.8	—	mA
		V _{INX} ≠ channel default	—	3.4	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.8	—	mA
I _{CC2}	Secondary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.3	—	mA
		V _{INX} ≠ channel default	—	1.4	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	1.5	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.7	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	14.2	—	mA
18012115411x V_{CC1} = 5V and V_{CC2} = 5V						
I _{CC1}	Primary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.4	—	mA
		V _{INX} ≠ channel default	—	2.8	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	3.1	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	11.1	—	mA
I _{CC2}	Secondary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.3	—	mA
		V _{INX} ≠ channel default	—	2.9	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.3	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	3.1	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	11.6	—	mA
18012015411x V_{CC1} = 3.3V and V_{CC2} = 3.3V						
I _{CC1}	Primary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	0.8	—	mA
		V _{INX} ≠ channel default	—	3.4	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.0	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.5	—	mA

Table 8: Electrical specifications part 3.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT
I _{CC2}	Secondary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.2	—	mA
		V _{INX} ≠ channel default	—	1.3	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	1.4	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	9.6	—	mA
18012115411x V_{CC1} = 3.3V and V_{CC2} = 3.3V						
I _{CC1}	Primary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.4	—	mA
		V _{INX} ≠ channel default	—	2.7	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.7	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	8	—	mA
I _{CC2}	Secondary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.4	—	mA
		V _{INX} ≠ channel default	—	2.9	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.7	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	8	—	mA
18012015411x V_{CC1} = 2.5V and V_{CC2} = 2.5V						
I _{CC1}	Primary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	0.8	—	mA
		V _{INX} ≠ channel default	—	3.4	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.0	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.3	—	mA
I _{CC2}	Secondary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.2	—	mA
		V _{INX} ≠ channel default	—	1.3	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	1.3	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	1.9	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	7.5	—	mA

Table 9: Electrical specifications part 4.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN ⁽¹⁾	TYP ⁽³⁾	MAX ⁽¹⁾	UNIT
18012115411x V_{CC1} = 2.5V and V_{CC2} = 2.5V						
I _{CC1}	Primary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.3	—	mA
		V _{INX} ≠ channel default	—	2.7	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.1	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.5	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	6.4	—	mA
I _{CC2}	Secondary side external power supply input current ⁽⁵⁾	V _{INX} = channel default	—	1.4	—	mA
		V _{INX} ≠ channel default	—	2.8	—	mA
		1Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.2	—	mA
		10Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	2.5	—	mA
		100Mbps, C _L = 15pF, 50% duty cycle square wave input signal	—	6.4	—	mA


7 ISOLATION SPECIFICATIONS

Table 10: Isolation specification table.

SYMBOL	PARAMETER	TEST CONDITIONS	TYP ⁽³⁾	UNIT
CLR	External clearance	Shortest distance through air between terminals	4	mm
CPG	External creepage	Shortest distance across package surface between terminals	4	mm
DTI	Distance through the insulation	Minimum internal clearance	19	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	IEC 60664-1 overvoltage category	Rated mains voltage ≤ 300 V _{RMS}	I-III	
		Rated mains voltage ≤ 400 V _{RMS}	I-III	
UL1577				
V _{ISO(max)}	Max. withstanding isolation voltage	V _{TEST} = V _{ISO} , t = 60s (qualification), V _{TEST} = 1.2 x V _{ISO} , t = 1s (100% production)	3750	V _{RMS}


8 APPROVALS

Table 11: Approvals.

SYMBOL	STANDARD	DESCRIPTION
	UL 1577, 5 th Edition	Nonoptical Isolating Devices – Component UL Category: FPPT2 & FPPT8 UL File No: E535458 Applicable for altitudes up to 2000m

9 RoHS, REACH

Table 12: RoHS, REACH.

RoHS directive		Directive 2011/65/EU of the European Parliament and the Council of June 8th, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.
REACH directive		Directive 1907/2006/EU of the European Parliament and the Council of June 1st, 2007 regarding the Registration, Evaluation, Authorization and Restriction of Chemicals (REACH).

10 PACKAGE SPECIFICATIONS

Table 13: Package specifications.

ITEM	PARAMETER	TYP ⁽³⁾	UNIT
Lead finish	—	Matte Sn	—
Weight	—	0.075	g

11 NOTES

- (1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
- (2) This value must never exceed 7V.
- (3) Typical numbers are valid at 25°C ambient temperature and represent statistically the utmost probability assuming the Gaussian distribution.
- (4) The human body model is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin. Test method is per JESD-22-114. The charged device model test method is per JESD22-C101.
- (5) Supply current measurements are made with no additional load connected to the primary and secondary external power supplies. The indicated values only describe the current required to supply the internal circuitry and external capacitive loads on the channel outputs based on the signal described in the test conditions.
- (6) 100% final production tested value. The qualified isolation voltage value is 5kV_{RMS}. For detailed isolation characteristics see the isolation specification table ([Isolation specification table](#)).

12 ISOLATION VOLTAGE

12.1 Isolation Voltage Testing

To verify the integrity of the isolation a test voltage is applied for a specified time across a component that is designed to provide electrical isolation. This test is known as 'High Pot Test', 'Flash Tested', 'Withstand Voltage', 'Proof Voltage', 'Dielectric Withstand Voltage' or 'Isolation Test Voltage'.

All digital isolators are 100% production tested at their stated isolation voltage. This is $4.5\text{kV}_{\text{RMS}}$ for 1s.⁽⁶⁾

The isolation test voltage indicated in this data sheet is for voltage transient immunity only. It does not allow this part to be used within a safety isolation system.

The digital isolator will function properly with several hundreds of volts applied continuously across the isolation barrier, however surrounding components must be individually analyzed to ensure proper insulation. Isolation measures must be taken into account to prevent any user-accessible circuitry from causing harm.

12.2 Dielectric Test Setup (High Pot Test)

Connect all input terminals together then all output terminals together (see figure below) before connecting the supply voltage. When testing, set the cut-off current to 1mA with a test voltage of $4.5\text{kV}_{\text{RMS}}$ and test time of 1s.⁽⁶⁾

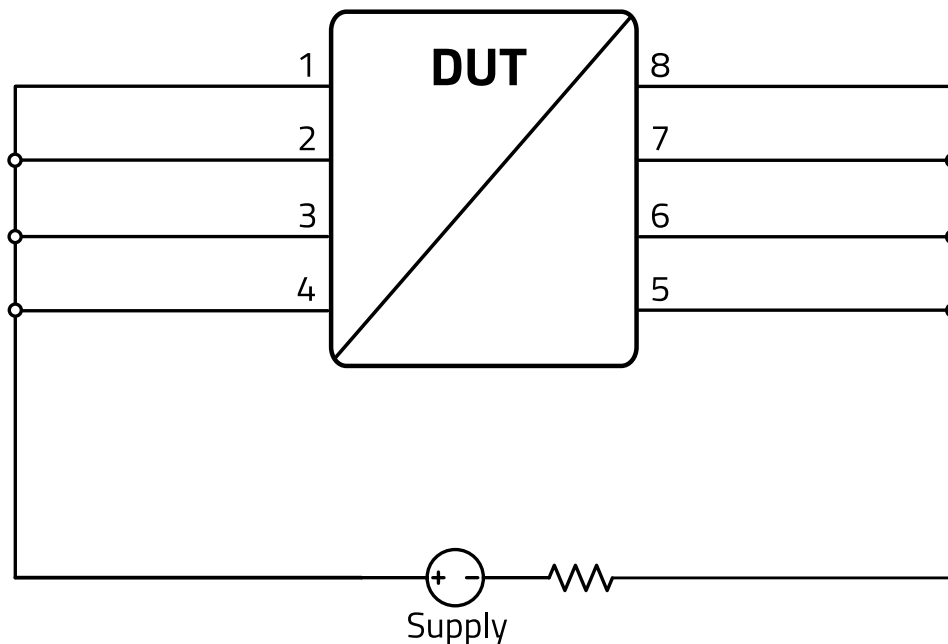


Figure 3: Dielectric test setup.

12.3 Repeated High-Voltage Isolation Testing

Typically, parts can withstand multiples of their stated test voltage and still perform optimally. However, repeated exposure to high voltage test conditions will degrade the component's isolation capabilities. It is recommended to keep high voltage isolation testing to a minimum to limit degradation of the device before its installation in an application. If repeated high voltage isolation testing is required, consider reducing the voltage by a significant amount (e.g. 20%) from the stated test voltage within the datasheet.

13 TYPICAL PERFORMANCE CURVES

If not otherwise specified, the following conditions apply: $T_A = 25^\circ\text{C}$.

13.1 DC Performance Curves

13.1.1 Quiescent Current vs. Ambient Temperature

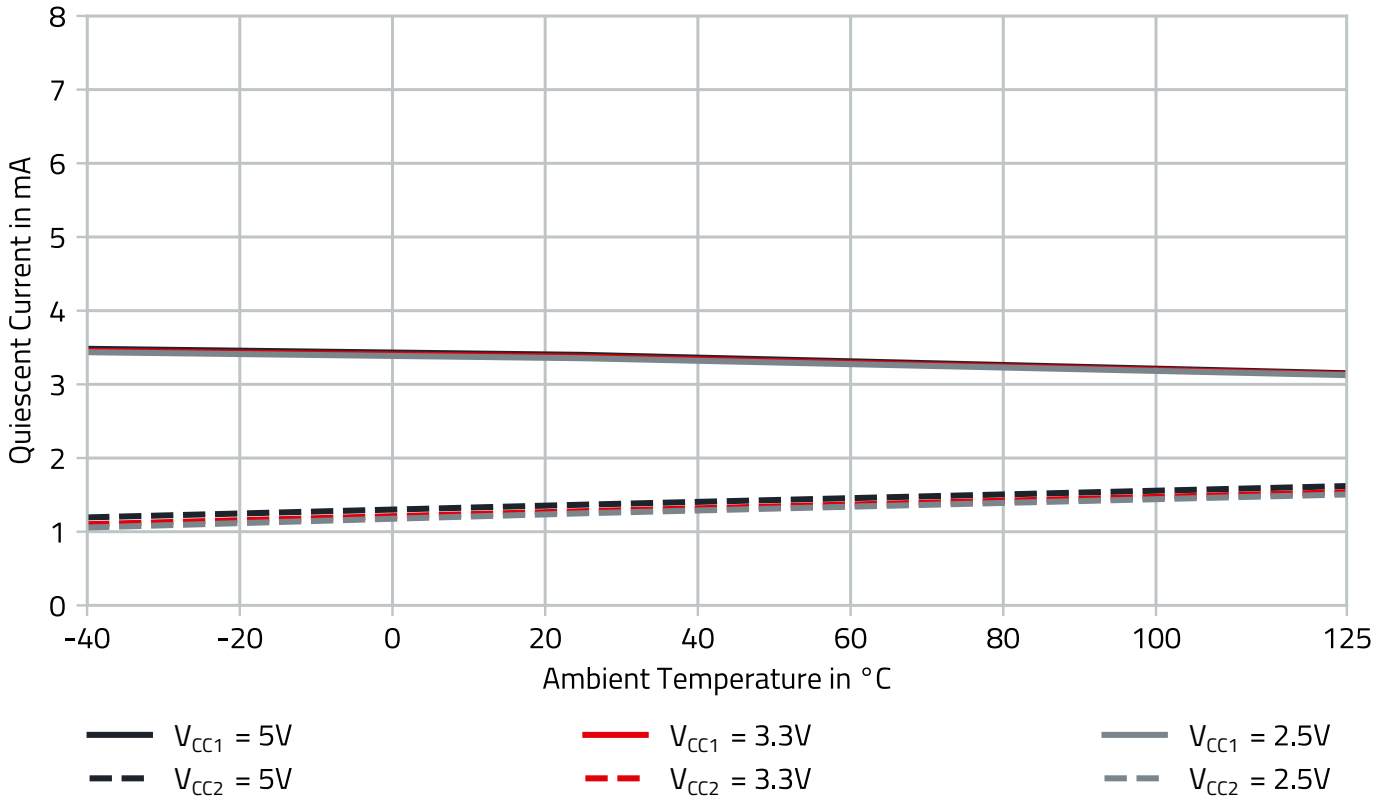


Figure 4: 18012015411H quiescent current, all channel inputs set to logic high.

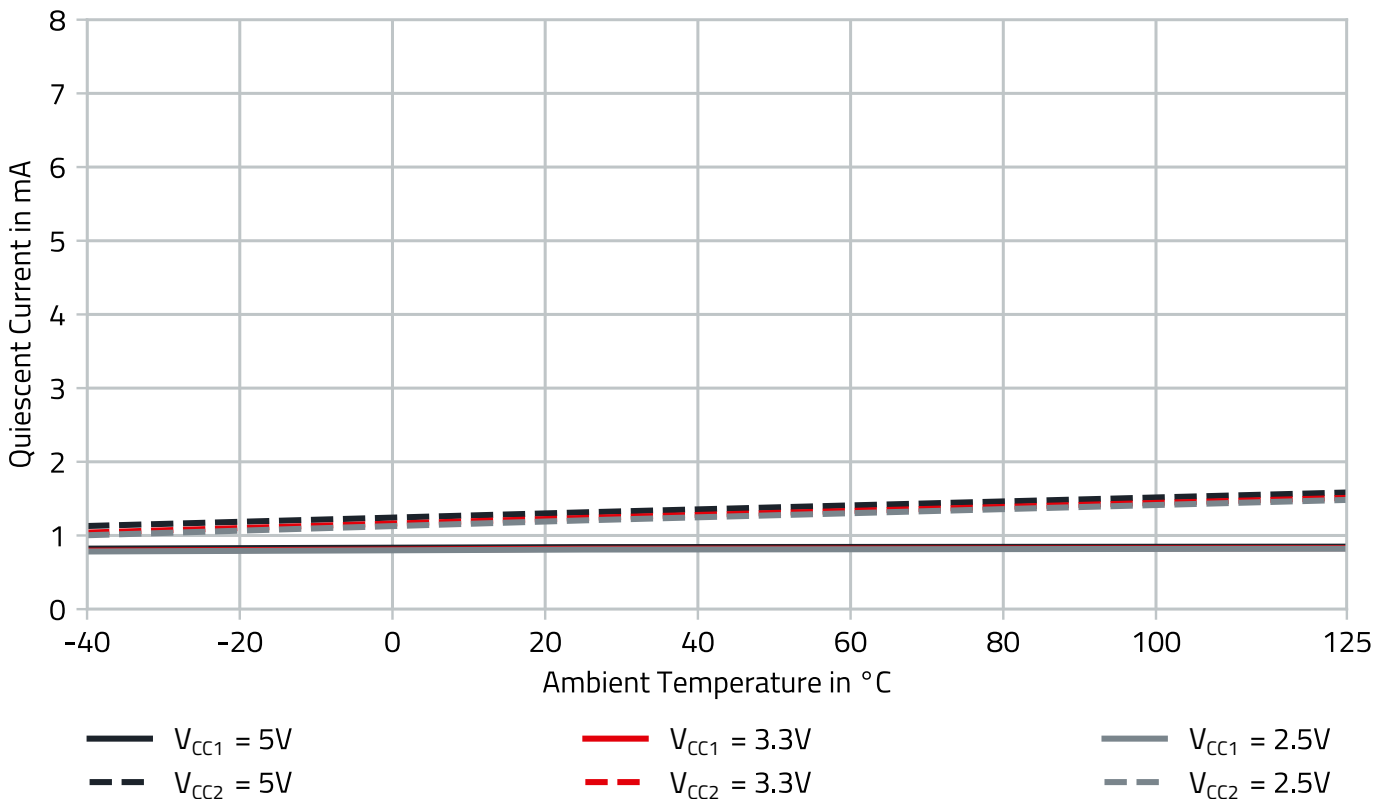


Figure 5: 18012015411H quiescent current, all channel inputs set to logic low.

13.1.2 Propagation Delay vs. Ambient Temperature

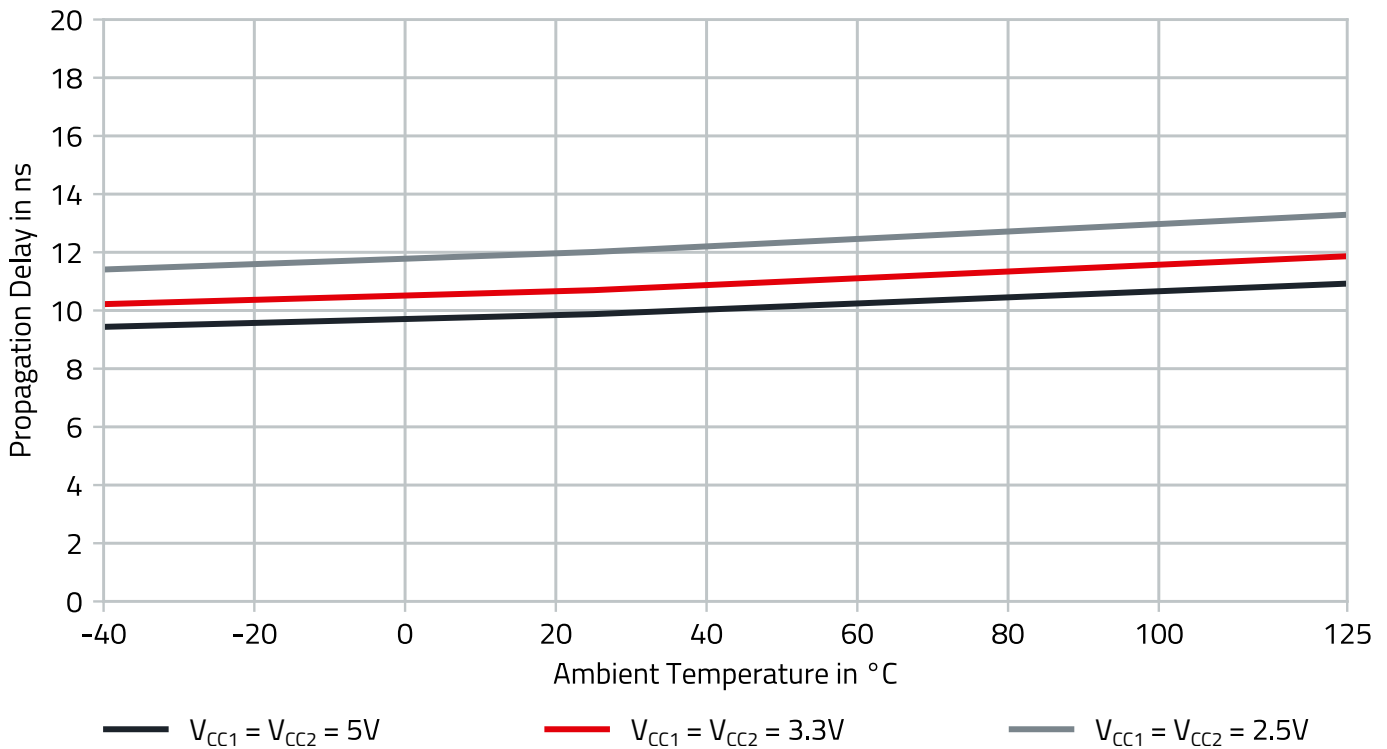


Figure 6: 18012x15411x propagation delay, all channels with low to high transition, $C_{LOAD} = 15pF$.

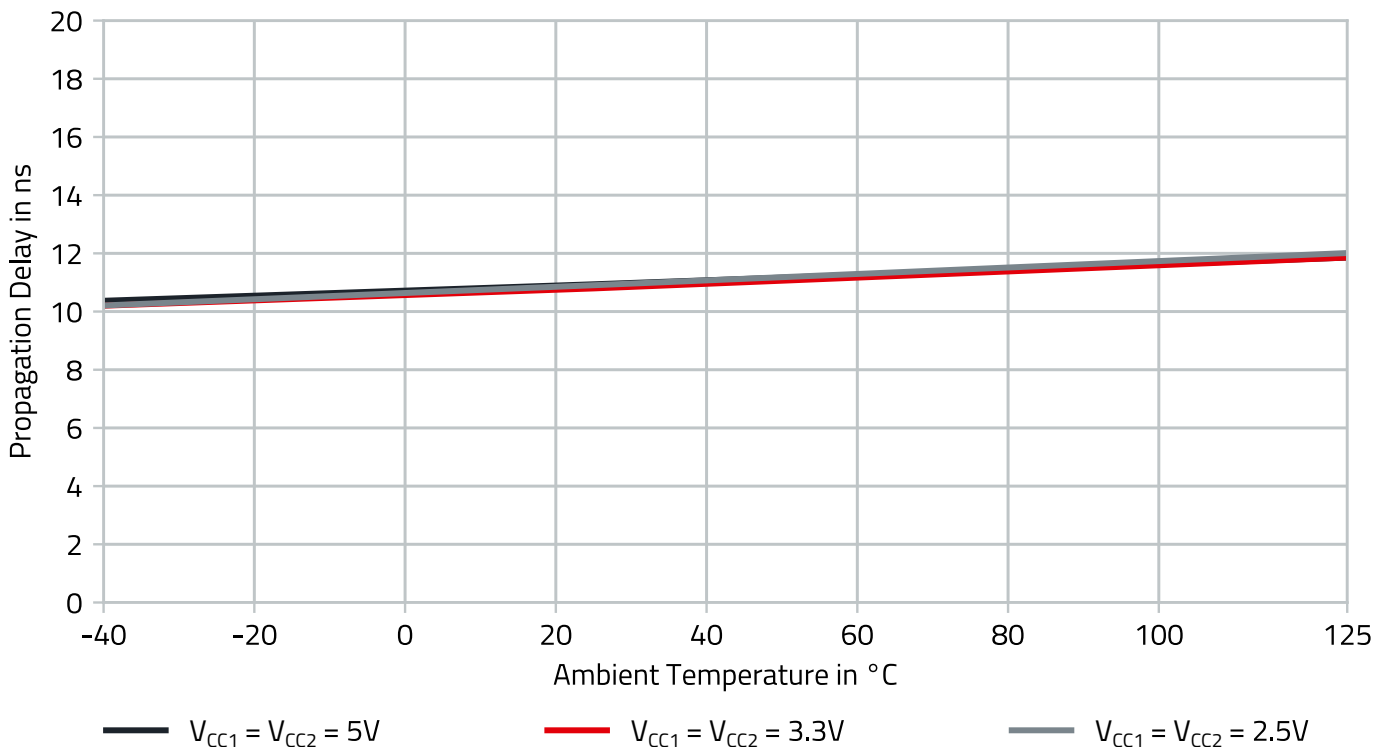


Figure 7: 18012x15411x propagation delay, all channels with high to low transition, $C_{LOAD} = 15pF$.

13.1.3 Supply Current vs. Ambient Temperature

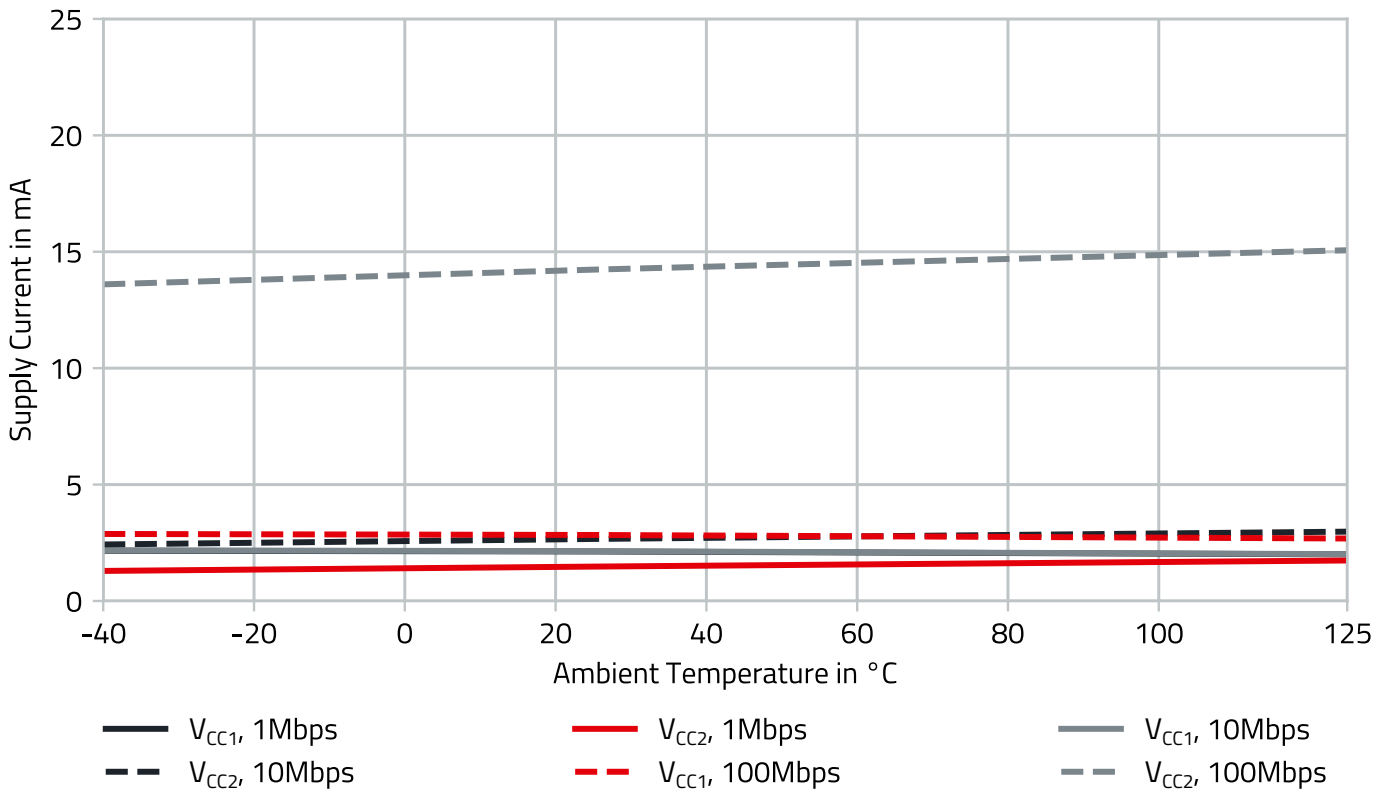


Figure 8: 18012015411x supply current $V_{CC1} = V_{CC2} = 5V$.

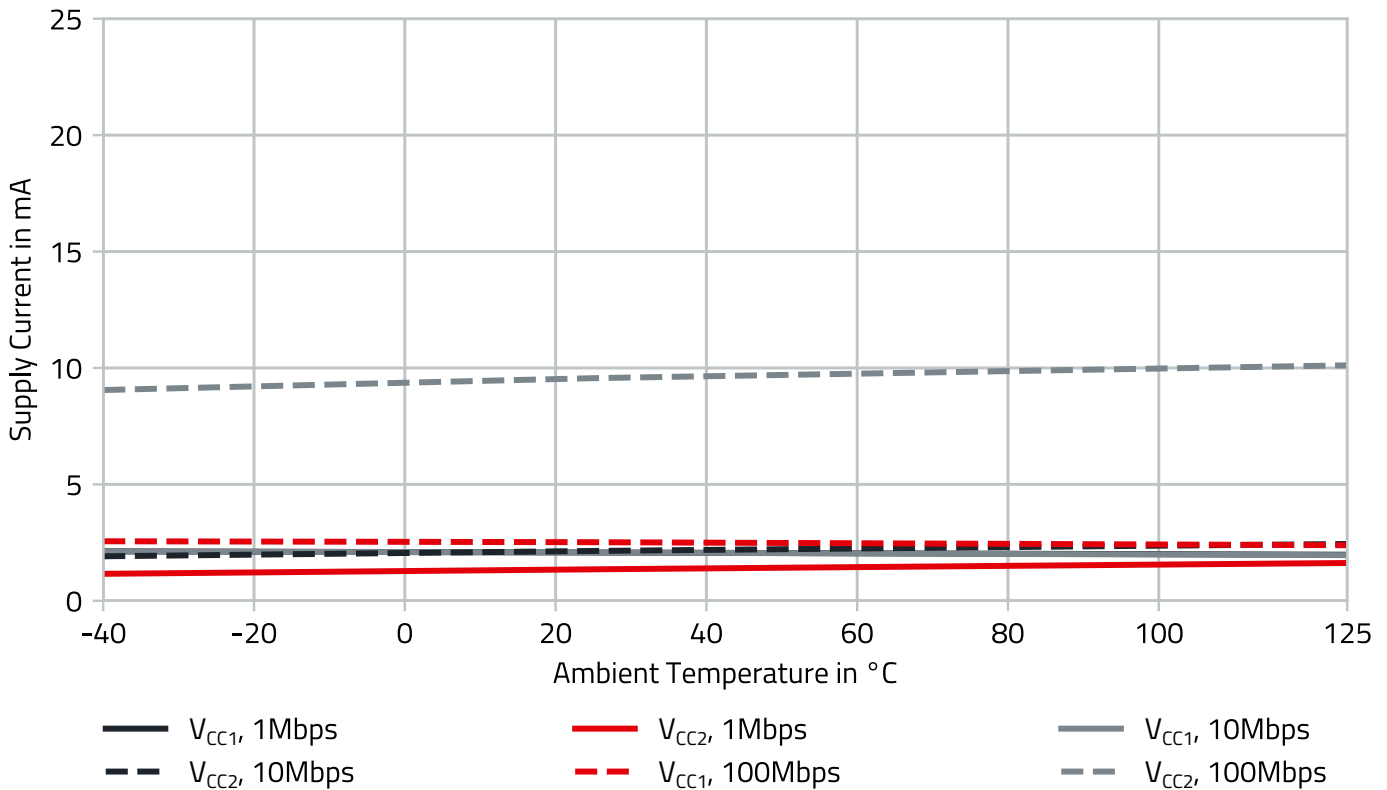


Figure 9: 18012015411x supply current $V_{CC1} = V_{CC2} = 3.3V$.

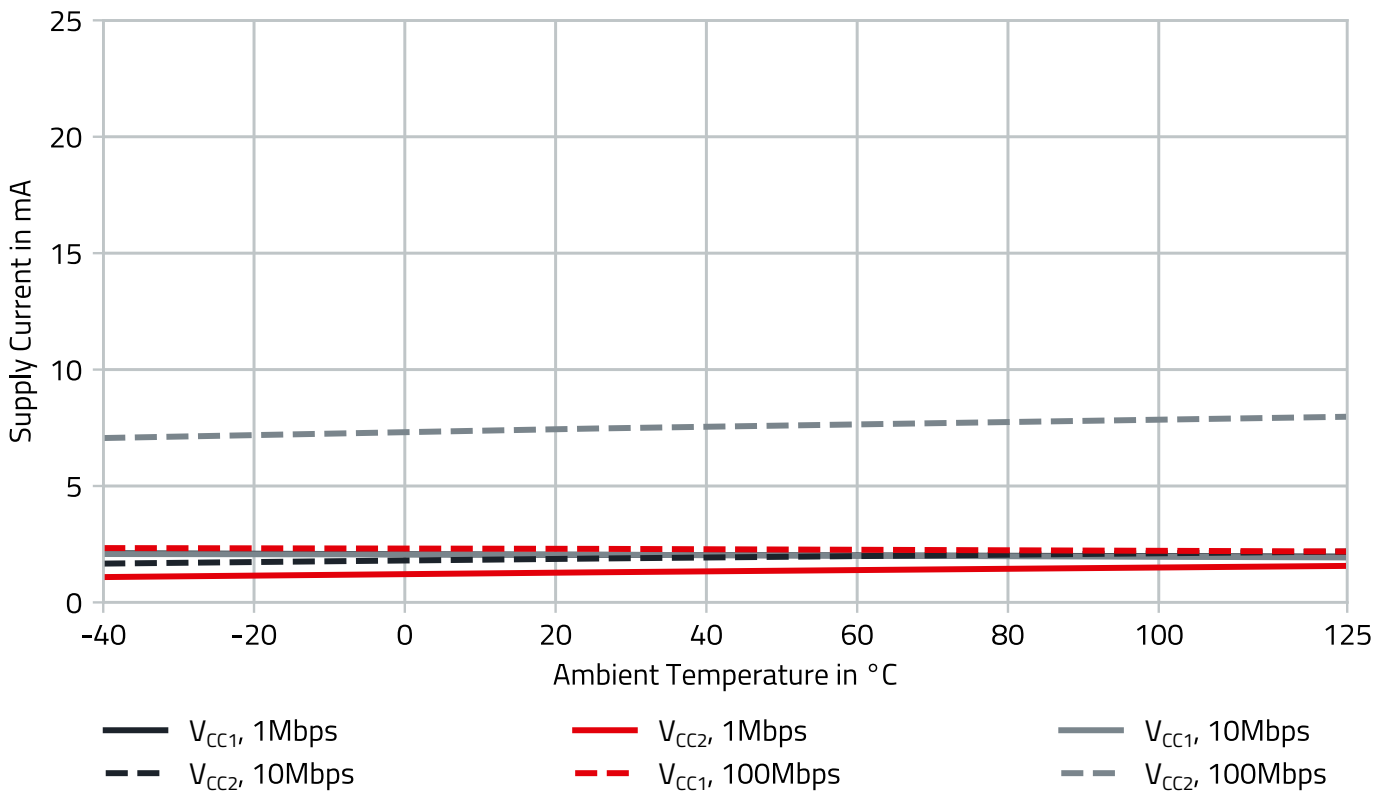


Figure 10: 18012015411x supply current $V_{CC1} = V_{CC2} = 2.5V$.

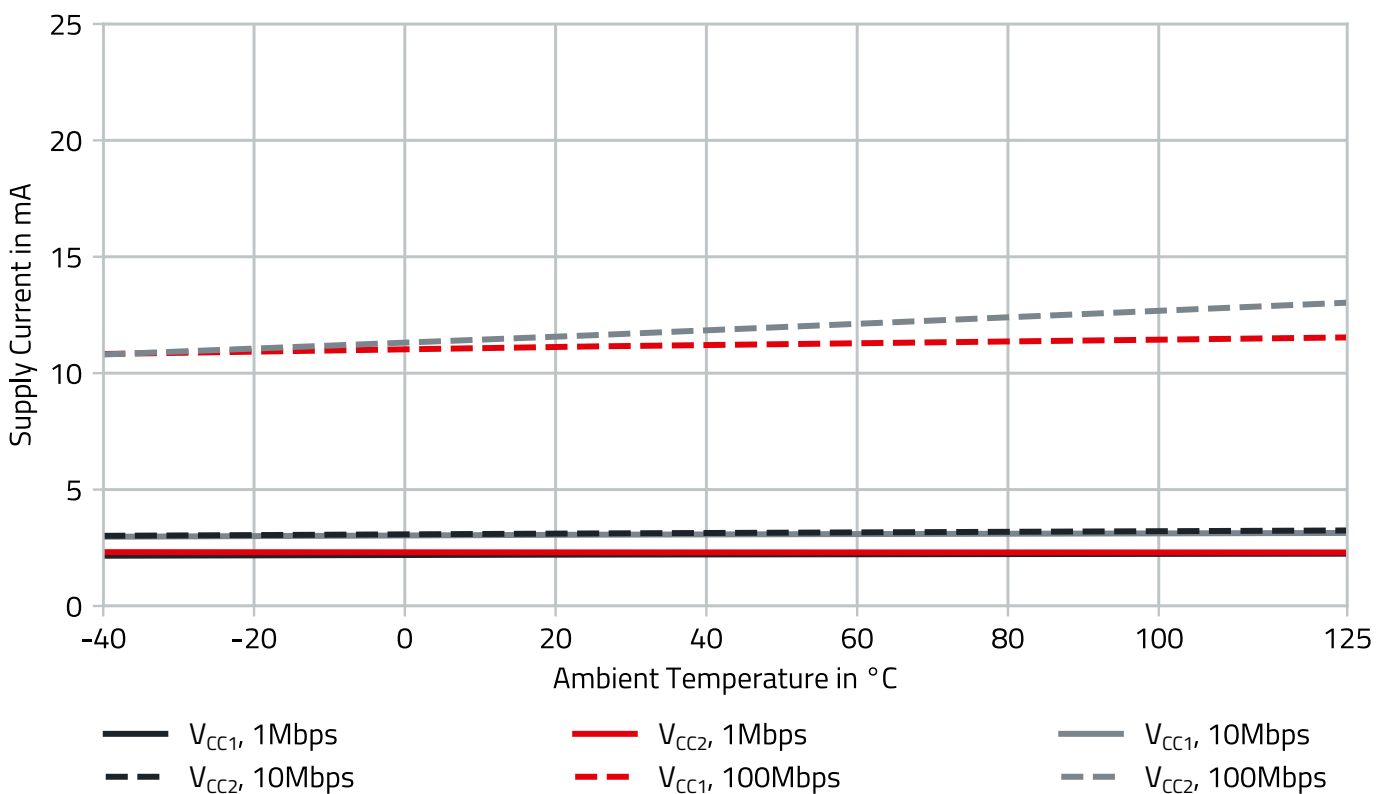


Figure 11: 18012115411x supply current $V_{CC1} = V_{CC2} = 5V$.

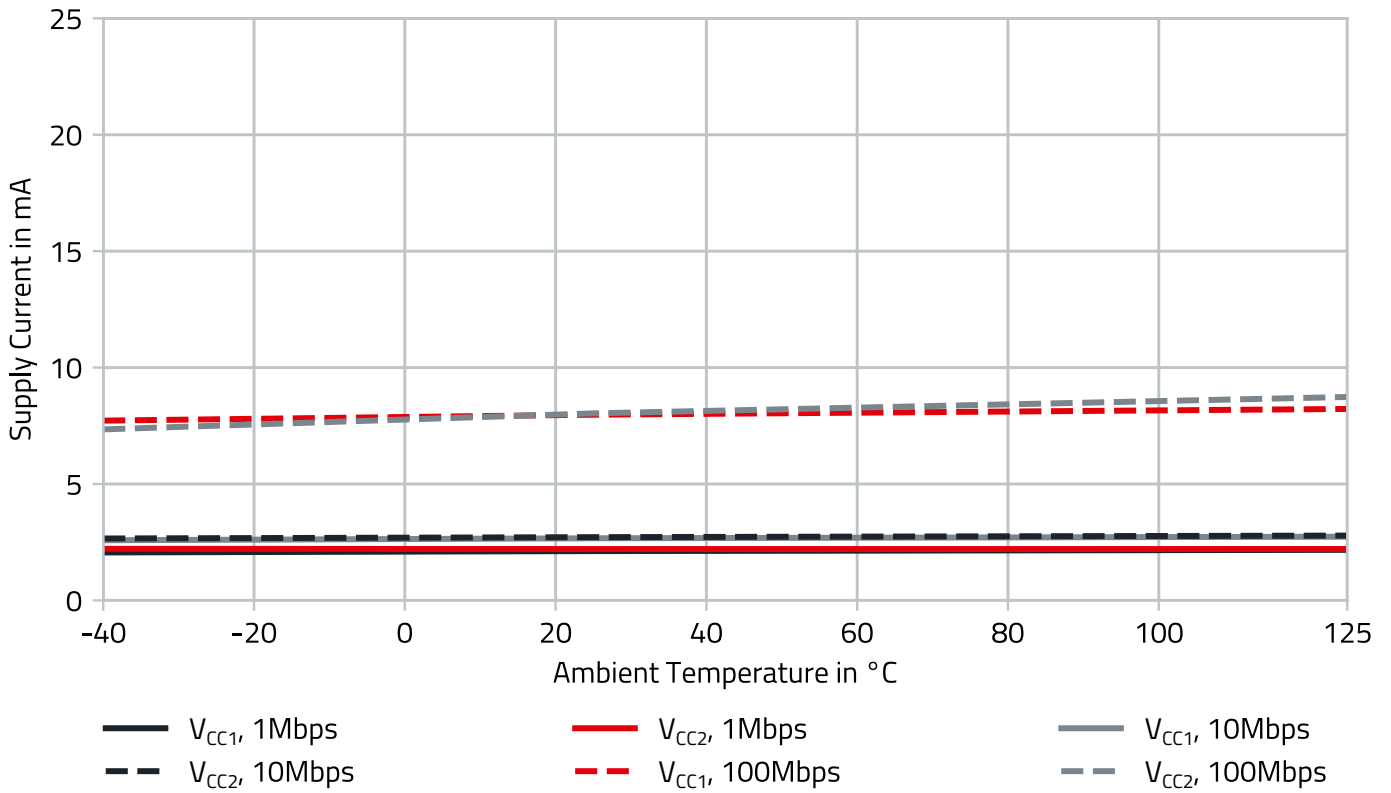


Figure 12: 18012115411x supply current $V_{CC1} = V_{CC2} = 3.3V$.

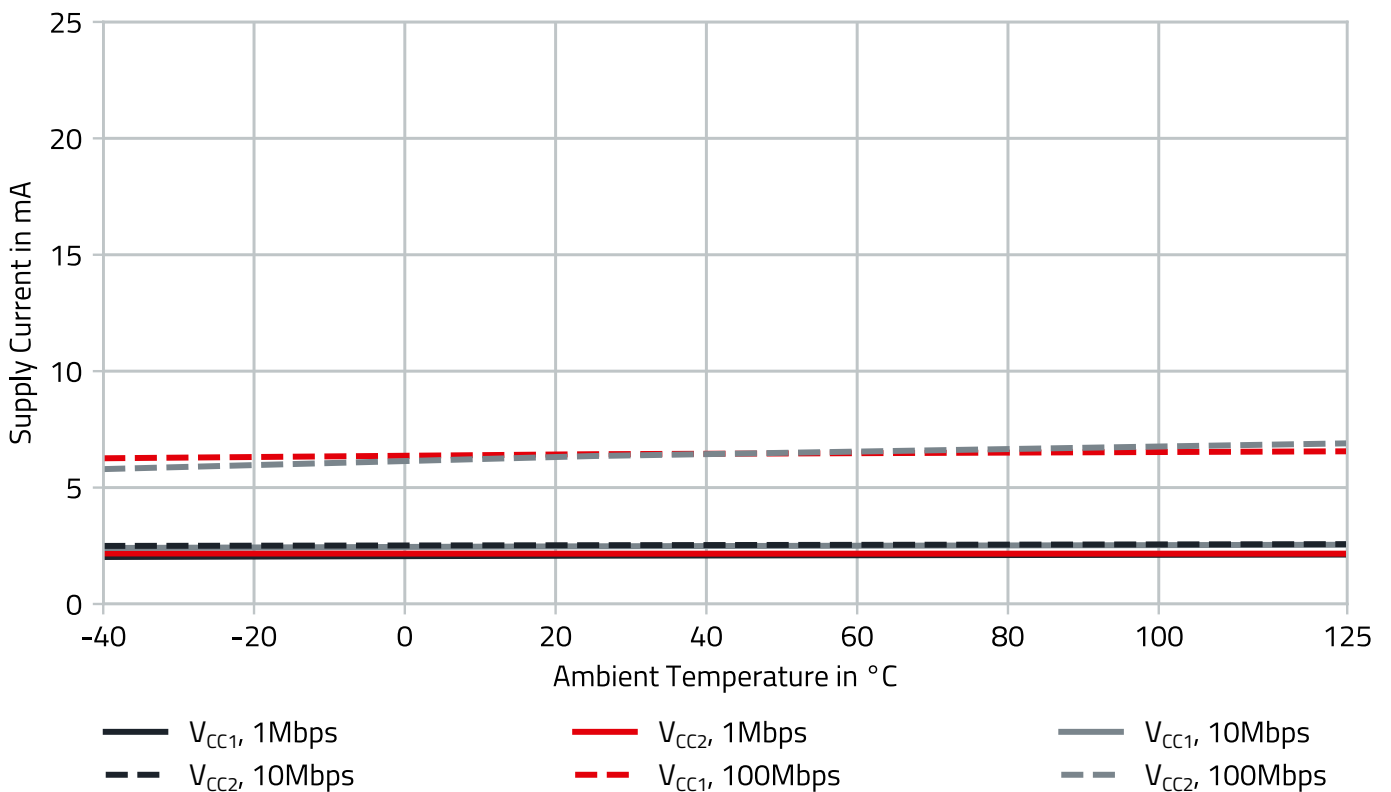


Figure 13: 18012115411x supply current $V_{CC1} = V_{CC2} = 2.5V$.

13.1.4 Supply Current vs. Data Rate

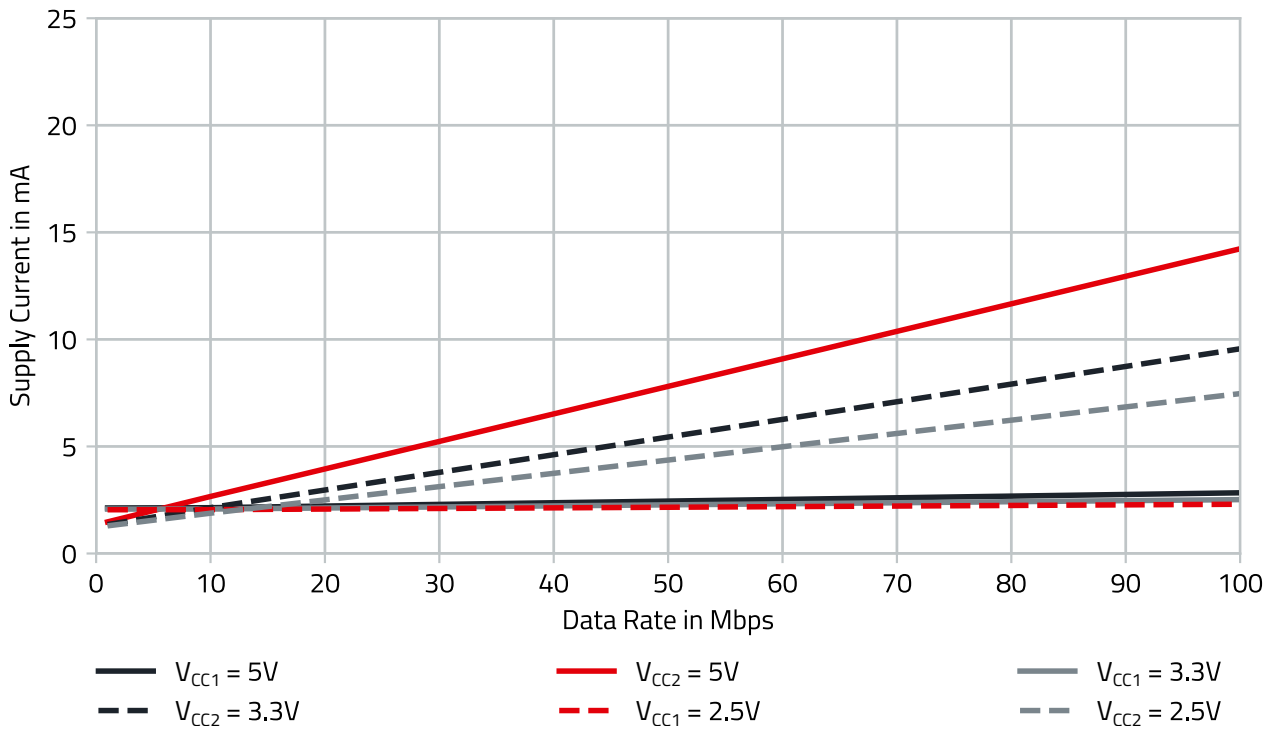


Figure 14: 18012015411x supply current vs. data rate.

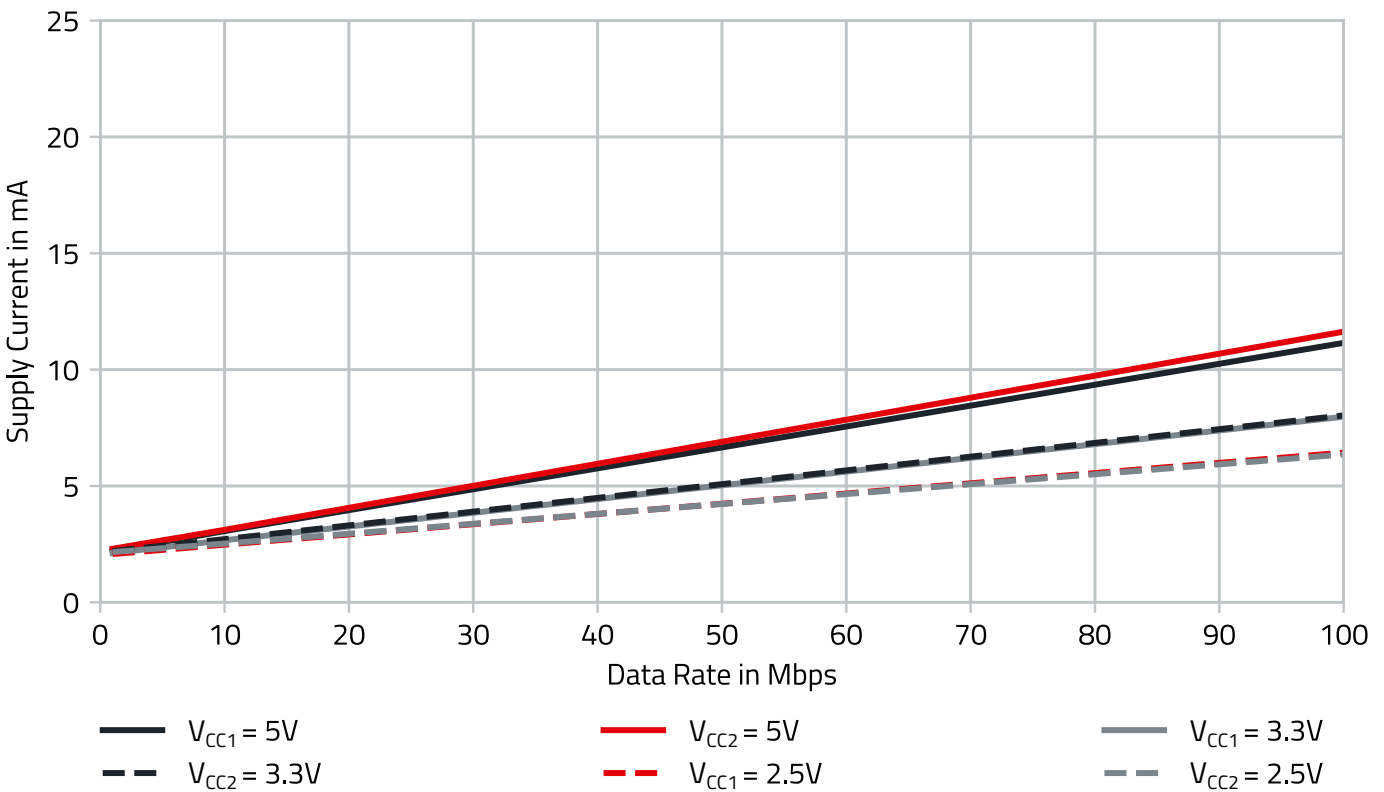


Figure 15: 18012115411x supply current vs. data rate.

13.1.5 High and Low Voltage Levels vs. Output Current

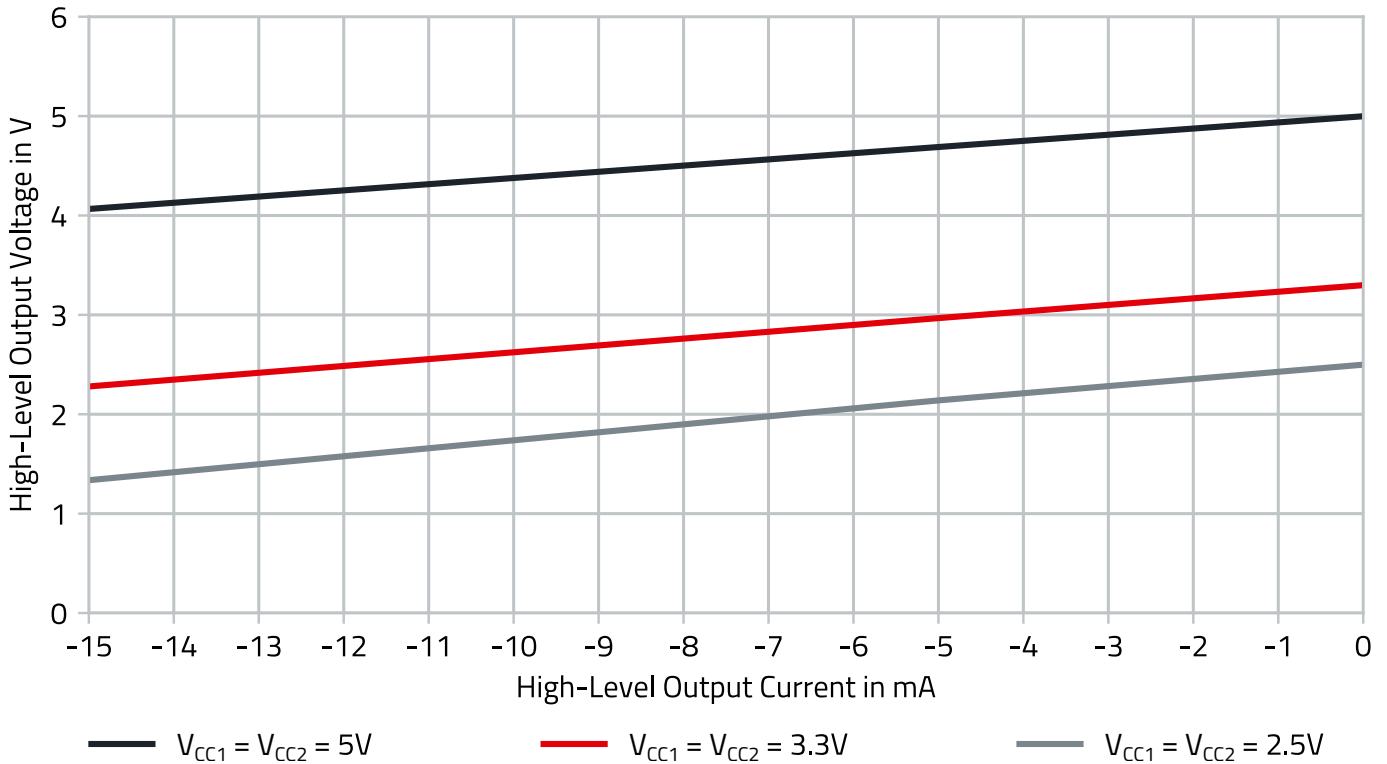


Figure 16: 18012x15411x high-level output voltage vs. high-level output current.

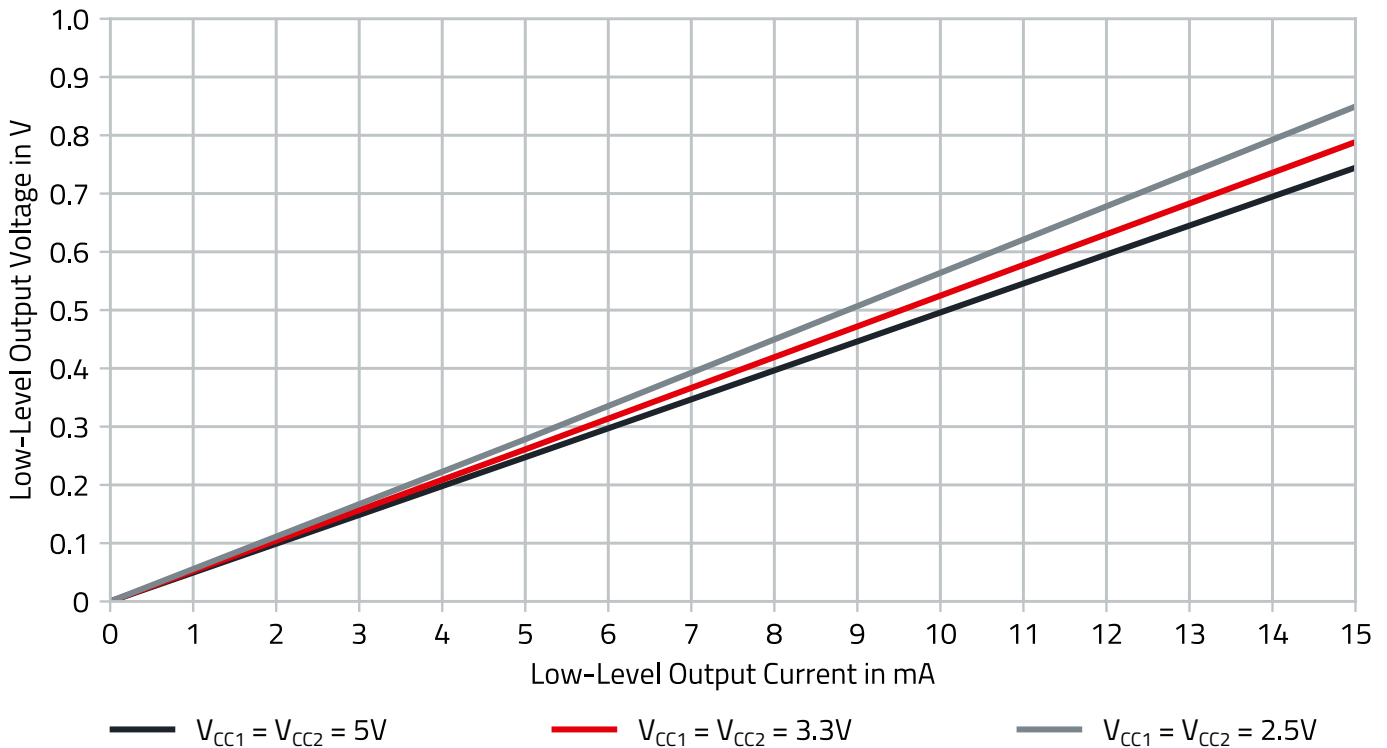


Figure 17: 18012x15411x low-level output voltage vs. low-level output current.

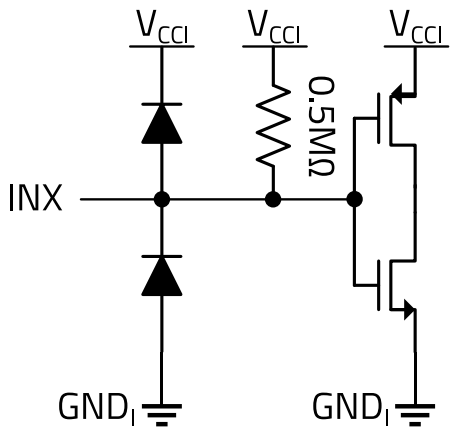
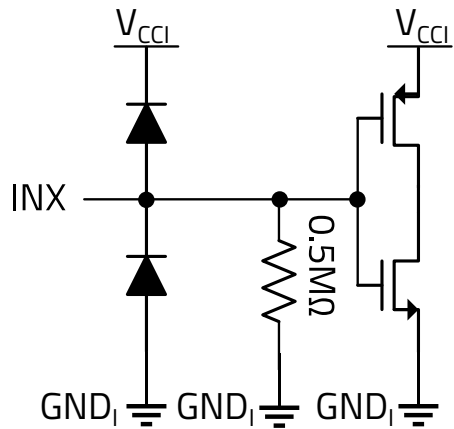
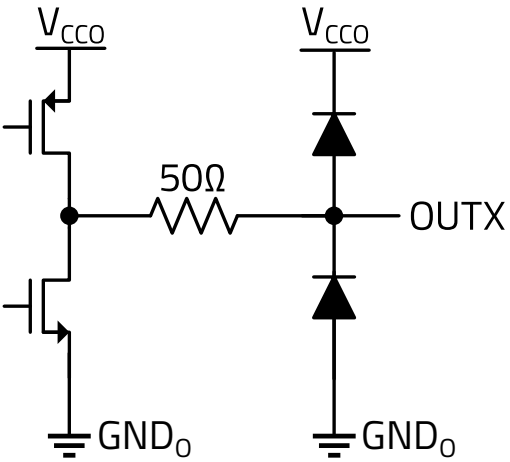
14 TRUTH TABLE

Table 14: I/O truth table.

V_{CC1}	V_{CC2}	Input V_{INX}	Output V_{OUTX}	Operation
$\geq 2.375V$	$\geq 2.375V$	H	H	Normal operation: The channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output: When input V_{INX} is open, the corresponding channel output goes to its default logic state.
$\leq 2V$	$\geq 2.375V$	X	Default	Default output: When the primary supply is unpowered, a channel output assumes the logic state based on its default configuration. Parts with H have a default of high while parts with L have a default of low.
X	$\leq 2V$	X	Undetermined	If V_{CC2} is unpowered, the channel output is undetermined.

15 I/O DESCRIPTION

Table 15: I/O schematics.

 <p>Figure 18: Default high channel input internal structure.</p>	 <p>Figure 19: Default low channel input internal structure.</p>
 <p>Figure 20: Channel output internal structure.</p>	

NOTE: For forward channels $V_{CCI} = V_{CC1}$, $V_{CCO} = V_{CC2}$, $GND_1 = GND1$ and $GND_0 = GND2$.
 For reverse channels $V_{CCI} = V_{CC2}$, $V_{CCO} = V_{CC1}$, $GND_1 = GND2$ and $GND_0 = GND1$.

16 TEST SCHEMATICS

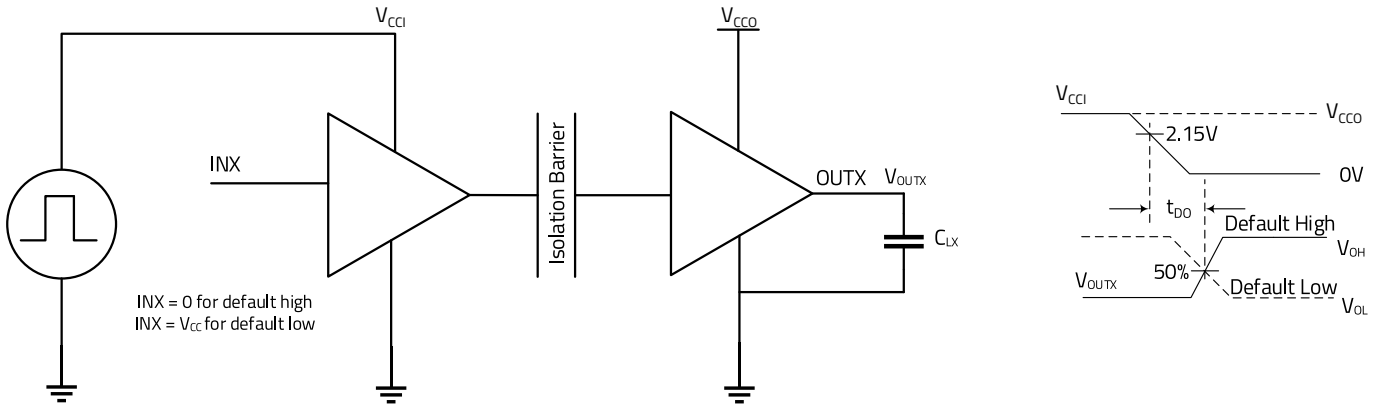


Figure 21: Default output delay .

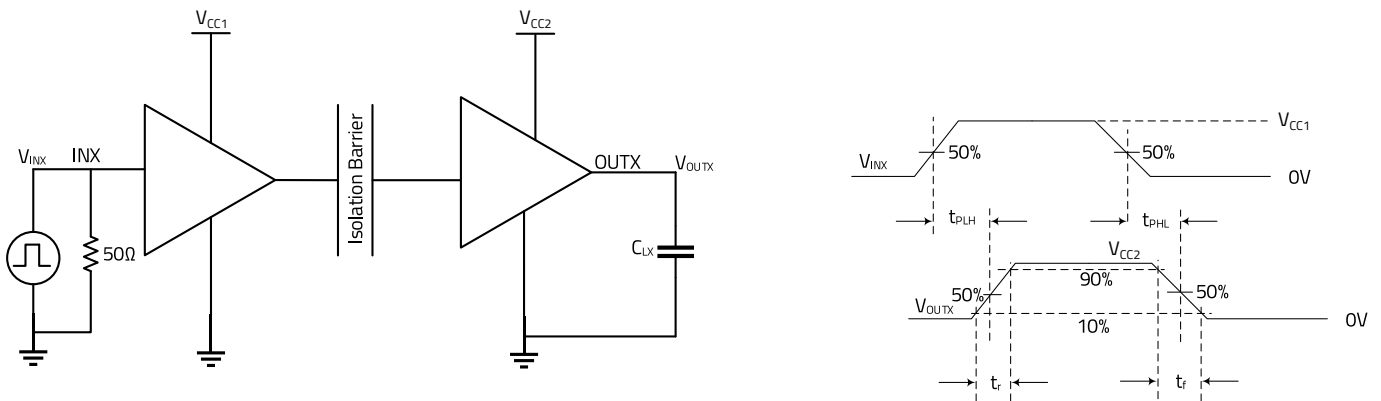


Figure 22: Propagation delay test schematic.

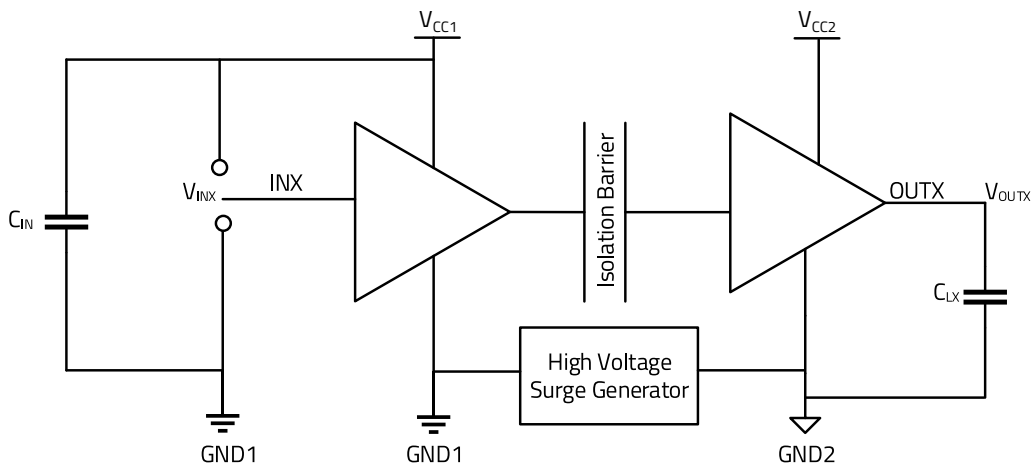


Figure 23: CMTI test schematic.

Note: C_{LX} = 15 pF and includes instrumentation and fixture capacitance within $\pm 20\%$.

17 BLOCK DIAGRAM

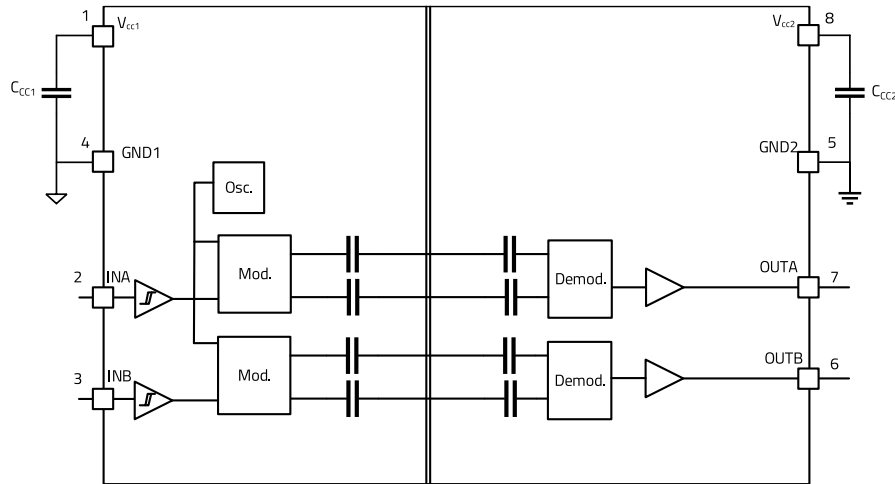


Figure 24: 18012015411x block diagram.

18 CIRCUIT DESCRIPTION

The WPME-CDIS digital isolator consists of two capacitive isolated digital channels that must be powered by two isolated supply voltages. The device is typically operated using 5V, 3.3V or 2.5V and the primary and secondary sides can be independently powered with any voltage within the operating conditions. The WPME-CDIS integrates the isolation capacitors in addition to the modulators and demodulators needed to construct the two isolated channels.

The isolation channels are realized using on/off key (OOK) modulation to transmit high or low speed signals through silicon dioxide isolation barriers. The on-chip oscillator is used to modulate the schmitt-triggered input signal. The modulator generates a differential signal that is transmitted through the capacitive isolation lines. The demodulator is located on the output side of the signal channel and used to amplify, filter and reconstruct the input signal with minimum propagation delay and distortion. Finally, the output of the demodulator is given to the output through buffer to improve the driving strength.

19 PROTECTION FEATURES

19.1 Input/Output Undervoltage Lockout (UVLO)

The device incorporates input and output undervoltage lockout (UVLO) to protect from unexpected behavior at input voltages below the recommended values. The thresholds of the UVLO are indicated in the [ELECTRICAL SPECIFICATIONS](#).

20 TYPICAL APPLICATION

The figure below depicts a typical application for a digital isolator used in a CAN bus configuration between a controller and transceiver.

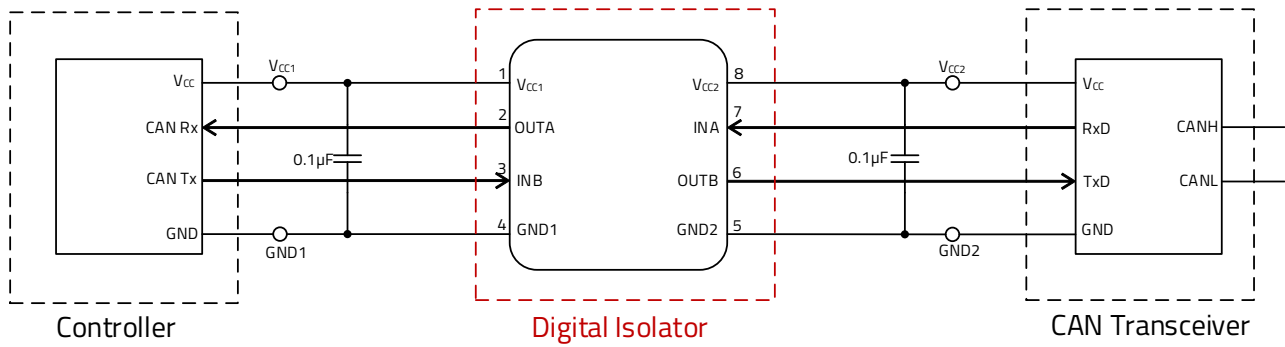


Figure 25: Typical application: CAN bus.

The 18012115411H and 18012115411L are shown in the above diagram in a conventional CAN implementation. The channel configuration allows for appropriate isolation and communication between the controller and transceiver.

21 HANDLING RECOMMENDATIONS

1. The digital isolator is classified as MSL3 (JEDEC Moisture Sensitivity Level 3) and requires special handling due to moisture sensitivity (JEDEC J-STD033D).
2. The parts are delivered in a sealed bag (Moisture Barrier Bag = MBB) and should be processed within one year.
3. When opening the moisture barrier bag, check the Humidity Indicator Card (HIC) for the color status. Bake parts prior to soldering in case indicator color has changed according to the notes on the card.
4. Parts must be processed after 168 hour (7 days) of floor life. Once this time has been exceeded, bake parts prior to soldering per JEDEC J-STD033D recommendation.
5. Maximum number of soldering cycles is two.
6. For minimum risk, solder the device in the last solder cycle of the PCB production.
7. The component lead material is copper (Cu) and the lead finish is Matte Tin (Matte Sn).
8. For solder paste use a standard SAC Alloy such as SAC 305, type 3 or higher.
9. The profile below is valid for convection reflow only.
10. Other soldering methods (e.g. vapor phase) are not verified and have to be validated by the customer at their own risk.

21.1 Soldering Profile

Table 16: Reflow solder profile.

Profile Feature	Symbol	Value
Preheat temperature minimum	T_{s_min}	150°C
Preheat temperature maximum	T_{s_max}	200°C
Preheat time from T_{s_min} to T_{s_max}	t_s	60-120 seconds
Liquidous temperature	T_L	217°C
Time maintained above T_L	t_L	60-90 seconds
Classification temperature	T_C	260°C
Peak package body temperature	T_P	$T_P \leq T_C$
Time within $T_C - 5^\circ\text{C}$ and T_C	t_p	$t_p \leq 30$ seconds
Ramp-up Rate (T_L to T_P)		3°C/second maximum
Ramp-down rate (T_P to T_L)		6°C/second maximum
Time 25°C to peak temperature		8 minutes maximum

Please refer to JEDEC J-STD020 for further information pertaining to reflow soldering of electronic components.

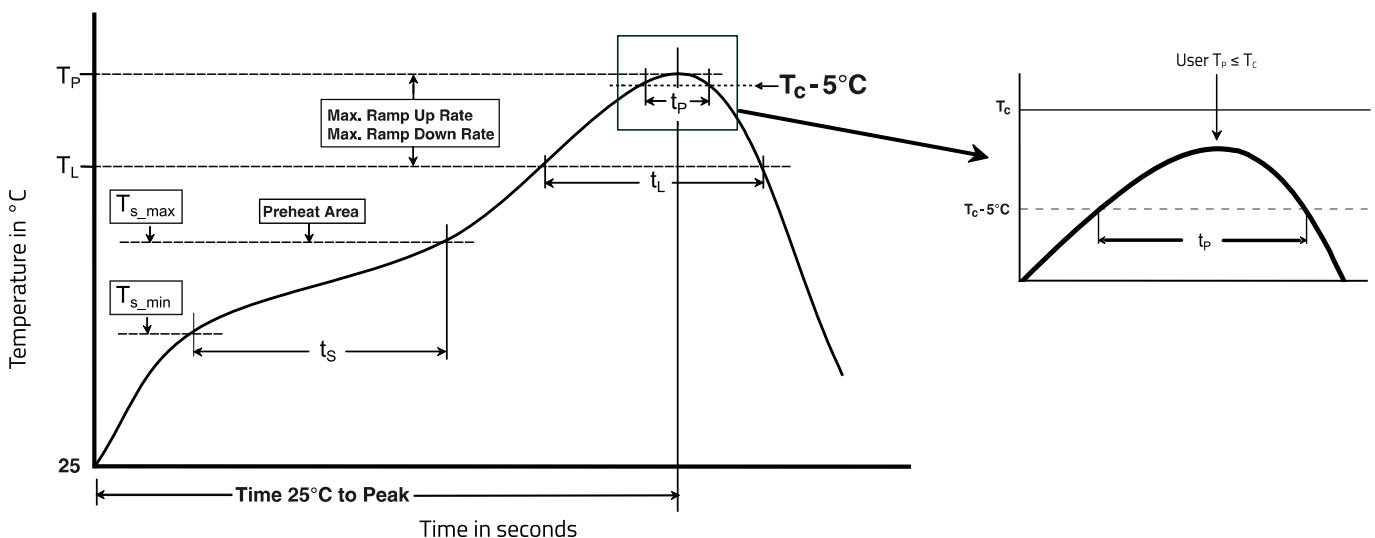


Figure 26: Soldering profile.

22 PHYSICAL DIMENSIONS

22.1 Component

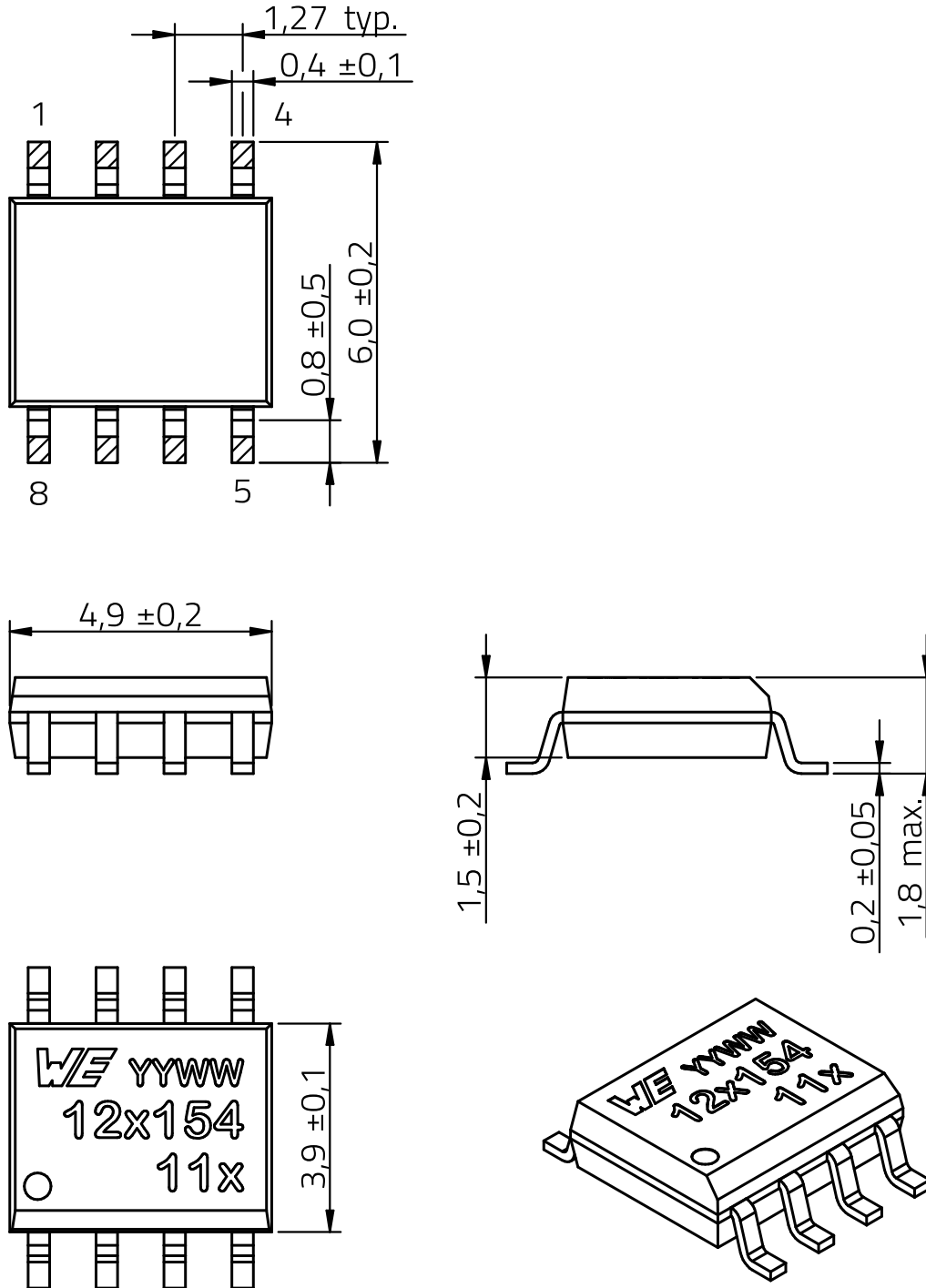


Figure 27: Component dimensions.

All dimensions in mm
 Tolerance: xx.x = ±0.5mm ; xx.xx = ±0.25mm unless otherwise noted

22.2 Recommended Landpattern

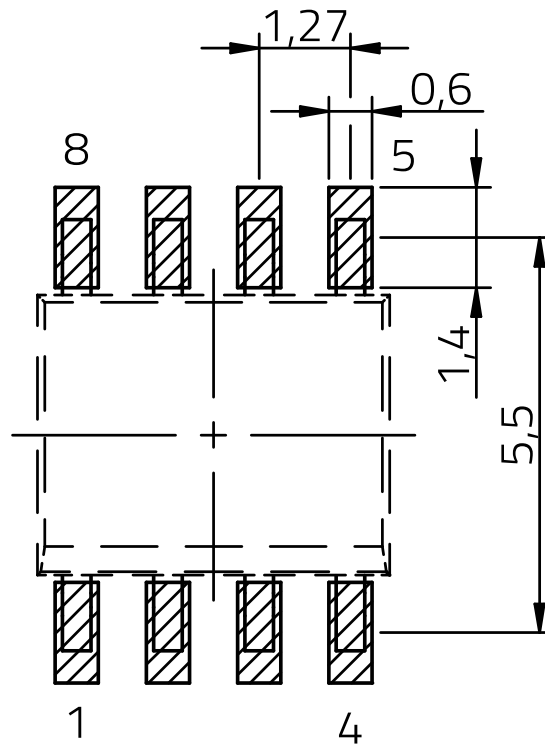


Figure 28: Recommended landpattern dimensions.
All dimensions in mm.

22.3 Packaging

Reel in mm

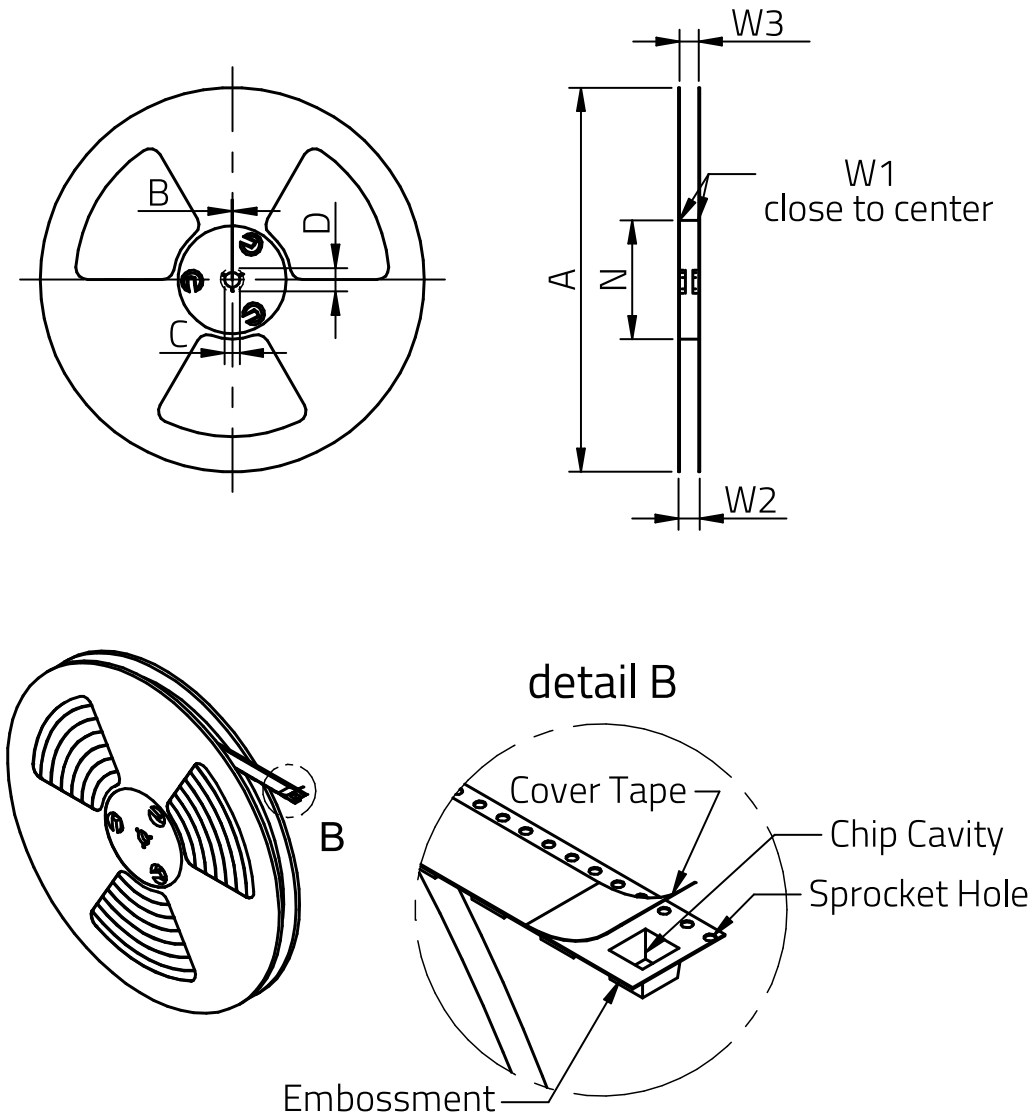


Figure 29: Reel dimensions.

Table 17: Reel dimensions.

A	B	C	D	N	W1	W2	W3	W3
±2.00	min.	min.	min.	min.	+2.00	max.	min.	max.
330.00	1.50	12.80	20.20	60.00	12.40	22.40	15.90	19.40

Reel material is polystyrene.
 All dimensions in mm.

Tape in mm

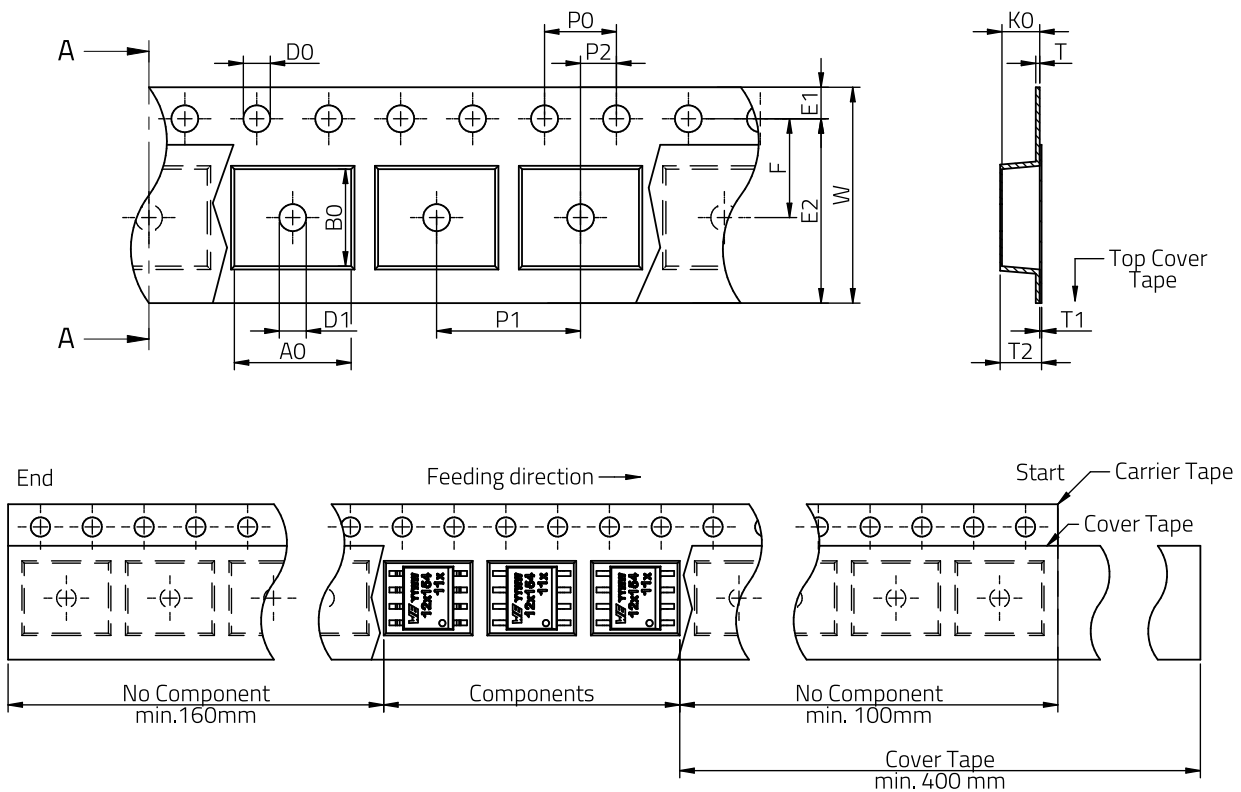


Figure 30: Tape dimensions.

Table 18: Tape dimensions part 1.

A0	B0	D0	D1	E1	E2	F	P0	P1	P2	W
typ.	typ.	min.	±0.10	min.	±0.10	±0.10	±0.10	±0.10	±0.10	±0.10
6.40	5.40	1.50	1.50	1.75	14.25	7.50	4.00	8.00	2.00	12.00

Table 19: Tape dimensions part 2.

K0	T	T1	T2	W
typ.	typ.	ref.	typ.	typ.
2.1	0.35	0.1	3.4	12

Tape material is polystyrene.
All dimensions in mm.



23 DOCUMENT HISTORY

Table 20: Document history.

Revision	Date	Description	Comment
1.0	October 2023	Initial release of data sheet	

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26 CAUTIONS AND WARNINGS

The following conditions apply to all goods within the product series of digital isolators of Würth Elektronik eiSos GmbH & Co. KG:

General:

- All recommendations according to the general technical specifications of the data-sheet have to be complied with.
- The usage and operation of the product within ambient conditions which probably alloy or harm the component surface has to be avoided.
- The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products
- Residual washing varnish agent that is used during the production to clean the application might change the characteristics of the body, pins or termination. The washing varnish agent could have a negative effect on the long term function of the product. Direct mechanical impact to the product shall be prevented as the material of the body, pins or termination could flake or in the worst case it could break. As these devices are sensitive to electrostatic discharge customer shall follow proper IC Handling Procedures.
- Customer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of Würth Elektronik eiSos GmbH & Co. KG components in its applications, notwithstanding any applications-related information or support that may be provided by Würth Elektronik eiSos GmbH & Co. KG.
- Customer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences lessen the likelihood of failures that might cause harm and take appropriate remedial actions
- Customer will fully indemnify Würth Elektronik eiSos and its representatives against any damages arising out of the use of any Würth Elektronik eiSos GmbH & Co. KG components in safety-critical applications

Product specific:

Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to comply with the technical reflow or wave soldering specification, otherwise this will void the warranty.
- All products are supposed to be used before the end of the period of 12 months based on the product date-code.
- Violation of the technical product specifications such as exceeding the absolute maximum ratings will void the warranty.
- It is also recommended to return the body to the original moisture proof bag and reseal the moisture proof bag again.
- ESD prevention methods need to be followed for manual handling and processing by machinery.

Disclaimer:

This electronic component has been designed and developed for usage in general electronic equipment only. This product is not authorized for use in equipment where a higher safety standard and reliability standard is especially required or where a failure of the product is reasonably expected to cause severe personal injury or death, unless the parties have executed an agreement specifically governing such use. Moreover Würth Elektronik eiSos GmbH & Co. KG products are neither designed nor intended for use in areas such as military, aerospace, aviation, nuclear control, submarine, transportation (automotive control, train control, ship control), transportation signal, disaster prevention, medical, public information network etc. Würth Elektronik eiSos GmbH & Co. KG must be informed about the intent of such usage before the design-in stage. In addition, sufficient reliability evaluation checks for safety must be performed on every electronic component which is used in electrical circuits that require high safety and reliability functions or performance. These cautions and warnings comply with the state of the scientific and technical knowledge and are believed to be accurate and reliable. However, no responsibility is assumed for inaccuracies or incompleteness.

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It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications. In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

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Any product-specific notes, warnings and cautions must be strictly observed. Any disregard will result in the loss of warranty.

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Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard we inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

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