STSPIN958

Datasheet

Scalable 5 A full-bridge driver for brushed DC motors

Features

- Operating voltage up to 58V
- Maximum output current up to 5 Arms
- Seven driving methods with dual half-bridge, single full-bridge and half-bridge parallel mode
- $R_{DS(ON)}$ HS + LS = 0.33 Ω typ.
- Adjustable power MOS slew rate
- Integrated amplifiers with two different embedded current control techniques
- Adjustable OFF-time with slow or mixed decay
- Low consumption standby
- Protections
  - UVLO
  - Overcurrent protection
  - Thermal shutdown

Application

- Stage lighting
- Factory automation
- ATM and money handling machines
- Textile machines
- Home appliances
- Robotics
- Antenna control
- Vending machines

Product status link

STSPIN958

Product label

SUSTAINABLE TECHNOLOGY

Description

The STSPIN958 is a 5A full bridge driver for brushed DC motors.

The power stage is designed with high dynamic performance, allowing to achieve high frequency PWM control with precise duty-cycle.

The device offers a current limiter with adjustable threshold and off-time with slow or mixed decay selection. Two amplifiers with fixed amplification factor are available for current sensing (using an external shunt resistor).

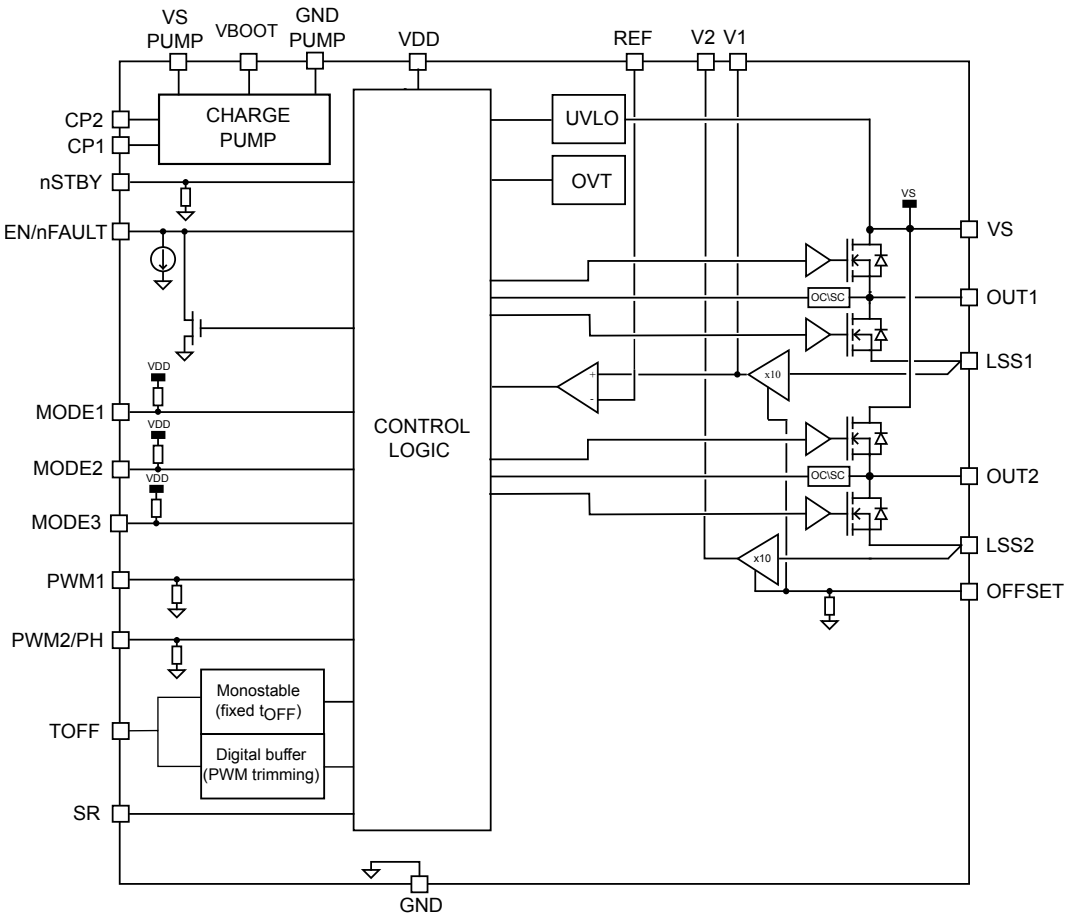
The adjustable slew-rate guarantees the best trade-off between performances and EMI.

Versatile power stage offers seven different ways of operation for a high level of flexibility.

The device offers a complete set of protection features including overcurrent, overtemperature and low bus voltage detection.

1 Block diagram

Figure 1. **Block diagram**



2 Electrical data

2.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 1 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute maximum ratings

Symbol	Parameter	Test condition	Value	Unit
V_{DD}	Control logic supply voltage		-0.3 to 4	V
V_S	Power stage supply voltage		-0.3 to 62	V
dV_S/dt	Supply voltage gradient		0.5	V/µs
V_{SPUMP}	Charge pump input voltage		V_S +/- 0.1 V	V
V_{BOOT}	Bootstrap voltage		-0.3 to 62	V
V_{OUT}	Output voltage	V_S < 61.4 V	V_S + 0.6	V
		V_S ≥ 61.4 V	62	
I_{OUT}	DC output current	Each output	Up to 5	A_{rms}
$I_{OUT,peak}$	Peak output current		Limited by OC protection	A
V_{LSS}	Low-side source voltage (LSSxx pins)		-0.6 to +2	V
V_{REFA}, V_{REFB}	Voltage range at pins REFA and REFB	V_{DD} = 4 V	-0.3 to V_{DD}	V
V_{SR}	Voltage range at pin SR	V_{DD} = 4 V	-0.3 to V_{DD}	V
V_{TOFFx}	Voltage range at pins T_{OFFx}	V_{DD} = 4 V	-0.3 to V_{DD}	V
V_{IN}	Logic input voltage	All digital inputs excluded MODE1, MODE2, MODE3 and OFFSET	-0.3 to 5.5	V
		MODE1, MODE2, MODE3 and OFFSET	-0.3 to V_{DD}	V
I_{OD}	Open drain outputs sink current	nFAULT	Up to 8	mA
T_{stg}	Storage temperature		-55 to 150	°C
T_j	Junction temperature		-40 to 150	°C

2.2 Recommended operating conditions

Table 2. Recommended operating conditions

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DD}	Control logic supply voltage		2.8(1)	3.3	3.6	V
V_S(2)	Power stage supply voltage		5.05		58(3)	V
V_{SPUMP}	Charge pump input voltage			V_S		V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{BO}	Bootstrap overdrive voltage	$V_{BOOT} - V_S$		3		V
V_{REFA}	Voltage range at pin REF		0.1		V_{DD}	V
V_{LSS1}, V_{LSS2}	Low-side source voltage		-0.6		+1	V
V_{OUT}	Output voltage		-0.6		V_S	V
V_{IN}(4)	Logic input voltage	Excluded MODE1, MODE2, MODE3, OFFSETA and OFFSETB	0		5	V
		MODE1, MODE2, MODE3, OFFSETA and OFFSETB	0		VDD	V
R_{TOFF}	Current limiter time setting resistor	Enabled	10		120	kΩ
		Disabled		0		
C_{TOFF}	Current limiter time setting capacitor	Enabled	0.1		5.6	nF
		Disabled		0		
R_{SR}	Slew rate selection resistor		See Table 7			
t_{pulse}	Minimum PWM pulse width		280			ns
t_{BOOT}	Charge pump capacitor charging time	C_{CP} = 100 nF C_{BOOT} = 1 µF		170		µs
f_{PWM}	Switching frequency		0		500(5)	kHz
C_{BOOT}	Bootstrap capacitor			1		µF
C_{CP}	Charge pump capacitor			100		nF
T_{amb}	Ambient temperature		-40		85(2)	°C

1. *Actual operative range can be limited by UVLO protections*
2. *Actual operative range according to heat dissipation performance of the application*
3. *In specific conditions (Tj ≥ 75 °C and RH ≥ 60%), the maximum V_S voltage is sustainable for a limited period*
4. *All digital inputs (excluding MODE1,MODE2,MODE3,and OFFSET) are 5 V tolerant*
5. *Actual operative range can be limited by the selected slew rate*

2.3 ESD protection ratings

Table 3. ESD protection ratings

Symbol	Parameter	Condition	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS-001-2014	H2	2	kV
CDM	Charge device model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014	C2a	500	V
		Corner pins only	C2	750	V

Symbol	Parameter	Condition	Class	Value	Unit
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS-002-2014			

2.4 Thermal data

Table 4. Thermal data

Symbol	Parameter	Condition	Value	Unit
R_{thJA}	Junction to ambient thermal resistance	Natural convection, according to JESD51-2a(1)	35.8	°C/W
$R_{thJCtop}$	Junction to case thermal resistance (top side)	Cold plate on package top, according to JESD51-12.01(1)	22.8	°C/W
$R_{thJCbot}$	Junction to case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-12.01(1)	4	°C/W
R_{thJB}	Junction to board thermal resistance	According to JESD51-8(1)	17.4	°C/W
Ψ_{JT}	Junction to top characterization	According to JESD51-12.01(1)	0.2	°C/W
Ψ_{JB}	Junction to board characterization	According to JESD51-12.01(1)	17	°C/W

1. *Simulated as per standard JEDEC (JESD51-7) in natural convection*

3 Electrical characteristics

Testing conditions: V_S = 58 V, V_{BOOT} = 61 V, V_{DD} = 3.3 V, unless otherwise specified.
Typical values are tested at T_j = 25 °C, minimum and maximum values are guaranteed by thermal characterization in the temperature range of -40 to 125 °C, unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply						
$V_{DDth(ON)}$	V_{DD} power-on reset	V_{DD} rising			2.7	V
$V_{DDth(Hyst)}$	V_{DD} power-on reset hysteresis	V_{DD} falling ($V_{DDth(ON)}$ - $V_{DDth(OFF)}$)	100		300	mV
$V_{Sth(ON)}$	V_S turn-on threshold	V_S rising			5.05	V
$V_{Sth(Hyst)}$	V_S turn-on threshold hysteresis	V_S falling ($V_{Sth(ON)}$ – $V_{Sth(OFF)}$)	100		300	mV
V_{BO}	Bootstrap overdrive voltage V_{BOOT} - V_{SPUMP}			3		V
$V_{BOth(ON)}$	V_{BO} turn-on threshold	V_{BO} rising			2	V
$I_{DD,STBY}$	V_{DD} consumption in standby	Standby			3	µA
$I_{S,STBY}$	V_S consumption in standby	Standby			1	µA
t_{STBY}	Standby time				600	µs
t_{WAKE}	Wake-up time				10	µs
Power stage						
$R_{DS(ON),LS}$	Low-side turn-on resistance	T_j = 25 °C		165		mΩ
$R_{DS(ON),HS}$	High-side turn-on resistance	T_j = 25 °C		165		mΩ
$t_{dIN(H)}$	Input high to high-side turn-on propagation delay	Maximum slew rate		300		ns
$t_{dIN(L)}$	Input low to low-side turn-on propagation delay	Maximum slew rate		300		ns
MT	Delay matching, HS and LS turn-on/off	Maximum slew rate MT = $\lvert t_{dH} - t_{dL} \rvert$			50	ns
SR_{rise}	Rising slew rate	R_{SR} = 1 kΩ R_{SR} = 2.2 kΩ R_{SR} = 5.6 kΩ R_{SR} = 10 kΩ		2 1.2 0.6 0.3		V/ns
SR_{fall}	Falling slew rate	R_{SR} = 1 kΩ R_{SR} = 2.2 kΩ R_{SR} = 5.6 kΩ R_{SR} = 10 kΩ		2 1.2 0.6 0.3		V/ns
Logic input and outputs						
V_{IL}	Low logic input voltage				0.8	V
V_{IH}	High logic input voltage		2			V
$V_{IL(EN)}$	Enable low logic input voltage				0.4	V

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{IH(EN)}$	Enable high logic input voltage		2.55			V
$V_{OL(nFAULT)}$	Low logic level output voltage (EN/nFAULTx)	I_{SINK} = 4 mA			0.4	V
V_{FAULT}	FAULT open drain release threshold		0.4		0.6	V
I_{PD}	EN/nFAULTA and EN/nFAULTB pull-down current			5		µA
R_{PDin}	Input pull-down resistor			570		kΩ
R_{PUin}	Input pull-up resistor (MODE1, MODE2, and MODE3)			570		kΩ
Current limiter						
t_{OFF}	Current limiter off-time See Figure 10	R_{OFF} = 10 kΩ C_{OFF} = 0.1 nF		1		µs
		R_{OFF} = 120 kΩ C_{OFF} = 5.6 nF		500		µs
Integrated amplifier						
A_{CL}	Gain	Full temp range	9.5	10	10.5	V/V
$t_{settling}$	Output voltage settling time	V_{in} 150 mV step C_L= 100 pF			200	ns
Protections						
I_{OC}	Overcurrent threshold	See Figure 13	7		14	A
T_{SD}	Thermal shutdown threshold		150			°C
$T_{SD(Hyst)}$	Thermal shutdown hysteresis			30		°C

4 Pin description

Figure 2. **Pin connection**

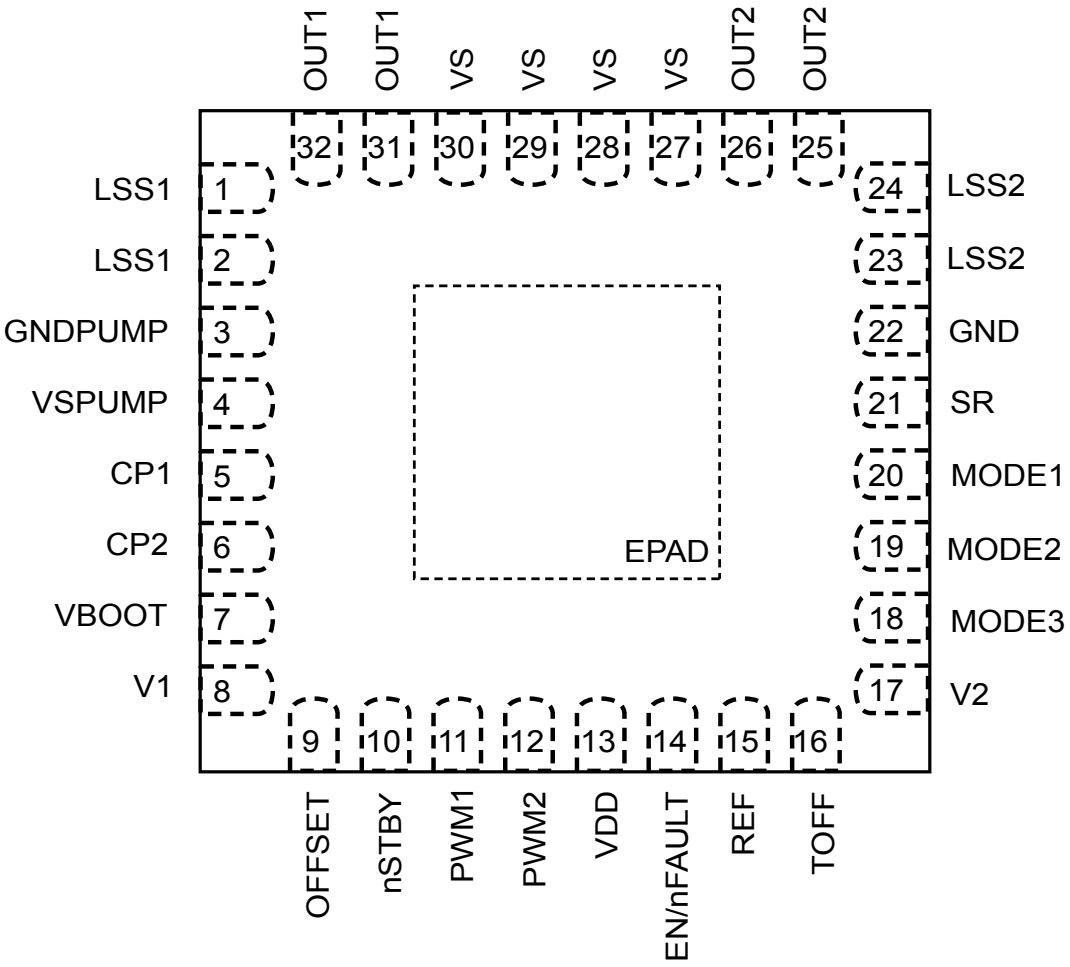


Table 6. **Pad list**

N.	Name	Type	Function
1	LSS1	Power	Low-side source half-bridge 1
2	LSS1	Power	Low-side source half-bridge 1
3	GNDPUMP	Ground	Ground charge pump
4	VSPUMP	Supply	Supply charge pump circuitry (internally connected to VS). In application must be connected to the CBOOT. It can be shorted to VS supply
5	CP1	Analog output	Charge pump oscillator output1
6	CP2	Analog output	Charge pump oscillator output2
7	VBOOT	Supply	Bootstrap voltage needed to drive the high-side MOSFETs
8	V1	Analog output	Amplified sense signal, half bridge 1
9	OFFSET	Digital input	Voltage level shift
10	nSTBY	Digital input	Active low standby input. When forced low the device enters in low consumption mode
11	PWM1	Digital input	Half-bridge 1 PWM input

N.	Name	Type	Function
12	PWM2/PH	Digital input	Half-bridge 2 PWM input/Phase input
13	VDD	Supply	Supply digital logic
14	EN/nFAULT	Logic input/open drain output	Logic input with open drain output. Full bridge enable (when low, the power stage is turned off); it is forced low by the integrated open-drain MOSFET when a failure occurs.
15	REF	Analog input	Reference voltage for PWM current limiter circuitry
16	TOFF(B)	Analog input Digital output	PWM current limiter off-time adjustment in fixed off-time mode Decay output signal in PWM trimming mode
17	V2	Analog output	Amplified sense signal, half bridge 2
18	MODE3	Digital input	Mode selector pin 3
19	MODE2	Digital input	Mode selector pin 2
20	MODE1	Digital input	Mode selector pin 1
21	SR	Analog input	Slew rate value selection
22	GND	Ground	Device ground
23	LSS2	Power	Low-side source half-bridge 2
24	LSS2	Power	Low-side source half-bridge 2
25	OUT2	Power	Power output half-bridge 2
26	OUT2	Power	Power output half-bridge 2
27	VS	Supply	Supply output power stages
28	VS	Supply	Supply output power stages
29	VS	Supply	Supply output power stages
30	VS	Supply	Supply output power stages
31	OUT1	Power	Power output half-bridge 1
32	OUT1	Power	Power output half-bridge 1

5 Description

The STSPIN958 is a protected full bridge with low $R_{DS(ON)}$ and high current capability.

The power stages are designed with high dynamic performance allowing to achieve high frequency PWM control with precise duty-cycle.

It integrates a full set of protections, PWM current limiter circuitry and amplifiers for the current sensing through an external shunt resistor.

5.1 Power supply

The device has three supply pins:

- VDD is the control logic supply voltage
- VS is the supply voltage for all the power stage
- VBOOT is the supply voltage for high-side gate drivers

During the power-up, the device is in Under Voltage Lock Out condition (UVLO) until the VS supply voltage rises above the $V_{Sth(ON)}$ threshold and the VBOOT supply voltage rises above the $V_{BOth(ON)}$ threshold.

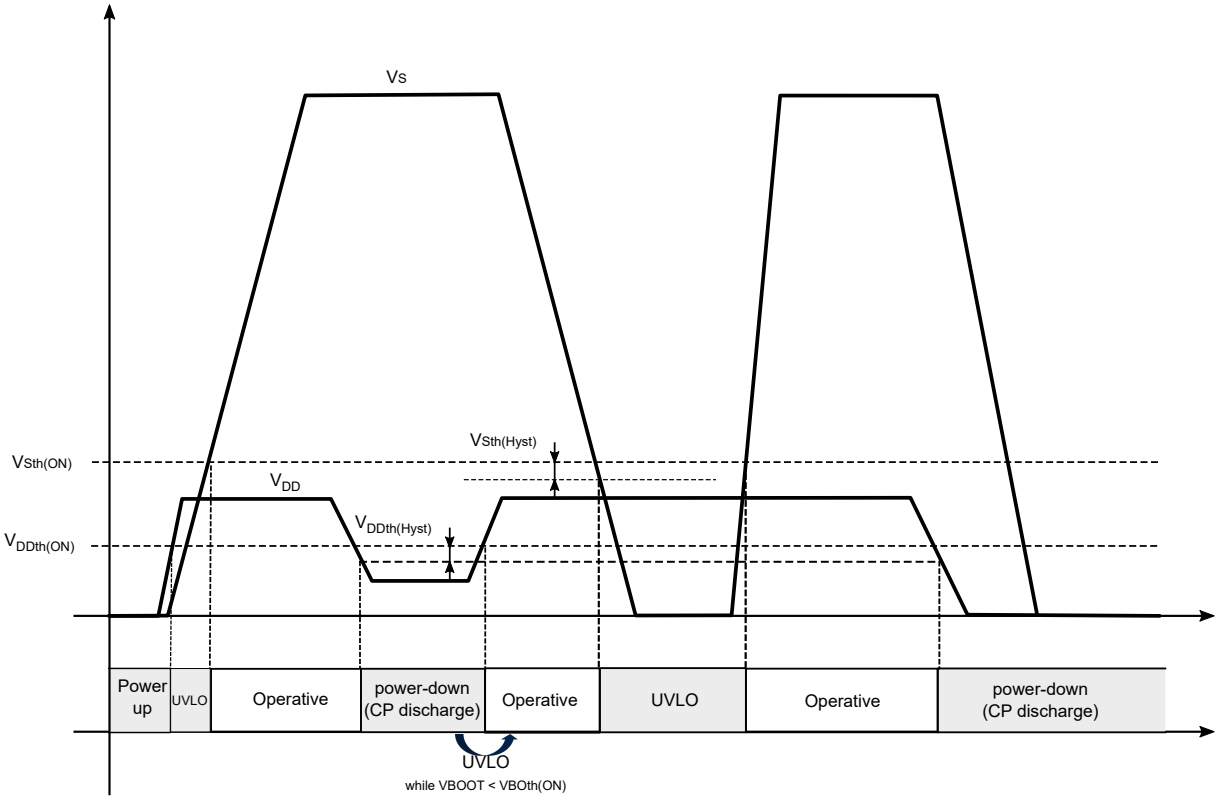
If during the operation the V_S supply falls below $V_{Sth(ON)} – V_{Sth(Hyst)}$, the device returns in UVLO status until the turn-on threshold is exceeded again by Vs.

If during the operation the V_{DD} supply falls below $V_{DDth(ON)} – V_{DDth(Hyst)}$, the device is powered down, power stages are disabled, and all the circuitry (charge pump included) is switched off. When VDD supply rises above $V_{DDth(ON)}$ the device is in UVLO condition and the charge pump is switched on; the device returns operative as soon as VBOOT rises above the $V_{BOth(ON)}$ threshold.

If during the operation the V_{BOOT} supply falls below $V_{BOth(ON)} – V_{BOth(Hyst)}$, the device returns in UVLO status until the turn-on threshold is exceeded again.

In UVLO condition, all the MOSFETs are off and the nFAULT is low.

Figure 3. Power-up and power-down sequences



5.2 Power stages and charge pump circuitry

The STSPIN958 integrates power NMOS half-bridges. The input PWM signal drives a corresponding half-bridge according to the driving mode selected (see Section 5.4 Driving logic). In order to achieve a precise duty-cycle and low jitter between different half-bridge activation, the propagation delay of PWM signals is optimized. Cross conduction is prevented thanks to a deadtime between high-side and low-side MOSFET status change.

A blanking circuitry filters the internally generated noise at each commutation of the power stages.

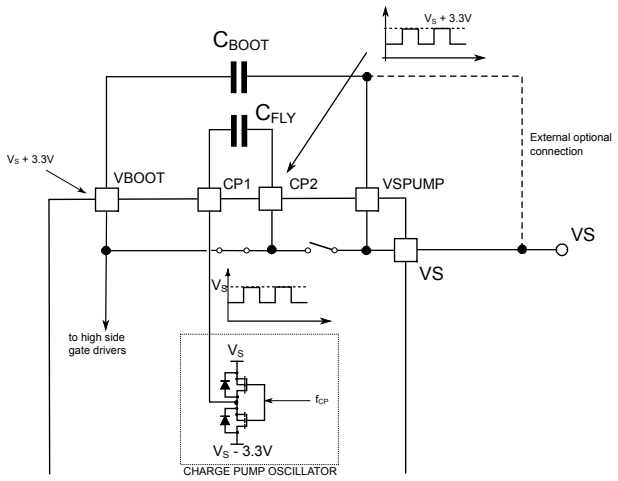
Each gate driving circuit for the high-side MOSFETs is supplied through a charge pump circuitry. The voltage VBOOT is obtained through an internal oscillator with integrated switches and external capacitors implementing a charge pump circuit as shown in Figure 4.

The slew rate of the power bridges output is set according to the value of the resistor connected to the SR pin as reported in Table 7.

Table 7. Slew rate selection

R_{SR} (± 5%)	Output slew rate (typ) [V/ns]
1 kΩ	2
2.2 kΩ	1.2
5.6 kΩ	0.6
10 kΩ	0.3

Figure 4. Charge pump circuitry



5.3 Integrated operational amplifiers

The device integrates two operational amplifiers with fixed A_{CL} amplification factor.

Each amplifier is internally connected to the source of a low-side MOSFET (LSS1 and LSS2).

The output is made externally available through a dedicated pin (V1 and V2).

One pin is also available (OFFSET) to allow a voltage level shift. When forced high, the amplifier output is shifted by VDD/2.

5.4 Driving logic

The device supports seven different driving modes according to the status of three input pins as listed in Table 8:

1. Dual half-bridge - fixed OFF-time
2. Single full-bridge - fixed OFF-time
3. Single half-bridge (parallel mode) - fixed OFF-time
4. Single full-bridge (mixed decay) - fixed OFF-time
5. Dual half-bridge - PWM trimming

6. Single full-bridge - PWM trimming
7. Single half-bridge (parallel mode) - PWM trimming

Table 8. Driving mode selection

MODE1	MODE2	MODE3	Mode	Current limiter mode
LOW	LOW	LOW	Dual half-bridge	Fixed OFF-time
LOW	HIGH	LOW	Single full-bridge	Fixed OFF-time
HIGH	LOW	LOW	Single half-bridge (parallel mode)	Fixed OFF-time
HIGH	HIGH	LOW	Single full-bridge (mixed decay)	Fixed OFF-time with mixed decay
LOW	LOW	HIGH	Dual half-bridge	PWM trimming
LOW	HIGH	HIGH	Single full- bridge	PWM trimming
HIGH	LOW	HIGH	Single half-bridge (parallel mode)	PWM trimming
HIGH	HIGH	HIGH	Reserved	Reserved

Important: It is not allowed to switch from one driving mode to another one during operation. In application, the MODE1, MODE2, and MODE3 inputs should be shorted to ground, left floating, or shorted to VDD.

MODE1, MODE2 and MODE3 inputs integrate an internal pull-up resistor.
EN/nFAULT input has an internal pull-down current.

5.4.1 Dual half-bridge mode

In dual half-bridge mode:

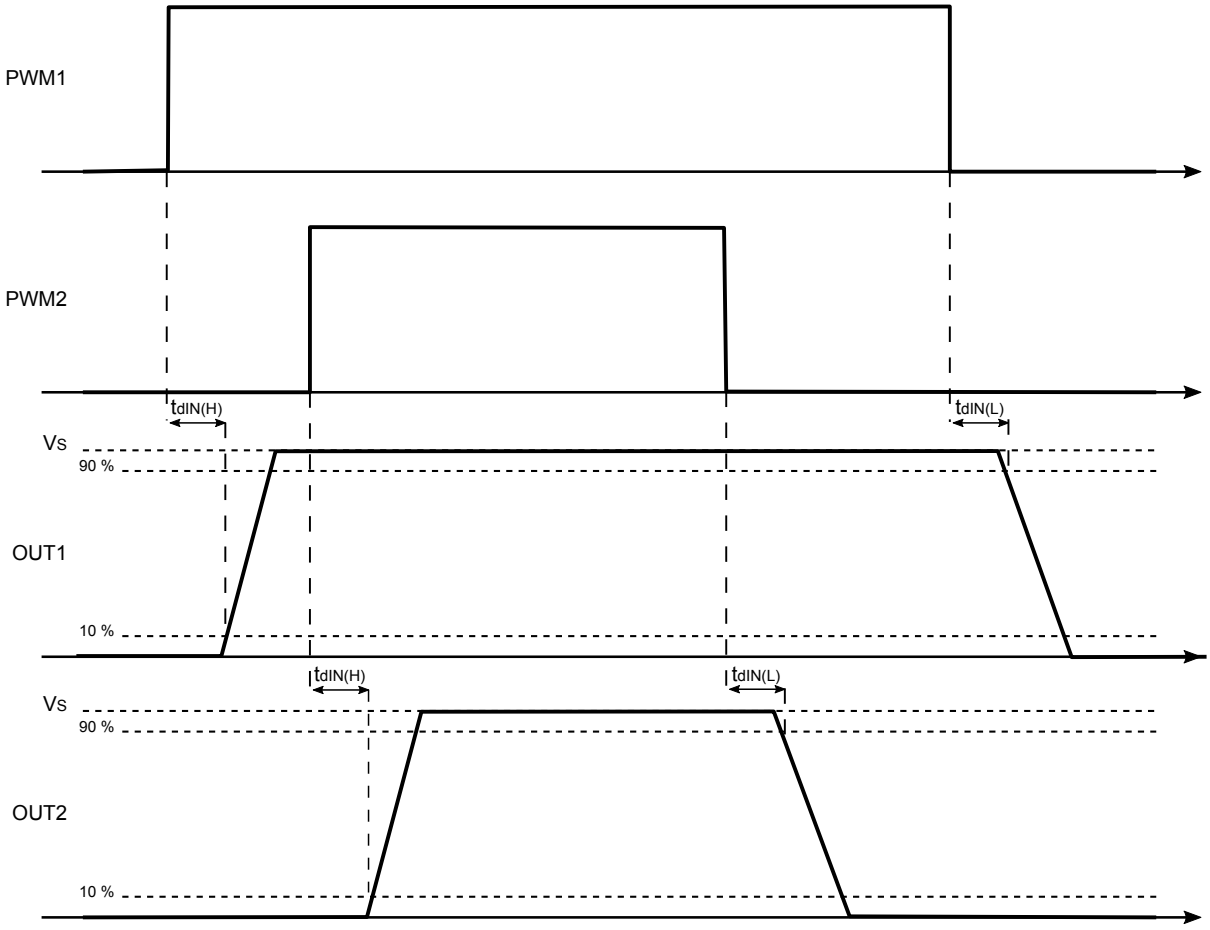
- Each PWM input drives the corresponding half-bridge
- Provided that TOFF is not short-circuited to ground, current limiter connected to V1 and REF operates for both the half bridges. When triggered, the low-side MOS is turned on and a slow decay is performed (see Section 5.6.1.1)
- If a fault condition occurs on half-bridge 1 or 2, EN/nFAULT pin is forced low and both the half-bridges are disabled

Table 9. Truth table – dual half-bridge mode

EN	PWM1	PWM2/PH	OUT1	OUT2
0	X(1)	X(1)	High-Z (2)	High-Z (2)
1	1	1	HS on	HS on
1	0	1	LS on	HS on
1	1	0	HS on	LS on
1	0	0	LS on	LS on

1. *X: don't care*
2. *High-Z: high impedance*

Figure 5. **Driver time diagram - dual half-bridge mode**



5.4.2 Single full-bridge mode

In single full-bridge mode:

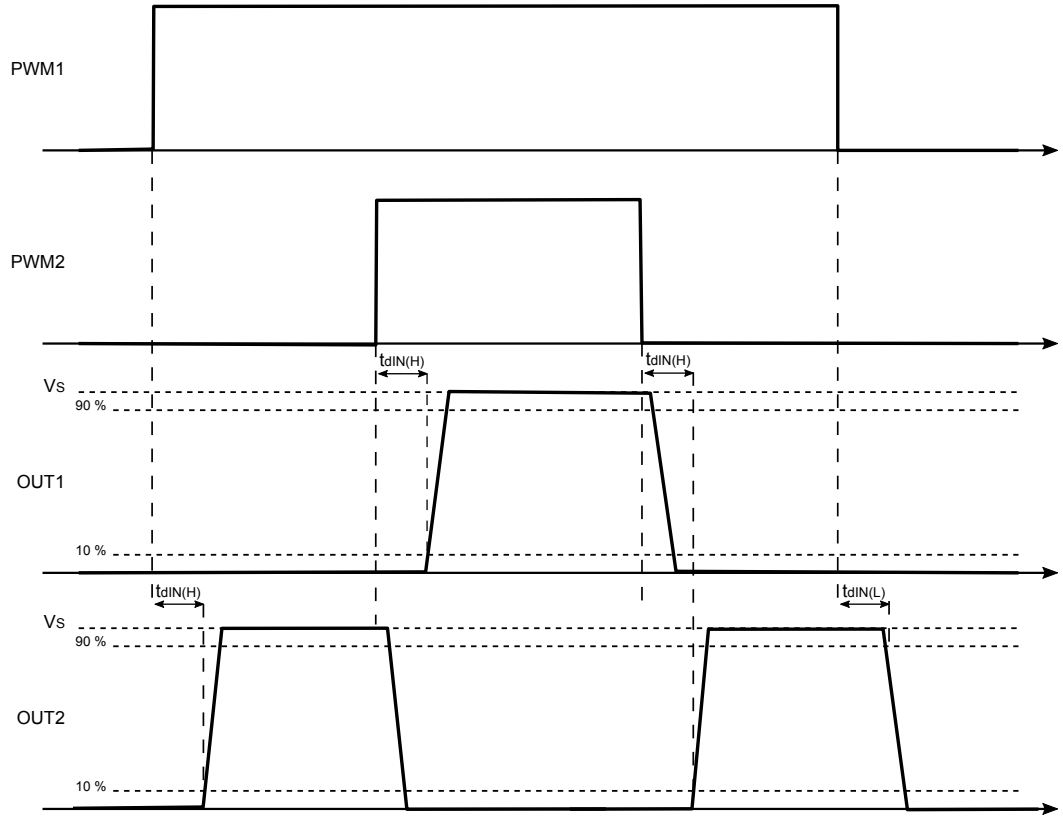
- The outputs of the full-bridge are controlled by the PWM1 and PWM2/PH inputs as reported in Table 10
- When the current limiter is triggered, the low-side MOS is turned on and a slow decay is performed (see Section 5.6.1.1)
- If a fault condition occurs, EN/nFAULT pin is forced low and both the half-bridges (1 and 2) are disabled

Table 10. **Truth table – single full-bridge mode**

EN	PWM1	PWM2/PH	OUT1	OUT2
0	X(1)	X(1)	High-Z(2)	High-Z(2)
1	0	X	LS on	LS on
1	1	1	HS on	LS on
1	1	0	LS on	HS on

1. *X: don't care.*
2. *High-Z: high impedance.*

Figure 6. **Driver time diagram - single full-bridge mode**



5.4.3 Single half-bridge mode - parallel operation

In this mode, the two half-bridges are driven in parallel to obtain a single high-current and low-resistance path:

- PWM1 and PWM2/PH drive the half-bridges as reported in Table 11.
- When current limiter is triggered, a slow decay is performed and the decay mode is selected through PWM2/PH input (see Section 5.6.1.2 and Section 5.6.2.2):
  - if PWM2/PH is low, the low-side MOS is turned on
  - if PWM2/PH is high, the output is in high-Z
- If a fault condition occurs, EN/nFAULT pin is forced low and both the half-bridges (1 and 2) are disabled

This operation mode requires short-circuiting the following pins:

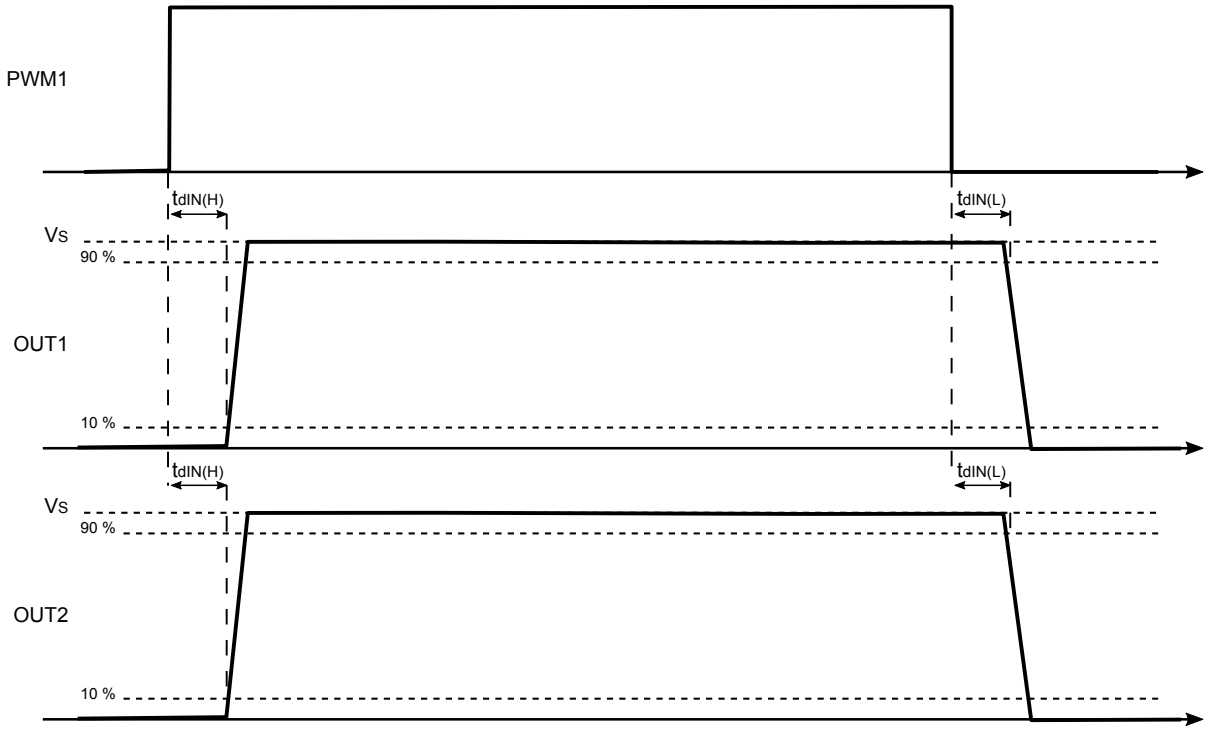
- OUT1 and OUT2
- LSS1 and LSS2

Table 11. **Truth table – single half-bridge mode (parallel operation)**

EN	PWM1	PWM2/PH	OUT1/2
0	X(1)	X(1)	High-Z(2)
1	0	See Section 5.6.1.2 and Section 5.6.2.2	LS on
1	1	See Section 5.6.1.2 and Section 5.6.2.2	HS on

1. *X: don't care.*
2. *High Z: high impedance.*

Figure 7. **Driver time diagram - single half-bridge mode (parallel operation)**



5.4.4 Single full-bridge mode – mixed decay operation

This mode is available only with the current limiter set in fixed OFF-time. The device is driven similarly to “Single full-bridge mode” (see Section 5.4.2); however, when current limiter is triggered, a mixed decay is performed as described in Section 5.6.1.3.

5.5 Standby

The device provides a low consumption mode. In this condition, the charge pump circuitry is turned off.

The device enters the standby mode by forcing low the nSTBY input for at least t_{STBY}. As soon as the input is high, the device returns operative after t_{WAKE} + t_{BOOT}.

In low consumption mode, the EN/nFAULT pin should not be left floating at any times.

During the wake-up, the device is in Under Voltage Lock Out condition (UVLO) until the VBOOT supply voltage rises above the $V_{BOth(ON)}$ threshold. After t_{BOOT}, the charge-pump circuitry charges the bootstrap capacitor and the device becomes operative.

5.6 PWM current control

The device integrates a current limiter internally connected to V1 and REF pins.

The input voltage of the amplifier (V_{LSS1}) is amplified by A_{CL} and output at V1. This voltage is compared with the respective reference voltage (V_{REF}). When $V_{V1} > V_{REF}$ the comparator triggers and the device operates according to the selected decay strategy. The reference voltage value, V_{REF}, must be selected according to the load current target value (peak value), the gain of the embedded amplifier (A_{CL}) and the sense resistors value.

Equation 1

$$V_{REFx} = R_{SENSE} \times A_{CL} + V_{AMPoffset} + V_{AMPoffset} \quad (1)$$

where $V_{AMPoffset}$ is equal to 0 (OFFSETx is low) or $V_{DD}/2$ (OFFSETx is high).

Two current limiter modes are available:

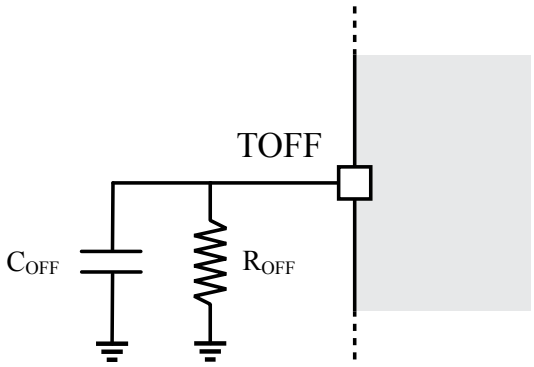
1. Fixed OFF-time
2. PWM trimming

5.6.1 Fixed OFF-time mode

When V_{1x} exceeds V_{REFx} the control circuitry sets the device in limiting status to reduce the current. During the t_{OFF} time, the commutation of the PWMx inputs are ignored.

The device returns to normal operation after a t_{off} time set according to the values of the R_{OFF} resistor and the C_{OFF} capacitor connected to TOFF pin as shown in Figure 8.

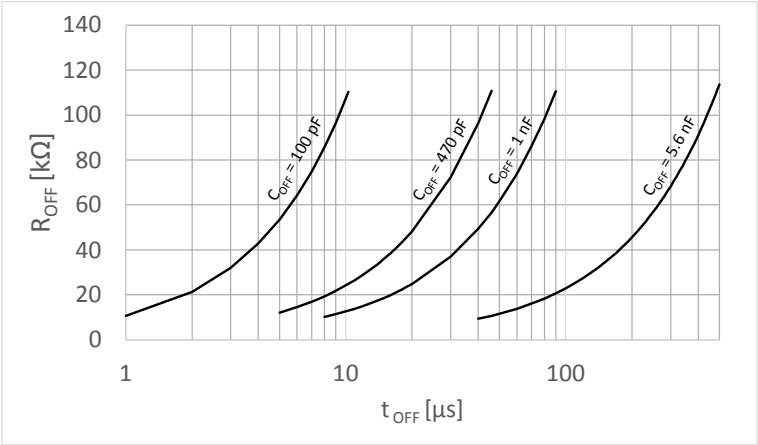
Figure 8. OFF-time regulation circuit



The recommended values for R_{OFF} and C_{OFF} are shown in Figure 9.

Short-circuiting TOFF to ground disables the current limiter.

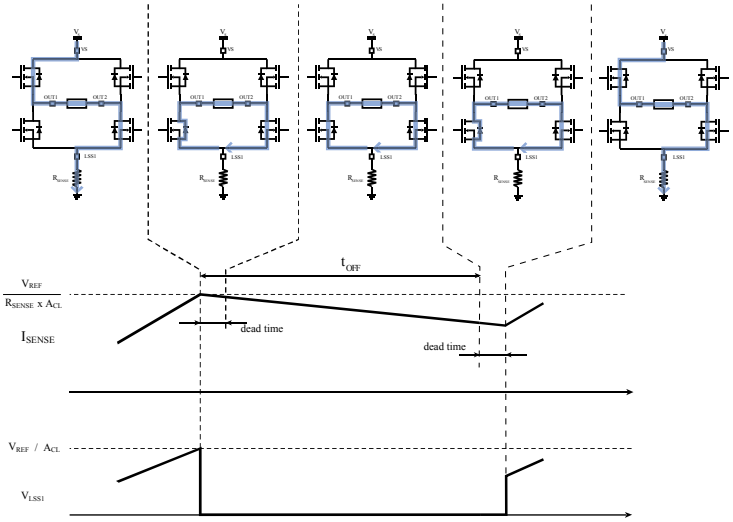
Figure 9. t_{OFF} vs. R_{OFF} and C_{OFF}



5.6.1.1 *Dual half-bridge and full-bridge operation mode (fixed OFF-time)*

In dual half-bridge and full-bridge operation modes, the current is limited turning on both the low-side MOS (slow decay). As soon as the OFF-time expires the bridges return in the ON state (see Figure 10).

Figure 10. **In dual half-bridge and full-bridge operation mode,**



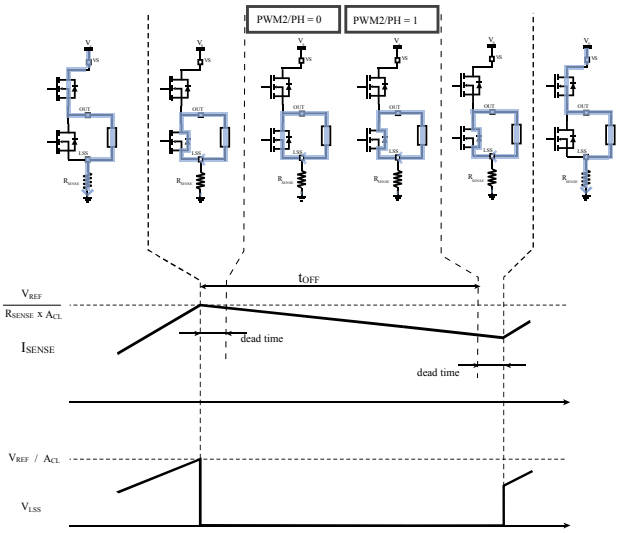
5.6.1.2 *Half-bridge parallel operation mode (fixed OFF-time)*

In half-bridge parallel operation mode, the decay strategy is determined by the status of PWM2/PH (see Figure 11)

- PWM2/PH is low: the low-side MOS is switched on
- PWM2/PH is high: the output is in high impedance (current recirculates in the body diode)

As soon as the OFF-time expires the bridges return in the ON state (see Figure 11).

Figure 11. **Current control in half-bridge parallel mode (fixed OFF-time)**

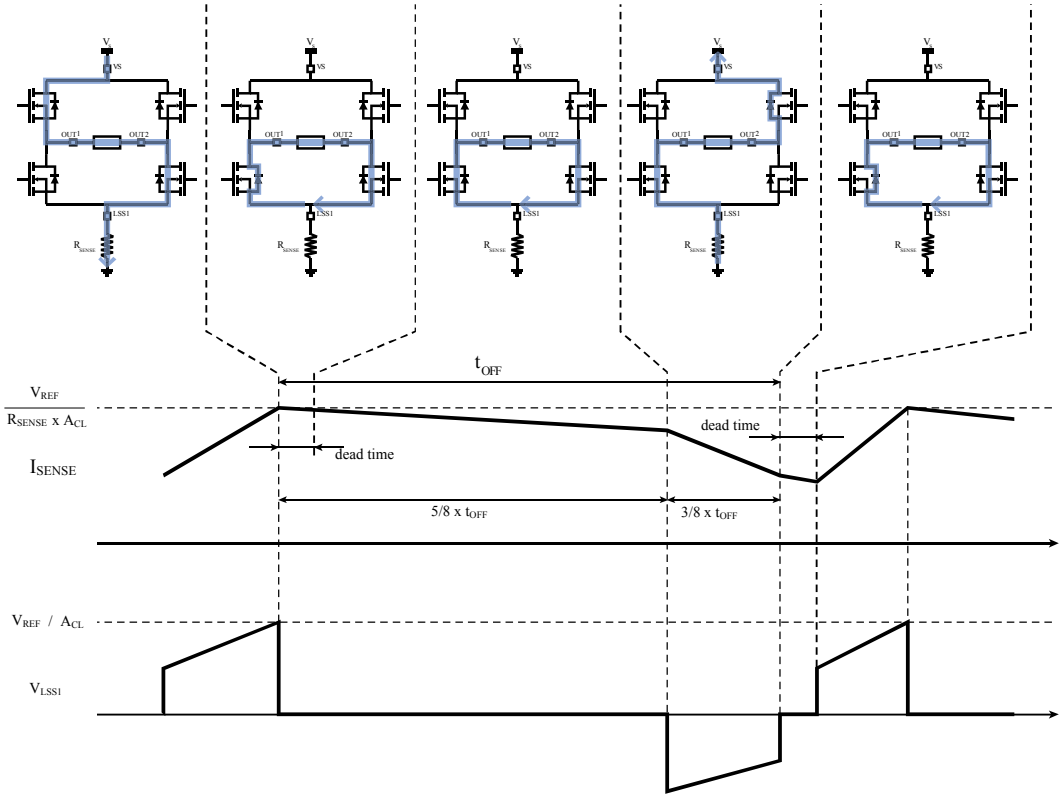


5.6.1.3 *Mixed decay operation mode (fixed OFF-time)*

In mixed decay operation mode, the current is limited turning on both the low-side MOS of the full-bridge (slow decay), the system switches from slow decay to quasi-synchronous fast decay (the sinking side of the bridge is put in high impedance) when the counter reaches a fixed threshold corresponding to a 5/8th of the total decay time (t_{OFF}).

As soon as the OFF-time expires the bridges return in the ON state (see Figure 12).

Figure 12. **Current control in mixed decay mode (fixed OFF-time)**



5.6.2 PWM trimming mode

When V_1 exceeds V_{REF} the control circuitry sets the device in limiting status to reduce the current. The decay strategy and the return to normal operation depends on the selected driving mode: full-bridge or parallel operation mode (mixed decay is not available with this current limiter mode).

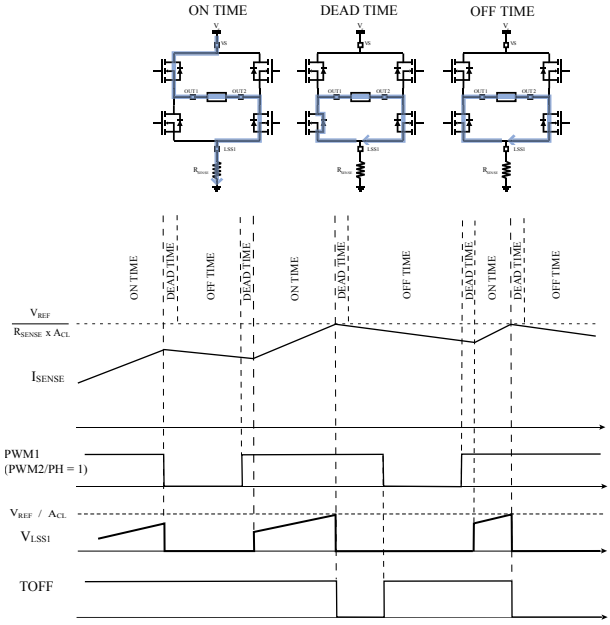
In PWM trimming mode the TOFF pin is a digital output and it is forced low during the current decay time.

5.6.2.1 Dual half-bridge and full-bridge operation mode (PWM trimming)

In dual half-bridge and full-bridge operation modes, the current is limited turning on both the low-side MOS (slow decay, see Figure 13. Current control in full-bridge mode (PWM trimming)). The device returns to normal operation if one of the following conditions occurs:

- nSTDBY is set low
- EN/nFAULTx is set low
- PWM1 is set low in full-bridge operation mode
- PWM1 and PWM2/PH are both set low in dual half-bridge mode

Figure 13. **Current control in full-bridge mode (PWM trimming)**



5.6.2.2 *Half-bridge parallel operation mode (PWM trimming)*

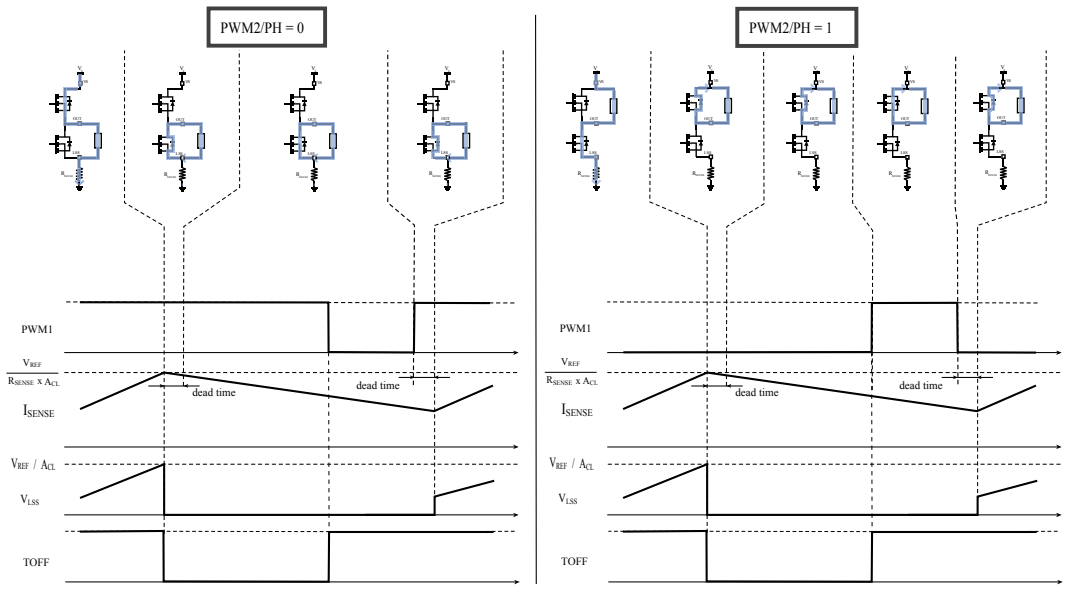
In half-bridge parallel operation mode, the decay strategy is determined by the status of PWM2/PH (see Figure 14):

- PWM2/PH is low: the low side MOS is switched on
- PWM2/PH is high: the output is in high impedance (current recirculates in the body diode)

The device returns to normal operation if one of the following conditions occurs:

- nSTDBY is set low
- EN/nFAULTx is set low
- PWM1 is set low, if PWM2/PH = 0
- PWM1 is set high, if PWM2/PH = 1

Figure 14. **Current control in half-bridge parallel mode (PWM trimming)**



5.6.3 Blanking

In order to avoid spurious triggering of the current limiter's comparator due to both internal and external noise (ringing, diode's recovery currents, etc.), the device integrates a blanking circuitry.

The blanking signal is generated at each commutation of the half-bridges 1 and 2.

When the bridge is in high impedance, blanking condition is always imposed.

5.7 Overcurrent protection

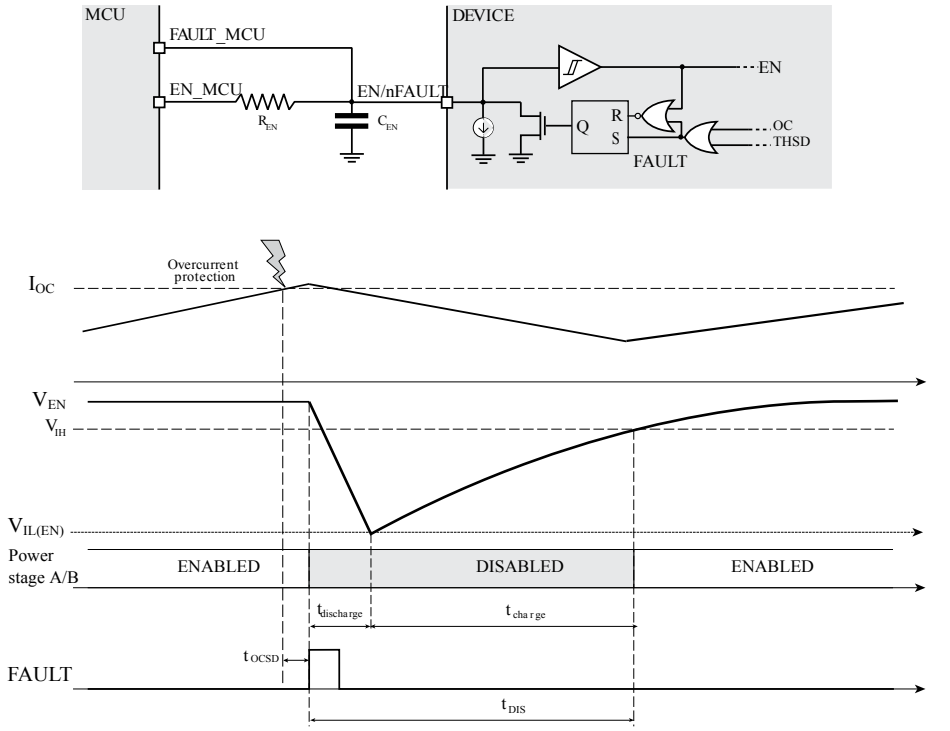
An integrated circuitry, independent from the current limiter, protects the power stage from overcurrent condition.

If the current flowing into one of the integrated MOSFETs exceeds the I_{OC} threshold, the OC protection turns off all the MOSFETs and forces low the EN/nFAULT open drain output.

The device holds this condition until the nFAULT input voltage falls below the V_{IL_EN} threshold.

In order to avoid spurious triggering due to noise, a deglitch filter with t_{OCSD} (OC protection) period is implemented.

Figure 15. Overcurrent protection timings



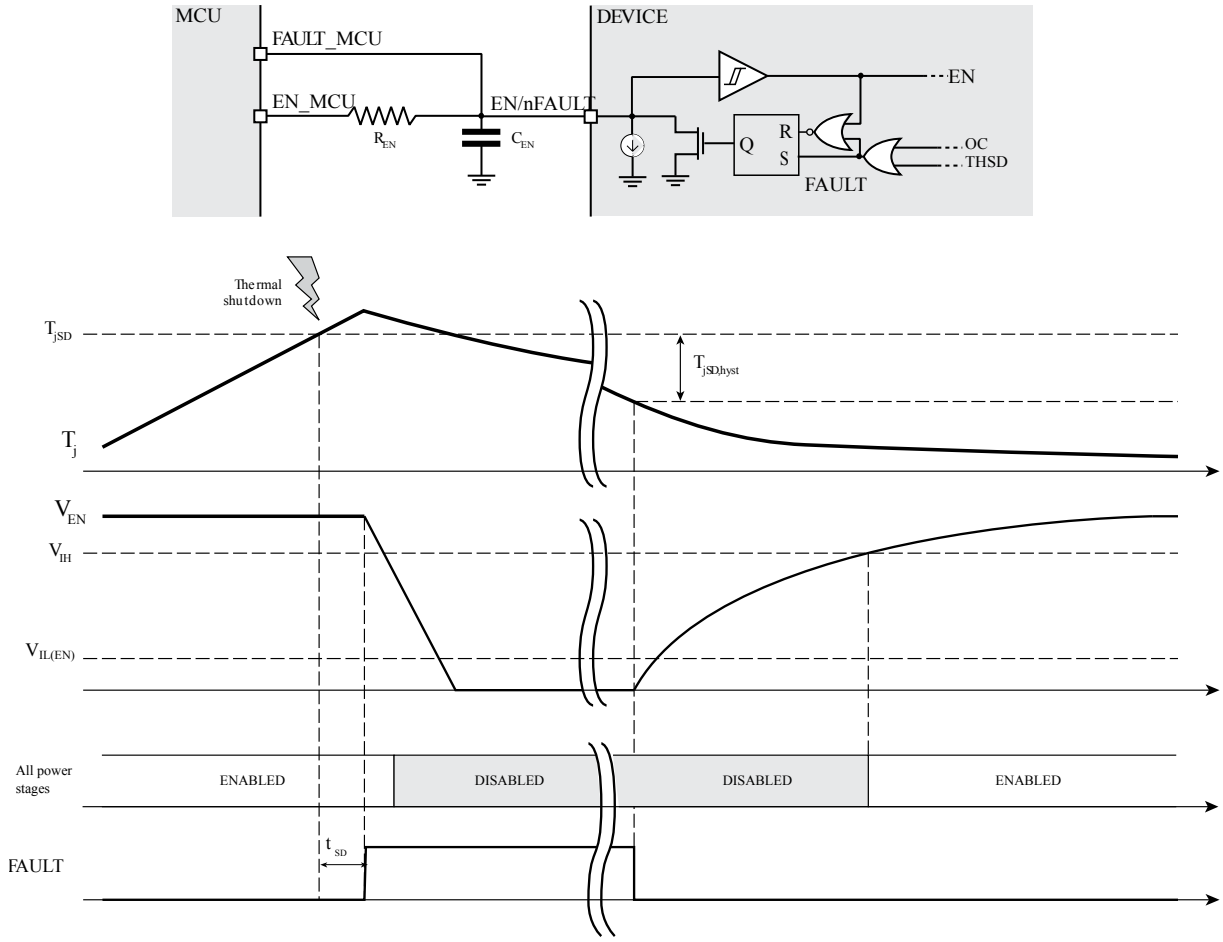
The total disable time after an overcurrent event can be set properly sizing the external network connected to the EN\nFAULT pin.

5.8 Thermal shutdown

The device integrates a thermal shutdown protection. When the internal temperature exceeds the T_{SD} temperature, the power stage is disabled until the temperature returns below T_{SD} - $T_{SD(Hyst)}$.

When the device is in thermal shutdown, the nFAULT is forced low (see Figure 16).

Figure 16. **Thermal shutdown sequence**



6 Characterization graphs

Figure 17. **Output slew rate vs. temperature (V_S = 58 V, normalized at T_J = 25 °C)**

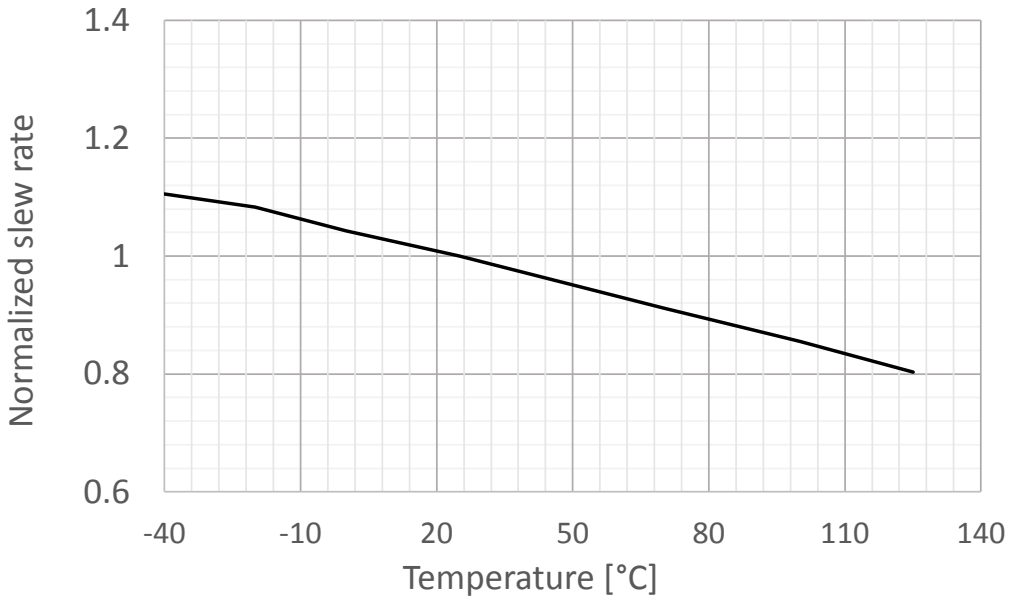


Figure 18. **Output slew rate derating vs. supply voltage (T_J = 25 °C)**

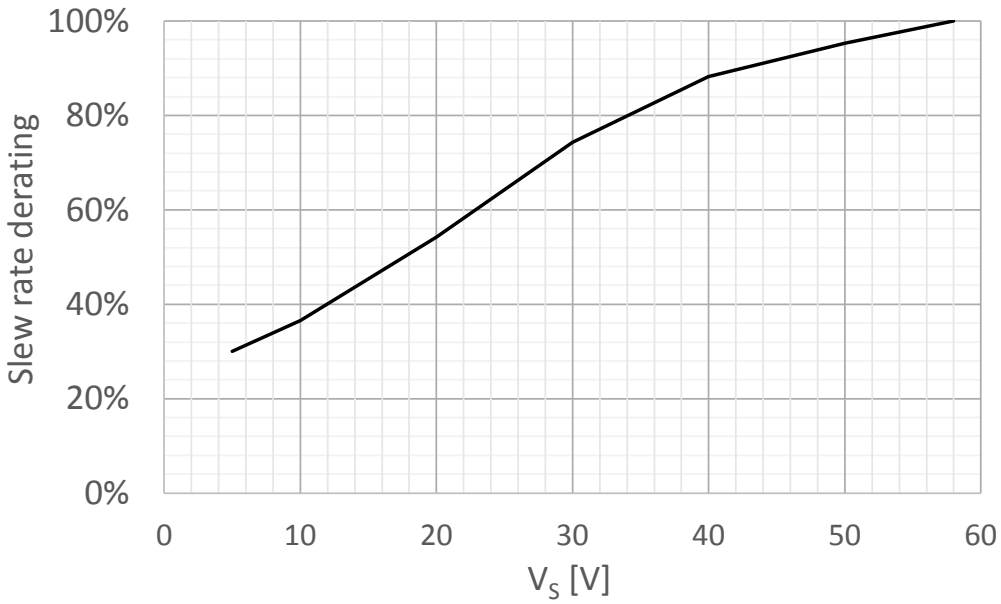


Figure 19. **Overcurrent threshold vs. temperature (V_S = 58 V, normalized at T_J = 25 °C)**

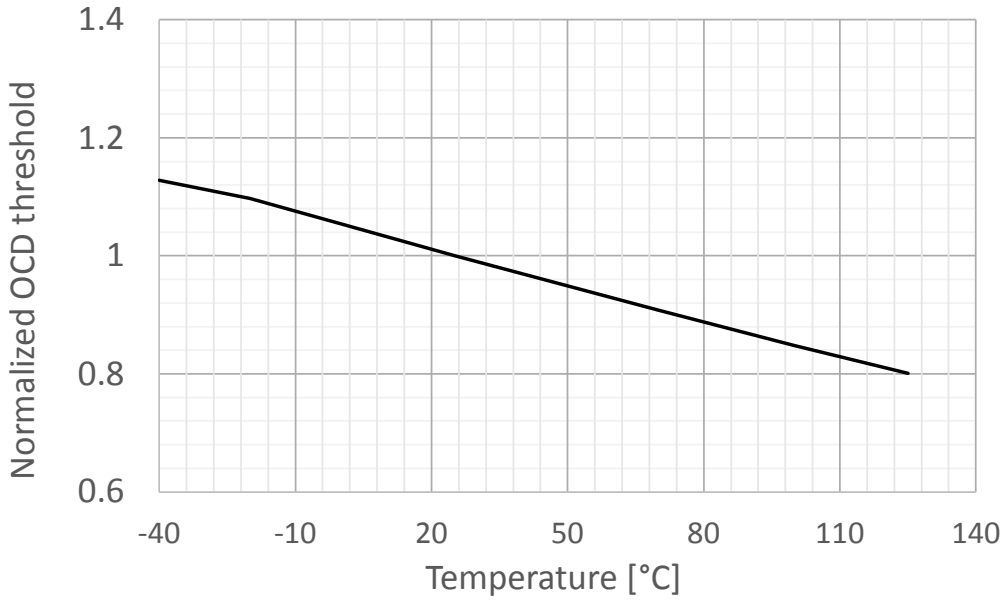


Figure 20. **Overcurrent threshold vs. supply voltage (T_J = 25 °C, normalized at V_S = 58 V)**

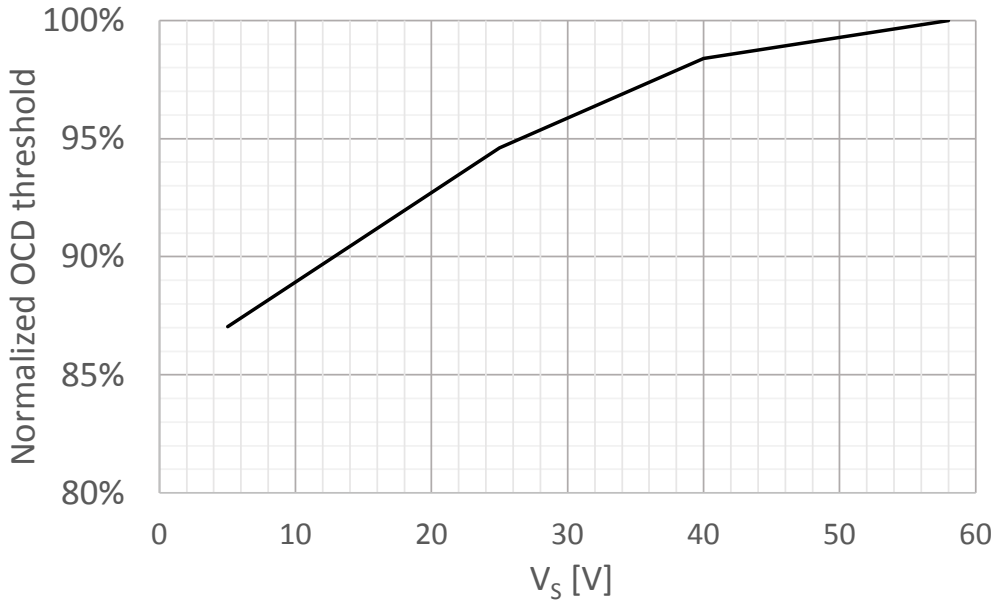
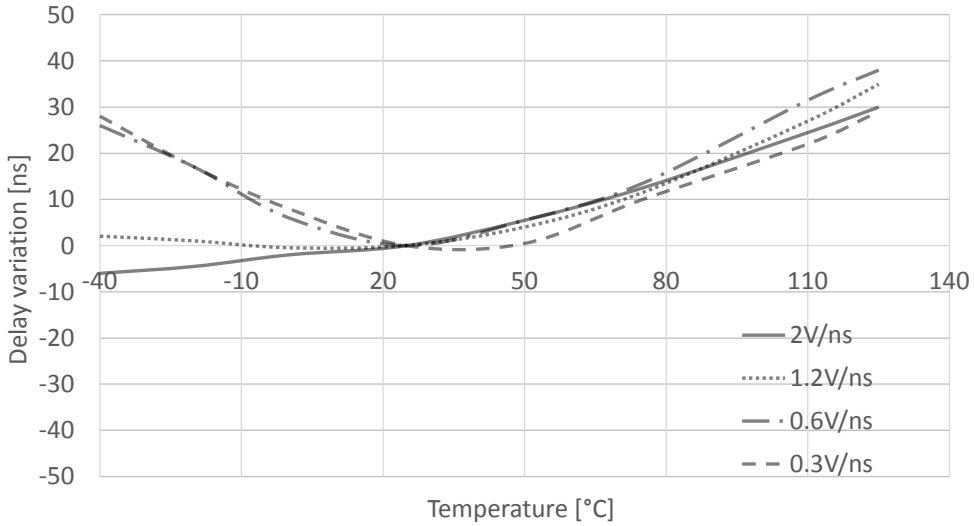


Figure 21. **PWM input to output propagation delay vs. temperature (referenced to T_j = 25 °C) T**

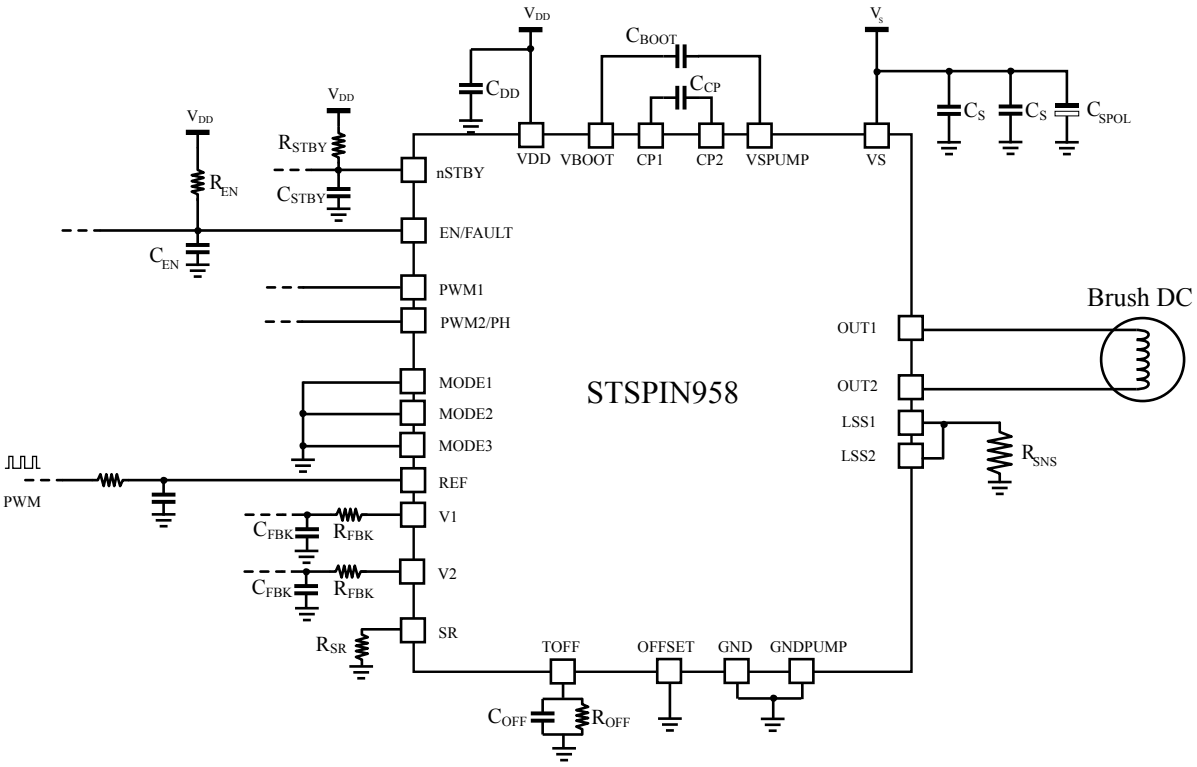


7 Typical application

Table 12. **Typical application value**

Name	Value
C_S	470 nF
C_{BULK}	220 µF
C_{DD}	220 nF
C_{CP}	100 nF
C_{BOOT}	1 µF
R_{SNS}	50 mΩ / 3W
C_{EN}	10 nF
R_{EN}	39 kΩ
C_{STBY}	1 nF
R_{STBY}	18 kΩ
R_{OFF}, C_{OFF}	22 kΩ, 1 nF (t_{OFF} = 18 µs)
C_{FBK}	100 pF
R_{FBK}	100 Ω
R_{SR}	5 kΩ (SR = 0.6 V/ns)

Figure 22. **Typical application schematic**



8 Layout guidelines

Two 470 nF bypass capacitors must be connected between the VS supply voltage pins and ground and one 220 nF bypass capacitor must be connected between the VDD supply pin and ground.

These capacitors must be low-ESR ceramic technology and placed as close to the pins as possible (VS and VDD pins) with a thick ground plane connection to the device GND pin.

A bulk capacitor is required to bypass the high current path. One or more capacitors should be placed as to minimize the length of high current paths between VS and GND. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers.

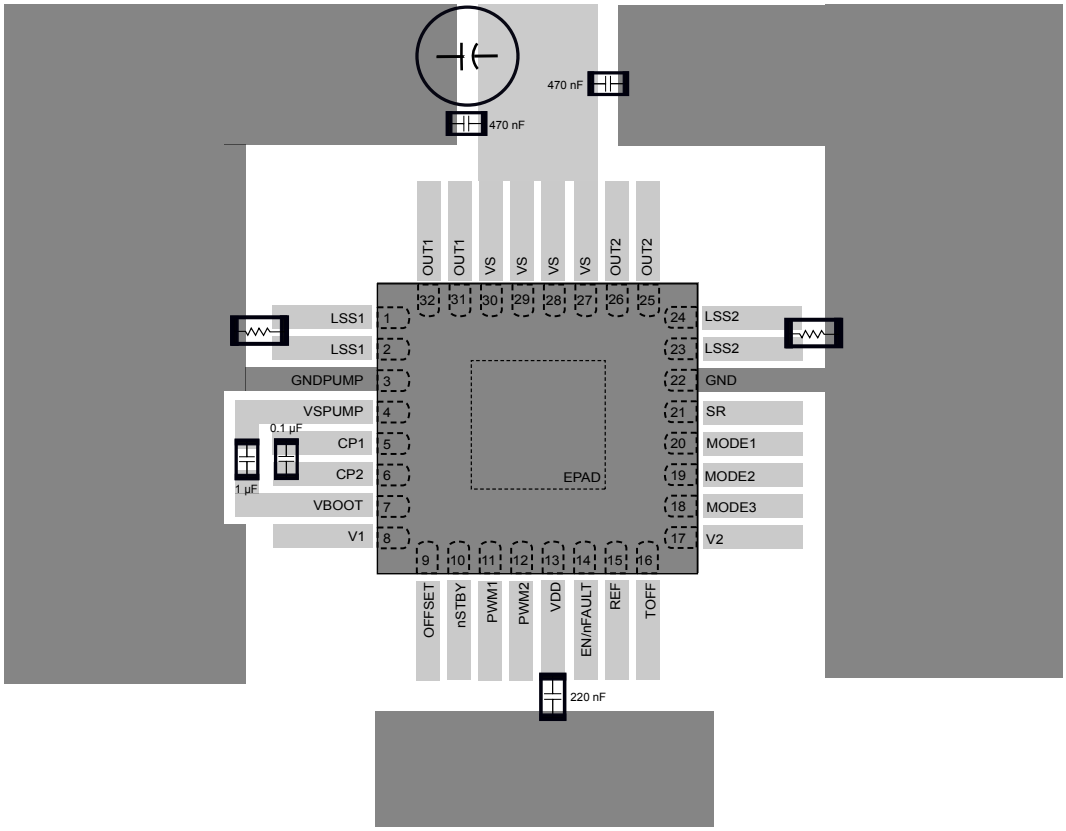
In application requiring the device switching at high slew rates or with high output currents, ground layers should be designed to separate digital and power ground. In this case, the exposed PAD must be connected to the power ground and the VDD bypass capacitor to the digital ground. The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on the SENSE and OUT pins.

The current sense resistors should be placed as close as possible to the device pins to minimize trace inductance between the device pin and resistors avoiding, where possible, to place them on a different board layer.

A low-ESR ceramic capacitor must be placed between the CP1 and CP2 pins (100 nF, rated for 16V) and between the VBOOT and VSPUMP pins (1 µF, rated for 16 V).

A layout example is shown in Figure 23. Layout example.

Figure 23. Layout example



9 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at www.st.com. ECOPACK is an STMicroelectronics trademark.

A customized VFQFPN32 5 x 5 package is proposed. A smaller EPAD, internally connected to the ground pin, is desired to place through holes on the bottom of the package. Lead plating is Nickel/Palladium/Gold (Ni/Pd/Au).

9.1 VFQFPN32 5 x 5 package information

Figure 24. VFQFPN32 (5 x 5 x 1.0 mm) package outline

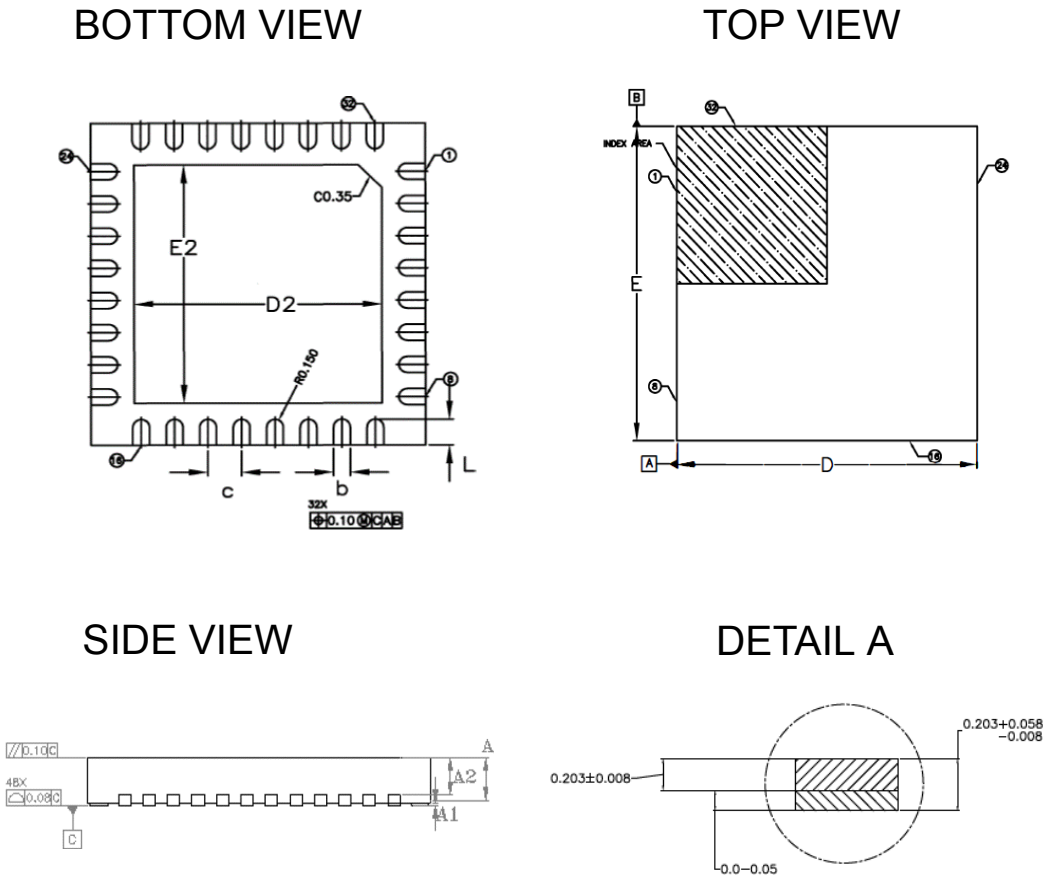
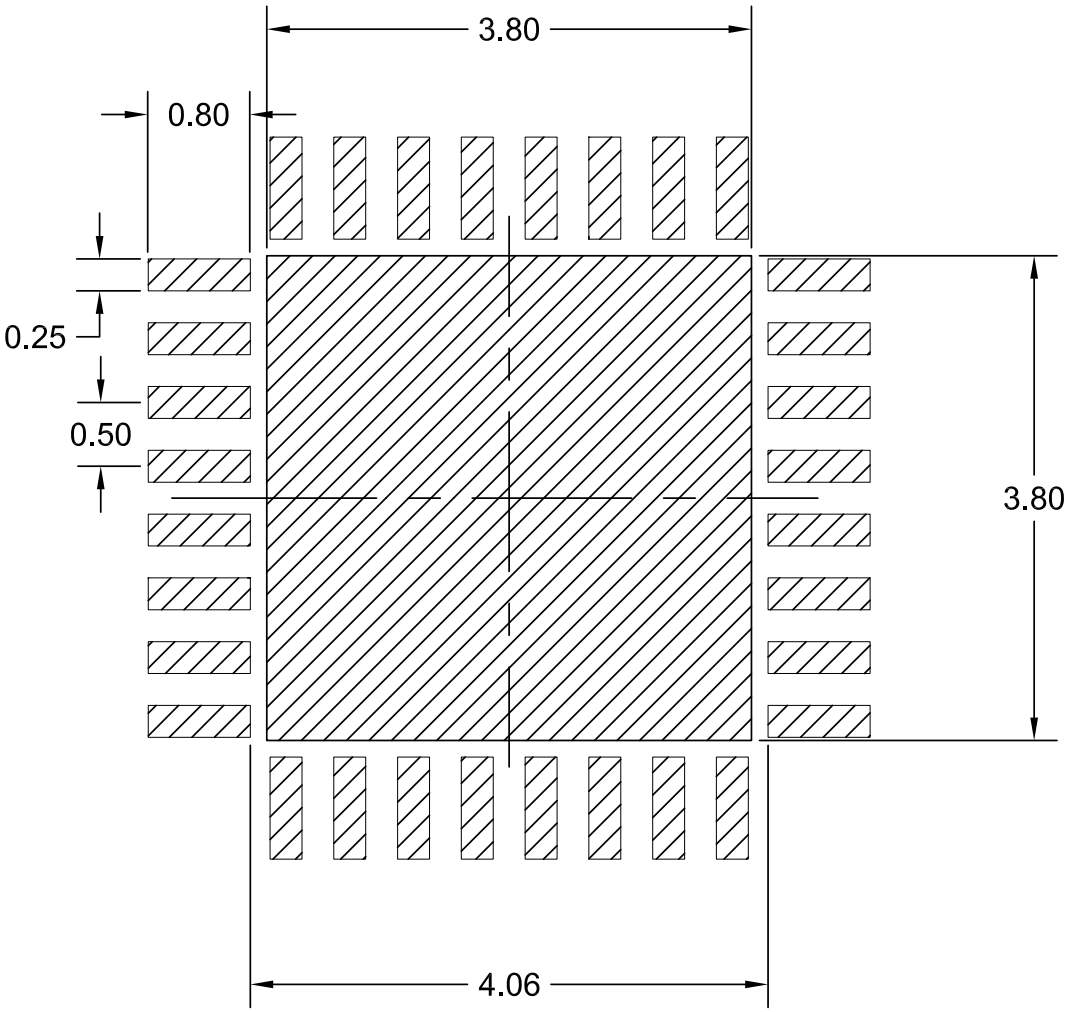


Table 13. **VFQFPN32 (5 x 5 x 1.0 mm) package mechanical data**

Dim.	(mm)		
	Min.	Typ.	Max.
A	0.90	0.95	1.00
A1	0		0.05
A3		0.20	
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
c		0.50	
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
L	0.30	0.40	0.50

Figure 25. **VFQFPN32 (5 x 5 x 1.0 mm) recommended footprint**



10 Ordering information

Table 14. **Device summary**

Order code	Package	Packaging
STSPIN958TR	VFQFPN32 5 x 5 x 1 – 32 L	Tape and reel
STSPIN958	VFQFPN32 5 x 5 x 1 – 32 L	Tray

Revision history

Table 15. **Document revision history**

Date	Version	Changes
07-Jul-2023	1	Initial release.
25-Oct-2023	2	Added P/N in Table 14

Contents

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