Zero-Drift, Single-Supply, Rail-to-Rail I/O Quad, Operational Amplifier

Enhanced Product

AD8574-EP

FEATURES

- Low offset voltage: 1 µV
- Input offset drift: 0.005 µV/°C
- Rail-to-rail input and output swing
- 5 V/2.7 V single-supply operation
- High gain: 145 dB typical
- CMRR: 140 dB typical
- PSRR: 130 dB typical
- Ultralow input bias current: 10 pA typical
- Low supply current: 750 µA per op amp
- Overload recovery time: 50 µs
- No external capacitors required

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Military temperature range (−55°C to +125°C)
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Product change notification
- Qualification data available on request

APPLICATIONS

- Temperature sensors
- Pressure sensors
- Precision current sensing
- Strain gage amplifiers

PIN CONFIGURATION

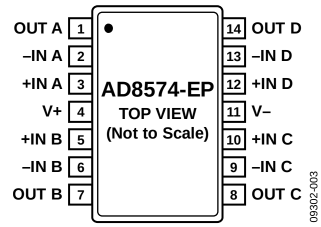

Figure 1. 14-Lead TSSOP

GENERAL DESCRIPTION

This amplifier has ultralow offset, drift, and bias current. The AD8574-EP is a quad amplifier, featuring rail-to-rail input and output swings. It is guaranteed to operate from 2.7 V to 5 V single supply.

The AD8574-EP provides benefits previously found only in expensive auto-zeroing or chopper stabilized amplifiers. Using a patented spread spectrum, auto-zero technique, the AD8574 eliminates the intermodulation effects from interaction of the chopping function with the signal frequency in ac applications.

With an offset voltage of only 1 µV and drift of 0.005 µV/°C, the AD8574-EP is perfectly suited for applications where error sources must be minimized.

The AD8574-EP is specified for the military temperature range (−55°C to +125°C). The AD8574-EP quad amplifier is available in a 14-lead TSSOP package.

Additional applications and technical information is available in the AD8571/AD8572/AD8574 data sheets.

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REVISION HISTORY

4/2018—Rev. 0 to Rev. A

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8/2010—Revision 0: Initial Version

SPECIFICATIONS

5 V ELECTRICAL CHARACTERISTICS

V_S = 5 V, V_{CM} = 2.5 V, V_O = 2.5 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	5	μV
		−55°C ≤ T_A ≤ +125°C			15	μV
Input Bias Current	I_B			10	50	pA
		−55°C ≤ T_A ≤ +125°C		1.0	1.5	nA
Input Offset Current	I_{OS}			20	70	pA
		−55°C ≤ T_A ≤ +125°C		150	200	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	120	140		dB
		−55°C ≤ T_A ≤ +125°C	115	130		dB
Large Signal Voltage Gain[1]	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 4.7 V	125	145		dB
		−55°C ≤ T_A ≤ +125°C	120	135		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C ≤ T_A ≤ +125°C		0.005	0.04	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	4.99	4.998		V
		R_L = 100 kΩ to GND at −55°C to +125°C	4.99	4.997		V
		R_L = 10 kΩ to GND	4.95	4.98		V
		R_L = 10 kΩ to GND at −55°C to +125°C	4.95	4.975		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		1	10	mV
		R_L = 100 kΩ to V+ at −55°C to +125°C		2	10	mV
		R_L = 10 kΩ to V+		10	30	mV
		R_L = 10 kΩ to V+ at −55°C to +125°C		15	30	mV
Short-Circuit Limit	I_{SC}		±25	±50		mA
		−55°C to +125°C		±40		mA
Output Current	I_O			±30		mA
		−55°C to +125°C		±15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	120	130		dB
		−55°C ≤ T_A ≤ +125°C	115	130		dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		850	975	μA
		−55°C ≤ T_A ≤ +125°C		1000	1075	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.4		V/μs
Overload Recovery Time				0.05	0.3	ms
Gain Bandwidth Product	GBP			1.5		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0 Hz to 10 Hz		1.3		μV p-p
		0 Hz to 1 Hz		0.41		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		51		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		2		fA/√Hz

[1] Gain testing is dependent upon test bandwidth.

2.7 V ELECTRICAL CHARACTERISTICS

V_S = 2.7 V, V_{CM} = 1.35 V, V_O = 1.35 V, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			1	5	μV
		−55°C ≤ T_A ≤ +125°C			15	μV
Input Bias Current	I_B			10	50	pA
		−55°C ≤ T_A ≤ +125°C		1.0	1.5	nA
Input Offset Current	I_{OS}			10	50	pA
		−55°C ≤ T_A ≤ +125°C		150	200	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 2.7 V	115	130		dB
		−55°C ≤ T_A ≤ +125°C	110	130		dB
Large Signal Voltage Gain[1]	A_{VO}	R_L = 10 kΩ, V_O = 0.3 V to 2.4 V	110	140		dB
		−55°C ≤ T_A ≤ +125°C	105	130		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−55°C ≤ T_A ≤ +125°C		0.005	0.04	μV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to GND	2.685	2.697		V
		R_L = 100 kΩ to GND at −55°C to +125°C	2.685	2.696		V
		R_L = 10 kΩ to GND	2.67	2.68		V
		R_L = 10 kΩ to GND at −55°C to +125°C	2.67	2.675		V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to V+		1	10	mV
		R_L = 100 kΩ to V+ at −55°C to +125°C		2	10	mV
		R_L = 10 kΩ to V+		10	20	mV
		R_L = 10 kΩ to V+ at −55°C to +125°C		15	20	mV
Short-Circuit Limit	I_{SC}		±10	±15		mA
		−55°C to +125°C		±10		mA
Output Current	I_O			±10		mA
		−55°C to +125°C		±5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	120	130		dB
		−55°C ≤ T_A ≤ +125°C	115	130		dB
Supply Current per Amplifier	I_{SY}	V_O = 0 V		750	900	μA
		−55°C ≤ T_A ≤ +125°C		950	1000	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ		0.5		V/μs
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			1		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0 Hz to 10 Hz		2.0		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		94		nV/√Hz
Current Noise Density	i_n	f = 10 Hz		2		fA/√Hz

[1] Gain testing is dependent upon test bandwidth.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S + 0.3 V
Differential Input Voltage[1]	±5.0 V
ESD (Human Body Model)	2000 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Differential input voltage is limited to ±5.0 V or the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for TSSOP packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
14-Lead TSSOP (RU)	180	36	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

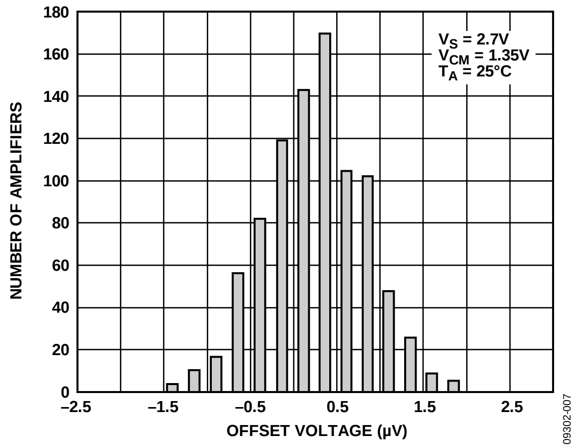

Figure 2. Input Offset Voltage Distribution

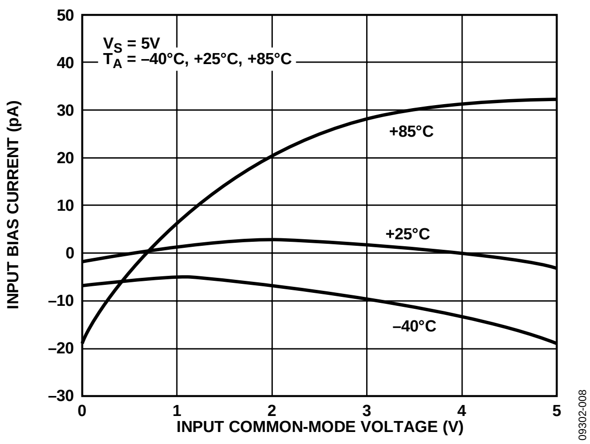

Figure 3. Input Bias Current vs. Input Common-Mode Voltage

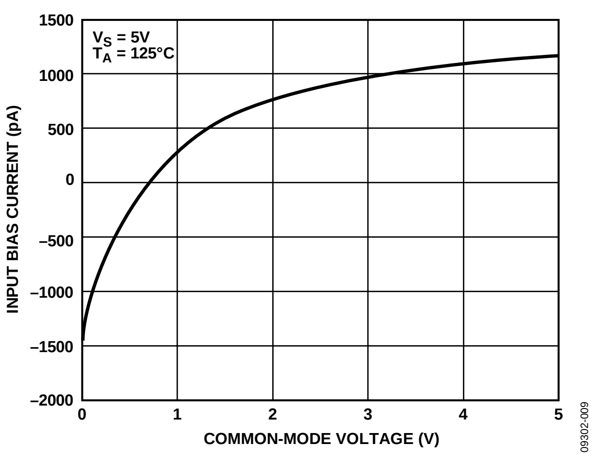

Figure 4. Input Bias Current vs. Common-Mode Voltage

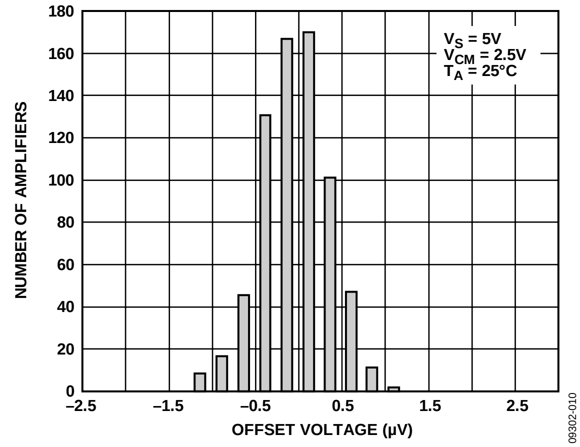

Figure 5. Input Offset Voltage Distribution

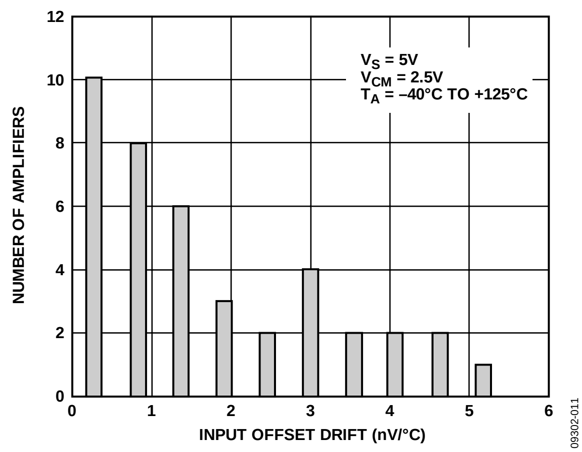

Figure 6. Input Offset Voltage Drift Distribution

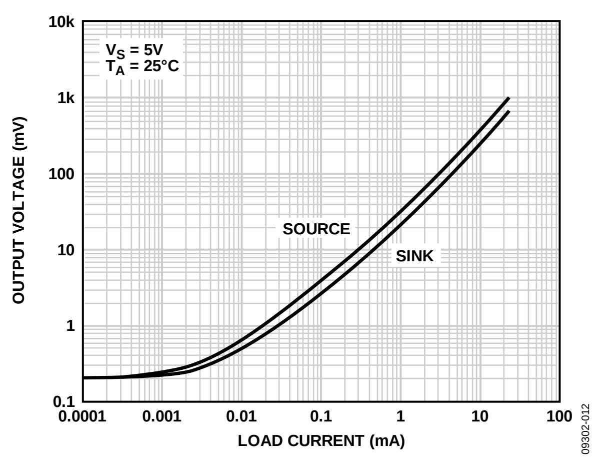

Figure 7. Output Voltage to Supply Rail vs. Load Current

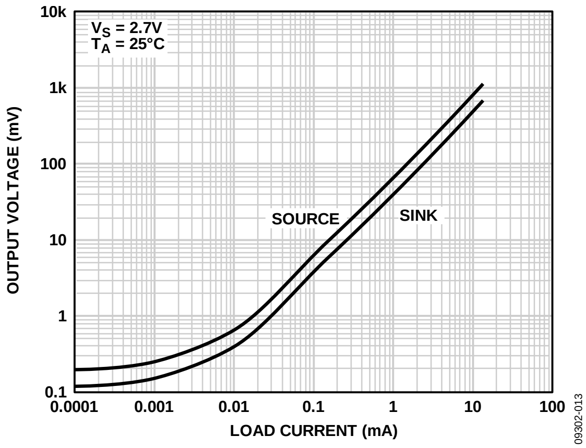

Figure 8. Output Voltage to Supply Rail vs. Load Current

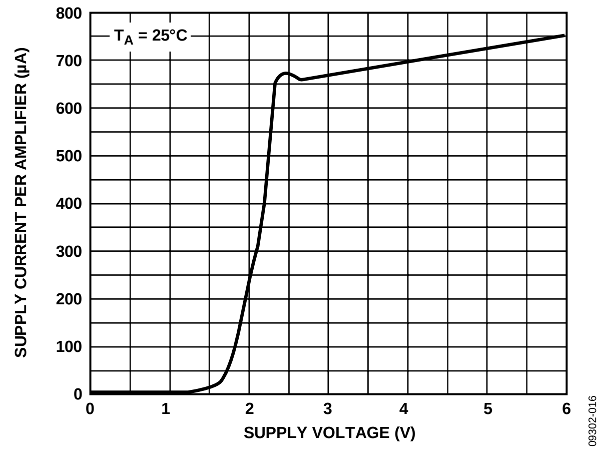

Figure 11. Supply Current per Amplifier vs. Supply Voltage

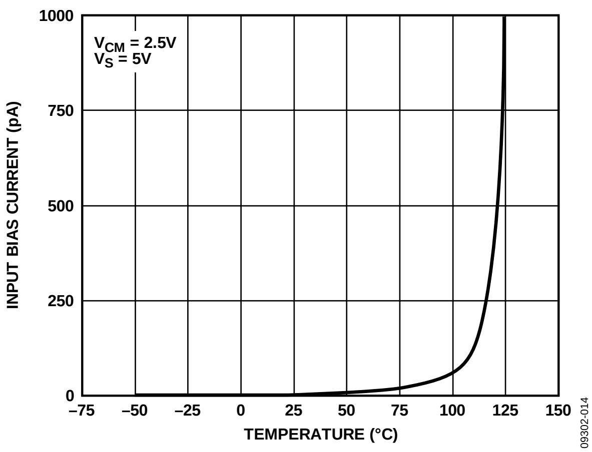

Figure 9. Input Bias Current vs. Temperature

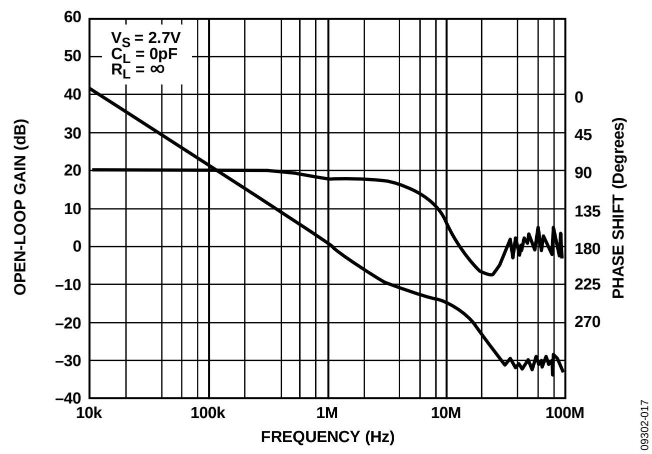

Figure 12. Open-Loop Gain and Phase Shift vs. Frequency

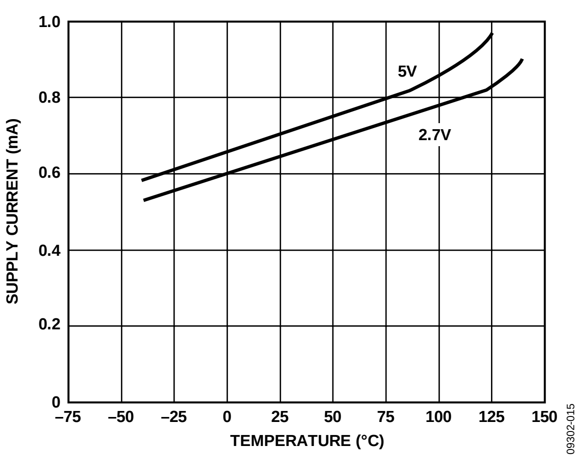

Figure 10. Supply Current vs. Temperature

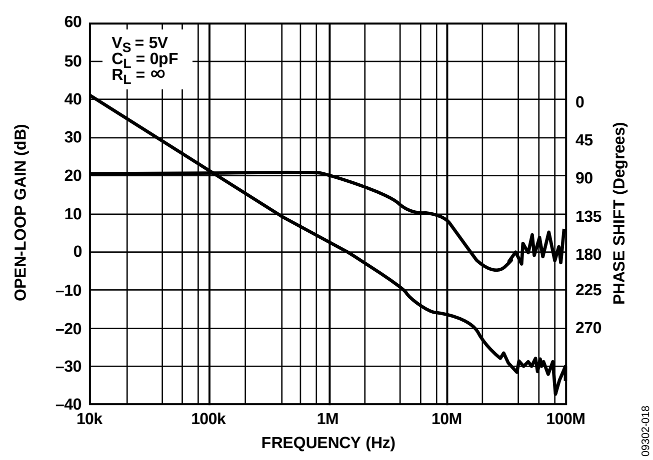

Figure 13. Open-Loop Gain and Phase Shift vs. Frequency

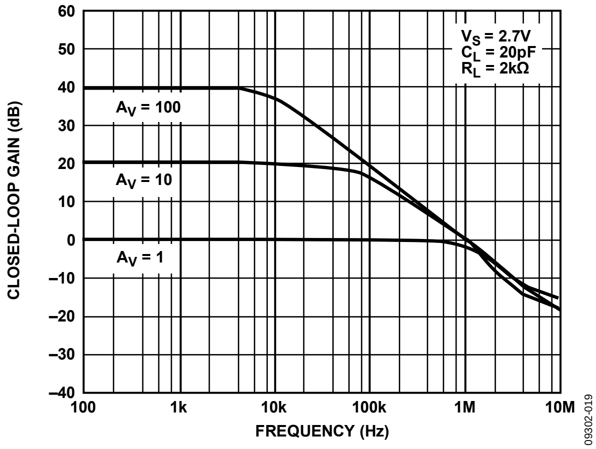

Figure 14. Closed-Loop Gain vs. Frequency

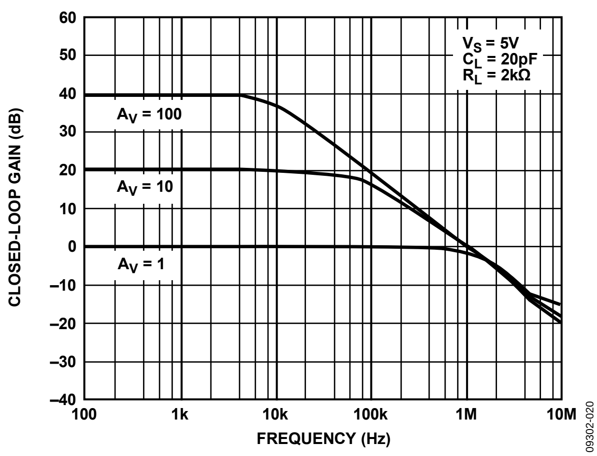

Figure 15. Closed-Loop Gain vs. Frequency

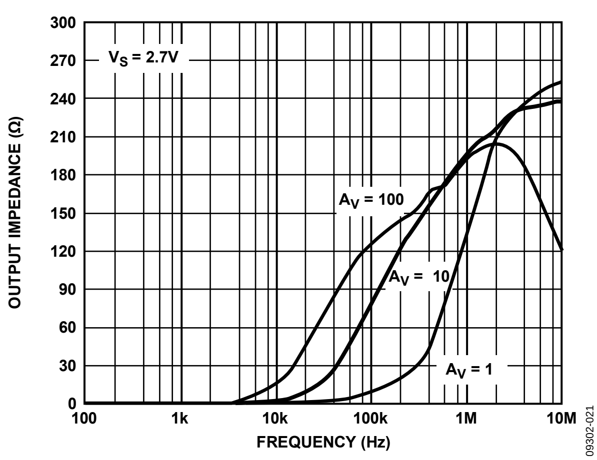

Figure 16. Output Impedance vs. Frequency

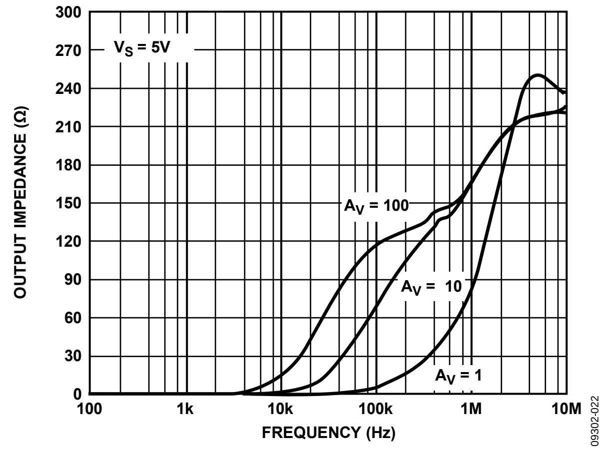

Figure 17. Output Impedance vs. Frequency

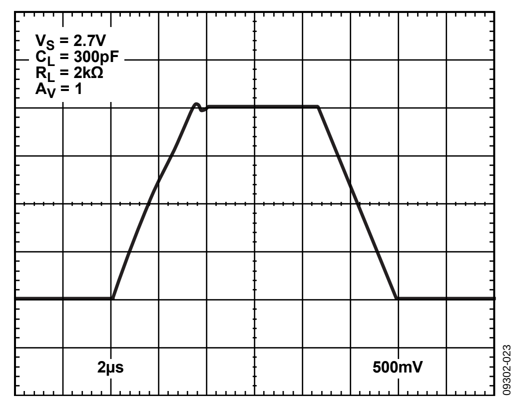

Figure 18. Large Signal Transient Response

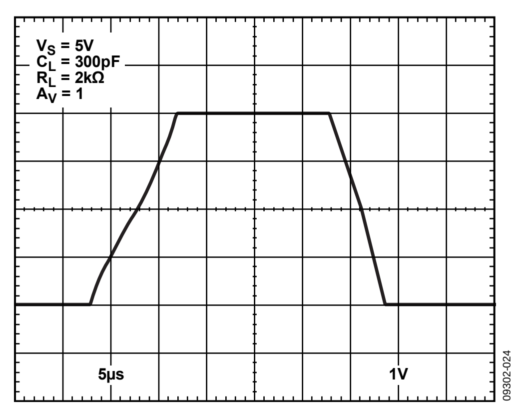

Figure 19. Large Signal Transient Response

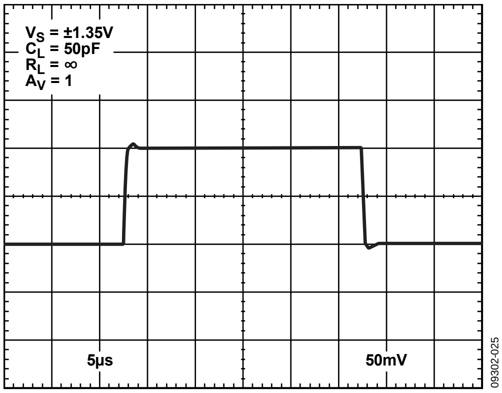

Figure 20. Small Signal Transient Response

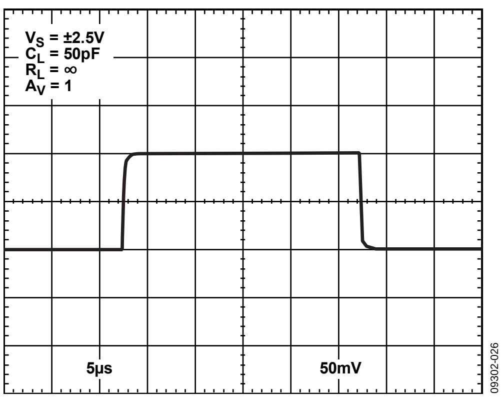

Figure 21. Small Signal Transient Response

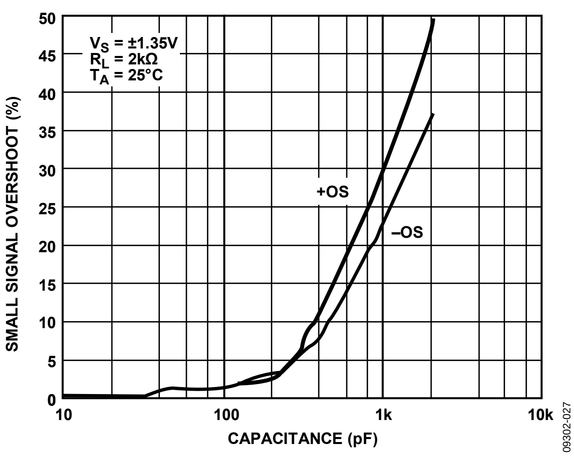

Figure 22. Small Signal Overshoot vs. Load Capacitance

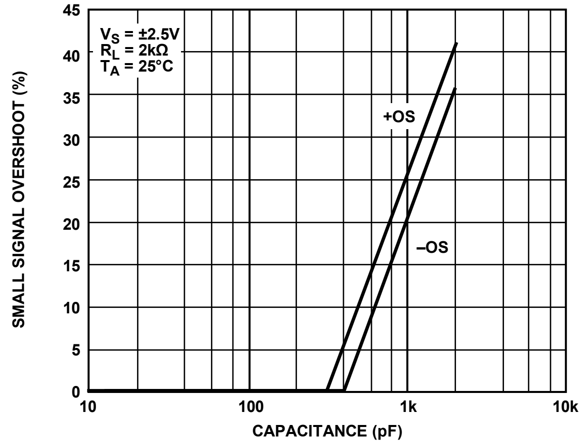

Figure 23. Small Signal Overshoot vs. Load Capacitance

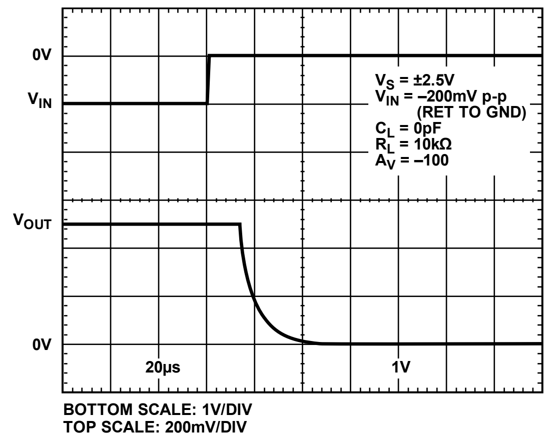

Figure 24. Positive Overvoltage Recovery

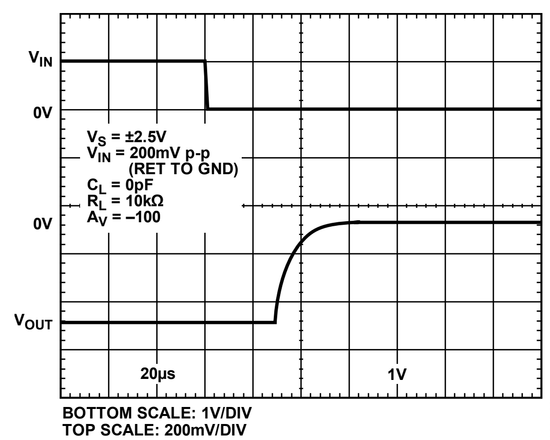

Figure 25. Negative Overvoltage Recovery

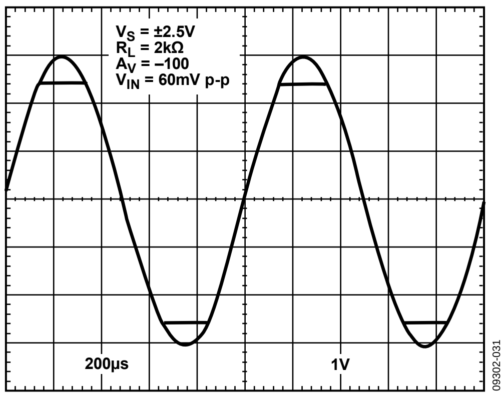

Figure 26. No Phase Reversal

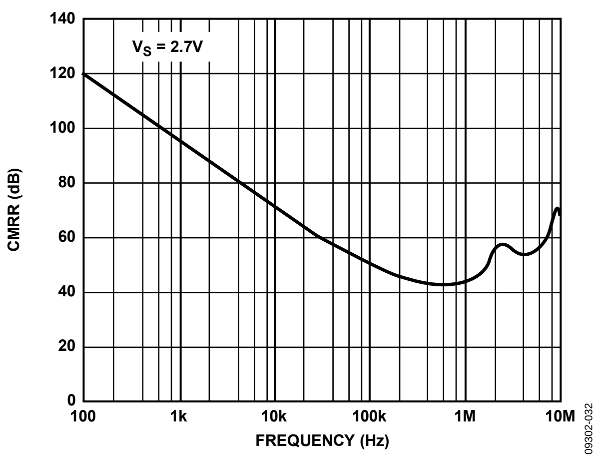

Figure 27. CMRR vs. Frequency

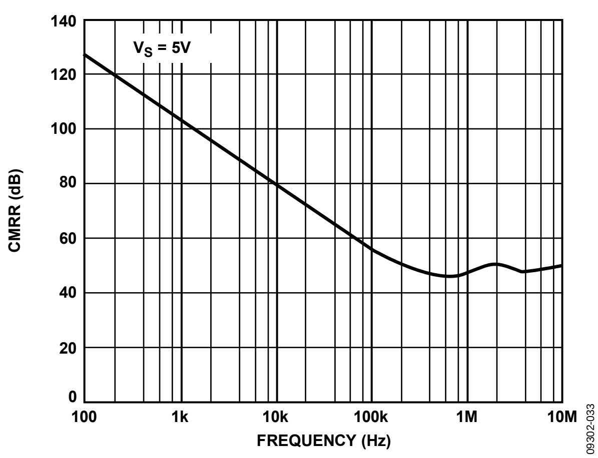

Figure 28. CMRR vs. Frequency

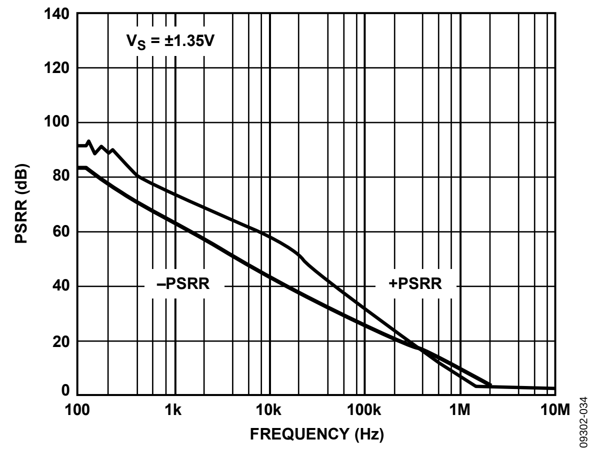

Figure 29. PSRR vs. Frequency

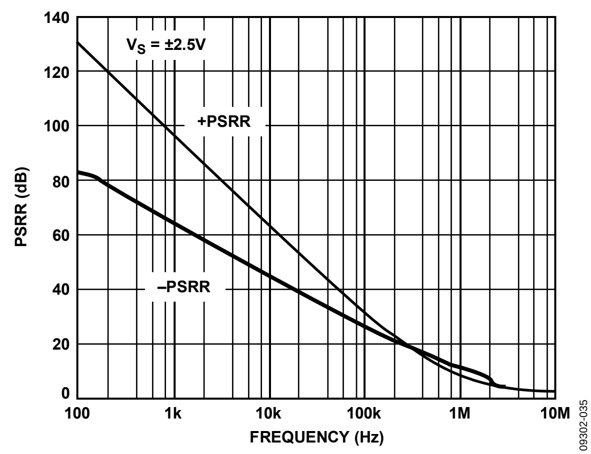

Figure 30. PSRR vs. Frequency

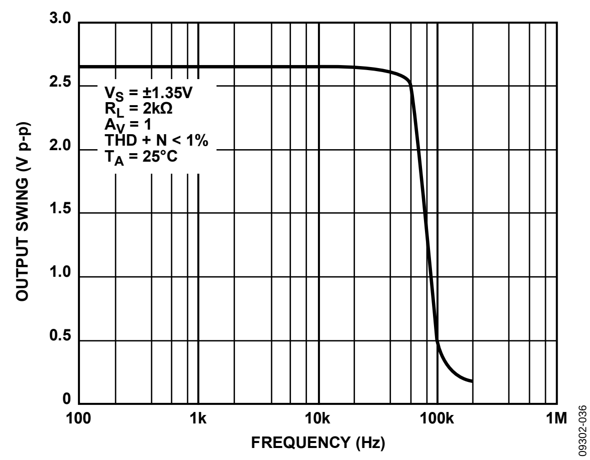

Figure 31. Maximum Output Swing vs. Frequency

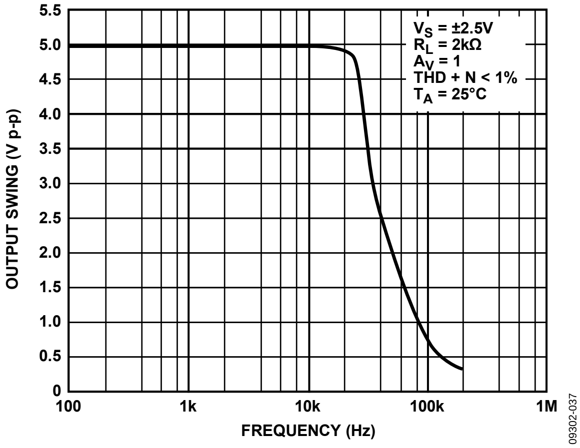

Figure 32. Maximum Output Swing vs. Frequency

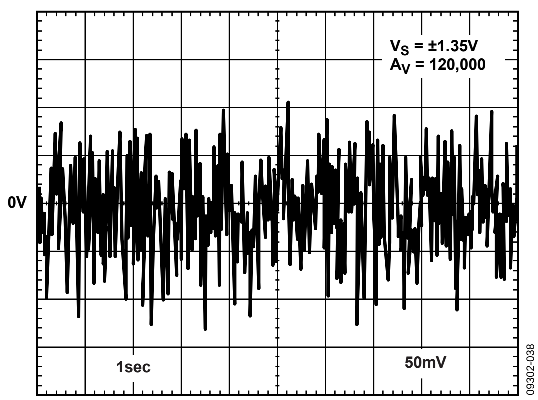

Figure 33. 0.1 Hz to 10 Hz Noise

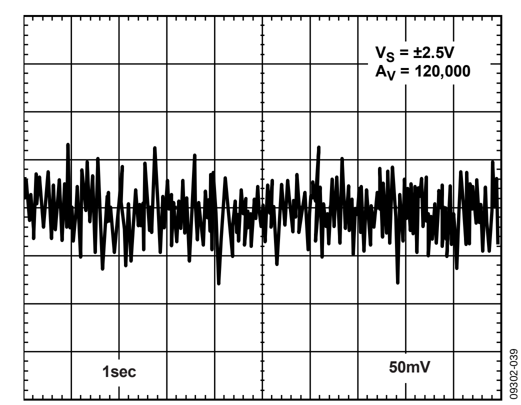

Figure 34. 0.1 Hz to 10 Hz Noise

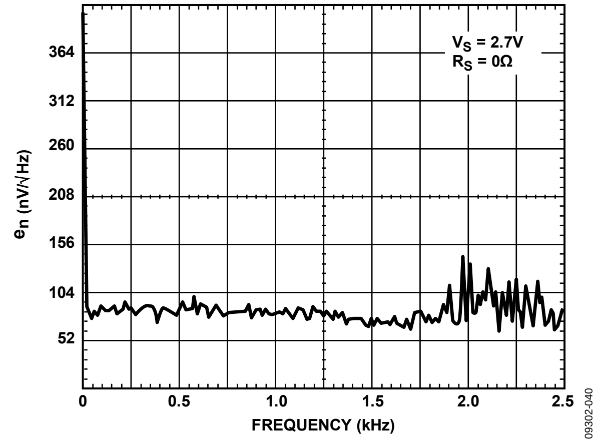

Figure 35. Voltage Noise Density from 0 Hz to 2.5 kHz

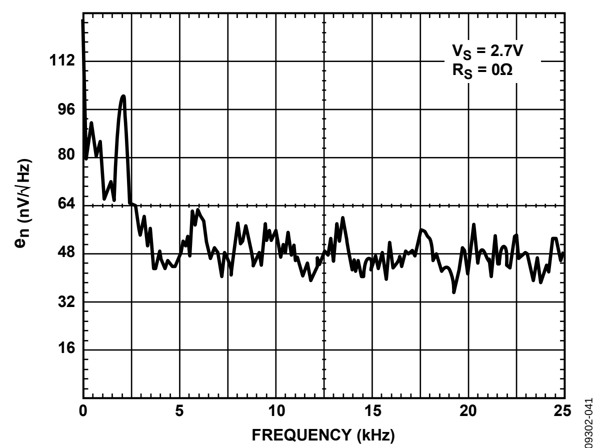

Figure 36. Voltage Noise Density from 0 Hz to 25 kHz

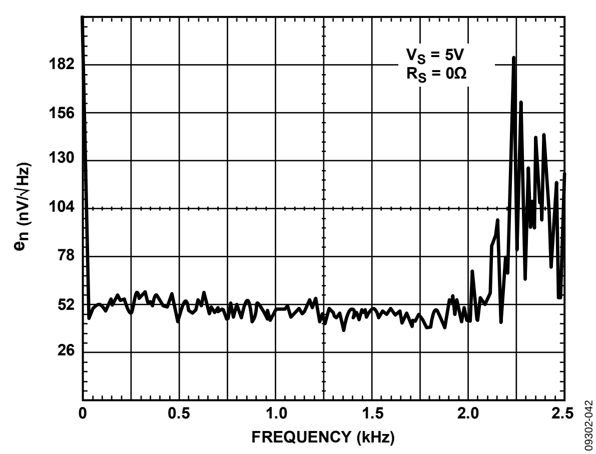

Figure 37. Voltage Noise Density from 0 Hz to 2.5 kHz

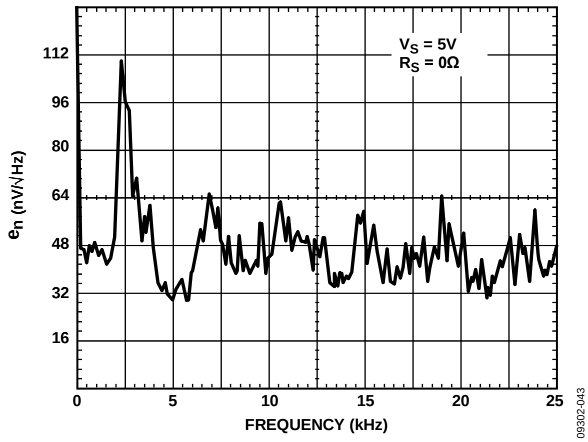

Figure 38. Voltage Noise Density from 0 Hz to 25 kHz

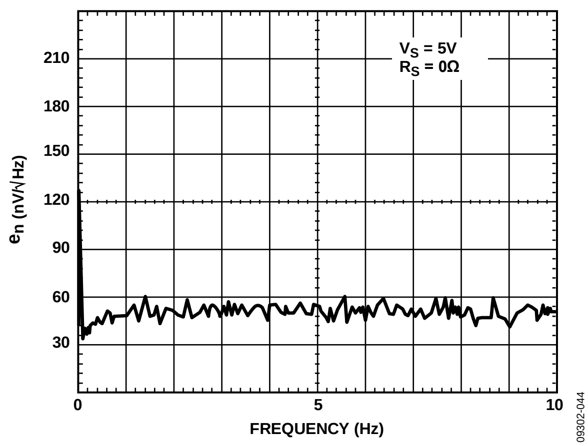

Figure 39. Voltage Noise Density from 0 Hz to 10 Hz

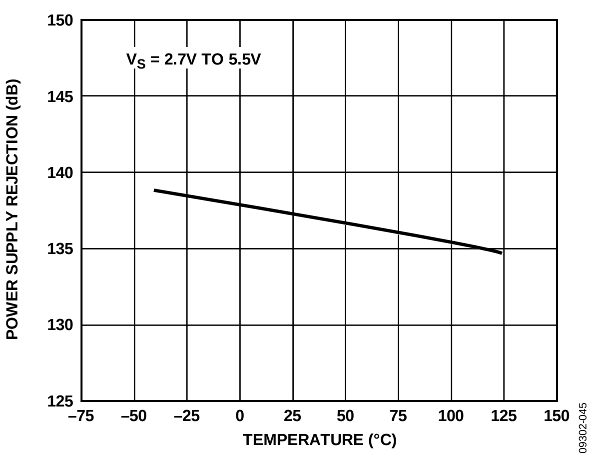

Figure 40. Power Supply Rejection vs. Temperature

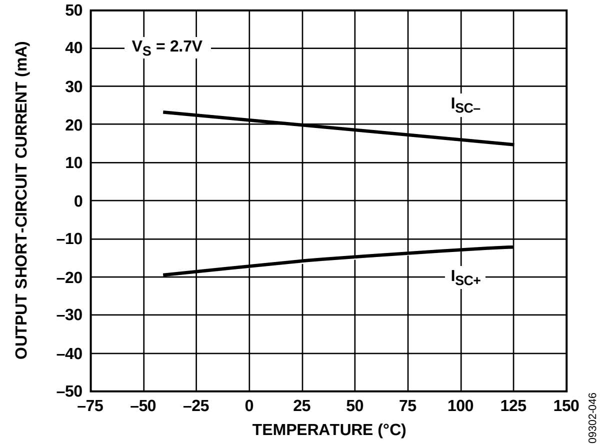

Figure 41. Output Short-Circuit Current vs. Temperature

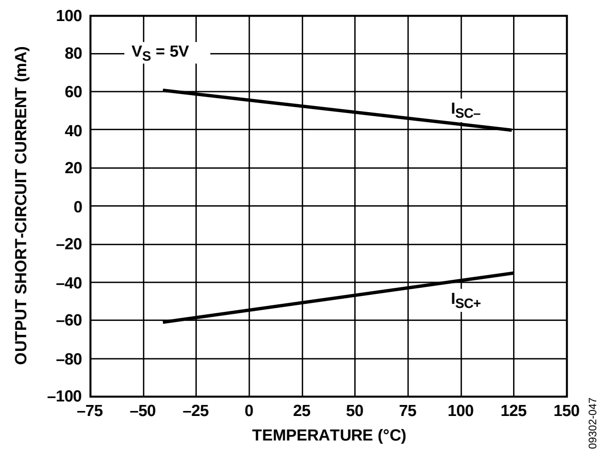

Figure 42. Output Short-Circuit Current vs. Temperature

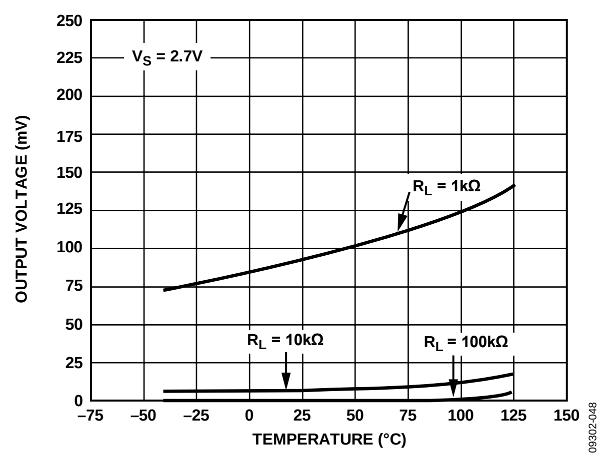

Figure 43. Output Voltage to Supply Rail vs. Temperature

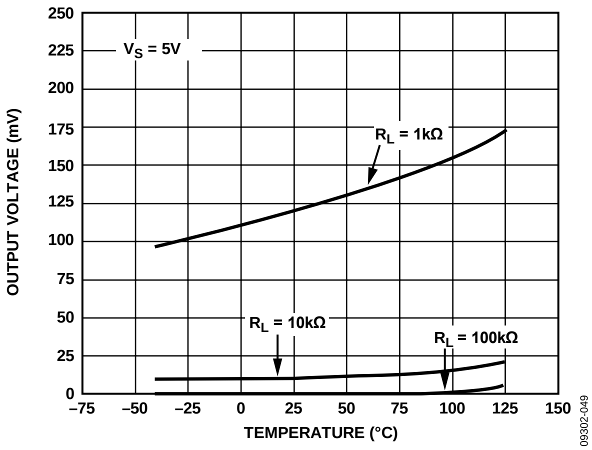

Figure 44. Output Voltage to Supply Rail vs. Temperature

OUTLINE DIMENSIONS

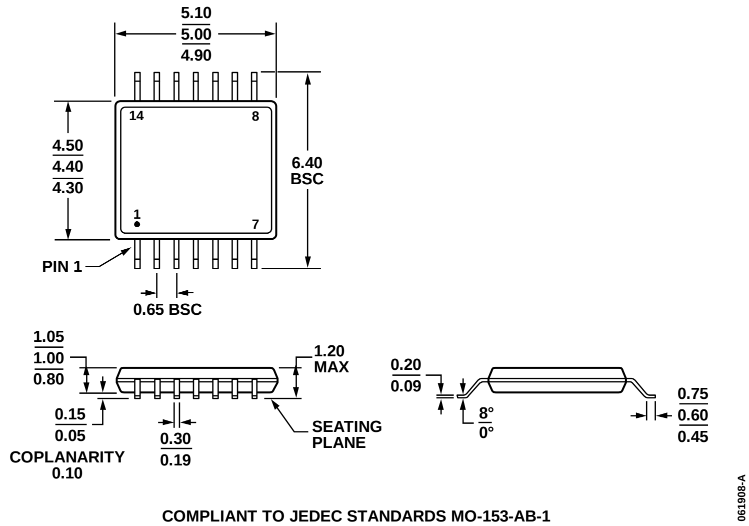

Figure 45. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD8574TRU-EP	−55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8574TRU-EP-RL	−55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8574TRUZ-EP	−55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8574TRUZ-EP-RL	−55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14

[1] Z = RoHS Compliant Part

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